Week 3 Embedded system design

1. Behavioral Description of a system include(s)
    a. Operations
    b. Functions
    c. Processes
    d. None of the above

Ans - a. Operations, b. Functions, c. Processes
Explanation - Behavioral description of a system includes Operations, Function, Processes etc that are required to convert input to output.

2. A system designed in VHDL consists of modules
    a. True
    b. False

Ans – b. False
Explanation – A system designed in verilog consists of module where as a system designed in VHDL is composed of entities each of which can have multiple architecture and a configuration chooses what architecture is used for a given instance of an entity.

3. Given 2 statements
    i. Functional Design is also Known as Back-End Design
    ii. Physical Design is also known as Front-End Design

    a. Both i. & ii. are False
    b. Both i. & ii. are True
    c. i. is True & ii. is False
    d. i. is False & ii. is True

Ans - a. Both i & ii are false
Explanation –
Functional Design is also Known as Front-End Design whereas Physical Design is also known as Back-End Design

4. Single line comments in verilog start with #
    a. True
    b. False

Ans – b. False
Explanation – Single line comments in verilog starts with //

5. We can design a memory element using Dataflow model
    a. True
    b. False

Ans – b. False
Explanation – We cannot design a memory element using a data flow model because in dataflow model outputs are defined in terms of input signal transformation i.e. only combinational elements can be deigned.

6. Given below a code of an module

```
module unknown(
        output a,b,c,d,
        input e,f);
            wire ne,nf;
            not inv1(nf,f);
            not inv2(ne,e);
            and A1(a,ne,nf);
            and A2(b,ne,f);
            and A3(c,e,nf);
```

and A4(d,e,f);
endmodule

the above module represents

a. Encoder
b. Decoder
c. Multiplexer
d. None of the Above

Ans – b. Decoder
Explanation- the module takes ‘e’ and ‘f’ as input and produces all 4 combinations of them.

7. Assign statement in dataflow modeling are executed parallely
   a. True
   b. False

Ans – a. True
Explanation – assign statements are concurrent in nature and thus are executed when there is an change in a variable on the right hand side of statement.

8. Parameters are compile time constants
   a. True
   b. False

Ans – b. False
Explanation – Parameters are runtime constants, are declared within a module, their scope lies within a module, can be overwritten during component instantiation and are used to make code scalable.

9.

The default value of variable is

a. X
b. 1
c. Z
d. 0

Ans – a. X
Explanation – By default variable have the value as ‘x’

10.

The default value of net is

a. X
b. 1
c. Z
d. 0

Ans – c. Z
Explanation - Net’s default value is ‘z’ i.e. high impedance

11.

Which type of device FPGA are?

a. SLD
b. SROM
c. EPROM
d. PLD

Ans – d. PLD
Explanation - Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.