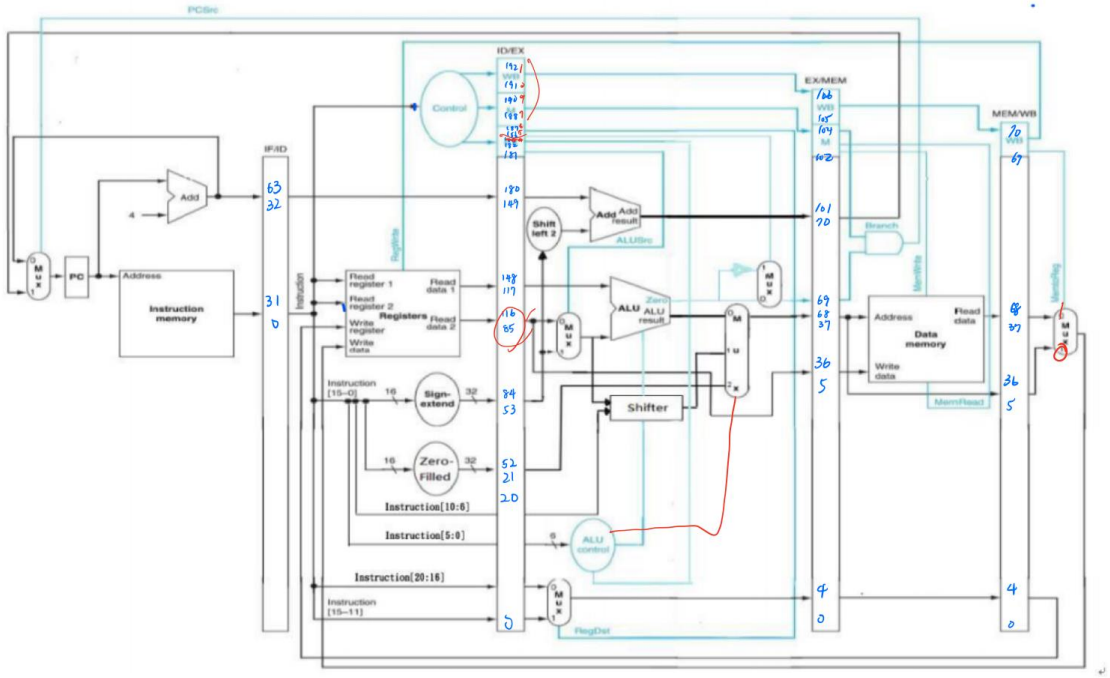
Computer Organization Lab5

The input fields of each pipeline register:

3. **Pipelined CPU**
   A. **Architecture diagram**



Compared with lab4, the extra modules:

Pipeline_Reg: 4 個存 Pipeline data & signal 的 register

Explain your control signals in sixth cycle (both test data

CO_P5_test_data1 and CO_P5_test_data2 are needed)

CO_P5_test_data1

MemtoReg: 0

RegWrite: 1

MemRead: 0

MemWrite: 0

RegDst:1

PCSrc:0

AluOP:010

ALUSrc:0

CO_P5_test_data2

RegWrite: 1

MemtoReg: 0

RegDst:0

PCSrc:0

AluOP:011

ALUSrc:1

MemRead: 0

MemWrite: 0

Problems you met and solutions:

原本想要分很多個 reg，後來發現題目要求用 4 個 reg，所以要一個一個算每個 reg 的大小(如圖)，中間有算錯幾次就不能跑

還有最後的 MemWriteReg 的 01 訊號是跟 Lab4 Reference 相反的，也是

找了一段時間才找到

Summary:

這個作業學會了如何在 CPU 中使用 pipeline reg 暫存 data & signal 達到加速執行的效果