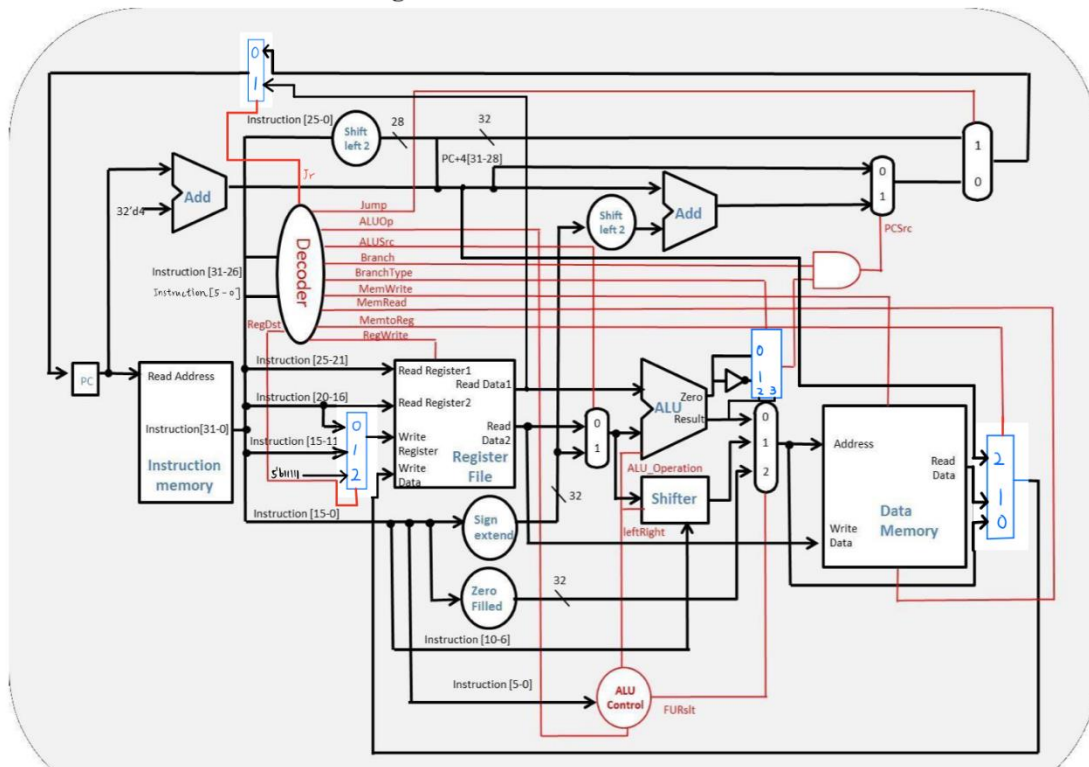


# Computer Organization Lab4

## 1. Architecture diagrams:

### 4. Architecture Diagram



## 2. Hardware module analysis:

Mux2to1: 2to1 的選擇器

Mux3to1: 3to1 的選擇器

Mux4to1: 4to1 的選擇器

Adder: 加法器

ALU: 對兩個輸入依照 ALU\_operation 進行運算

ALU\_Ctrl: 依照 funct, ALUOP 決定 FURslt, ALU\_operation, leftRight

**Data\_Memory:** 讀/寫記憶體

**Decoder:** 依照 opcode, funct(Jr 會用到)決定 Jr, Jump, RegDst, RegWrite, ALUOP, ALUSrc, Branch, BranchType, MemWrite, MemRead, MemtoReg.

**Instr\_Memory:** 讀 Instruction

**Program\_Counter:** 控制 PC

**Reg\_File:**控制 Register

**Sign\_Extend:** 把 16bit extend 到 32bit, 維持正負號

**Zero\_Filled:** 把 16bit 前面補 0 補到 32bit

**Shifter:** 把輸入進行位移

### **3. Finished part:**

All

### **4. Problems you met and solutions:**

加分題一開始完全沒頭緒要怎麼做，後來想到可以增加控制訊號及用 mux 解決 (像我額外寫了 4to1 的 mux)，改了以後又發現某些 module 也要一起改，來來回回確認很容易看錯。

### **5. Summary:**

寫這個作業想的時候花很多時間，但最麻煩的時候是 debug，我第一次可以跑

的時候是 17 分，發現有一個字大小寫打錯變 49 分，後來又發現有一個地方

1' b1 打成 1' b0，改完後就全對了。人生好難~

```
命令提示字元 - vvp lab4
> finish
** Continue **

C:\Users\USER\Desktop\lab4>iverilog -o lab4 TestBench.v

C:\Users\USER\Desktop\lab4>vvp lab4
WARNING: TestBench.v:140: $readmemb(CO_P4_test_data1.txt): Not enough words in the file for the requested range [0:31].

=====
(A) basic score:          75 / 75
=====
    Congratulation. You pass TA's pattern
=====
TestBench.v:600: $stop called at 270000 (lps)
** VVP Stop(0) **
** Flushing output streams.
** Current simulation time is 270000 ticks.
> finish
** Continue **

C:\Users\USER\Desktop\lab4>iverilog -o lab4 TestBench.v

C:\Users\USER\Desktop\lab4>vvp lab4
=====
(B) advance set1:         15 / 15
=====
    Congratulation. You pass TA's pattern
=====
TestBench.v:600: $stop called at 5720000 (lps)
** VVP Stop(0) **
** Flushing output streams.
** Current simulation time is 5720000 ticks.
> finish
** Continue **

C:\Users\USER\Desktop\lab4>iverilog -o lab4 TestBench.v

C:\Users\USER\Desktop\lab4>vvp lab4
WARNING: TestBench.v:142: $readmemb(CO_P4_test_data2_2.txt): Not enough words in the file for the requested range [0:31].

=====
(C) advance set2:         10 / 10
=====
    Congratulation. You pass TA's pattern
=====
TestBench.v:600: $stop called at 180000 (lps)
** VVP Stop(0) **
** Flushing output streams.
** Current simulation time is 180000 ticks.
```