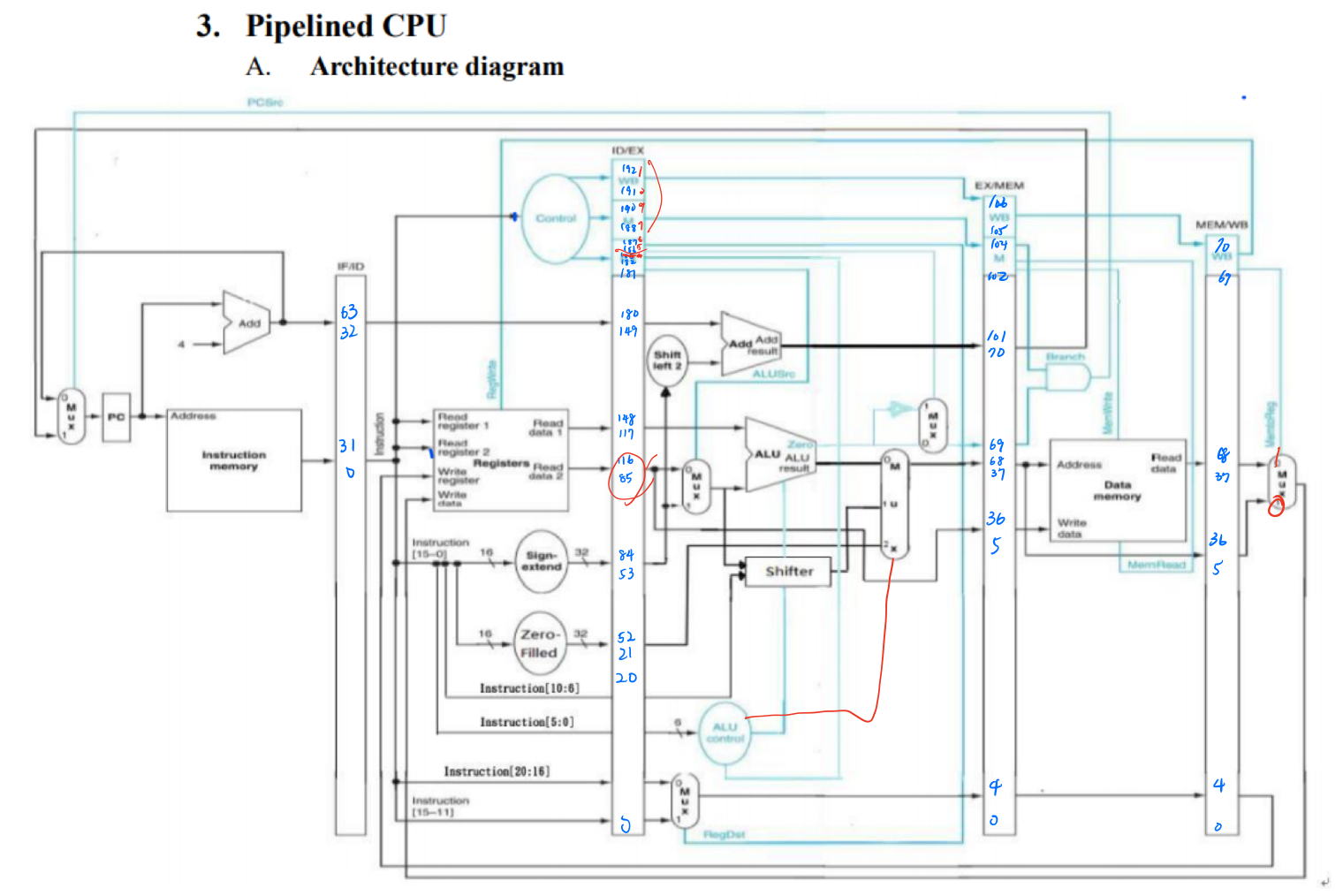
**Computer Organization Lab5**

**The input fields of each pipeline register:**

****

**Compared with lab4, the extra modules:**

**Pipeline\_Reg: 4個存Pipeline data & signal的 register**

**Explain your control signals in sixth cycle (both test data**

**CO\_P5\_test\_data1 and CO\_P5\_test\_data2 are needed)**

**CO\_P5\_test\_data1**

**MemtoReg: 0**

**RegWrite: 1**

**MemRead: 0**

**MemWrite: 0**

**RegDst:1**

**PCSrc:0**

**AluOP:010**

**ALUSrc:0**

**CO\_P5\_test\_data2**

**RegWrite: 1**

**MemtoReg: 0**

**RegDst:0**

**PCSrc:0**

**AluOP:011**

**ALUSrc:1**

**MemRead: 0**

**MemWrite: 0**

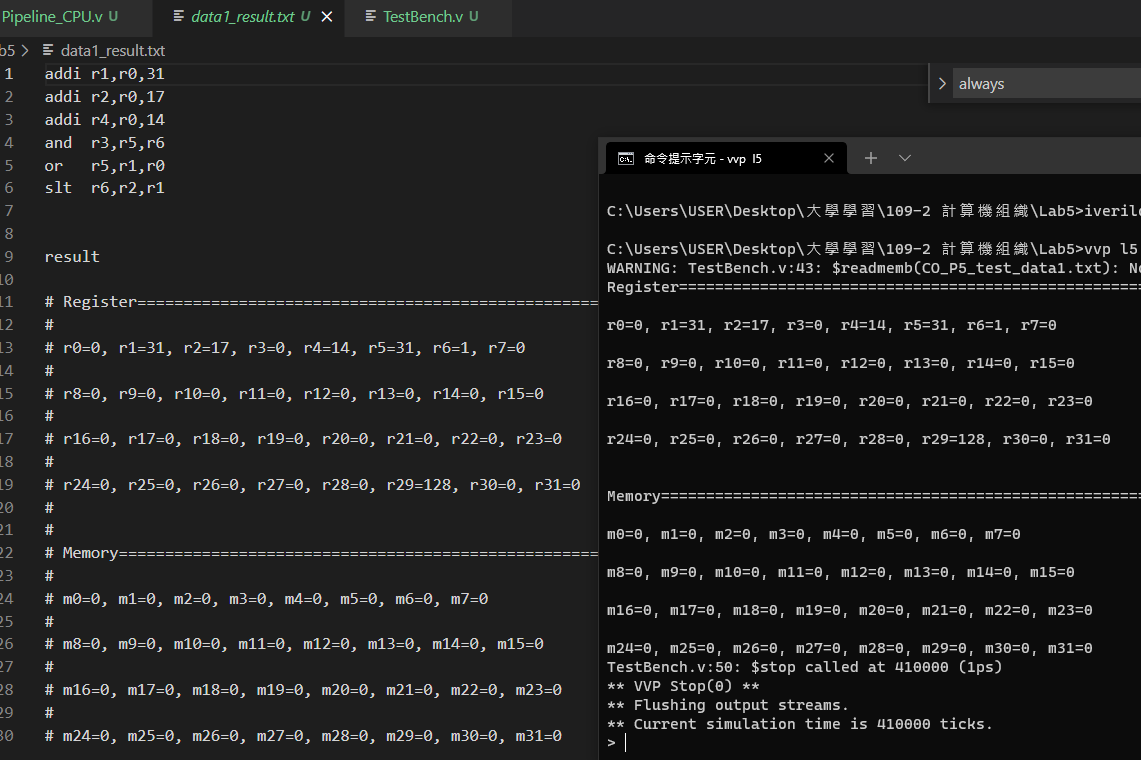
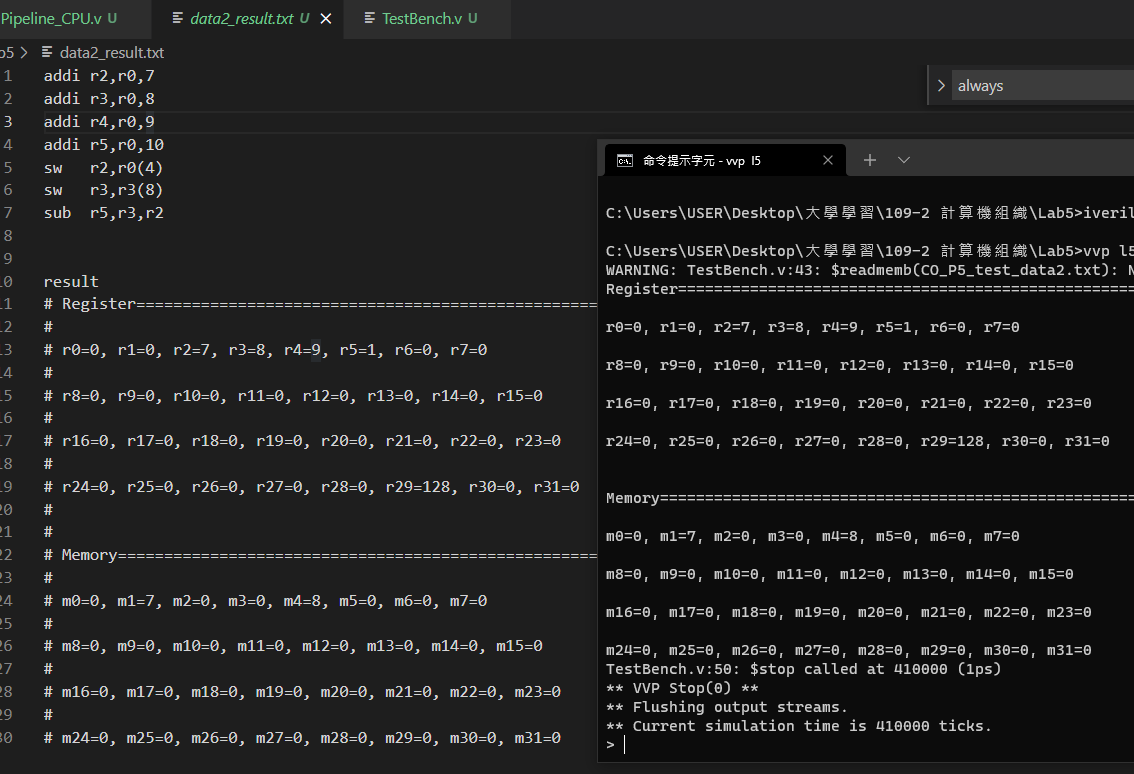
**Problems you met and solutions:**

**原本想要分很多個reg，後來發現題目要求用4個reg，所以要一個一個算每個reg的大小(如圖)，中間有算錯幾次就不能跑**

**還有最後的MemWriteReg的01訊號是跟Lab4 Reference 相反的，也是找了一段時間才找到**

**Summary:**

**這個作業學會了如何在CPU中使用pipeline reg暫存data & signal達到加速執行的效果**

**+**