Experiment No. 2

Title: Design combinational logic circuit using Logic Gates.

Batch: B1 **Roll No.: 16010420133** **Experiment No.: 2**

Aim: Design combinational logic circuit using Logic Gates.

Resources needed: Simulation Platform

Theory:

What is Combinational Logic Circuit?

Ans:

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are following −

- The output of combinational circuit at any instant of time, depends only on the levels present at input terminals.
- The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

Block diagram

Procedure:

a) Design combinational circuit for
   i. 4 bit Binary to Gray code converter
   ii. 4 bit Even Parity checker
b) Simulate both the designed circuits.
c) Verify the designed truth table.
d) Upload the Schematic Diagram generated on Simulation Software as well as Writeup containing Questions asked in writeup, CO and Conclusion.
e) Please note every document uploaded on google classroom should be labelled as Exp_<No>_<RollNo>_<schematic/writeup>.pdf

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Observations and Results: Observe the output for different input combinations.

Problem: To design 4 bit Binary to Gray code converter

Outcomes:-

Inputs: $B_3B_2B_1B_0$
Outputs: $G_3G_2G_1G_0$

Input				Output			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Expressions are:-

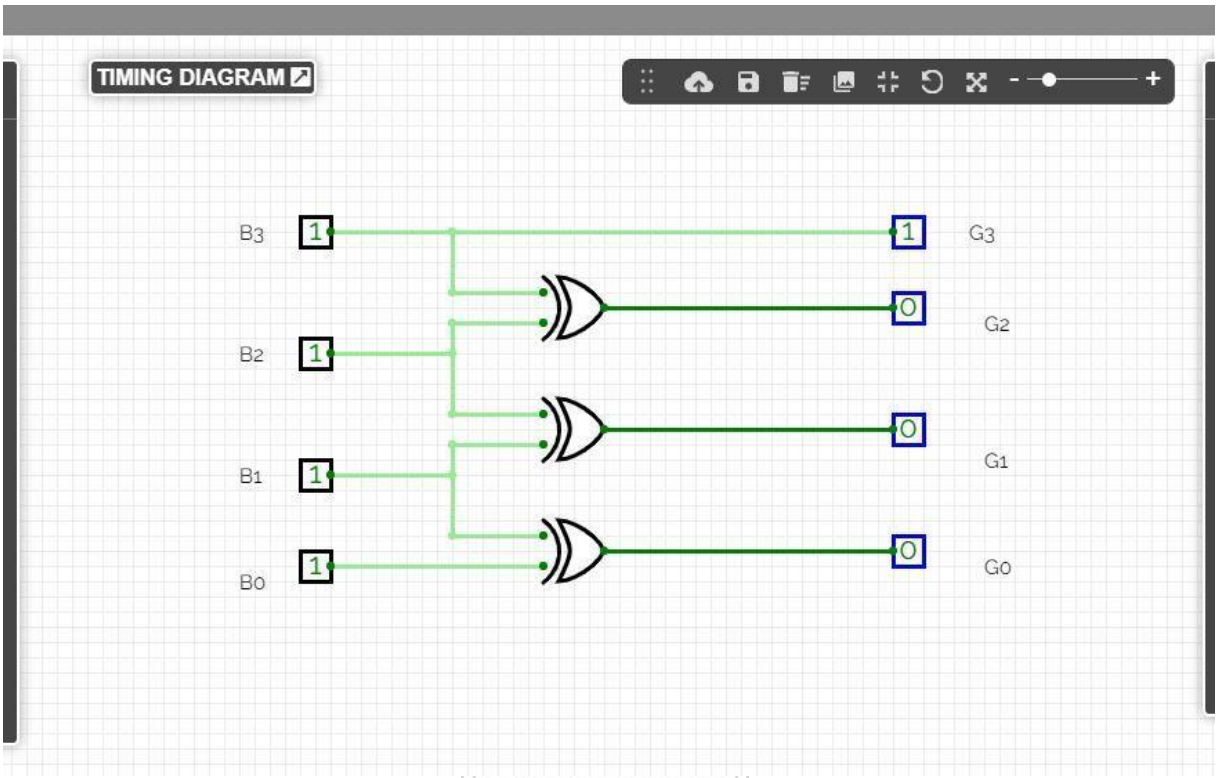
G3=B3

G2=B3 $\oplus$ B2

G1=B2 $\oplus$ B1

G0=B1$\oplus$ B0

Simulation:-



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Problem: To design a 4 bit Even Parity Checker

Inputs: ABCD

Output: Y

Truth Table:
Considering,
0 to be No error
1 to be error

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

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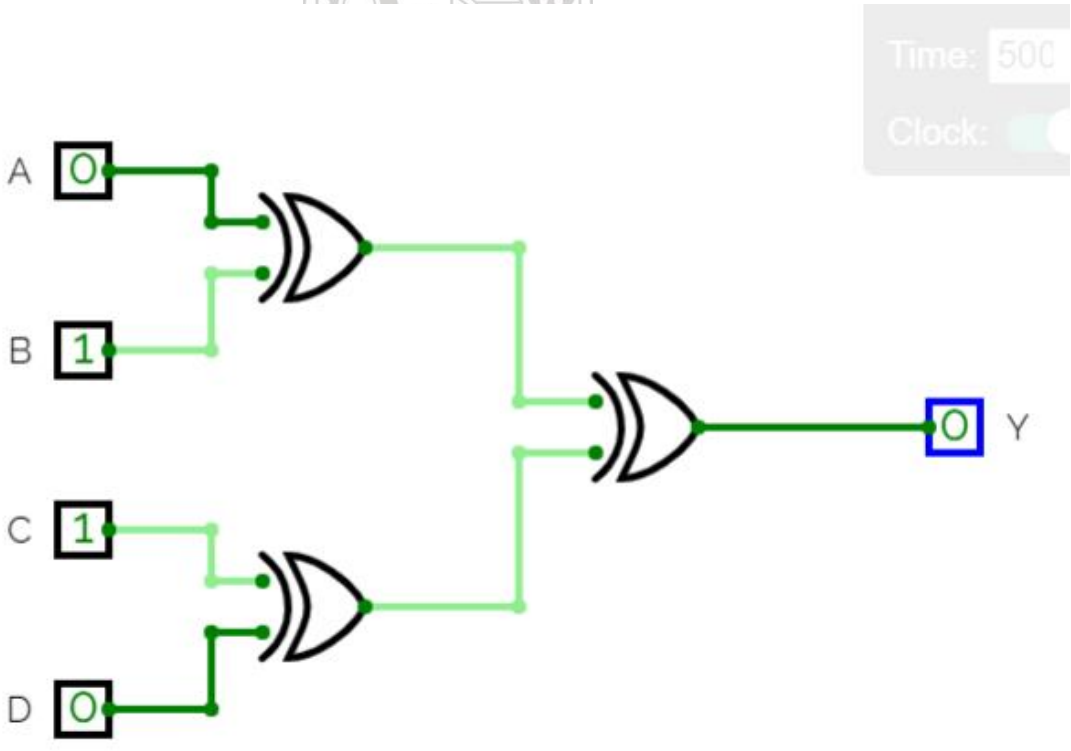
CircuitVerse Simulation:



Outcomes: Design the combinational and sequential circuits using basic building blocks

Conclusion:

In this chapter, the design of basic cells has been reviewed. The specific design of the XOR gate has been detailed, as well as the complex gates.

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill

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