Experiment No. 5

Title: Implementation of 3 bit synchronous up-down counter using T flips flops

Batch: B1 **Roll No.: 16010420133** **Experiment No.: 5**

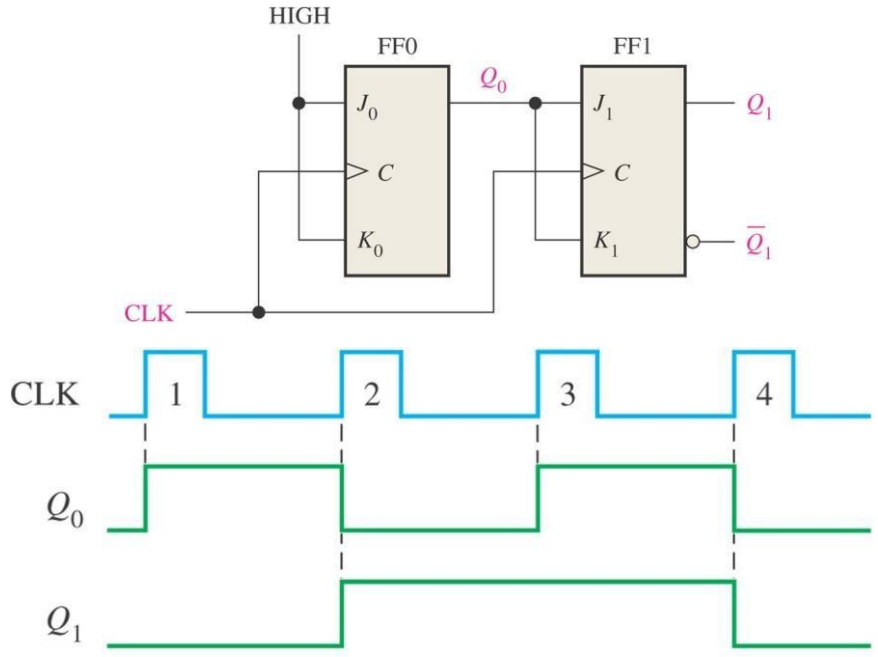
Aim: Implementation of 3 bit synchronous up-down counter using T flips flops

Resources needed: Simulation Software, (Circuitverse).

Theory:

Synchronous Counter Operation
Synchronous counters have a common clock pulse applied simultaneously to all flip-flops.

A 2-Bit Synchronous Binary Counter
Note that both the J and K inputs are connected together. The flip-flop will toggle when both are a 1 (FF0) Also the transition at clock pulse 2 works because of propagation delay effects. Q0 is still high on the input of Q1 at the instant clock 2 hits so FF1 changes state. A short time later clock 2 has propagated through FF0 and it goes low.



Truth table of J K flip flop

Inputs			Outputs		comments
J	**K**	**CLK**	**Q_1**	**Q'_1**	
0	0	↑	Q_0	Q'_0	No change
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	Q'_0	Q_0	Toggle

Design procedure of Synchronous counter

1. Find the number of flip-flops.
2. Write the count sequence in tabular form
3. Determine the flip-flop inputs which must be present for desired next state from the present state using excitation table of the flip-flops.
4. Prepare K-map for each flip-flop input in terms of flip-flop outputs as the input variables.
5. Simplify the K-maps and get the minimized expressions for each flip-flop input.
6. Connect the circuit using flip-flops and other gates corresponding to the minimized expression.

Design A 3-Bit Synchronous up- down Binary Counter using T flip-flops: (Include the timing diagram)

Solution: (Design the counter step by step- Create a soft copy or use separate assignment sheet and scan for solution)

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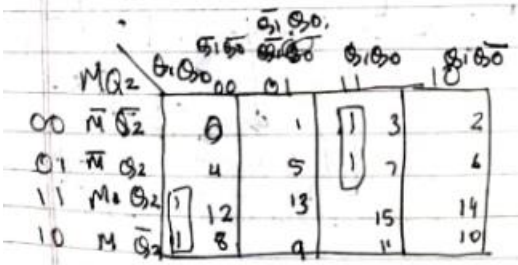
Truth Table Present state, Next state, ip of FF

No	control ip (M)	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	1
1	0	0	0	1	0	1	0	0	1	1
2	0	0	1	0	0	1	1	0	0	1
3	0	0	1	1	0	0	0	1	1	1
4	0	1	0	0	1	0	1	0	0	1
5	0	1	0	1	1	1	0	0	1	1
6	0	1	1	0	1	1	1	0	0	1
7	0	1	1	1	1	0	0	1	1	1
8	1	0	0	0	0	1	1	1	1	1
9	1	0	0	1	1	0	0	0	0	1
10	1	0	1	0	0	0	1	0	1	1
11	1	0	1	1	0	1	0	0	0	1
12	1	1	0	0	0	1	1	1	1	1
13	1	1	0	1	1	0	0	0	0	1
14	1	1	1	0	1	0	1	0	1	1
15	1	1	1	1	1	1	0	0	0	1

K Map:-



$T_2 = M\bar{Q}_1\bar{Q}_0 + \bar{M}Q_1Q_0$

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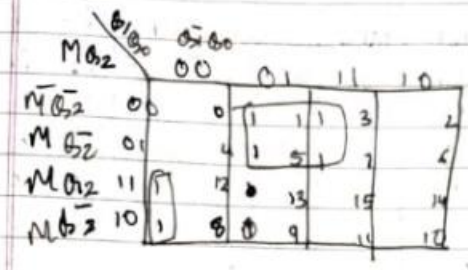
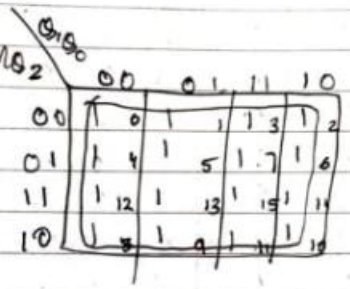


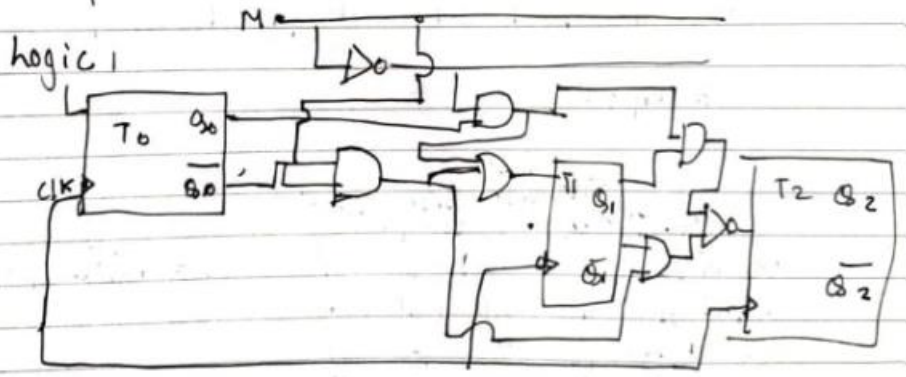
$T_1 = \bar{M}Q_0 + M\bar{Q_0}$



$T_0 = 1$

Implementation

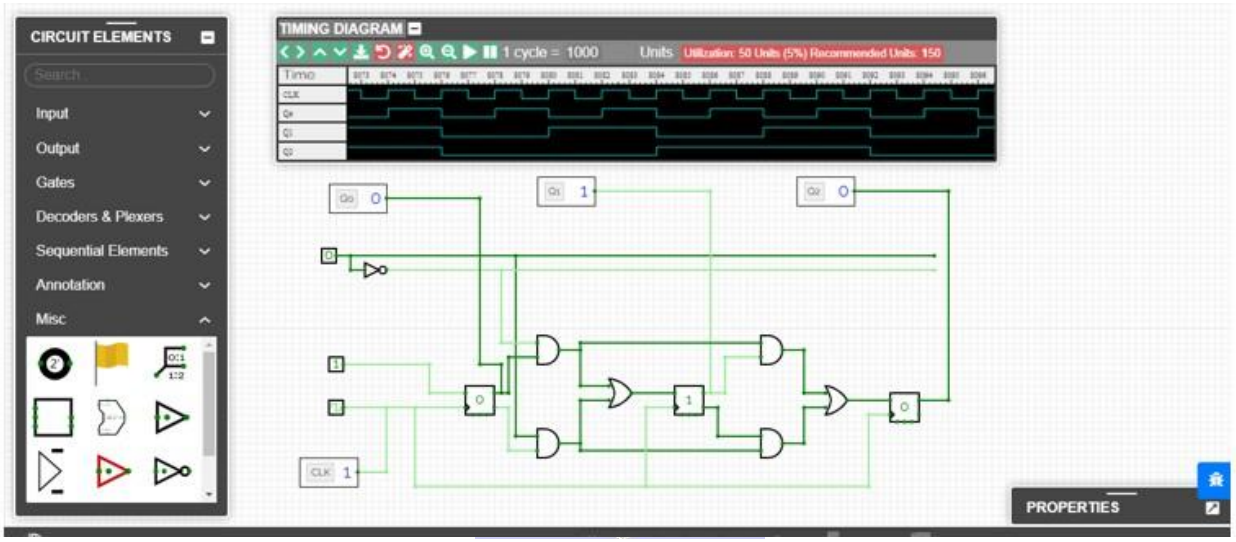
logic 1

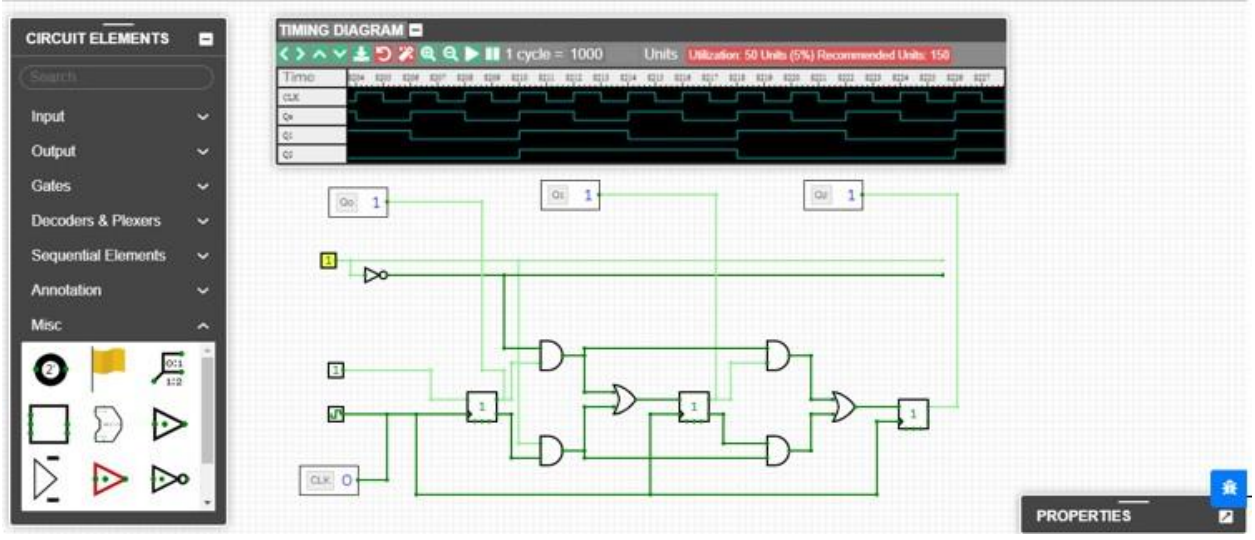


Procedure:

1. Design a 3 bit synchronous counter using T flip-flop as per the design procedure mentioned in theory.
2. Simulate the logic design using T flip-flops on the simulation software.
3. Verify the output of the designed and simulated counter for the proper sequence.
4. Generate the output timing diagram on simulator.
5. Upload Schematic and Timing Diagram generated on Simulator as instructed during lab session.

Observations and Results: Observe the UP-DOWN counter timing diagram as per actual outputs and identify the changes needed in the counter circuit to make the circuit work only as 3bit UP counter.





Outcomes: Design the combinational and sequential circuits using basic building blocks.

Conclusion: We have successfully implemented a 3 bit synchronous up-down counter using T flips flops.

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of faculty in-charge with date

References:

Books/ Journals/ Websites:

1. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill.
2. http://www.electronics-tutorials.ws/counter/count_4.html