Soumil Krishnanand Heble

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Education

Master of Science, Computer Engineering **GPA: 4.00**

North Carolina State University, Raleigh, NC **Anticipated May 2020**

Coursework: Microprocessor Architecture, Architecture of Parallel Computers, ASIC and FPGA Design, Advanced Microarchitecture, ASIC Verification and Data Parallel Processors

Bachelor of Technology, Electronics & Instrumentation Engineering **GPA: 9.23**

Vellore Institute of Technology (VIT), Vellore, India **May 2016**

VIT University Merit Scholarship Holder, 2016, Top 10% of the class

Technical Skills

Software Skills: • C/C++ • OpenMP • Verilog • Python • Linux • Bash • Git

Technical Software: • ModelSim • Synopsys Design Compiler • Autodesk EAGLE • MATLAB • NI Multisim

Work Experience

Indian Institute of Technology, Hyderabad, India **Aug 2016 – Jul 2018**

Project Assistant, Wireless Networks Lab

- Built, fabricated and debugged an IEEE 802.15.4 wireless transceiver (IITH Mote) for low power, low data-rate applications and achieved a 36x lower standby power consumption compared to previous designs.
- Adapted Contiki OS for IITH Mote and developed sensor drivers for the OS and a multi-hop network based on Contiki's Link Layer Rime Protocol.
- Led a team of four to deploy a 30 node IoT network to monitor crop growth environment as a part of a 5 year collaborative project between IIT Hyderabad and University of Tokyo, Japan.

Projects

Cache Coherence Protocol Simulator for Symmetric Multiprocessing Systems **Dec 2018**

- Explored the impact of snoopy, bus based write invalidate (MSI, MESI) and write update (Dragon) cache coherence protocols on coherence misses, bus transaction traffic and memory I/O traffic by designing a simulator for SMP systems.

SHA256 Hardware Accelerator **Nov 2018**

- Engineered a SHA256 hardware accelerator using Verilog HDL and verified functionality by comparing results with a high level language implementation of the algorithm in python.
- Synthesized the design with Synopsys design compiler utilizing 45nm standard cells and achieved a cell area of 15852 um^2, verified setup and hold timings for a clock speed of 125 MHz.

Cache Memory Hierarchy Simulator **Oct 2018**

- Devised a configurable cache memory hierarchy simulator that accepts a CPU memory access trace and prints out key memory hierarchy performance metrics.
- Programmed a generic cache structure with optional victim cache and uses the LRU replacement policy and WBWA write policy. Different hierarchy configurations were simulated and compared with the help of CACTI data from HP.

Extracurricular Activities

- Runner-up in VIT Embedded Design Contest, 2013, for formulating a touch-screen gaming console
- Mentored students in practical electronics as Innovation Head and Core Committee Member of The Electronics Club (TEC), VIT
- Managed inter-university events as a Board Member of IEEE Robotics and Automation Society, VIT University Chapter (2014-2015)

Additional Projects

Dynamic Instruction Scheduling Simulator for Superscalar Out-of-Order Pipeline **Dec 2018**

- Designed a dynamic instruction scheduler for an N instruction wide superscalar out-of-order pipeline that accepts a dynamic instruction trace with 3 types of arithmetic instructions of 1, 2 and 5 execution cycles.
- The performance of the pipeline was evaluated for various sizes of issue queue, re-order buffer and pipeline width for GCC and Perl trace files and the best configuration was selected for each trace.

Dynamic Branch Predictor Simulator **Nov 2018**

- Developed a dynamic branch predictor simulator that accepts a branch address trace and reports branch prediction rate for the model being simulated.
- Modelled bimodal, gshare and a bimodal-gshare hybrid branch predictors with 2-bit counter for each entry in the branch prediction table.

WiFi Connected IoT Plant Monitor **May 2016**

- Constructed an IoT plant health monitoring and irrigation optimization system based on ESP8266 WiFi module and published the data on an online IoT cloud platform using MQTT protocol.
- Achieved 48% water savings over the on-campus irrigation system using local soil moisture data and weather forecast data obtained from the Internet.

Muscle Controlled Robotic Arm **Sept 2014**

- Designed an analog front-end for 3 lead EMG (muscle activity) acquisition system and performed ADC, filtering and FFT using TI MSP430 development board.
- Team member for the project titled "Muscle Controlled Robotic Arm" which was a contender in the Texas Instruments India Analog Design Challenge of 2014.

Publications

- **S.Heble**, A.Kumar, K.V.V.D.Prasad, S.Samirana, P.Rajalakshmi and U.B.Desai, "A low power IoT network for smart agriculture," 2018 IEEE 4th World Forum on Internet of Things, doi:10.1109/WF-IoT.2018.8355152
- M.Subashini, S.Das, **S.Heble**, U.Raja and R.Karthik, "Internet of Things based Wireless Plant Sensor for Smart Farming," May 2018, Indonesian Journal of Electrical Engineering and Computer Sciences