Soumil Krishnanand Heble

+1 (919) 985-0666 • soumil.heble@gmail.com • linkedin.com/in/soumilheble • github.com/soumilheble

Education

Master of Science, Computer Engineering **GPA: 4.00/4.00**
North Carolina State University, Raleigh, NC Anticipated Dec 2019

Bachelor of Technology, Electronics & Instrumentation Engineering **GPA: 9.23/10.00**
Vellore Institute of Technology (VIT), Vellore, India May 2016
VIT University Merit Scholarship Holder, 2016, Top 10% of the class

Skills

Software Skills: C, C++, Verilog, SystemVerilog, Linux, Git, Perforce, UVM, Bash, Make, Python, Doxygen

Technical Software: ModelSim, Questa, Synopsys Design Compiler, Synopsys DVE/Verdi, Autodesk EAGLE, NI Multisim

Coursework: Microprocessor Architecture, Architecture of Parallel Computers,
ASIC and FPGA Design, Advanced Microarchitecture, ASIC Verification, Computer Networks,
Electronic System Level and Physical Design, Advanced Verification with UVM and Quantum Computing Architecture

Experience

Co-op Engineer - Cores Verification, AMD Inc., Boxborough, MA May 2019 – Aug 2019

- Enabled SV Assertions and Synthesizable Checkers in the Hybrid Emulation Model for next generation flagship AMD x86 CPU Core. Root-caused issues with emulation infrastructure and collaborated with tool vendor to fix the issues.
- Collaborated with the physical design team and emulation/simulation tool vendor in the project to explore viability of using emulation flow generated data for low-level power analysis.
- Ported and Enabled infrastructure for running Emulation flow based regressions on future generation flagship AMD x86 CPU Core by resolving the infrastructure and testbench issues.

Projects

Functional Verification of OpenCores I^{2}C Master Bus Controller May 2019

- Designed a complete testbench in SystemVerilog for functional verification of an I^{2}C Multiple Bus Controller IP.
- UVM style base classes were used to develop the Verification IP to enable horizontal and vertical reuse.
- Devised a test plan and wrote a mix of directed and randomized tests to achieve 92.35% coverage with 86.75% code coverage.

Store Vector Memory Dependence Predictor (Group Project) May 2019

- Retrofitted a cycle accurate model of a RISC-V based superscalar core with Store Vector based memory dependence predictor and carried out sensitivity analysis and compared performance with Sticky Bit and Oracle memory dependence predictors.
- Under ideal conditions (no bottlenecks) the average performance across AStar and Hmmer SPEC CPU2006 benchmarks is about 1.12x (compared to sticky bit) but the advantage is negligible once real branch prediction is turned on.

Cache Coherence Protocol Simulator for Symmetric Multiprocessing Systems Dec 2018

- Explored the impact of snoopy, bus based write invalidate (MSI, MESI) and write update (Dragon) cache coherence protocols on coherence misses, bus transaction traffic and memory I/O traffic by designing a simulator for SMP systems.

Superscalar Out-of-Order Pipeline Simulator Dec 2018

- Designed an N instruction wide superscalar out-of-order pipeline that accepts a dynamic instruction trace with 3 types of arithmetic instructions of 1, 2 and 5 execution cycles.
- The performance of the pipeline was evaluated for various sizes of issue queue, re-order buffer and pipeline width for GCC and Perl trace files and the best configuration was selected for each trace.

SHA256 Hardware Accelerator Nov 2018

- Synthesized the design RTL using Synopsys design compiler utilizing 45nm standard cells and achieved a cell area of 15852 um^2, verified setup and hold timings for a clock speed of 125 MHz.
- Improved the design clock speed by pipelining certain parts of the algorithm and used parallel prefix adders to reduce combinational logic delay.

Cache Memory Hierarchy Simulator Oct 2018

- Developed an N level cache hierarchy simulator with an optional victim cache at each level. The simulator uses the least recently used replacement policy with write-back write-allocate policy.
- A combination of hierarchies were simulated, upto level 2 cache and their performance was compared on the metrics of area, cache access misses and memory transaction count.