Soumil Krishnanand Heble

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Education

Master of Science, Computer Engineering — GPA: 4.00/4.00

North Carolina State University, Raleigh, NC — **Anticipated Dec 2019**

Coursework: ASIC Verification, Advanced Microarchitecture, ASIC and FPGA Design, Microprocessor Architecture, Architecture of Parallel Computers and Computer Networks

Bachelor of Technology, Electronics & Instrumentation Engineering — GPA: 9.23/10.00

Vellore Institute of Technology (VIT), Vellore, India — **May 2016**

Skills

Software Skills: C, C++, Verilog, SystemVerilog, Linux, Bash, Python, Git, GNU Make, Doxygen

Technical Software: ModelSim, Synopsys Design Compiler, Questa Advanced Simulator, Autodesk EAGLE, NI Multisim

Academic Projects

Functional Verification of OpenCores I^2C Multiple Bus Controller — Ongoing

- Developed an I^2C Bus Functional Model using SystemVerilog to interface with the DUT.
- Currently developing a class based, structured testbench that enables horizontal and vertical reuse. The testbench will be used to perform constrained random test on the DUT.

MIPS R10000 Style Modern Superscalar Rename Stage for RISC-V Simulator — Feb 2019

- Implemented a physical register pointer based rename stage for a cycle-accurate, configurable superscalar RISC-V microprocessor simulator.

Cache Coherence Protocol Simulator for Symmetric Multiprocessing Systems — Dec 2018

- Explored the impact of snoopy, bus based write invalidate (MSI, MESI) and write update (Dragon) cache coherence protocols on coherence misses, bus transaction traffic and memory I/O traffic by designing a simulator for SMP systems.

Superscalar Out-of-Order Processor Simulator — Dec 2018

- Designed a configurable, N wide, superscalar out-of-order processor based on Tomasulo's algorithm.
- Analyzed the effect of varying the issue queue size and superscalar width on the peak IPC of the processor.

SHA256 Hardware Accelerator — Nov 2018

- Synthesized the accelerator RTL using Synopsys Design Compiler utilizing 45nm standard cells and achieved a cell area of 15852 um^2, verified setup and hold timings for a clock speed of 125 MHz.
- Improved the design clock speed by pipelining certain parts of the algorithm and used parallel prefix adders to reduce combinational logic delay.

Dynamic Branch Predictor Simulator — Nov 2018

- Developed a dynamic branch predictor simulator that accepts a branch address trace and reports branch prediction rate for the model being simulated.
- Modelled bimodal, gshare and a bimodal-gshare hybrid branch predictors with 2-bit counter for each entry in the branch prediction table.

Cache Memory Hierarchy Simulator — Oct 2018

- Developed an N level cache hierarchy simulator with an optional victim cache at each level. The simulator uses the least recently used replacement policy with write-back write-allocate write policy.
- Different hierarchy configurations were simulated and compared with the help of CACTI data from HP.

Experience

Indian Institute of Technology, Hyderabad, India — Aug 2016 – Jul 2018

Project Assistant, Wireless Networks Lab

- Redesigned and fabricated an IEEE 802.15.4 wireless transceiver (IITH Mote) for low power, low data-rate applications and achieved a 36x lower stand-by power consumption compared to the previous design.
- Adapted Contiki OS for IITH Mote and developed sensor drivers for the OS and a multi-hop network based on Contiki's Link Layer Rime Protocol.
- Led a team of four to deploy a 30 node IoT network to monitor crop growth environment as a part of a 5 year collaborative project between IIT Hyderabad and University of Tokyo, Japan.

Leadership

- Mentored students in practical electronics as Innovation Head and a Core Committee Member of The Electronics Club (TEC) at the Vellore Institute of Technology.