Verilog Assignment 7: Design and synthesize a 32-bit processor using Verilog

Instruction Set Design

Instruction Format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

opcode	*Rs*	*Rt*	*Rd*		*func*

opcode	*Rs*	*Rt*	*shamt*	*func*

opcode	*Rs*		*Immediate(16-bit)*	*func*

opcode	*Rs*	*Rt*		*func*

opcode		*Immediate(26-bit)*

Operation Encoding:

Operation	Opcode	Function encoding
Arithmetic and Logic Instructions:		
ADD	000	00000
ADDI	000	00001
SUB	000	00010
SUBI	000	00011
AND	000	00100
ANDI	000	00101
OR	000	00110
ORI	000	00111
XOR	000	01000
XORI	000	01001
NOT	000	01010
SLA	000	01011
SLAI	000	01100
SRA	000	01101
SRAI	000	01110
SRL	000	01111
SRLI	000	10000

Operation	Opcode	Function encoding
Load and Store Instructions:		
LD	001	00000
ST	001	00001
LDSP	001	00010
STSP	001	00011
Branch Instructions:		
BR	010	00000
BMI	010	00001
BPL	010	00010
BZ	010	00011
Stack Instructions:		
PUSH	011	00000
POP	011	00001
CALL	011	00010
RET	011	00011
Register to Register Transfer:		
MOVE	100	-
Program Control:		
HALT	101	00000
NOP	101	00001

Register Encoding:

Register	Register Encoding	Register	Register Encoding
R0	00000	R9	01001
R1	00001	R10	01010
R2	00010	R11	01011
R3	00011	R12	01100
R4	00100	R13	01101
R5	00101	R14	01110
R6	00110	R15	01111
R7	00111	SP	10000
R8	01000	PC	---

Control Unit Design

Datapath and Control Signals Schematic diagram: