COURSE-WISE SYLLABUS

Semester III

Year	2	**Course Code:** 21BSC3C3ELE1L	**Credits**	**04**
Sem.	3	**Course Title: Programming in C and Digital Design using Verilog**	**Hours**	**60**

Course Pre-requisites, if any	NA	
Formative Assessment Marks: 40	Summative Assessment Marks: 60	Duration of ESA: 2 hrs.

Course Objectives	After the successful completion of the course, the student twill be able to: ➢ The ability to code and simulate any digital function in Verilog HDL. ➢ Know the difference between synthesizable and non-synthesizable code. ➢ Understand library modelling ,behavioural code and the differences between simulator algorithms and logic verification using Verilog simulation. ➢ Learn good coding techniques required for current industrial practices. Gain the knowledge of programming the system using C programming language
Course Outcomes	At the end of the course the student should be able to: 1.Reproduce the I-V characteristics of various MOSFET devices, 2.Explain the behaviour and characteristics of power devices such as UJT, SCR, Diac, Triac etc. 3.Calculate various device parameters' values from their V I characteristics. 4.Explain various Operational amplifier parameters 5.List various applications of Operational amplifier. 6.Explain IC 555 as a timer with applications 7.Understand K-Map and simplify Boolean expressions 8.Analyse combinatorial and sequential circuits
Unit No.	**Course Content**
Unit- I	**C Programming**: Introduction, Importance of C, Character set, Tokens, keywords, identifier, constants, basic data types, variables: declaration & assigning values. Structure of C program. Arithmetic operators, relational operators, logical operators, assignment operators, increment and decrement operators, conditional operators, bitwise operators, expressions and evaluation of expressions, type cast operator, implicit conversions, precedence of operators. **Arrays:** Basics of arrays, declaration, accessing elements, storing elements, two-dimensional and multi-dimensional arrays. Input output statement – sprintf(), scanf() and getch(), and library functions (math and string related functions). **(15 Hours)**
Unit- II	**Decision making, branching, and looping**: if, if-else, else-if, switch statement, break, for loop, while loop and do loop. **Functions**: Defining functions, function arguments and passing, returning values from functions, example programs. **Pointers**: Pointer declaration, assigning values to pointers, pointer arithmetic, array names used as pointers, pointers used as arrays, pointers and text strings, pointers as function parameters. **Structures**: Structure type declarations, structure declarations, referencing structure

	members, referencing whole structures, initialization of structures, structure bit fields. **(15 Hours)**
Unit -III	**Overview of Verilog HDL**: Evolution of CAD, emergence of HDLs, typical HDL flow, Trends in HDLs. **Hierarchical Modelling Concepts**: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block, Lexical conventions. Data types, system tasks, compiler directives. **Modules and Ports**: Module definition, port declaration, connecting ports, hierarchical name referencing. **Gate-Level Modelling**: Modelling using basic Verilog gate primitives, Description of and/or and buf/not type gates, Rise, fall and turn-off delays, min, max, and typical delays. Combinational logic circuit design using Gate level modelling. **(15 Hours)**
Unit -IV	**Dataflow Modelling**: Continuous assignments, delay specification, expressions, operators, operands, operator types. **Behavioral Modelling**: Structured procedures, initial and always, blocking and non-blocking statements. Delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. **Tasks and functions**: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. Combinational and sequential logic circuit design using all three modelling. **(15 Hours)**
Recommended Leaning Resources	
Reference Books	1 Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis," 2nd Edition, Prentice Hall PTR, 2006. 2 E. Balagurusamy, "Programming in ANSI C", 4th Edition, Tata McGraw-Hill, 2008. 3 Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", 5th Edition, Springer, 2002. 4 Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition, Pearson Education, 2010. 5 Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley Eastern, 2016. 6 Nazeih M. Botors, "HDL Programming VHDL and Verilog", 1st Edition, Dreamtech Publication, New Delhi, 2006. 7 Yashavant P. Kanetkar, "Let us C", 18th Edition, BPB Publications, 2021. 8 T Jeyapoovan, "A First Course in Programming with C," Vikas Publishing Pvt LTD, 2004. 9 Kevin Skahill, "VHDL for Programmable Logic,"Pearson Education, 2006. 10 Cyril P R, "Fundamentals of HDL Design," Pearson, 2010.

Laboratory Experiments:

Year	I	**Course Code:** 21BSC3C3ELE1P	**Credits**	**2**
Sem.	1	**Course Title: Programming in C and Digital Design using Verilog**	**Hours**	**4 Hrs/week**
Formative Assessment Marks: 25		Summative Assessment Marks:25	Duration of ESA: 4 hrs.	
Note: Minimum of 08 programmes to be written and executed in each section				
Sl. No		**Part -A: Programming in C Laboratory**		
		Write and execute C Program to 1. Find the area and circumference of a circle 2. Find the biggest and smallest elements in a series		

	3. Find the factorial of a given number 4. Check the prime number in a series 5. Find the roots of quadratic equation 6. Find the gross salary of an employee 7. Remove all vowels from a string 8. Upper case and lower-case conversion and vice-versa 9. Reverse a string using library functions 10. Reverse a string without using library 11. Check whether the string is palindrome or not 12. Arrange the array in ascending and descending order using bubble sort 13. To perform arithmetic operations for a matrix. 14. Display prime numbers between intervals 0 to 100 15. Find GCD of two numbers.
	Part – B: Verilog HDL Laboratory
	Write and execute Verilog code to realize 1. Realization of logic gates. 2. Encoder without priority and with priority. 3. Multiplexer, De-multiplexer. 4. Comparator, Code converters – Binary to Gray and vice versa. 5. Adder/Subtractor (Half and Full) using different modelling styles. 6. 4-bit parallel adder and 4-bit ALU/8-bit ALU. 7. SR, D, JK, T-flip-flops. 8. To realize counters: Up/Down (BCD and Binary). 9. 4-bit Binary counter, BCD counters (Synchronous reset) and any arbitrary sequence counters. 10. 4-bit Binary counter, BCD counters (Asynchronous reset) and any arbitrary sequence counters. 11. Modelling of Universal shift registers.

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OPEN ELECTIVE

Year	2	**Course Code:** 21BSC3O3ELE3	**Credits**	03
Sem.	3	**Course Title: Application of Electronics-1**	**Hours**	40
Formative Assessment Marks: 40		Summative Assessment Marks: 60	Duration of ESA:.02 hrs.	

Unit No.	**Course Content**	**Hours**
Unit I	**BasicElectronics** Introduction to circuit components- Resistors, capacitors, inductor, transformer, diode and transistor. Symbols, pimples. LED and LCD display, relay, fuse ,switches, wires.AC and DC applications.	(10 hours)
Unit II	**Applied Electronics** Electronicinstruments:DMM,CRO,Biomedicalinstruments-ECG,EEG,EMG,pHmeter,X-ray, sphygmomanometer, Glucometer, Digital thermometer. Sensor-OMR, MICR, Scanner, Barcode reader.	(10 hours)
Unit III	**Power Supplies** DC power supply, Rectifiers-principle, Types Inverter and UPS. Adopter and SMPS. Inverter and UPS. Mobile chargers.	(10 hours)
Unit IV	**Electronic calculators** Types, Functions of Basic calculators- block diagram, Scientific calculator Keypad ,use of calculator.	(10 hours)