Semester II

Year	I	Course Code: 21BSC2C2ELE2L	Credits	04
Sem.	1	Course Title: ANALOG AND DIGITAL ELECTRONICS	Hours	52

Course Pre-requisites, if any	NA	
Formative Assessment Marks: 40	Summative Assessment Marks: 60	Duration of ESA: 2 hrs.

Course Outcomes	At the end of the course the student should be able to: 1.Reproduce the I-V characteristics of various MOSFET devices, 2.Explain the behaviour and characteristics of power devices such as UJT, SCR, Diac, Triac etc. 3.Calculate various device parameters' values from their V I characteristics. 4.Explain various Operational amplifier parameters 5.List various applications of Operational amplifier. 6.Explain IC 555 as a timer with applications 7.Understand K-Map and simplify Boolean expressions 8.Analyse combinatorial and sequential circuits	
Unit No.	**Course Content**	**Hours**
Unit- I	**JFET**: Types - p-channel and n-channel, working and I-V characteristics - n-channel JFET, parameters and their relationships, Comparison of BJT and JFET. **MOSFET:** Enhancement MOSFET, Depletion MOSFET (n-channel and p-channel), Construction, working, symbols, drain and transfer characteristics, VMOS, UMOS Power MOSFETs, handling, MOS logic, symbols and switching action of MOS, NMOS inverter. **UJT:** Basic construction, working, equivalent circuit and I-V characteristics, intrinsic stand-off ratio, relaxation oscillator. **SCR:** Construction, VI characteristics, working, symbol, and applications – HWR and FWR. **DIAC and TRIAC:** Construction, working, characteristics, applications, (mention only).	**13**
Unit- II	**Operational Amplifier:** Qualitative study of Differential Amplifier, four modes of Differential Amplifier, Basic information of Op-amp (Types of IC Manufactures designations Package Types, Temperature ranges and pin identifications. Block diagram of Op-amp, ideal version of operational amplifier. Operational amplifier parameters input offset voltage, input offset current, input bias current, Total output offset voltage Thermal drift, CMRR and Slew Rate Explanation of voltage offset null circuit for 741. Concept of virtual ground. Voltage series (non-inverting) and Voltage-shunt (Inverting) negative feedback circuits' derivation of voltage gain input resistance, output resistance bandwidth and Total output offset voltage, numerical problems. **APPLICATIONS OF OP-AMPLIFIER:** Op-amp adder, Subtractor. Current to Voltage converter and Voltage to Current converter circuits, Low voltage DC voltmeter, Integrator, Differentiator, Qualitative study of op-amp as comparator. **Filter:** First order active filters- low pass & high pass Filters, band pass, band reject filters. (Qualitative only). **Timer (IC 555):** Introduction, Block diagram, Astable and Monostable multivibrator circuits. (Numerical Examples wherever applicable).	**13**
Unit -III	**Logic Families:** Logic Families-classification of digital ICs. Characteristics of logic families, circuit description of TTL NAND gate with totem pole	

	and open collector. TTL IC terminology. CMOS NAND, comparison of TTL and CMOS families. Combinational Logic Circuits: SOP and POS, Minterm, Maxterm, SOP, SPOS, Simplification of Boolean expressions, Karnaugh map (2, 3 and 4 variable map) Pair, quad and octets. Simplification of Boolean function using K-map (Overlapping groups, rolling the map, redundant group and Don't care conditions). **Design of Arithmetic logic circuits:** Half Adder, Full Adder, Half Subtractor, Full Subtractor. 4-bit parallel binary adder, 2-bit and 4-Bit magnitude comparator. Encoder, decimal to BCD priority encoder. Decoder, 2:4 decoder, 3:8 decoder, BCD to decimal decoder, BCD to 7-Segment decoder, Multiplexer - 4:1 and 8:1 multiplexer, Demultiplexer - 1:4 and 1:8 demultiplexer - logic diagram and truth table of each.	**13**
Unit -IV	**Sequential Logic Circuits:** Flip-Flops - SR Latch, RS, D and JK Flip-Flops. Clocked (Level and Edge Triggered) Flip-Flops. Pre-set and Clear operations. Race- around conditions in JK Flip-Flop. Master- Slave JK and T Flip-Flops. Applications of Flip-Flops in semiconductor memories, RAM, ROM and types. **Registers and Counters:** Types of Shift Registers, Serial-in-Serial-out, Serial-in- Parallel-out, Parallel-in-Serial-out and Parallel-in-Parallel-out Shift Registers (only up to 4 bits), applications. **Counters:** Ring counter, Johnson counter applications. **Asynchronous Counters:** Logic diagram, Truth table and timing diagrams of 4-bit ripple counter, modulo-n counters. **Synchronous Counter:** 4-bit decade Counters.	**13**
Recommended Leaning Resources		
Reference Books	(1) Electronic devices and circuit theory by Boylestad, Robert Nashelsky (2) Electronic Devices Conventional Current Version by Thomas L. Floyd (3) David A. Bell "Electronic Devices and Circuits", 5th Edition, Oxford Uni.Press, 2015 (4) OP-Amps and Linear Integrated Circuit, R. A. Gayakwad, 4th edn, 2000, Prentice Hall (5) Operational Amplifiers and Linear ICs, David A. Bell, 3rd Edition, 2011, Oxford University Press. (6) R.S. Sedha, "A Text book of Applied Electronics", 7th edition. S. Chand and Company Ltd. 2011 (7) Thomas L. Floyd, Digital Fundamentals, Pearson Education Asia (1994) (8) Digital Principles and Applications, A.P. Malvino, D.P. Leach and Saha, 7th Ed., 2011, Tata McGraw (9) Fundamentals of Digital Circuits, Anand Kumar, 2nd Edn, 2009, PHI Learning Pvt. Ltd. (10) Digital Circuits and systems, Venugopal, 2011, Tata McGraw Hill. (11) Digital Systems: Principles & Applications, R.J. Tocci, N.S. Widmer, 2001, PHI Learning. (12) Digital Electronics, S.K. Mandal, 2010, 1st edition, McGraw Hill	

Laboratory Experiments:

Year	I	Course Code: 21BSC2C2ELE2P	Credits	2
Sem.	1	Course Title: ANALOG AND DIGITAL ELECTRONICS *(Hardware and Circuit Simulation Software)*	Hours	4 Hrs/week
Formative Assessment Marks: 25		Summative Assessment Marks:25	Duration of ESA: 4 hrs.	

Sl. No	Experiment
	PART A (Any Five)
1	Study of JFET characteristics – determination of parameters.
2	Study of MOSFET characteristics – determination of parameters.
3	UJT characteristics and relaxation oscillator
4	SCR characteristics – determination of Holding current and firing voltage for different gate currents.
5	Design of inverting amplifier using Op-amp & study the frequency response.
6	Design of non-inverting amplifier using Op-amp & study the frequency response.
7	Op-amp as a adder and subtractor.
	Design and study of differentiator using op-amp for different input waveforms.
8	Design and study of integrator using op-amp for different input waveforms.
9	Design and study of first order low-pass filters using op-amp.
10	Design and study of first order high-pass filters using op-amp.
11	Astable multivibrator using IC-555 timer.
12	Monostable multivibrator using IC-555 timer.
	PART B (Any Five)
13	Half Adder and Full Adder using logic gates
14	Half Subtractor and Full Subtractor logic gates
15	Study of the Encoders and priority encoders.
16	Study of Multiplexer using logic gates.
17	Study of Demultiplexer using logic gates.
18	Study of 2-bit and 4-bit magnitude comparators.
19	Study of Clocked RS, D and JK Flip-Flops using NAND gates.
20	Study of 4-bit Shift Register – SISO, modification to ring counter using IC 7495.

OPEN ELECTIVE

Year	I	Course Code: 21BSC2O2ELE2	Credits	03
Sem.	1	Course Title: Electronics for Everyone	Hours	40

Course Pre-requisites, if any	NA	
Formative Assessment Marks: 40	Summative Assessment Marks: 60	Duration of ESA: 2 hrs.

Unit No.	Course Content	Hours
Unit- I	**Timer (IC 555):** Introduction, Block diagram, Astable and Monostable multivibrator circuits and its application **Phase Locked Loop (PLL):** Functional block diagram – Phase detector / Comparator, Voltage Controlled Oscillator, Low pass filter. **Applications of PLL:** Frequency multiplier / Division, AM detection.	10
Unit- II	**Operational Amplifier:** Introduction to Differential Amplifier, Block diagram of Op-Amp, Schematic symbol, Equivalent circuit for ideal op-amp, ideal voltage transfer curve, Characteristics Op-Amp, Op-Amp parameters, Op-Amp configurations (Open and closed loop configuration), Concept of Virtual Ground. **Op-Amp Applications:** Inverting and non-inverting amplifier, Summing Amplifier, Difference Amplifier, Integrator, Differentiator, Instrumentation Amplifier, Phase-shift and Wein bridge oscillator.	10
Unit -III	**Transducers (Basic Working):** Introduction, types of transducer, Displacement transducers - Resistive (Potentiometric, Strain Gauges – Types, Gauge Factor, bridge circuits, Semiconductor strain gauge) Capacitive (diaphragm), Hall effect sensors, Magneto- strictive transducers, Microphone, Touch Switch, Piezoelectric sensors, Opto-Electronic transducer (Photo conductive or LDR, Photo emissive, Photo voltaic, Semiconductor Photo diode, Photo transistor), Temperature sensor (electrical and non-electrical), Pressure sensor.	10
Unit -IV	**Data Acquisition using Arduino:** Arduino--Birth, Open-Source community, Functional Block Diagram, Functions of each Pin, Arduino Development Boards: IDE, I/O Functions, Looping Techniques, Decision Making Techniques, Designing of 1st sketch, Programming of an Arduino (Arduino ISP), Serial port Interfacing, Basic Interfacing and I/O Concept, Interfacing LED, Switch,7seg LED, different sensors.	10
Laboratory Demonstration	1.Study of basic Monostable / Astable multivibrator. 2.Light detection using 555 timers. 3.Study of basic inverting and non-inverting amplifier. 4.Study of basic integrator / differentiator circuit. 5.Test the different Arduino Boards, Open-Source and Arduino Shields. 6.Install Arduino IDE and its development tool. 7.Develop a program to Blink LED for 1second. 8.Interfacing of various sensors with Arduino development board.	
Recommended Leaning Resources		
Reference Books	1.R.P. Bali, Consumer Electronics, Pearson Education (2008) 2.R.G. Gupta, Audio and Video systems, Tata McGraw Hill (2004)	

ASSESSMENT METHODS

Evaluation Scheme for Internal Assessment:

Theory:

Assessment Criteria	40 marks
1st Internal Assessment Test for 30 marks 1 hr after 8 weeks and 2nd Internal Assessment Test for 30 marks 1 hr after 15 weeks. Average of two tests should be considered.	30
Assignment	05
Activity	05
Total	**40**

Assessment Criteria	25 marks
1st Internal Assessment Test for 20 marks 1 hr after 8 weeks and 2nd Internal Assessment Test for 20 marks 1 hr after 15 weeks. Average of two tests should be considered.	20
Assignment/Activity	05
Total	**25**

Practical:

Assessment Criteria	25 marks
Internal test	15
Viva Voce / basic understanding of the concept	05
Journal/Practical Record	05
Total	**25**

Scheme of Evaluation for Practical Examination

Sl. No.	Particulars	Marks Allotted Max. 25
1.	Basic formula with description, nature of graph if any & indication of unit	05
2.	Tracing of schematic ray diagram/Circuit diagram with description and tabulation	05
4.	Experimental skill & connection	05
5.	Record of observation,	05
6.	Calculation including drawing graph	04
7.	Result with unit	01
	Total	**25**