Design for Analog Circuits - Laboratory Report

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Assignment 2

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1 Differential Amplifier

1.1 Aim

To perform DC, AC and transient simulation on the BJT based differential amplifier circuit provided and obtain its DC operating point, frequency response and AC output with sinewave input.

1.2 Schematic

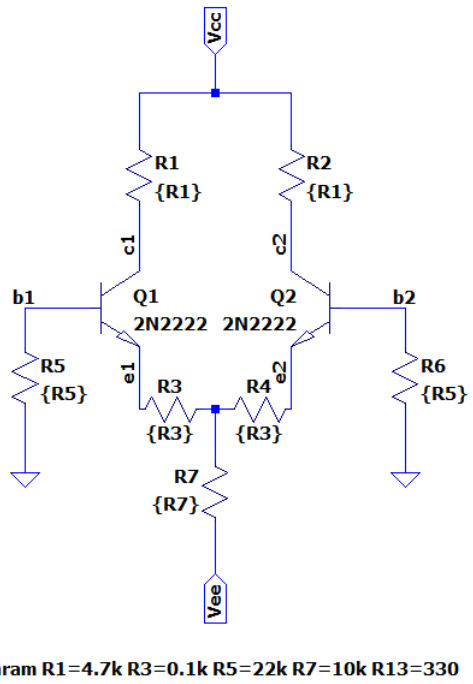

Figure 1: LTSpice Schematic of the Differential Amplifier Circuit

1.3 DC Operating Point Simulation

The following table shows the DC operating point values of the amplifier as obtained from simulation using $R_1 = R_2 = 4.7k\Omega, R_3 = R_4 = 100\Omega, R_T = 10k\Omega, R_5 = R_6 = 22k\Omega$:

Parameter	Value
I_{B_1}	$4.525\mu A$
I_{B_2}	$4.525\mu A$
V_{B_1}	$0.1V$
V_{B_2}	$0.1V$
I_T	$1.915mA$
V_{C_1}	$5.521V$
V_{C_2}	$5.521V$

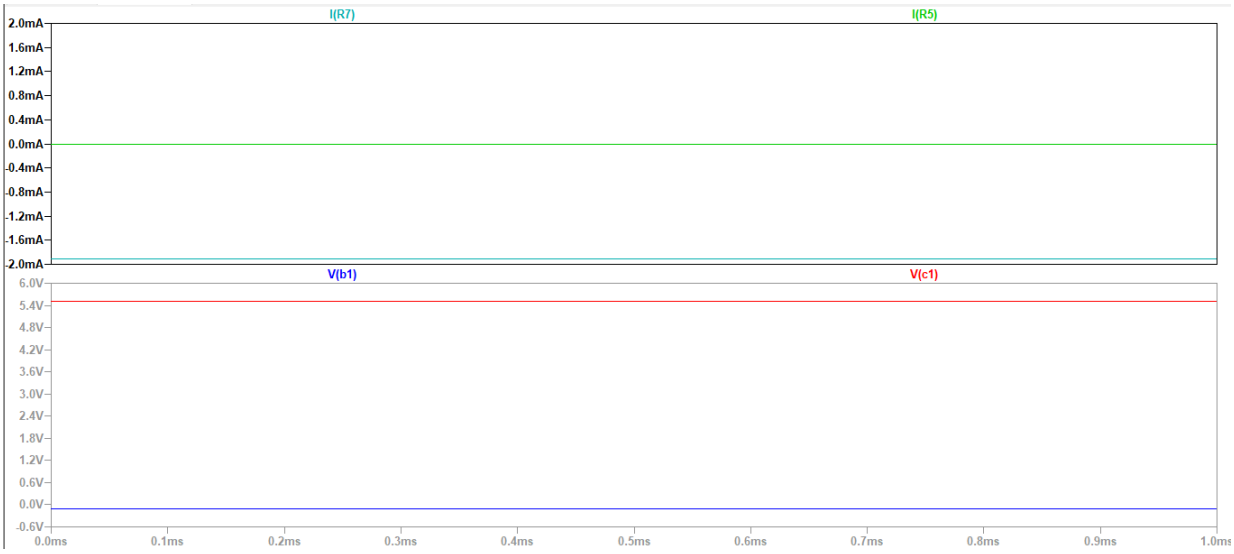

Figure 2: DC Operating Point Simulation of Differential Amplifier

1.4 Transient Simulation with sinewave input

Figure 3 shows the transient simulation results of the differential amplifier with a 20 mV amplitude sine wave signal input at the base of Q_1. The AC operating point values of the

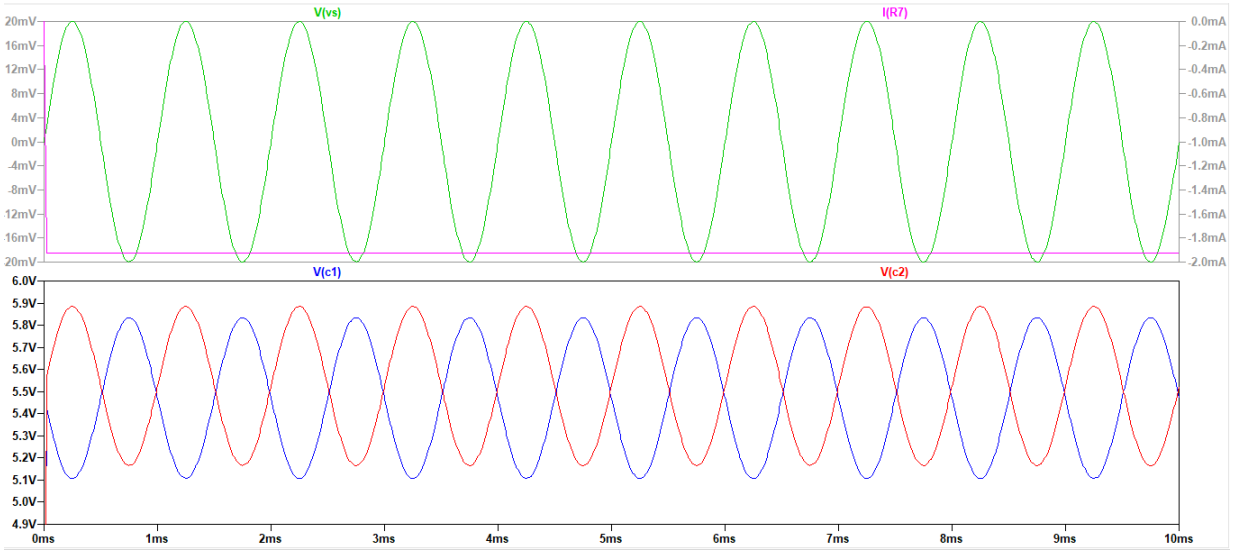

Figure 3: Transient Simulation of Differential Amplifier with 20 mV sinewave input

amplifier as obtained from simulation using $R_1 = R_2 = 4.7k\Omega, R_3 = R_4 = 100\Omega, R_T = 10k\Omega, R_5 = R_6 = 330\Omega$ are tabulated as follows (please note that all values are peak to peak):

Parameter	Value
V_{C_1}	$0.7283V$
V_{C_2}	$0.7190V$
I_T	$2\mu A$

1.5 Evaluation of A_{DM} and A_{CM}

Figure 4 below shows the LTSpice schematic of the differential amplifier with fully differential inputs for small signal AC analysis (for evaluation of differential mode gain (A_{DM}) (component values as in §1.4):

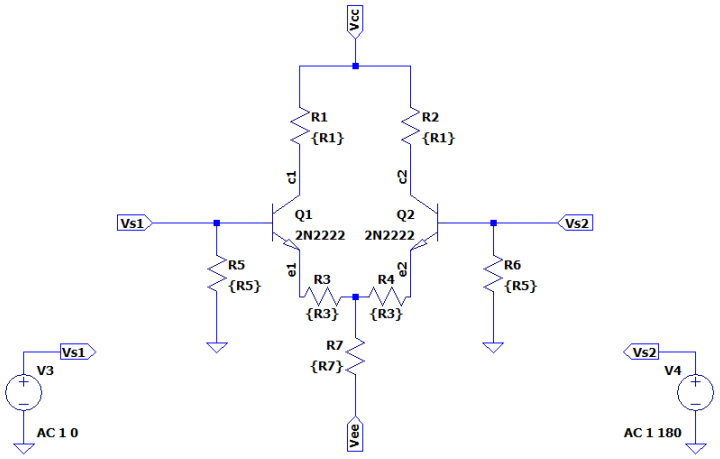

Figure 4: LTSpice Schematic for evaluation of A_{DM}

Figure 5 below shows the magnitude and frequency response of the amplifier with fully differential mode input. We obtain a differential gain of 31.22 dB = 36.39 . The upper cutoff frequency obtained from the simulation is 6.06 MHz .

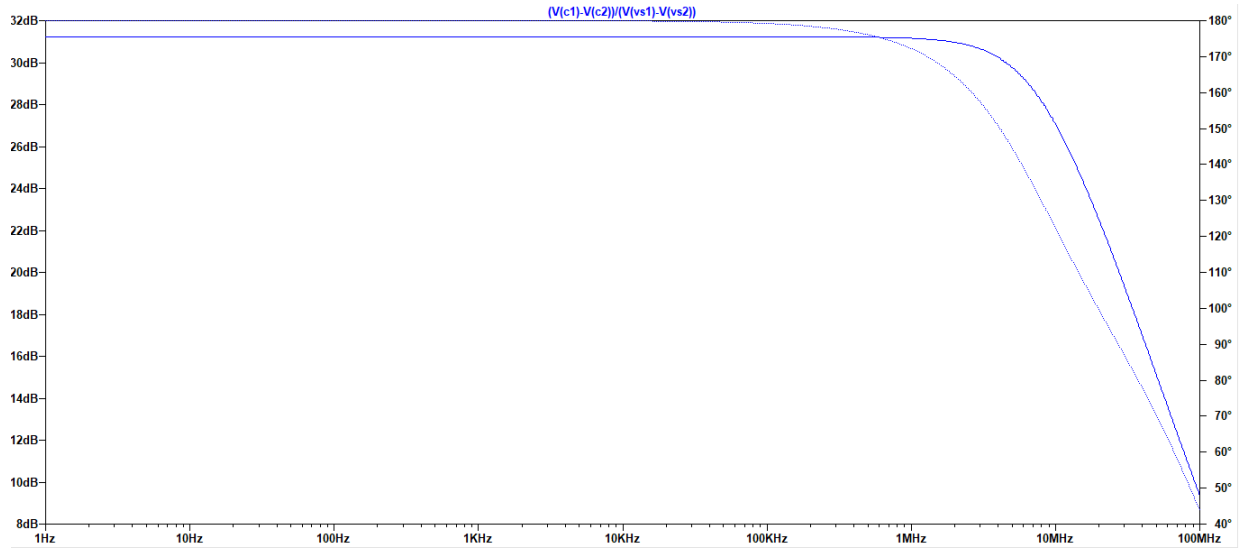

Figure 5: AC simulation for finding A_{DM}.

The LTSpice schematic for evaluation of common mode gain (A_{CM}) is shown in Figure 6 below. The magnitude and frequency response of the amplifier with common mode input is shown in Figure 7 . The obtained common mode gain in the 3 dB bandwidth of the differential amplifier is -12.69 dB = 0.232.

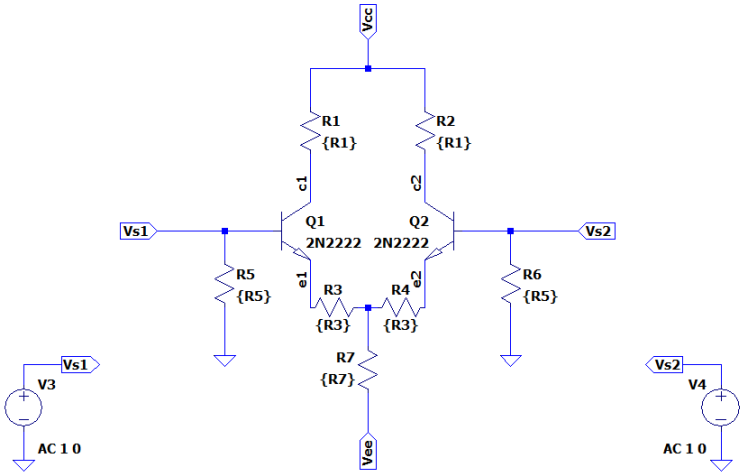

Figure 6: LTSpice Schematic for evaluation of A_{CM}

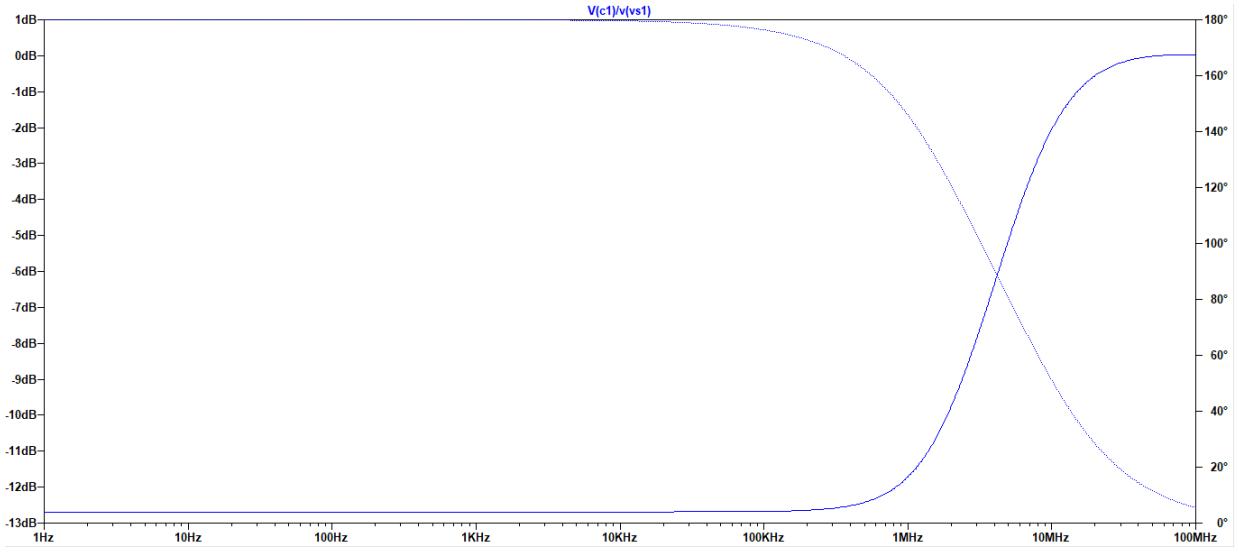

Figure 7: AC simulation for finding A_{CM}.

1.6 Gain Calculation from §1.4

We have obtained A_{DM} & A_{CM} from §1.5. Now we calculate the gain values from our results obtained in §1.4 and verify the same.

Collector AC voltage of Q_1 (V_{C_1})	=	$-0.3642sin(\omega t)V$
Collector AC voltage of Q_2 (V_{C_2})	=	$0.3595sin(\omega t)V$
Input AC voltage of Q_1 (V_{B_1})	=	$0.02sin(\omega t)$ V
Input AC voltage of Q_2 (V_{B_2})	=	$0V$
Differential input voltage (V_{DM})	=	$V_{B_1} - V_{B_2} = 0.02sin(\omega t)V$
Common model Input voltage (V_{CM})	=	$(V_{B_1} + V_{B_2})/2 = 0.01sin(\omega t)V$
Differential output voltage ($V_{O_{DM}}$)	=	$V_{C_1} - V_{C_2} = -0.7237sin(\omega t)V$
Common mode output voltage ($V_{O_{CM}}$)	=	$(V_{C_1} + V_{C_2})/2 = -0.00235sin(\omega t)V$
Differential gain (A_{DM})	=	$V_{O_{DM}}/V_{DM} = -36.19$
Common mode gain (A_{CM})	=	$V_{O_{CM}}/V_{CM} = -0.235$

1.7 DC Bias and Offset Quantities

1. From §1.3, when no input signal is applied to Q_1 and Q_2, we obtained $I_{B_1} = I_{B_2} = 4.525\mu A$. So we can say that input bias current $I_{in-bias} = 4.525\mu A$ for this amplifier. As the bias current is equal for both inputs, the input offset current $I_{in-offset} = 0$.
2. With no signal at input, we have $V_{C_1} = V_{C_2}$. So output voltage offset $V_{out-offset} = 0$.

2 Conclusion

1. The common mode gain starts rising at 6MHz (when the differential gain falls) and the again becomes flat after 50 MHz.

2. The differential output $V_{C_1} - V_{C_2}$ is not affected by the common mode signal.

3. The tail current I_T remains fairly constant with non-zero differential and common mode input.

4. The CMRR of the amplifier is 156.85 which ensures good signal immunity against common mode noise. This can further be improved by using a current source to bias the tail of the amplifier (simply increasing value of R_T will increase the DC voltage at C_1 and C_2 limiting the maximum output signal swing).