E0 284: Digital VLSI Circuits

Project: ASIC design for implementation of ELM inference engine

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Introduction

- ASIC design for implementation of an Extreme Learning Machine (ELM) inference engine.
- Application of the ELM engine – classification of handwritten digits from 0-9.
- Dataset: Semeion Handwritten Digit Dataset (UCI ML repository). Each image is a 16X16 binary matrix vectorized to 256 bits.

Network Description

- Fully connected network . Each input node is connected to all hidden neurons; each hidden neuron connected to all output nodes.
- Network parameters - 256 input nodes (vectorized binary image), 3000 hidden neurons, 10 output nodes(corresponding to digits 0-9).
- Activation function used - RelU .
- Output is a 10 bit array – MSB = 1 stands for digit 0, LSB=1 stands for digit 9.

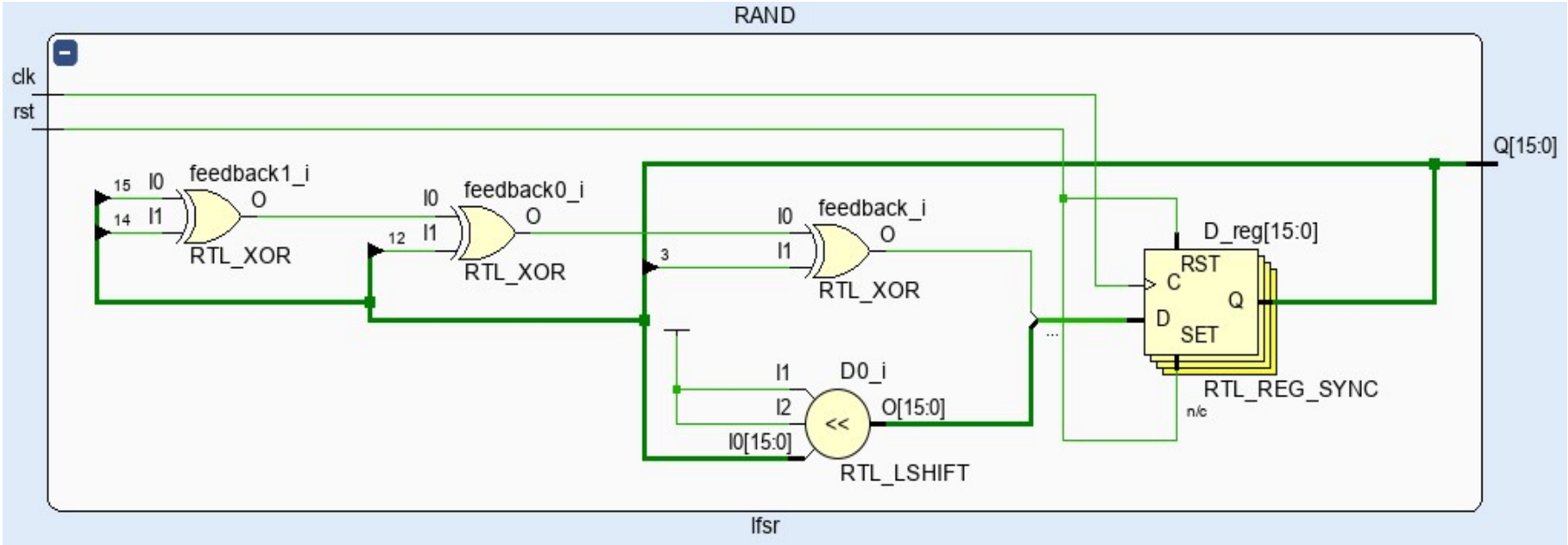
Software Implementation

- Implementation of LFSR logic in matlab to generate input-to-hidden layer weights.
- Number of hidden neurons reduced to 3000.
- Fixed point design approach:
  - 15 bits allotted for fraction in W10 and W21..
  - Total memory needed for weights and biases ~ 60 kilobytes.
  - Size of multiplier needed – 32 bit X 16 bit.
- Python script (rom_generator.py) used to convert W21 matrix generated in MATLAB to 10 ROM files W21_1 to W21_10. The ROMs contain a 13 bit address line (addresses 0 to HIDDEN_NODES -1) and 16 bit data line.

LFSR Implementation

- Seed of LFSR – 0110001100101100
- Feedback algorithm –

  Always @ posedge clk Q>>1, Q[0]<=Q[15]^Q[14]^Q[12]^Q[3]



Block diagram of LFSR

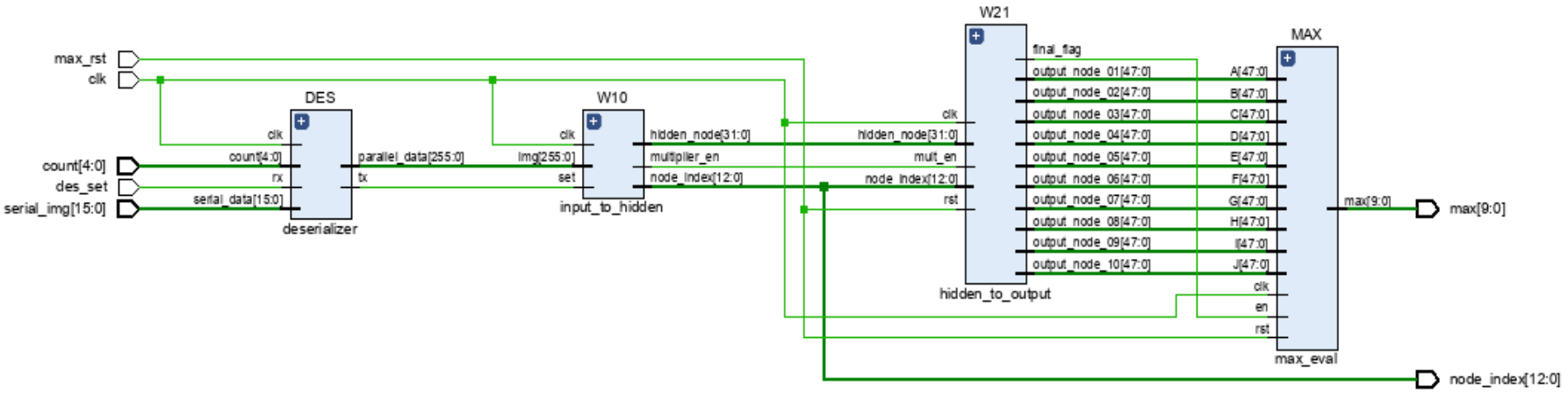
Hardware Specifications

- Frequency of operation – 100 MHz
- Latency – 32+256*hidden nodes(3000)+10 clock cycles.
- Initiation interval – 32+256*hidden nodes(3000)+12 clock cycles.
- I/O list –

PORT	BIT WIDTH	DIRECTION
data_set	1	INPUT
serial_img	16	INPUT
count	5	INPUT
clk	1	INPUT
max_rst	1	INPUT
output_layer	10	OUTPUT
node_index	13	OUTPUT

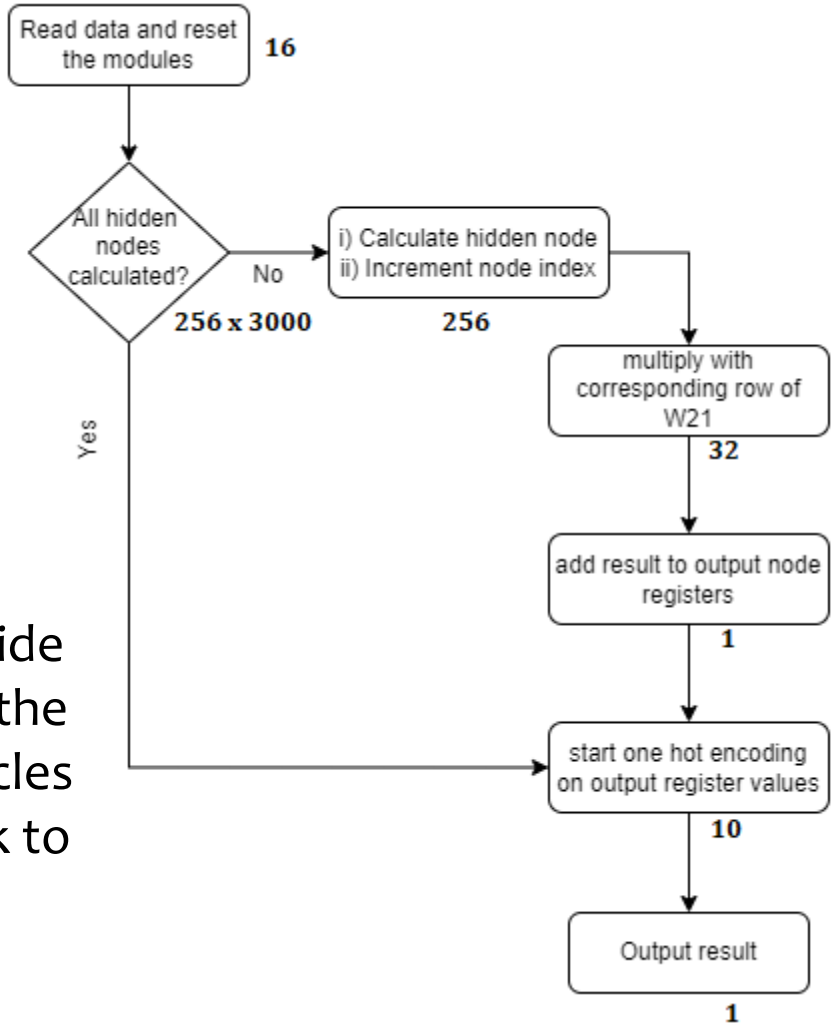
Hardware Architecture

- DES – concatenates the 16 bit serial data chunks to a 256 bit parallel data.
- W10 – calculates the hidden neuron values and employs the activation function (RelU).
- W21 – calculates the output neuron values.
- MAX – calculates the maximum of the 10 output neuron values.



Hardware block diagram

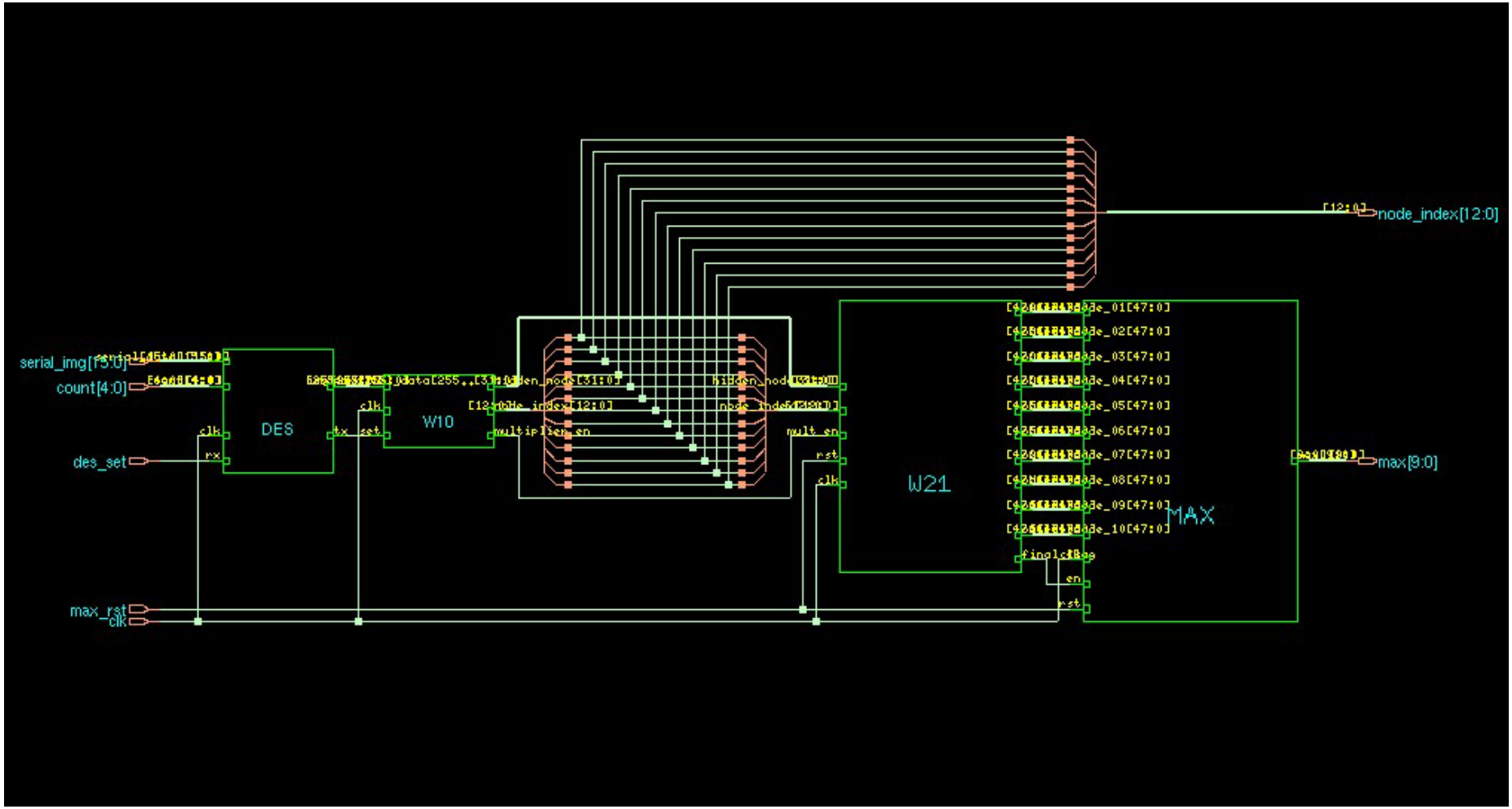
Control FSM



(Note: number beside each block denote the number of clock cycles taken by each block to complete)

System Flowchart

Hardware Schematic



HW Simulation

- Image data and the answer stored as a Verilog ROM and instantiated in testbench.
- Testbench provides the image index (1-493) as input. The index samples demonstrated for digits 0-9 are – 13(0), 366(1), 51(2), 14(3), 49(4), 120(5), 169(6), 119(7), 23(8) and 14(9).

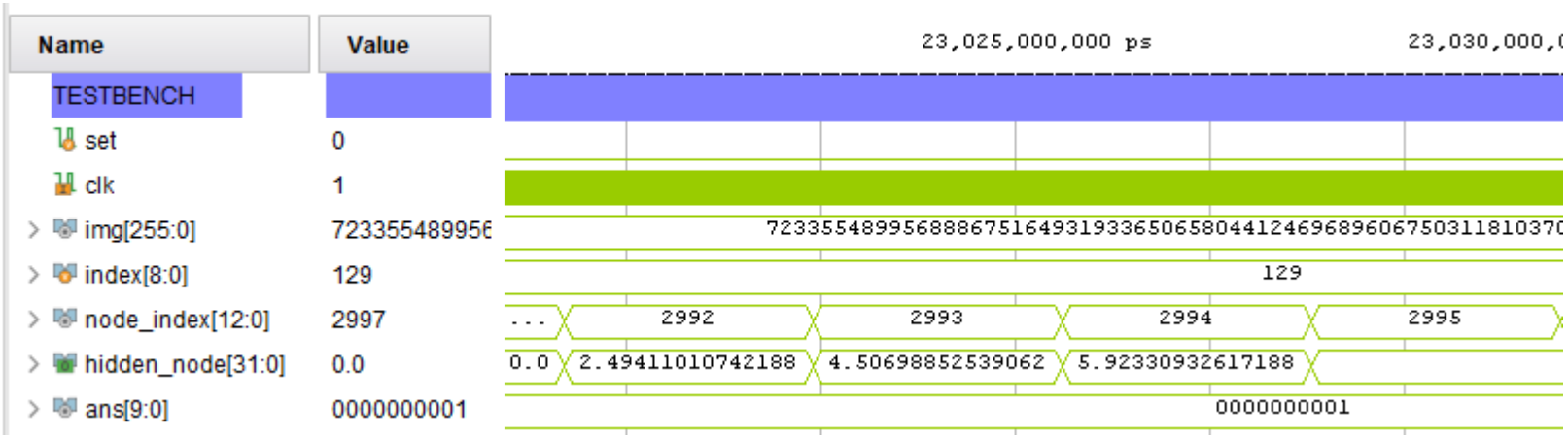
```
module test_images(input [8:0] addr,  output reg [255:0] data);
  always @ (addr) begin
     case(addr)
      9'd1: data <=256'b0000000000111111000000001111000100000011
      9'd2: data <=256'b0111111111111100111000000000111100000000
      9'd3: data <=256'b0111111111100000111000001111000011000000
      9'd4: data <=256'b0000000001111111000000011110001100001111
      9'd5: data <=256'b0000111100000000000111100000000000111100
      9'd6: data <=256'b0000000000000110000000000000111000000000
```

Image ROM

```
module test_images_answers(input [8:0] addr,  output reg [9:0] data);
  always @ (addr) begin
     case(addr)
      9'd1: data <=10'b0000001000;
      9'd2: data <=10'b0001000000;
      9'd3: data <=10'b0000000010;
      9'd4: data <=10'b0000001000;
      9'd5: data <=10'b0100000000;
      9'd6: data <=10'b0100000000;
```

Answer ROM

HW Simulation

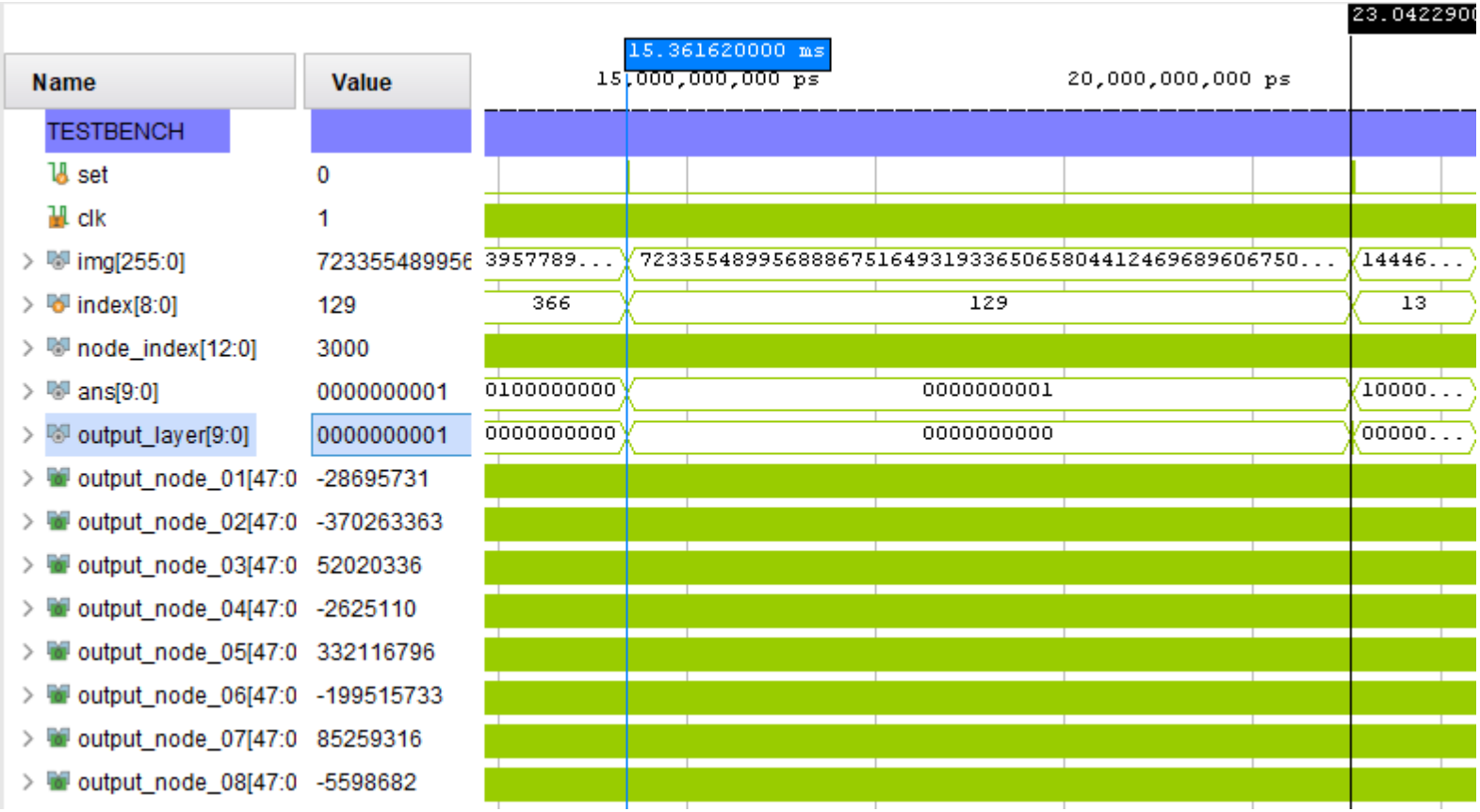


Verilog hidden neuron output (image – 129, neurons 2992– 94)

2992	2993	2994
2.494110107421875	4.506988525390625	5.923309326171875

MATLAB hidden neuron output for the above

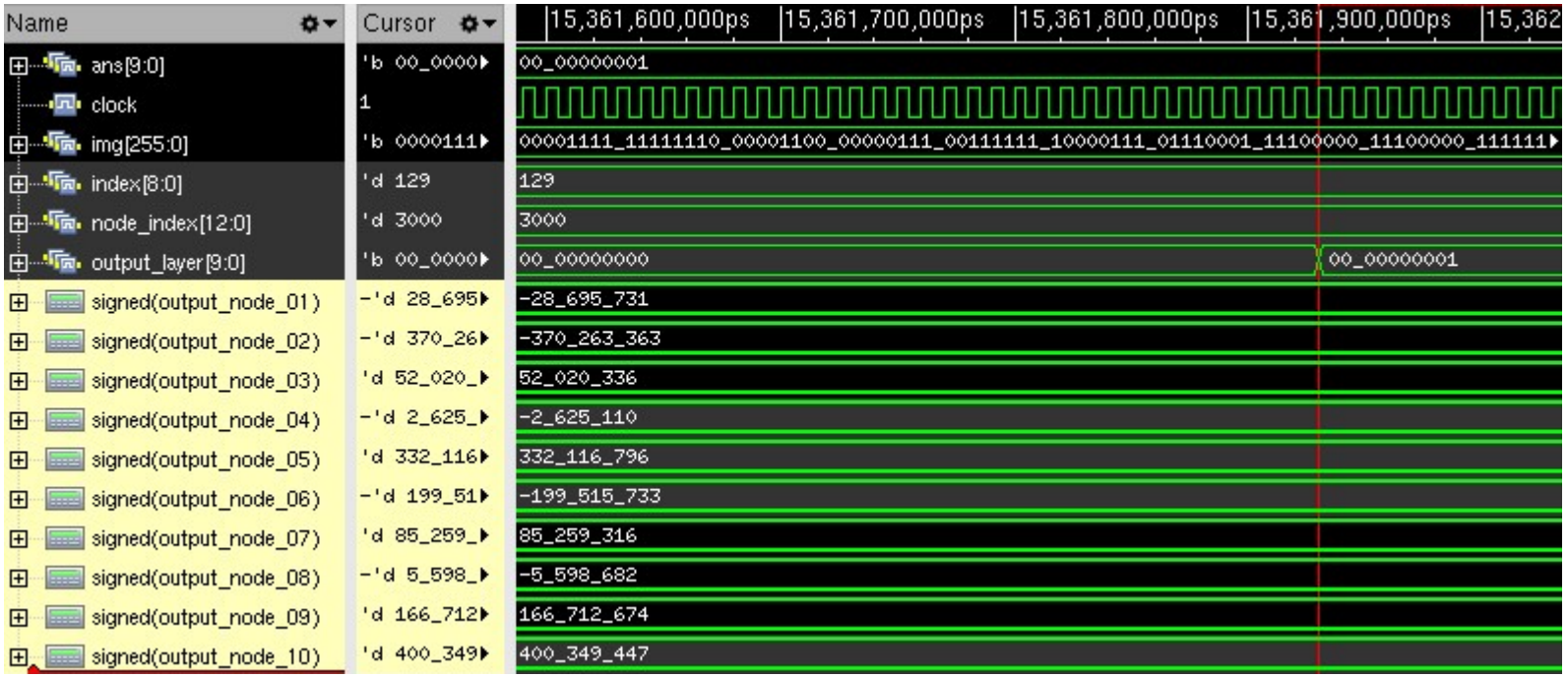
Pre-synthesis Simulation Waveform



Pre-synthesis simulation waveforms: image – 129

(left marker – input is provided. Right marker – outputs ready)
(values in left pane denotes final output node values)

Post-synthesis Simulation Waveform



Post-synthesis simulation waveforms: image – 129

(Note – the output node values in pre and post synthesis waveforms are plotted as signed decimal numbers for ease of comparison)

Accuracy Results

- Software Accuracy:
  - Train data: 100 %
  - Testing with floating point weights: 85.3955 %
  - Test data with fixed point weights: 85.1927 %

- Accuracy on HW:
  - Pre-synthesis: (10 images) – 100 %
  - Post-synthesis: (same 10 images) – 100 %

Synthesis Reports

Cost Group	Critical Path Slack	TNS	Violating Paths
clk	889.0	0.0	0
default	No paths	0.0	
Total		0.0	0

Instance Count	
Leaf Instance Count	45813
Physical Instance count	0
Sequential Instance Count	3176
Combinational Instance Count	42637
Hierarchical Instance Count	67

Area	
Cell Area	88544.484
Physical Cell Area	0.000
Total Cell Area (Cell+Physical)	88544.484
Net Area	0.000
Total Area (Cell+Physical+Net)	88544.484

Max Fanout	3176 (clk)
Min Fanout	0 (MAX/lt_69_70_Y_gt_65_70/NE)
Average Fanout	2.9
Terms to net ratio	3.8946
Terms to instance ratio	3.9647

QOR report

Synthesis Reports (contd.)

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	4.11976e-07	7.47525e-04	3.17724e-05	7.79709e-04	49.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	1.54292e-06	5.53742e-04	2.56099e-04	8.11384e-04	51.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	1.95490e-06	1.30127e-03	2.87871e-04	1.59109e-03	100.00%
Percentage	0.12%	81.78%	18.09%	100.00%	100.00%

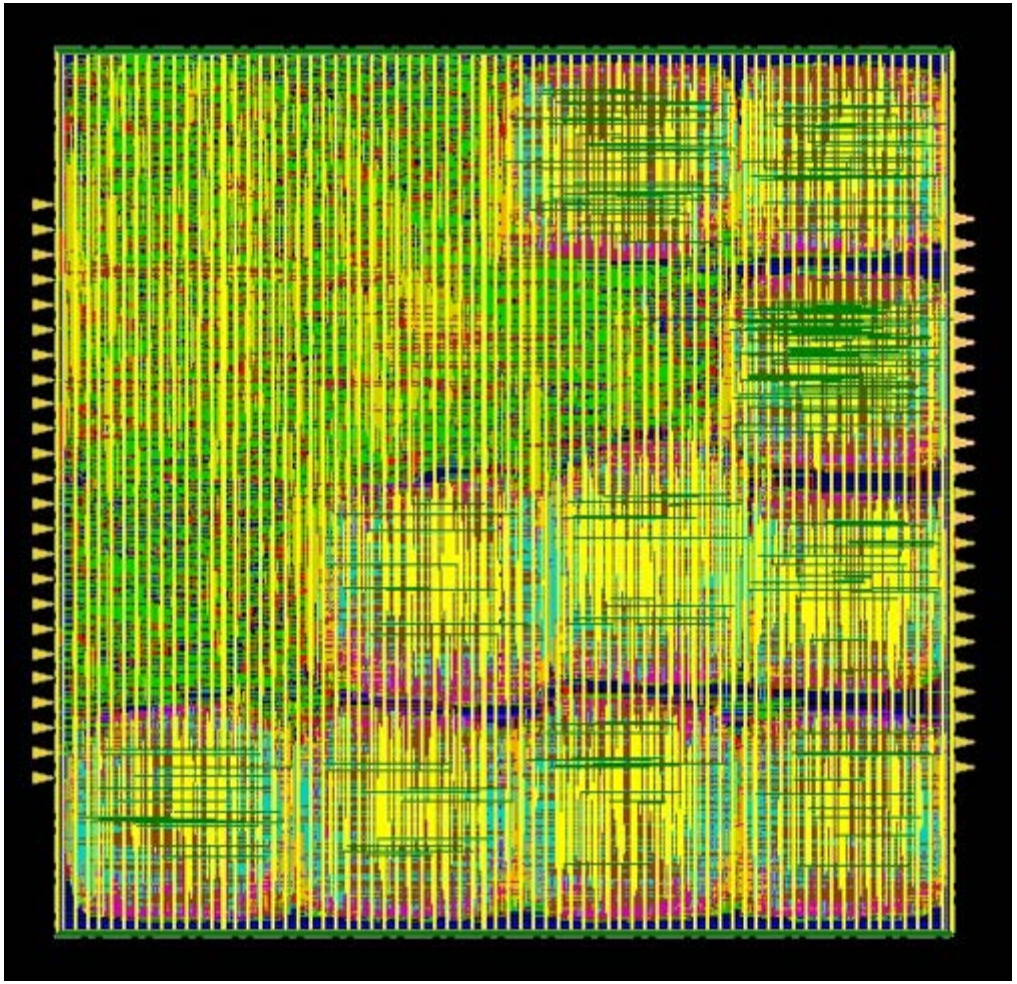
POWER report

LEC Report

```
================================================================================
                          Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                 1
     Not-mapped DFF/DLAT is detected:                          yes
--------------------------------------------------------------------------------
3. User modification to design:                                             0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                        0
--------------------------------------------------------------------------------
6. Compare Results:                                                 FAIL:NONEQ
================================================================================
```

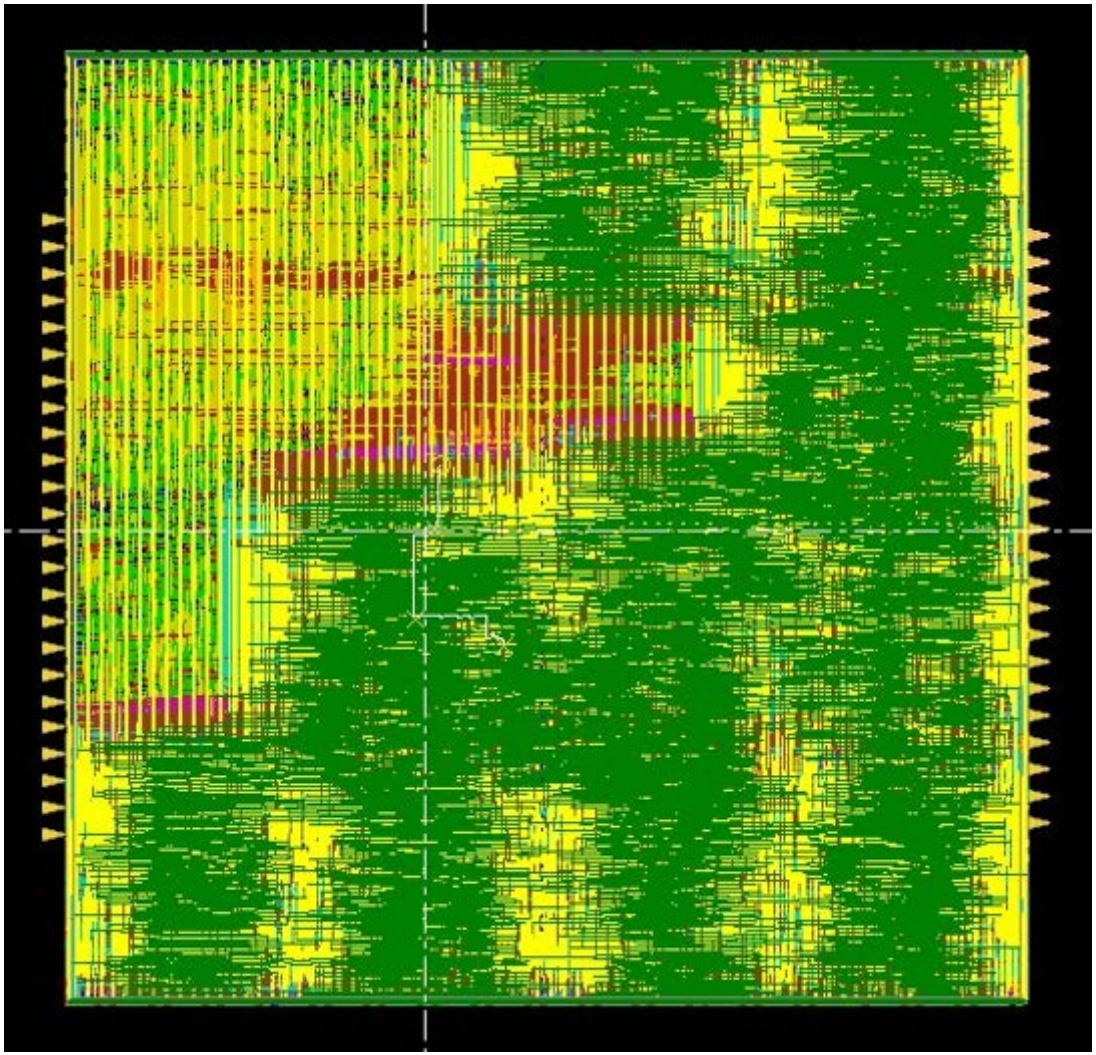
LEC report

Placement



Placed Design

Routing



Routed Design

Post-Routing Reports

```
Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.014  |  0.014  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  3992   |  3992   |    0    |
+--------------------+---------+---------+---------+
```

Setup time analysis

```
Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.008  |  0.008  |  6.991  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  4287   |  3992   |  1260   |
+--------------------+---------+---------+---------+
```

Hold time analysis

```
Total Power
----------------------------------------------------------------
Total Internal Power:        2.20936707            34.1492%
Total Switching Power:       4.25708009            65.7999%
Total Leakage Power:         0.00329269             0.0509%
Total Power:                 6.46973985
----------------------------------------------------------------
```

Power report

```
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 6
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 6 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
```

Geometry report

```
Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Nov 27 19:08:27 2021
Time Elapsed: 0:00:07.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:06.4  MEM: 0.000M)
```

Connectivity report

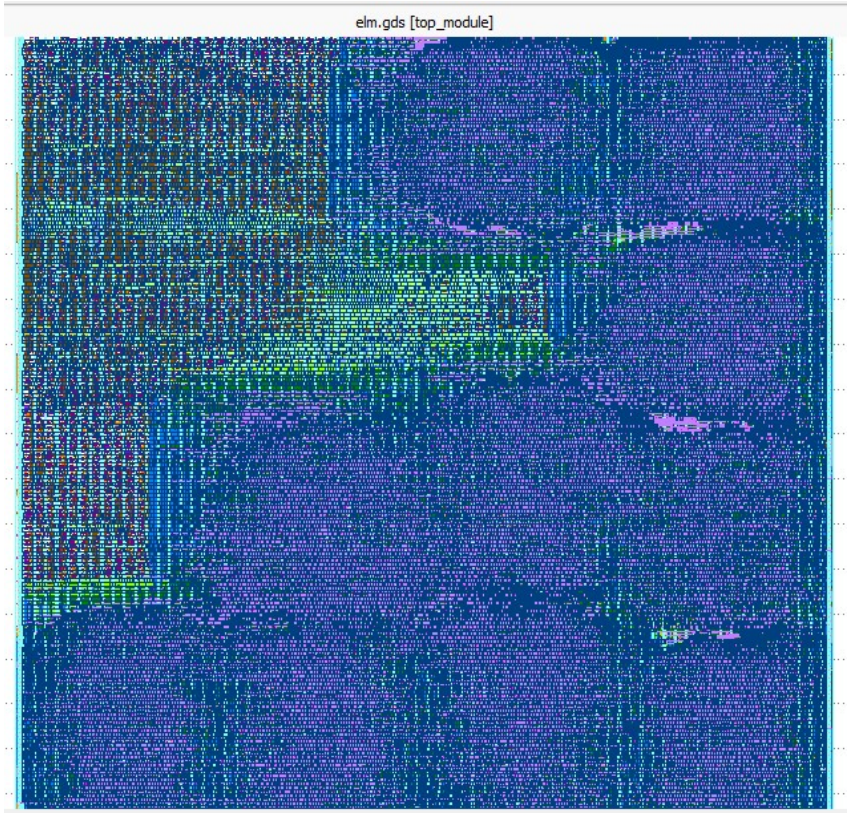
GDS

```
Blockages                              0

Custom Text                            0

Custom Box                             0
Trim Metal                             0
######Streamout is finished!
```

GDS streamout from terminal



GDS of ASIC

Conclusions

- Number of neurons in hidden layer = 3000
- Accuracy on synthesized HW = 85.1927 %
- Clock Frequency = 100 MHz
- Latency = 32+256*3000+10 clock cycles ≈ 7.68 ms
- Initiation Interval = 32+256*3000+12 clock cycles ≈ 7.68 ms
- Total Area = 88544.484
- Total Power (post-routing) = 6.46973985
- Setup TNS and WNS (post-routing) = 0 and 0.014 ns
- Hold TNS and WNS (post-routing) = 0 and 0.008 ns

Thank You

Learning Outcomes

- Writing synthesisable Verilog code for a complex digital system.
- Detailed overview of the entire ASIC design process from RTL to GDS.
- Elementary concepts of neural networks.