E0 284: Digital VLSI Circuits
Lab Assignment-3:
COMBINATIONAL and SEQUENTIAL LOGIC DESIGN USING VERILOG

Submission Deadline: 31st Oct, 11:59 PM

Instructions:

1. Assume any missing data.
2. Write Verilog code and corresponding test benches. Proper comments would be appreciated as it will help us understand your code.
3. Prepare a descriptive report which includes your **FSM** (if it's sequential). Also, paste the elaborated design generated by the tool and all the testbench waveforms wherever required and it should be clearly labelled and visible.
4. Make subfolder for each question like q1, q2 …, and keep Verilog design file(s) and corresponding test bench of a particular question in its respective subfolder.
5. Keep all the subfolders (corresponding to each question) along with your report in a single folder name formatted as **<FirstName_LastName_SRNo_DVLSI_ASSIGN3>**
6. Submit the **<FirstName_LastName_SRNo_DVLSI_ASSIGN3>.zip** file in the **Teams** only.

NOTE: DO NOT COPY code from web or peers. This assignment is designed to help you understand basic modules and it might be helpful in upcoming project.

Question-1:

The Traffic Authority asked you to design an overspeed control system with minimum hardware requirements.

The system takes speed of a vehicle as an input to control the LEDs as follows:

- If speed < 50 km/h, Green light glows continuously.
- If 50 <= speed < 90km/h, Yellow light glows for 5 sec
- If speed >= 90 km/h, Red light blinks for 10 sec with frequency of 1 Hz and duty cycle of 50%.
  (Assume only one light glows/blinks at a time, and only one vehicle is under observation at a time)

Question-2:

You have two matrix (both 2x2)
A = [1.2 2.3; 2.2 -2.2] B = [1.8 -8.3; 1.2 3.2;]
Use shift and add method to multiply and **fixed-point methods** (width 16-bit) to realise the functionality. You can verify the result of your multiplication from MATLAB. (choose binary point position as per your convenience)

Question-3:

There are 4 lights which are blinking independently with time periods **t1, t2, t3** and **t4** (all-natural number) on same duty cycle. All are reset at time **t=0**. Implement a Verilog code to find out the time at which all the lights will flash together. Given maximum period of each light is **15 sec**. Your program should work on any combination of **t1, t2, t3** and **t4**.

Question-4:

You are responsible for digital radio signal detection. You are supposed to intercept and detect the pattern **101011** in the digital signal which is of interest to you. The pattern appears in the signal after a definite interval which is unknown to you. The bits in the digital signal are coming continuously and serially at 1 Gbps. Implement suitable FSM for your design.

Note: You have started intercepting the signals somewhere in between. Your FSM should work regardless of your start time.

Question-5:

Build a four-bit left shift register that also acts as a down counter. Data is fed to the least significant bit first when **shift_ena** is 1. The number currently in the shift register is decremented when **count_ena** is 1. Both **shift_ena** and **count_ena** are never high together.