A Highly Efficient Wide Battery Voltage Range Dual Active Bridge-based Single-stage Bidirectional EV Onboard Charger Without Low-Frequency Harmonics in the Charging Current

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***Abstract*—This paper introduces an on-board charger circuit capable of converting 1-phase AC to DC in a single stage. The circuit integrates a PWM 2-level voltage-sourced inverter (VSI) and a dual active bridge (DAB) converter into a unified single-stage structure with the help of a suitably crafted modulation strategy. Single-phase 1-stage topologies are known to suffer from significant double line-frequency ripple in the charging current. The proposed combined pulse-width and phase-shift modulation strategy achieves active power decoupling without any extra circuitry, eliminating the double line-frequency AC ripple in the battery charging current. This also enables the least RMS DAB current trajectory throughout the line cycle while facilitating Zero Voltage Switching (ZVS) for enhanced efficiency. The paper begins by detailing the working principle of the proposed converter, followed by an analytical examination of the modulation strategy. Simulation results indicate a peak power-stage efficiency exceeding 98% for a 3.6kW 1-phase system operating within a battery voltage range of 300V-500V. Experimental validation at 500W demonstrates efficiency levels consistent with the predicted values.**

***Index Terms*—On-board charger(OBC), single-stage, 1- stage, active power decoupling (APD), minimum RMS current, ZVS**

I. Introduction

Today, the automotive industry is driving the rapid development of electric vehicle (EV) charging infrastructure, focusing on increased efficiency, reduced size, and improved battery pack health. To address the challenge of long cruising ranges, vehicles are increasingly equipped with larger battery packs. However, off-board fast charging stations are insufficient to meet the decentralized charging requirements due to their limited numbers and high installation costs. On-board chargers (OBCs) with high-power charging capabilities are emerging to fill this gap. EV chargers take either a 3-phase or 1-phase grid supply. Generally, for OBCs, with less than 10kW applications, a single-phase connection is preferred. Being an AC-DC conversion system, the power-stage-wise OBC converter topology is of two types: 2-stage and 1-stage. While 2-stage on-board chargers need an AC-DC PFC converter in the first stage and a DC-DC high-frequency (HF) isolated converter

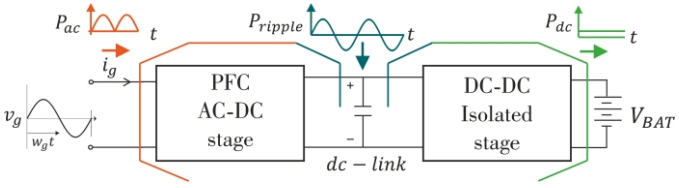

Fig. 1. Active power decoupling in 2-stage topology by installing large electrolytic capacitor in the dc-link

in the second stage [1] [2], 1-stage circuits perform both the operations in one stage. Single-stage OBCs offer significant advantages over 2-stage OBCs, in terms of reduction in device counts, higher power density, and elimination of poor life-span large DC-link capacitors. However, due to the higher charge packing density of electrolytes compared to film capacitors, a large capacitor bank is installed in 2-stage solutions. These capacitors filter the ripple energy (P_{ripple}) completely, i.e. the difference between AC power ($P_{ac}=\frac{v_g i_g}{2}(1-cos(2\omega_g t)$) and the constant DC power, making the converters capable of DC charging (see fig 1) [3]. Independent switching of the two stages this filtering easier. In contrast, newly emerged single-stage circuits [4] [5] [6] use a full-wave rectifier as the front-end and feed rectified grid voltage to the DAB, nullifying the requirement of the energy storage capacitor. As the front end is providing only rectification, PFC is performed by the DAB. However, this passive rectification leads to sinusoidal charging.

Sinusoidal charging refers to the presence of a 60-70% grid frequency AC component in the battery charging current, which can increase impedance and lead to capacity fade in the battery cells [7]. In 1-phase 1-stage AC-DC circuits, the usage of common switching devices for both the PFC and HF isolation at the AC side legs makes it difficult to isolate the ripple power from the output power. An extensive amount of research is there to employ an active ripple energy storage circuit inside 1-phase PWM rectifiers for active power

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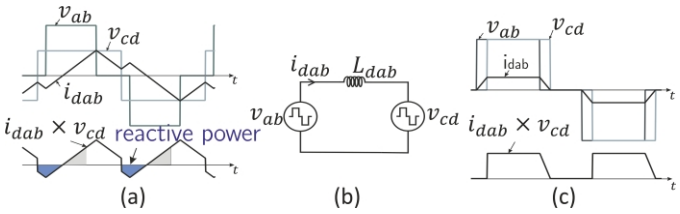

Fig. 2. (a)Reactive power loss in DAB circuit due to mismatch between HF ac RMS voltages v_{ab} and v_{cd}(b) DAB converter equivalent circuit (c) Flat-topped DAB current with zero reactive power loss

decoupling (APD) [3] [8]. However, those APD circuits are not part of the main power circuits. Employing those inside OBCs is not a wise choice due to increased complexity and efficiency constraints.

In this paper, a 1-phase, 1-stage isolated on-board charger topology is shown which doesn't compromise with the quality of input AC power and output DC power despite being a 1-stage topology. It draws the line current with a unity power factor and negligible distortion while giving a constant DC current to a voltage source output like a Battery. The isolation works on the DAB principle. A combined pulse-width and phase-shift modulation strategy is selected which features two core advantages:

- There is no reactive power loss in the HF DAB operation (see fig 2) under the proposed modulation.
- This modulation brings the least RMS DAB current trajectory minimizing the conduction loss to the minimum while enhancing the ZVS range.

Section II explains the operating principles through detailed discussions on topological derivation, modulation strategy, and control architecture. Section III presents simulation and hardware results to substantiate these concepts. Section IV conducts a comparative study of the loss profile, followed by the conclusion in Section V.

II. Operating Principle

A. Topology Description

In an effective unity gain operation (shown in fig. 3(b), $V_{BUS} = nV_{BAT}$), a classical DC-DC DAB converter operates with fixed-duty single-phase-shift (SPS) modulation. Phase shift determines the amount of power transferred. High-frequency dab current becomes flat-topped in this operation. Benefits unfold from two major aspects – (a) all the switches turn on with the ZVS transition, even at light load, and (b) zero reactive power loss in the HF link as switching cycle RMS magnitude of both the HF-link excitations v_{ab} and v_{cd} are the same. The drawback arises from the increased switching and conduction losses when the converter deviates from the unity gain operation. The proposed single-stage AC-DC converter aims to maintain the aforementioned advantages even in scenarios where the duty of the AC side bridge varies sinusoidally.

The proposed topology is derived by combining the VSI PFC front-end stage fig.3(a) and DC-DC DAB stage fig.3(b)

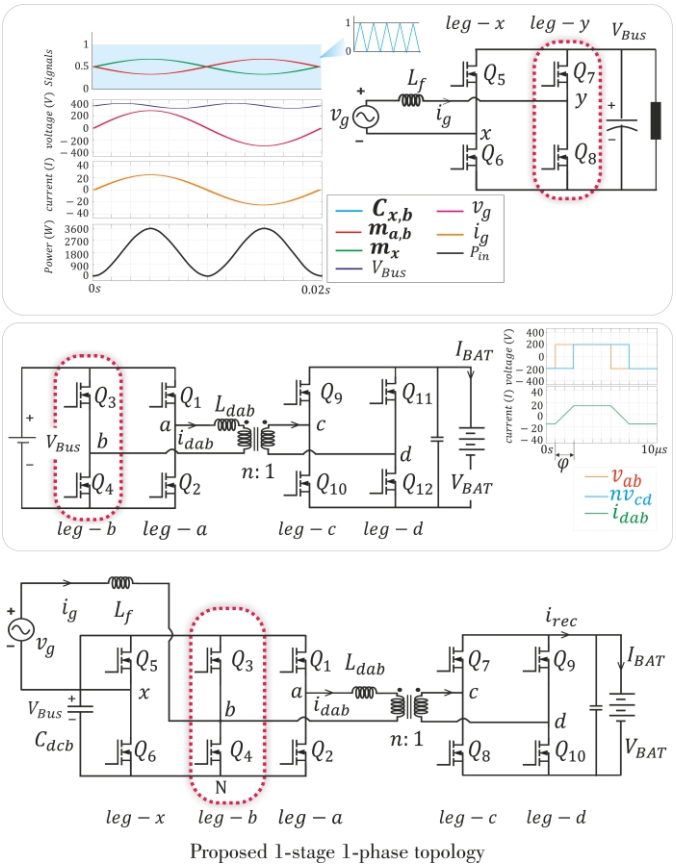

Fig. 3. Concept of Topology derivation (a)2-level VSI as front-end PFC stage. The voltage source V_{BUS} can be regulated by changing the modulation index (b) The DC-DC DAB stage with unity conversion ratio single-phase-shift (SPS) modulation. (c) The proposed single-stage converter combines a PFC leg and a DAB leg into a single hybridized leg $'leg-b'$ to take both the line current i_g and DAB current i_{dab}

into a single stage. The $'leg-y'$ of the PFC stage & $'leg-b'$ of the DC-DC DAB stage are fused in a single hybrid leg i.e. the $'leg-b'$ of the proposed architecture fig.3(c). The $'leg-b'$ and $'leg-x'$ are conventionally modulated like VSI. To generate the high-frequency waveform for DAB operation, the $'leg-a'$ carrier is shifted by a half-switching cycle to $'leg-b'$. Therefore, in the proposed converter, $'leg-b'$ is functionally hybrid in grid voltage rectification and high-frequency DAB operation. The advantage of using a full-bridge rectification is the reduced voltage stress of AC side devices and less ripple in the line current. The DC side of the converter is a conventional H-bridge-like DC-DC DAB operation.

B. Power-loss Optimized Dual Pulse-width and Phase-shift Modulation Strategy

The proposed modulation strategy builds upon the results of two previous modulation strategies reported earlier [9] [10]. To better understand the impact of this modulation strategy, it is beneficial to stack the modulation into three layers, with Layer 3 being the proposed one. Considering that the switching of the AC side three-leg bridge is influenced by the PFC operation, the remaining control variables are the phase-shift ϕ between

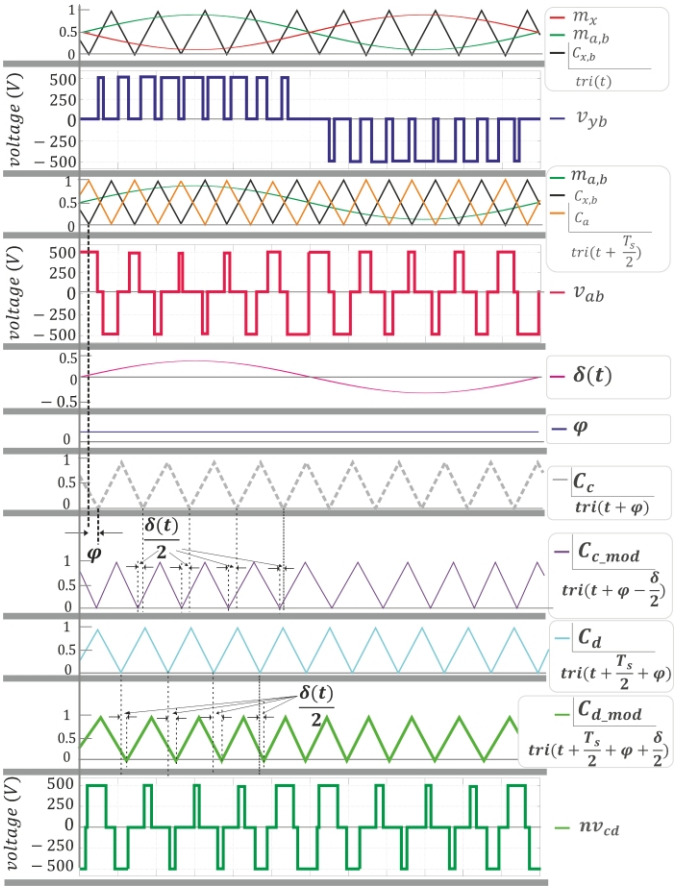

Fig. 4. Simplistic waveforms to explain Layer 2 modulation: The concept of sinusoidal carrier shifting at DC side active bridge to achieve identical pulse-width of v_{ab} and nv_{cd} and a flat-topped DAB current profile.

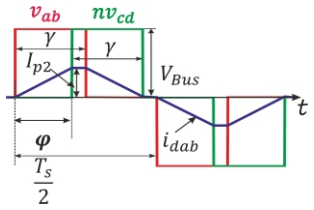

Fig. 5. Ideal HF under layer 2: Flat-top modulation scheme

the two active bridges and the pulse-width modulation of the DC side full bridge output, denoted as nv_{cd}.

The carrier for $'leg-b'$ and $'leg-x'$ is $C_{x,b}$: tri(t). As the carrier signal is the same for $'leg-b'$ and $'leg-x'$, only the line-frequency component of the switch node voltage v_{bx} appears on the grid terminal and the switching frequency ripple appears across the input filter inductor L_f. The modulating signal for $'leg-x'$ is m_x and $'leg-b'$ is $m_{a,b}$. m_x is $0.5(1-m_{ac})$ and $m_{a,b}$ is $0.5(1+m_{ac})$ where

$$m_{ac} = m_g \sin(\omega_g t) \tag{1}$$

ω_g represents the angular frequency of the supply grid. The modulating function, $m_{a,b}$ is common for both $'leg-b'$ and $'leg-a'$ so that no line frequency component appears at the AC side bridge output v_{ab}. Carrier of $'leg-a'$, $C_a : tri(t+\frac{T_s}{2})$ is half switching cycle phase shifted to $C_{x,b}$.As a result, a varying pulse-width HF voltage comes at v_{ab}. The pulse width of v_{ab} is assumed as $\gamma(t)$ and it can be expressed as

$$\gamma(t) = \frac{T_s}{2}[1-(m_{ac})^2] \tag{2}$$

The switching cycle RMS value of v_{ab} is

$$v_{ab_{RMS}}|_{T_s} = V_{Bus}\sqrt{1-(m_{ac})^2} \tag{3}$$

Now Layer-1 of the modulation scheme goes with square wave excitation of the DC side full-bridge. The only control variable is phase-shift ϕ here, whereas, the pulse width of nv_{cd} is fixed. The outcome of layer 1 includes huge reactive power loss as the RMS value of v_{ab} is continuously changing, whereas the RMS value of nv_{cd} gets fixed over the grid cycle. Layer 2 is called flat-top modulation scheme which targets to eliminate the reactive power loss which requires the RMS value of v_{ab} and v_{cd} to be the same per switching cycle. To vary the pulse width of nv_{cd} identical to v_{ab}, a differential carrier shifting function is introduced here. The function is δ. The layer-2 carrier signal of leg-c: $C_{c_{mod}}$ is shifted $\frac{\delta(t)}{2}$ towards the lagging direction to layer 1 carrier signal: C_c . Likewise, $C_{d_{mod}}$ is shifted $\frac{\delta(t)}{2}$ towards the leading direction to C_d [see fig 4]. The control variable $\delta(t)$ is tied to modulation function $m_g \sin(\omega_g t)$ which is already derived by the PLL block. Also, to match the magnitude of nv_{cd} and v_{ab}, V_{BUS} is regulated proportionally to V_{BAT} with the help of HF transformer turns ratio i.e. n:1 AC side to DC side.

$$\delta(t) = m_{ac} = m_g \sin(\omega_g t) \tag{4}$$

For the time being, ϕ is considered to be dc quantity being a PI controller output. The outcome of layer-2 modulation in the HF DAB-link looks like fig. 5. The value of I_{p2} can be calculated as

$$I_{p2} = \frac{V_{BUS}}{L_{dab}}\,\phi \tag{5}$$

Combining eq.3 and eq. 5, power transfer per switching cycle can be derived as

$$P_{dab}|_{L2} = \frac{V_{BUS}^2 T_s}{4L_{dab}}(1-|m_{ac}|-\frac{2\phi}{T_s}) \tag{6}$$

In layer 3 i.e. the proposed modulation scheme, the phase shift is not a PI controller output. Phase shift is also modulated by the active power reference using eq. 7.

$$P_{dab}|_{L3} = \frac{V_{BUS}^2 T_s}{4L_{dab}}(1-|m_{ac}|-\frac{2\phi_{mod}}{T_s}) = P_0 \tag{7}$$

ϕ_{mod} is the active power reference modulated phase-shift and P_0 is the rated power.The aim is to push constant switching cycle power through the DAB-link over the grid cycle. Thus, in the proposed modulation scheme, the active power transmitted through the dual active bridge (DAB) circuit per switching cycle is regulated by adjusting the phase shift. Fig 7 shows the variation of switching cycle RMS values of

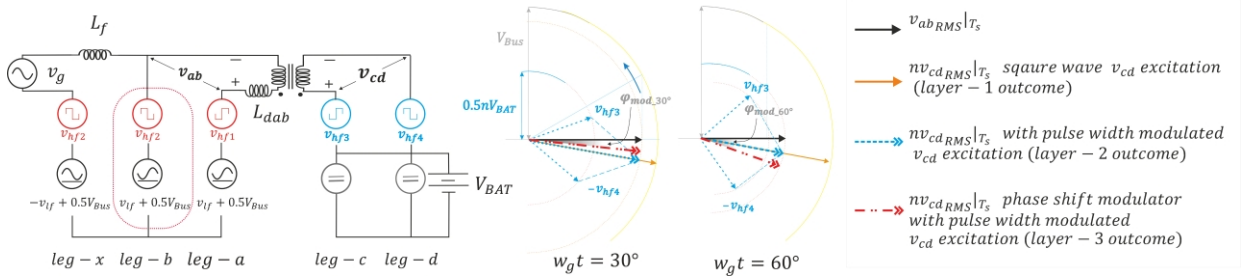

Fig. 6. Equivalent circuit of the proposed converter with high-frequency plane phasor representation. Two line cycle instants are shown to show the effect of layer-wise modulation strategies discussed on the switching cycle RMS value of nv_{cd}.

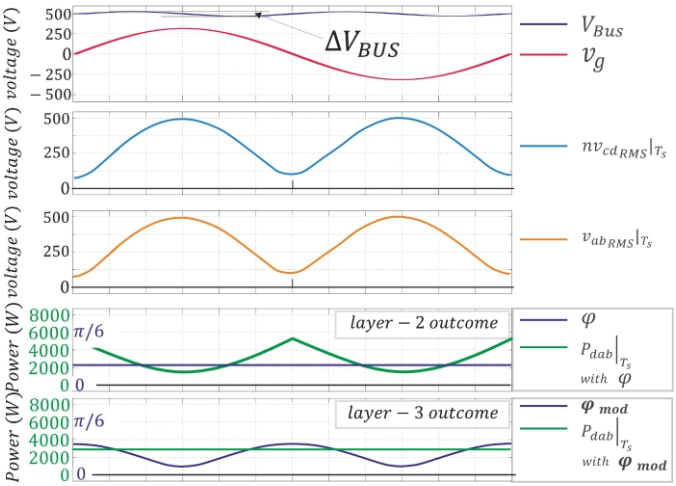

Fig. 7. Ideal waveforms for layer-2 (reactive power less flat-top modulation) and layer-3 (proposed) modulation.

TABLE I
PARAMETERS OF THE SELECTED DESIGN

Description	Value
Rated Conditions	P_0=3.6kW, V_{BAT}= 300V-500V Grid supply v_g=220V, 1-phase, 50Hz
Devices Q_1-Q_{10}	1.2kV, 40mohm,NTHL040N120SC1
Switching frequency Q_1-Q_{10}	100kHZ
Regulated Bus Voltage V_{BUS}	450-500V
AC input filter inductor L_f	500μH, $EE80/38/20$ core,Litz. wire
DC link capacitor C_{dcb}	500μF, C4AQCEW6130A3BJ(X4)
HF Transformer	Turns ratio= 500:400 (AC:DC side) $EE80/38/20$ core,Litz. wire L_m=2.32mH,L_{lk}=6.84μH (AC side)
DAB Inductor	6.32 μH, $EE42/21/15$ Litz. Wire
Controller IC	XE6SLX9 Spartan-6 FPGA
Efficiency	96.5-98.2% (300-500V, 300W-3.6kW)

the v_{ab} and nv_{cd} over the line cycle followed by the effects of the layer-2 and layer-3 modulation. The control architecture is shown in fig 8. Grid current i_g is actively shaped by a proportional-resonant(PR) controller which takes the sensed grid voltage SOGI PLL output.

To investigate the idea in phase-plane see fig 6. With the layer-1 modulation approach, the $nv_{cd_{RMS}}|_{T_s}$ is (shown in green arrow) unchanged from $\omega_g t = 30$ degrees to $\omega_g t = 60$ degrees even though $v_{ab_{RMS}}|_{T_s}$ (sky arrow) is changing. After incorporating the differential carrier shifting treatment in the battery side H-bridge in layer-2 modulation, $nv_{cd_{RMS}}|_{T_s}$ is equal to $v_{ab_{RMS}}|_{T_s}$ within every switching cycle(the pink arrow). With the phase-shift variation in layer 3 of the modulation scheme, the result(blue arrow) is the magnitude-wise same as layer 2 but the phase shift is adjusted to the pulse-width variation to condition the constant power flow.

III. Simulation and Experimental Results

The design parameters of the proposed converter are given in table I. Input AC power fluctuations cause the DC bus to have a second harmonic ripple to handle the power imbalance. Here, note that in layer-2, phase-shift ϕ is generated by a PI controller regulating the V_{BUS} to nV_{BAT}. Although, the PI controller has a very low gain at twice the grid frequency, ϕ is not essentially a constant.ϕ also gets double line frequency variation reflected from the power imbalance.

However, this variation is not shaped properly and not synchronized with the pulse-width change of $v_{ab_{RMS}}|_{T_s}$ or $nv_{cd_{RMS}}|_{T_s}$ as seen from the simulation result presented in fig10. t_1 denotes the zero-crossing instant of grid-cycle and t_2 denotes the positive peak instant of grid-cycle. In the layer-3 outcome, variation of ϕ_{mod} being a controlled output, ϕ_{mod} is minimum , ΔV_{BUS} is zero at t_1 and ϕ_{mod} is maximum,ΔV_{BUS} is maximum at t_2 in layer-3 outcome.However, this is not the case for the layer 2 outcome as that is without phase-shift modulation. Experimental results in fig 9 (a)(b) shows DAB-link waveforms carried out at P_0= 2kW, V_{BAT}=300V, v_g=220V, 50Hz taking two different grid cycle instant. The flat-topped operation of DAB current is highlighted here which is a common condition for both level-2 and level-3 schemes. The effect of phase-shift modulation is highlighted in 9 (c)(d). Both are 500-watt results, 9 (c) is with phase shift modulation (layer-3) and (d) is without phase-shift modulation (layer-2). The reduction in low-frequency

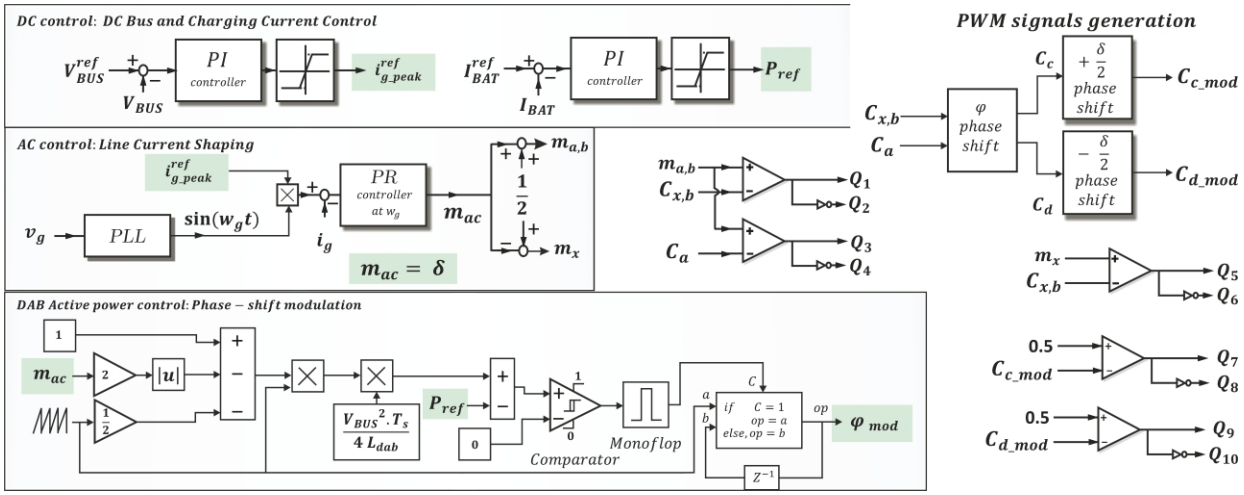

Fig. 8. The Control Architecture for dual phase-shift and pulse-width modulation strategy

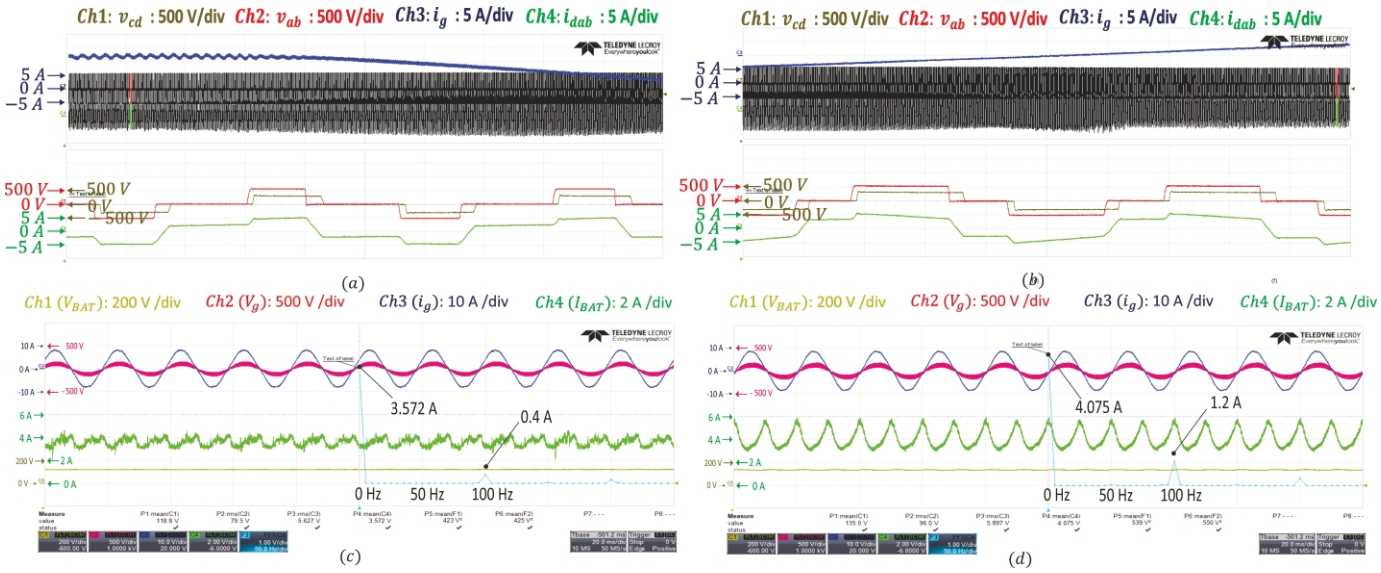

Fig. 9. Experimental Results: HF waveforms at 2kW, V_{BAT}=300 V for flat-top modulation when the phase-shift modulator is not activated, zoomed near the line current peak (a) and line current zero-crossing (b). It can be seen that the pulse width of v_{ab} and nv_{cd} are identical in both the instants and i_{dab} is flat-topped. (c)500W result with the proposed modulation i.e. phase-shift modulator is activated, the FFT result of charging current I_{BAt} is 0.4A whereas at the same power level when phase-shift modulator deactivated the 100Hz component becomes 1.2A (d).

ripple percentage is 35% to 5% over the average value of charging current I_{BAT}. The efficiency measured matches with the predicted value of 97.8% at 500-watt loading. An image of the hardware prototype is attached in fig11.

IV. Power Loss Analysis

The trajectory of $i_{dab_{RMS}}|_{T_s}$ for V_{BAT}=400V,P_0= 3.6kW over a grid cycle is shown in fig12 for three different modulation schemes. It can be understood that Level 3 modulation i.e. combined constant power phase-shift and pulse-width modulation gives the most optimum condition loss. In the loss profile breakdown chart shown in fig 13 (for the same operating conditions), the conduction loss cut down is clear. Also, the proposed modulation brings enhanced ZVS switching region for AC side devices which is affected by the bipolar grid voltage and current. Being a fully PFC leg $leg - x$ observes only grid current i_g. That's why 50% ZVS turn-on and 50% ZVS turn-off happens in a grid cycle for both the switches in $leg - x$. In the hybrid leg, as the devices see both the line current and the HF DAB current, Q_3loses for ZVS turn-on near the negative peak of the line current and Q_4 near the positive peak. Both top and bottom switches in this hybrid leg achieve nearly 65% ZVS switching in level 3 modulation which is increased from 48% in level 2 modulation. The DC side active bridge devices always go through ZVS/ZCS switching during turn-on, thanks to the flat-topped shaped DAB current. Turn-off loss is a major drawback in the DC-DC DAB converter circuits. The scenario is also the same for the level 1 fixed-duty modulation scheme. As the DC side H-bridge switches

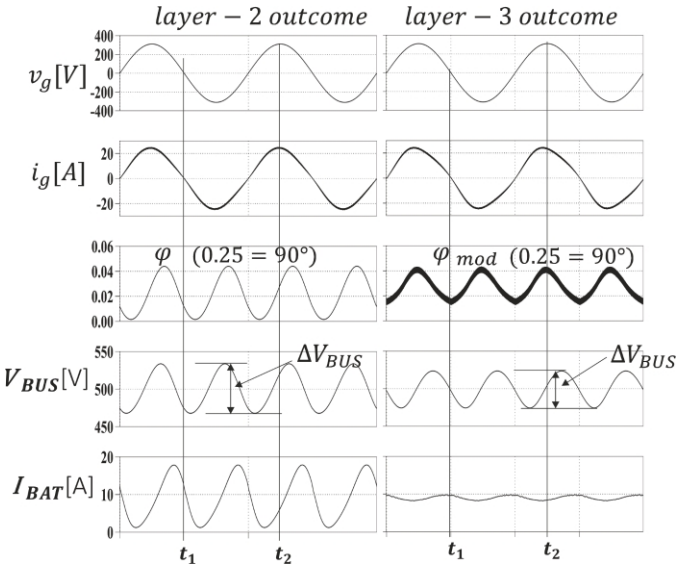

Fig. 10. simulation Results for highlighting the comparison between the layer 2: flat-top modulation and layer 3: the proposed modulation strateg

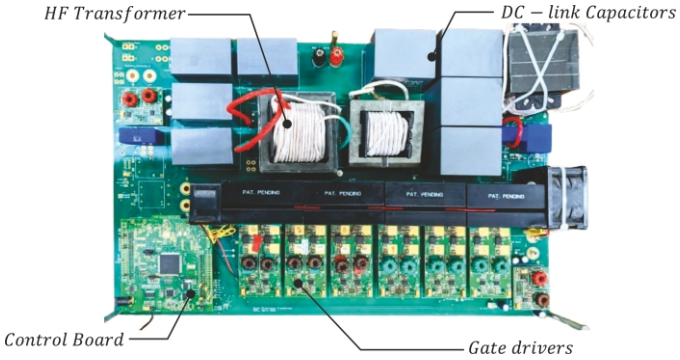

Fig. 11. The Hardware Protoype

with 0.5 duty, the turn-off loss comes in a total of 55.4 watts (1.5% in a 3.6kW system). With pulse-width variation in level 2 modulation, the turn-off wattage loss comes down to 19.16 (0.53% in a 3.6kW system), and with the level 3 modulation, this comes down to 16.7 watts (0.463% in a 3.6kW system).

V. Conclusion

This paper presents a DAB-based 1-phase 1-stage on-board charger, achieving active power decoupling. The proposed modulation strategy combines a pulse-width modulator for the DC-side full bridge to eliminate reactive power loss and an active power-dictated phase-shift modulator to eliminate double line-frequency ripple in the battery charging current. This approach ensures the least RMS DAB current trajectory across the grid cycle and improves the soft switching region. A comparative study is shown to highlight the significant reduction in the power loss profile. Preliminary hardware results are provided to support these findings. Detailed design considerations and full-load hardware results will be presented in a subsequent article.

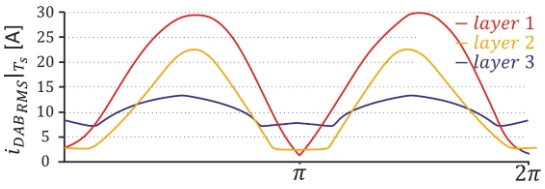

Fig. 12. Trajectory of $i_{dab_{RMS}}|_{T_s}$ for 400V, 3.6kW operation

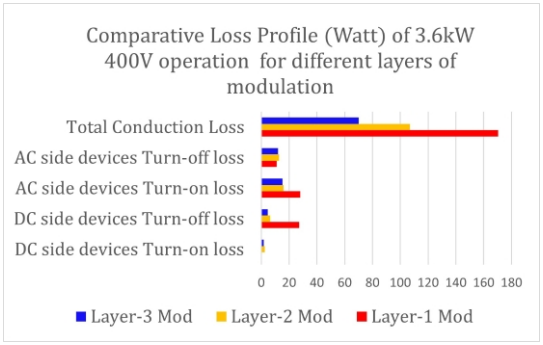

Fig. 13. Loss profile breakdown for 400V, 3.6kW operation

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