SOUMYA MITTAL

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INTERESTS

Integrated circuit test, circuit defect diagnosis including scan diagnosis, physically-aware diagnosis and cell-aware diagnosis, failure data analysis, defect modeling, machine learning

EDUCATION

Carnegie Mellon University — Pittsburgh, PA

PhD in Electrical and Computer Engineering [GPA: 3.87/4] — Expected Dec 2019

Advisor: Prof. Shawn Blanton

Thesis: Learning Enhanced Diagnosis of Logic Circuit Failures

Indian Institute of Technology (IIT) Roorkee — Roorkee, INDIA

Bachelor of Technology in Electronics and Communication Engineering [GPA: 8.76/10] — May 2014

RESEARCH EXPERIENCE

Carnegie Mellon University — Pittsburgh, PA

- Development of an effective digital circuit diagnosis methodology (PhD Thesis)
  - Developed a hybrid deterministic-statistical physically-aware diagnosis approach called *LearnX* that identifies and characterizes a defect within a circuit
    - Improves diagnostic resolution by **30%** for 36 silicon test cases without losing accuracy
  - Developed a back-end and a front-end (cell-aware) layout-analysis technique that further strengthens *LearnX*
    - Improves physical resolution by **2X** when compared with state-of-the-art commercial/EDA software
- Towards efficient digital circuit diagnosis using machine learning
  - Engineered features from test failure data to identify fail logs that result in insignificant diagnosis result
  - Generated and augmented training data via fault simulation and diagnosis
  - Achieves up to **9X** speed-up in a virtual scenario
- Test chip design, test and diagnosis
  - Collaborated on the design of a logic test chip that reflects design characteristics of actual product layouts and diagnoses multiple defects effectively
  - Developed a "Design-for-Diagnosis" method that creates a design from scratch to guarantee **optimal** defect localization accuracy

PROFESSIONAL EXPERIENCE

Intel Corporation — Hillsboro, OR

Graduate Technical Intern — May – Aug 2016

- Evaluated testability and diagnosability of logic block architectures of two different test chip designs

GlobalFoundries, Fab8 — Malta, NY

Summer Intern — July – Aug 2015

- Implemented a physically-aware diagnosis technique that improved diagnostic resolution by 26% without degrading accuracy on 18 silicon test cases for a 14nm FinFET test chip design
- Developed Python APIs for extracting data from the physical layout database to efficiently enable rapid root-cause identification

TECHNICAL SKILLS

EDA Software (Cadence):	Modus/Encounter Test, Virtuoso, SoC Encounter
EDA Software (Mentor Graphics):	Tessent, Calibre, Eldo
EDA Software (Synopsys):	TetraMAX, Design Compiler
Programming Languages:	Python (including Pandas/NumPy/Matplotlib), C, MATLAB, SQLite, Verilog, Tcl

ADDITIONAL EXPERIENCE

Carnegie Mellon University
Pittsburgh, PA

Teaching Assistant

- Digital Systems Testing and Testable Design (18-765) Spring'16, Fall'17, Fall'18, Fall'19
  - Led weekly review and discussion sessions in class
  - Held office hours, and graded exams, homework assignments and projects
- Summer Academy of Mathematics and Science (SAMS) Summer'17, Summer'18, Summer'19
  - Taught self-developed lectures on the basics of programming and circuits

AWARDS

- 1st place in the Ph.D. Forum competition at the European Test Symposium (ETS), 2019
- Neil and Jo Bushnell Fellowship in Engineering, 2018
- Carnegie Institute of Technology Dean's Fellowship for graduate studies, 2014-2019
- Merit Scholarship by Central Board of Secondary Education (CBSE) for undergraduate studies, 2010-2014
- Excellence Award by Indian Institute of Technology (IIT) Roorkee Heritage Foundation, 2013
- Summer Undergraduate Research Award (SURA) by IIT Roorkee, 2012

PATENTS

1. **S. Mittal** and R. D. Blanton; US Patent Application 62/922,401; Integrated Circuit Defect Diagnosis using Machine Learning; Carnegie Mellon University.
2. R. D. Blanton *et al*.; US Patent Application 62/761,725; Logic Characterization Vehicle Design, Test and Diagnosis; Carnegie Mellon University.

PUBLICATIONS

3. **S. Mittal** and R. D. Blanton, "LearnX: A Hybrid Deterministic-Statistical Defect Diagnosis Methodology," IEEE European Test Symposium (ETS), May 2019.
4. C. Fang, Q. Huang, **S. Mittal** and R. D. Blanton, "Diagnosis Outcome Preview through Learning," IEEE VLSI Test Symposium (VTS), Apr 2019.
5. Q. Huang, C. Fang**, S. Mittal** and R. D. Blanton, "Improving Diagnosis Efficiency via Machine Learning," IEEE International Test Conference (ITC), Nov 2018.
6. **S. Mittal** and R. D. Blanton, "NOIDA: Noise-resistant Intra-cell Diagnosis," in IEEE VLSI Test Symposium (VTS), Apr 2018.
7. **S. Mittal** and R. D. Blanton, "PADLOC: Physically-Aware Defect Localization and Characterization," IEEE Asian Test Symposium (ATS), Nov 2017.
8. B. Niewenhuis, **S. Mittal** and R. D. Blanton, "Multiple-defect diagnosis for Logic Characterization Vehicles," IEEE European Test Symposium (ETS), May 2017.
9. **S. Mittal**, Z. Liu, B. Niewenhuis and R. D. Blanton, "Test chip design for optimal cell-aware diagnosability," IEEE International Test Conference (ITC), Nov 2016.
10. P. Fynan, Z. Liu, B. Niewenhuis, **S. Mittal**, M. Strojwas and R. D. Blanton, "Logic characterization vehicle design reflection via layout rewiring," IEEE International Test Conference (ITC), Nov 2016.
11. B. Niewenhuis, Z. Dexter Liu, **S. Mittal** and R. D. Blanton, "Logic characterization vehicle design for yield learning," SEMI Advanced Semiconductor Manufacturing Conference (ASMC), May 2016.
12. Z. Liu, B. Niewenhuis, **S. Mittal** and R. D. Blanton, "Achieving 100% cell-aware coverage by design," Design, Automation & Test in Europe Conference & Exhibition (DATE), Mar 2016.