Digital System Design SS2024

Lab 2: Parallel Processing (Digital Audio Filter)

Report submitted by:

Soumya Ranjan Sabat
Matrikelnr: 1127993

Azaz Hassan Khan
Matrikelnr: 1128032

May/29/2024

Content

1   Introduction

The main purpose of this lab is to display selected filter number on the attached 7-segment display. The 7- segment display is attached to the Pmod JA1+JB1 of ZedBoard. Parallel processing in FPGAs is demonstrated by analysing the implementation of algorithms for Digital filters.

- Study of the top-level RTL design
- VHDL design of the Camera Emulator
- Simulation of the Camera Emulator
- Test of HDMI Display Controller on ZedBoard

1.1   Tasks

1.1.1   I2S data format for audio data exchange

Q1. Explain the data format I2S for audio data exchange between Audio Codec and Zynq device! Name data signals and clock signals of this data format by studying ADAU1761 product description!
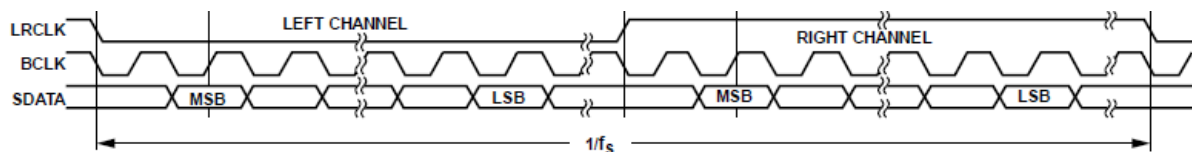
- LRCLK: Serial Data Port Frame Clock
- BCLK: Serial Data Port Bit Clock
- SDATA: Audio serial data

Serial data port Bit clock, BCLK has a frequency configured in accordance with the desired sampling bit rate. On every Negative edge trigger of BCLK one audio data bit is transmitted. The whole frame is sent twice, one to the left channel and one to the right channel of the Zync DSP block. LRCLK has duty cycle of 50% and on every negative edge of LRCLK data is sent to right channel and on every positive edge of LRCLK data is sent to left channel.

1.1.2   Analysis and understanding RTL Design

Q1. What is the purpose of the multiplexer hphone_l_i and hphone_r_i?

Input is being sampled by the audio codec from input GPIO pins. Sampled inputs are subjected to low pass filters to cancel the external noise associated with it. There are three filters with different lengths and filtering capabilities and one dsp block with no filtering. Any one of the three filters or the block with no filtering can be selected by the user. Hphone_l_i and Hphone_r_i takes the filtered outputs as input and user filter choice as selection bits and delivers corresponding output.

User selection for MUX output:

00	No Filtering
01	Filter with length 8
10	Filter with length 16
11	Filter with length 32

Q2. What is the function of Inst_dsp_block?

It takes AD converted signal from Audio Codec and sends the same to output without filtering.

Q3. Which port is connected to the serial data output of ADC?

ADC_SDATA/GPIO1 (pin 26): ADC Serial Output Data (ADC_SDATA).

Q4. Which port is connected to the serial data input of DAC?

DAC_SDATA/GPIO0 (pin 27): DAC Serial Input Data (DAC_SDATA).

Q5. Which clock frequency is used for signal MCLK?

Clock frequency of MCLK is 24MHz and sampling frequency of ADC and DAC is 48 KHz.

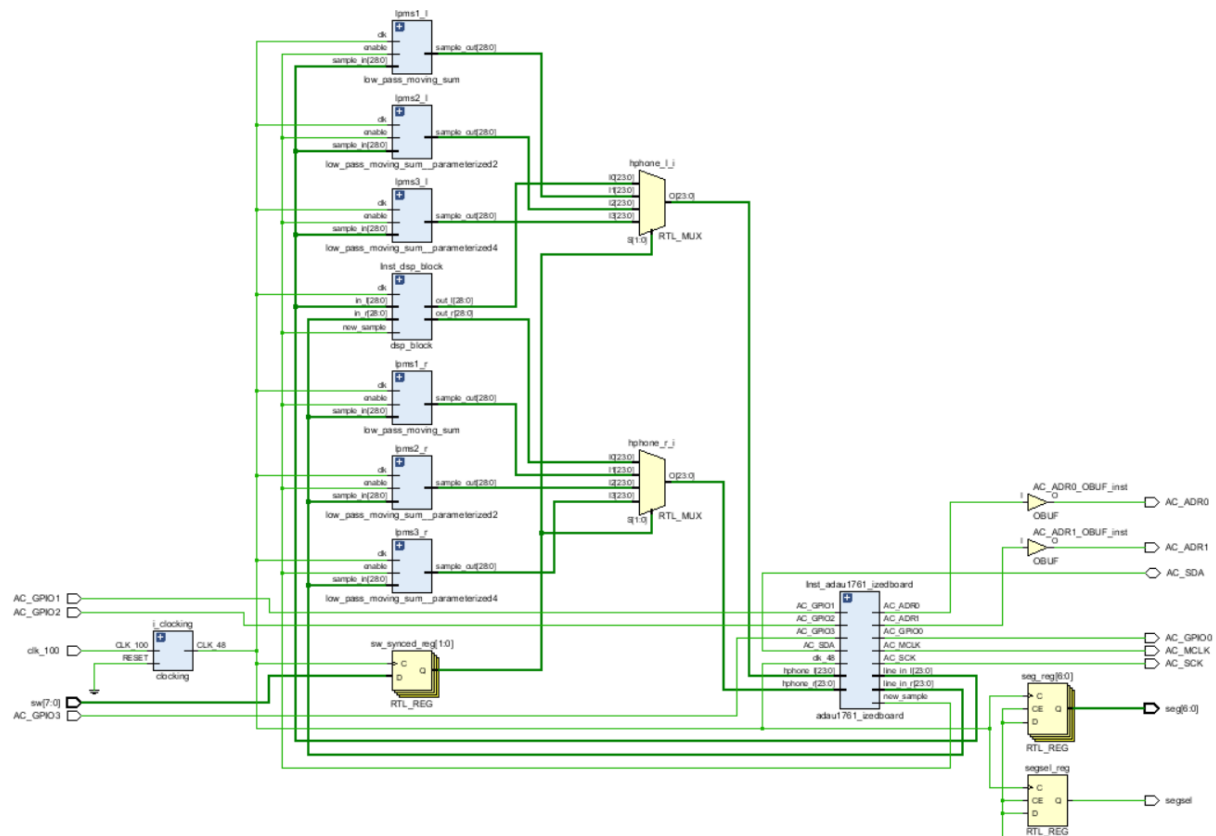**Q6**. What is the filter length N of the three low pass filters?

Filter lengths N of the three low pass filters are 8, 16 and 32 respectively.

Cutoff Frequency, Fc = sampling frequency/ filter length

For Filter lengths:
- N =8, Fc = 6 KHz
- N=16, Fc = 3 KHz
- N=32, Fc = 1.5 KHz

1.1.3 Top Level Inputs and Outputs

Input Signals	Description
AC_GPIO1	Digital Audio Serial Data ADC Output (I2S MOSI)
AC_GPIO2	Digital Audio Bit Clock Input/Output (I2S_bclk)
clk_100	Clock configuration
sw [7:0]	filter select
AC_GPIO3	Digital Audio Left-Right Clock Input/Output (I2S_LR)

Output Signals	Description
AC_ADR0	I2C Address Bit 0/SPI Latch Signal
AC_ADR1	I2C Address Bit 1/SPI Data Input
AC_SDA	I2C Serial Data Interface(bidirectional)
AC_GPIO0	Digital Audio Serial-Data DAC Input (I2S MISO)
AC_MCLK	Master Clock input(codec)
AC_SCK	I2C Serial Data interface
seg [6:0]	7 segments
segsel	cathode

2 References

[1] "VHDL Programming by Example" by Douglas L. Perry

[2] "VHDL: Analysis and Modeling of Digital Systems" by Zainalabedin Navabi

[3] "FPGA Prototyping by VHDL Examples: Xilinx MicroBlaze MCS SoC" by Pong P. Chu

[4] "The Zynq Book" by Louise H. Crockett et al.

[5]