Digital System Design
SS 2022

Lab 3: JPEG-Encoder

Report submitted by :

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Content

1 Introduction

The Vivado IP integrator lets you create complex system designs by instantiating and interconnecting IP from the Vivado IP catalog or from other sources. Here, we want to analyze a DCT-IP (discrete cosine transform) core and synthesize it onto a FPGA programmable logic.

The purpose is to use the hardware implementation of DCT to perform a fast JPEG conversion. For this we use Zynq device, a SoC from Xilinx. The SoC combines an ARM dual-core Cortex-A9 Processing System with FPGA programmable logic.

Here we go through a workflow of how to create an IP on FPGA programmable logic and how to interface it with a C++ project running on ARM processor to finally build a hardware/software-codesign. The major goal of this codesign is performance optimization.

2 Questions

2.1 Part A : Analysis of Custom IP

(a):

Task-Description:

Draw a block diagram of the VHDL module “DCT_AAN”! Briefly explain with the help of IP documentation how to calculate the 2D DCT of a 8x8 matrix.

Analysis:

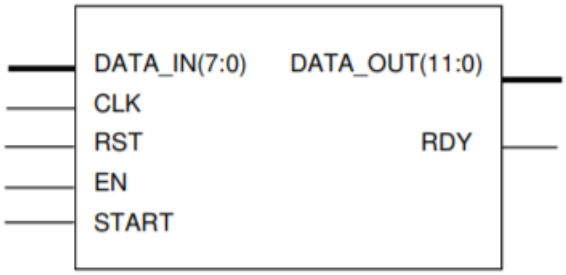

Figure 1.1: Block diagram of DCT_AAN module

- I2S is a serial bus designed for digital audio devices. It handles audio data separately from the clock signals.
- A 2D DCT transforms a 8x8 array into 8x8 result array.
- The 8-point DCT transforms the columns and then the rows.
- The input 8x8 image data block consists of integers in the range 0 to 255. Before the DCT calculation, the mean value 128 is subtracted from input data to minimize the redundancy in the input data block.
- An image is split into several macroblocks.
- To calculate the DCT coefficients for a single block. The proposed implementation is optimized by the total amount of described floating point operations.

- The floating-point divisions by constants are replaced with multiplications by reciprocals or arithmetic shifts.
- An image with 8x8 blocks (1st kernel) splits into macroblocks.
  Each macroblock contains 8 blocks (2nd kernel) which is split into macroblocks.
  Each macroblock contains 16 blocks (short kernel). The image is split with different grids.
- The described approach takes into account the structure of matrix T A that exhibits high redundancy and symmetry of matrix elements.

$$A^T = \frac{1}{\sqrt{8}} \cdot \left[\begin{array}{cccc|cccc} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ a & c & d & f & -f & -d & -c & -a \\ b & e & -e & -b & -b & -e & e & b \\ c & -f & -a & -d & d & a & f & -c \\ \hline 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ d & -a & f & c & -c & -f & a & -d \\ e & -b & b & -e & -e & b & -b & e \\ f & -d & c & -a & a & -c & d & -f \end{array}\right],$$

where a,b,c,d,e,f stand for (9):

$$a = \sqrt{2}\cos\left(\frac{\pi}{16}\right) \quad d = \sqrt{2}\cos\left(\frac{5\pi}{16}\right)$$
$$b = \sqrt{2}\cos\left(\frac{\pi}{8}\right) \quad e = \sqrt{2}\cos\left(\frac{3\pi}{8}\right)$$
$$c = \sqrt{2}\cos\left(\frac{3\pi}{16}\right) \quad f = \sqrt{2}\cos\left(\frac{7\pi}{16}\right)$$

Thus, the 8-point DCT equation $Y = A^T X$ can be decomposed in (10):

$$\begin{bmatrix} Y(0) \\ Y(2) \\ Y(4) \\ Y(6) \end{bmatrix} = \frac{1}{\sqrt{8}} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 \\ b & e & -e & -b \\ 1 & -1 & -1 & 1 \\ e & -b & b & -e \end{bmatrix} \cdot \begin{bmatrix} X(0)+X(7) \\ X(1)+X(6) \\ X(2)+X(5) \\ X(3)+X(4) \end{bmatrix}$$

$$\begin{bmatrix} Y(1) \\ Y(3) \\ Y(5) \\ Y(7) \end{bmatrix} = \frac{1}{\sqrt{8}} \cdot \begin{bmatrix} a & -c & d & -f \\ c & f & -a & d \\ d & a & f & -c \\ f & d & c & a \end{bmatrix} \cdot \begin{bmatrix} X(0)-X(7) \\ X(6)-X(1) \\ X(2)-X(5) \\ X(4)-X(3) \end{bmatrix}$$

Figure 1.2: 8-point DCT

(b):

Task-Description:

A test bench for the DCT-IP core is also available. Explain the functions of the three components “TEST_DCT “, “DCT_BEH“ and “BMP_Generator“! What function does the process “ERROR_CALC“ have?

Analysis:

TEST_DCT

- It is the test bench of DCT IP where we instantiate the BMP_Generator, DCT_AAN and DCT_BEH modules to check the DCT behavior.
- The data pattern is generated using the module BMP_Generator.
- Discrete Cosine Transform is calculated in two methods in this module.
  The first method is calculated using the DCT_AAN module and the other method is calculated using DCT_BEH module.

DCT_BEH

- It is a behavioural model of the DCT processor.
- It computes the floating-point calculations.
- Its results are rounded to 12 bits. Therefore, it serves as the standard model.

BMP_Generator

- Generates dataflow of testing arrays.
- In one mode, it generates predefined arrays, in another mode it does randomized ones.

Error_Calc

- This calculates the differences in the output data of DCT_AAN and DCT_BEH.
- The resulting signals are ERROR which are of signal subtraction, SERROR as the sum of squared errors for a single data array and QUADMEAN which is the result mean square error value for the current array.

2.2 Part B : Verification of the Custom IP

(a):

Task-Description:

Explain the meaning of the following output signals: DCT[11:0], DCT_STD[11:0], ERROR, QUADMEAN!

Analysis:

- DCT [11:0]: Output Data value is displayed here.
- DCT_STD [11:0]: Signal from DCT_BEH.
  It computes the floating-point calculations. Its results are rounded to 12 bits. Therefore, it serves as the standard model.
- The differences in the output data of DCT_AAN and DCT_BEH are calculated. The resulting signals are ERROR which of signal subtraction, QUADMEAN which is the result mean square error value for the current array.

(b):

Task-Description:

Verify the functionality of the custom IP using the provided test bench. Simulate at least for 20µs. What is the delay (number of clock cycles) between first data input and first data output? How many clock cycles does it take to read in one input matrix? Give the min. and max. value of mean square error for this simulation! Attach simulation snapshots to verify your findings!

Analysis:

- The delay between first data input and first data output is 133 clock cycles.
- It takes 64 clock cycles to read in 8x8 input matrix.
- The min. and max. value of mean square error for this simulation are 0 and 1.04582503316759.

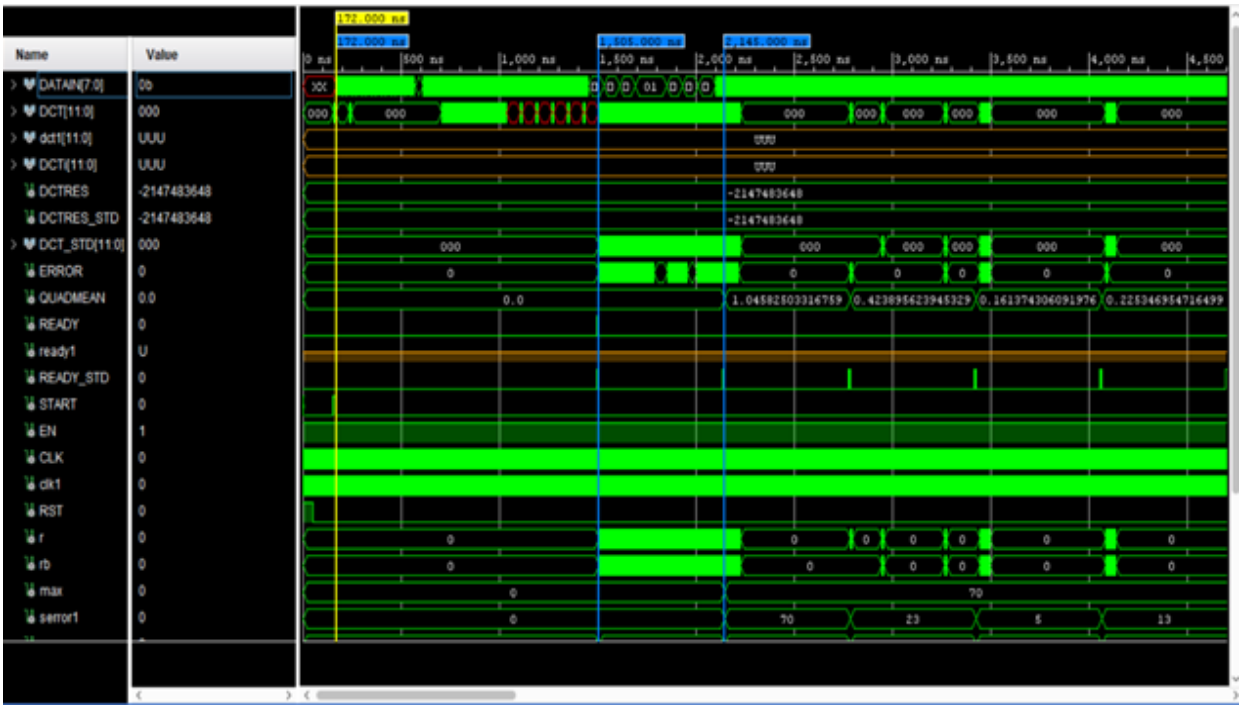

Figure 1.3: Simulation

2.3 Part C : Instantiation of DCT core

Task-Description: VHDL-code for instantiation of the DCT core

Analysis: Shown below in Figure 1.4

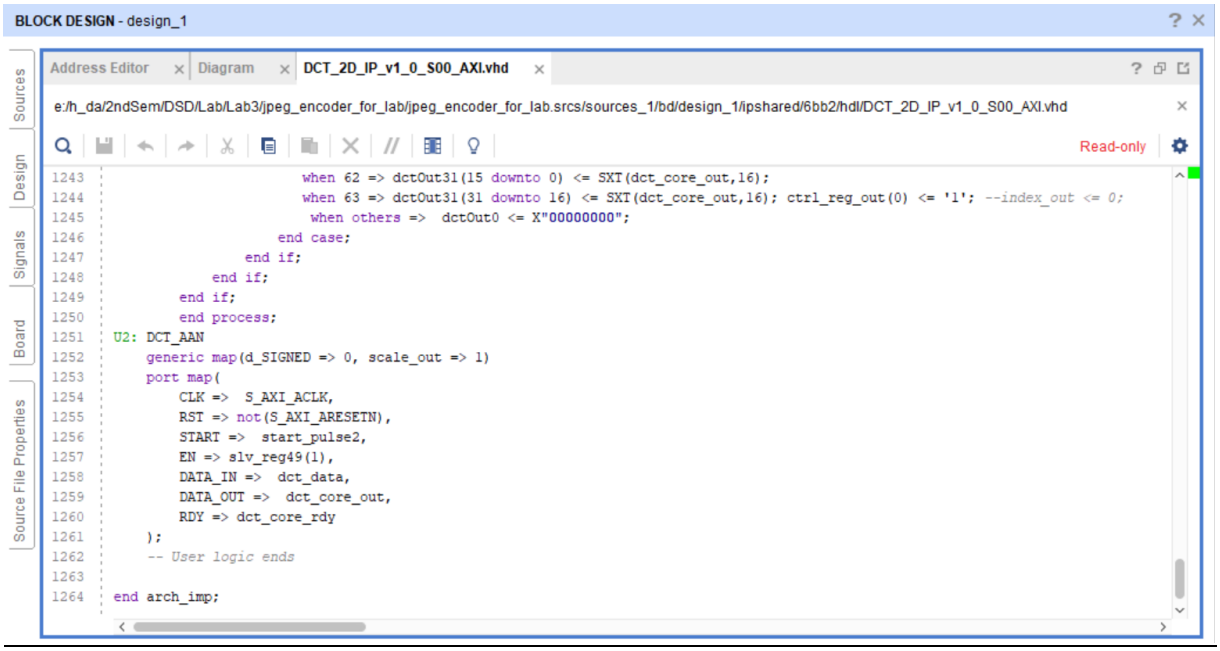

Figure 1.4: VHDL-code for instantiation of the DCT core

2.4 Part D : JPEG Encoder

Task-Description: Screenshot of folder jpeg_encoder (step 12) including jpeg_encoder.elf with time stamp of your windows screen!

Analysis:

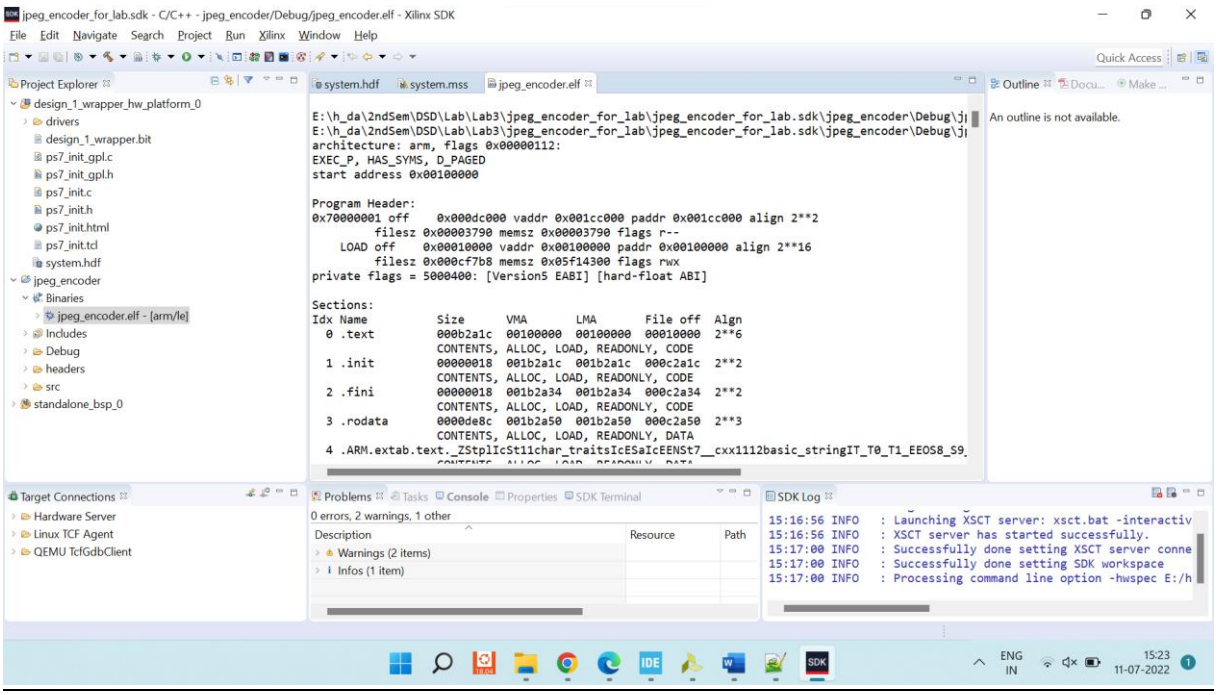

Figure 1.5: jpeg_encoder.elf

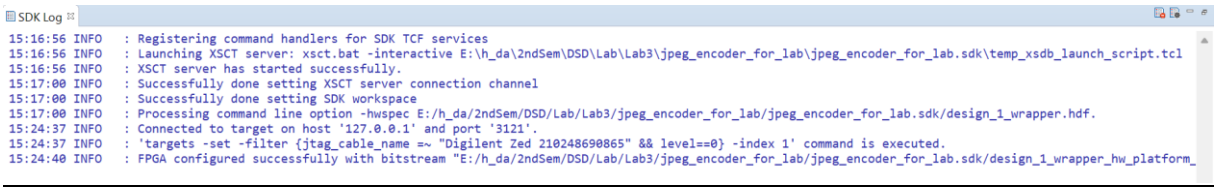

Figure 1.6: Programming FPGA

2.5 Part E : Statistics

Task-Description: Screen shot of statistics in Terminal 1 (step14)! Compare BMP vs JPEG regarding size and quality!

Analysis:

- The screenshots of the statistics are shown in Figure 1.7 below followed by BMP vs JPEG image size and quality.
- The size of BMP images is larger than that of the JPEG images. This shows that the JPEG images have been compressed.

Connected to: Serial (COM4, 115200, 0, 8)

```
Connected to COM4 at 115200
Already connected to port: COM4INFO: Push start button to start encoder

INFO: Push start button to start encoder

INFO: Encoder FSM init started...

INFO: Collecting bmp files.

TRACE: Adding bmp file: BLU.BMP

TRACE: Adding bmp file: FLAG_B24.BMP
TRACE: Adding bmp file: RAY.BMP

INFO: Initialized!

INFO: Initializing Bitmap image instance.

INFO: Loading Bitmap Header informations.

INFO: Bitmap loaded: /BMP/BLU.BMP

INFO: Bitmap File size:    86454 byte
INFO: Bitmap Image width:  200 pixels

INFO: Bitmap Image height: 144 pixels

INFO: Converting file /BMP/BLU.BMP
INFO: Initializing JPEG image.

INFO: Creating JPEG header informations.

INFO: JPEG file with header informations has been created /JPG/BLUJPG .

INFO: Creating corresponding JPEG file: /JPG/BLUJPG

INFO: Converting Bitmap pixel to JPEG pixel values.
```

Connected to: Serial (COM4, 115200, 0, 8)

```
OLED: Status: 94%

INFO: Converting image row: 71 of 75
OLED: Status: 96%

INFO: Converting image row: 72 of 75

OLED: Status: 97%
INFO: Converting image row: 73 of 75
OLED: Status: 98%

INFO: Converting image row: 74 of 75

OLED: Status: 100%

INFO: Converting image row: 75 of 75

INFO: JPEG Image conversion for: /JPG/RAY.JPG finished.

INFO: JPEG File size: 760006 byte

INFO: JPEG compression rate: 100

INFO: JPEG image /BMP/RAY.BMP was encoded in: 28131ms

INFO: I/O time amount: 15150ms

INFO: Bitmap Block extraction time amount: 136ms

INFO: DCT time amount: 2405ms

INFO: Color Conversion time amount: 1251ms

INFO: Quantization time amount: 1782ms

INFO: Huffman encoding time amount: 7330ms
```

Figure 1.7: Statistics

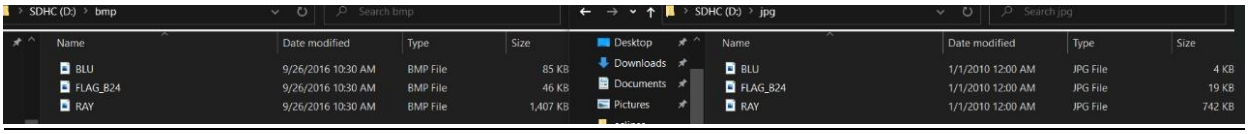

Figure 1.8: BMP vs JPG file size

Figure 1.9: BMP vs JPG picture quality