

Digital System Design

SS 2023

Lab 3: JPEG-Encoder

Report submitted by :

GeethuSagar Ajitha
Matrikelnr : 1119258

Riya Alias
Matrikelnr : 1119262

Najmeddine Bouzambila
Matrikelnr: 738345

July/10/2023

Content

1	Introduction	3
2	Task1: Verification of DCT-IP	3
2.1	Analysis of the Custom IP	3
2.2	Verification of the Custom IP	4
3	Task2: Integration of DCT-IP into JPEG encoder project.....	5
3.1	Instantiating the DCT_AAN core.....	5
3.2	Jpeg_Encoder	6
3.3	Screenshot of Statics in Terminal and compare BMP and JPEG images	7

1 Introduction

In this lab, we use a powerful feature within the Vivado Design Suite called the Vivado IP integrator. The Vivado IP integrator lets us create complex system designs by instantiating and interconnecting IP from the Vivado IP catalog or from other sources. We want to analyze a DCT-IP core and synthesize it onto a FPGA programmable logic. The purpose is to use the hardware implementation of DCT to perform a fast JPEG conversion

2 Task1: Verification of DCT-IP

2.1 Analysis of the Custom IP

a) Draw a block diagram of the VHDL module, DCT_AAN"! Briefly explain with the help of IP documentation how to calculate the 2D DCT of a 8x8 matrix. Hint: You may have to analyze its subcomponents

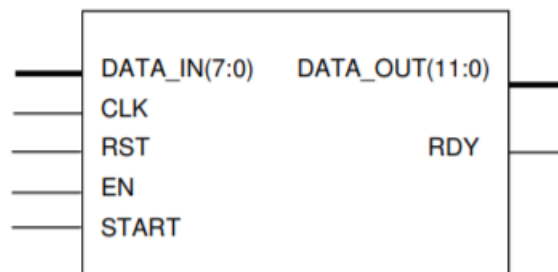


Fig 1: DCT_AAN block

A 2D discrete cosine transform (DCT) is applied to an 8x8 array, resulting in an 8x8 array of coefficients. The DCT is performed by first transforming the columns and then the rows of the input 8x8 image data block. The values in the input data block range from 0 to 255, and before the DCT calculation, the mean value of 128 is subtracted to reduce redundancy in the data.

The implementation of the DCT coefficients calculation for a single block is optimized based on the total number of floating-point operations involved. Instead of using floating-point divisions with constants, more efficient operations such as multiplications by reciprocals or arithmetic shifts are utilized. The image is divided into macroblocks, with each macroblock containing 8 blocks (referred to as the second kernel), and these blocks are further split into macroblocks, with each macroblock containing 16 blocks (referred to as the short kernel). Various grids are used to partition the image. This approach considers the structure of matrix T A, which demonstrates significant redundancy and symmetry in its elements.

$$A^T = \frac{1}{\sqrt{8}} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ a & c & d & f & -f & -d & -c & -a \\ b & e & -e & -b & -b & -e & e & b \\ c & -f & -a & -d & d & a & f & -c \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ d & -a & f & c & -c & -f & a & -d \\ e & -b & b & -e & -e & b & -b & e \\ f & -d & c & -a & a & -c & d & -f \end{bmatrix},$$

where a, b, c, d, e, f stand for (9):

$$\begin{aligned} a &= \sqrt{2} \cos\left(\frac{\pi}{16}\right) & d &= \sqrt{2} \cos\left(\frac{5\pi}{16}\right) \\ b &= \sqrt{2} \cos\left(\frac{\pi}{8}\right) & e &= \sqrt{2} \cos\left(\frac{3\pi}{8}\right) \\ c &= \sqrt{2} \cos\left(\frac{3\pi}{16}\right) & f &= \sqrt{2} \cos\left(\frac{7\pi}{16}\right) \end{aligned}$$

Thus, the 8-point DCT equation $Y = A^T X$ can be decomposed in (10):

$$\begin{aligned} \begin{bmatrix} Y(0) \\ Y(2) \\ Y(4) \\ Y(6) \end{bmatrix} &= \frac{1}{\sqrt{8}} \begin{bmatrix} 1 & 1 & 1 & 1 \\ b & e & -e & -b \\ 1 & -1 & -1 & 1 \\ e & -b & b & -e \end{bmatrix} \begin{bmatrix} X(0) + X(7) \\ X(1) + X(6) \\ X(2) + X(5) \\ X(3) + X(4) \end{bmatrix} \\ \begin{bmatrix} Y(1) \\ Y(3) \\ Y(5) \\ Y(7) \end{bmatrix} &= \frac{1}{\sqrt{8}} \begin{bmatrix} a & -c & d & -f \\ c & f & -a & d \\ d & a & f & -c \\ f & d & c & a \end{bmatrix} \begin{bmatrix} X(0) - X(7) \\ X(6) - X(1) \\ X(2) - X(5) \\ X(4) - X(3) \end{bmatrix} \end{aligned}$$

b): A test bench for the DCT-IP core is also available. Explain the functions of the three components „TEST_DCT“, „DCT_BEH“ and „BMP_Generator“! What function does the process „ERROR_CALC“ have?

DCT_BEH: The behavioral model of the DCT processor performs the floating-point calculations and produces results rounded to 12 bits. This model serves as the standard representation for comparison purposes.

BMP_Generator: This module generates the dataflow of testing arrays. It has two modes: one for generating predefined arrays and another for generating randomized arrays.

Error_Calc: This component calculates the discrepancies between the output data of DCT_AAN and DCT_BEH. It generates three signals: ERROR, which represents the difference between the two signals through subtraction, SERROR, which represents the sum of squared errors for a single data array, and QUADMEAN, which provides the mean square error value for the current array.

2.2 Verification of the Custom IP

Task Description(a): Explain the meaning of the following output signals: DCT[11:0], DCT_STD[11:0], ERROR, QUADMEAN!

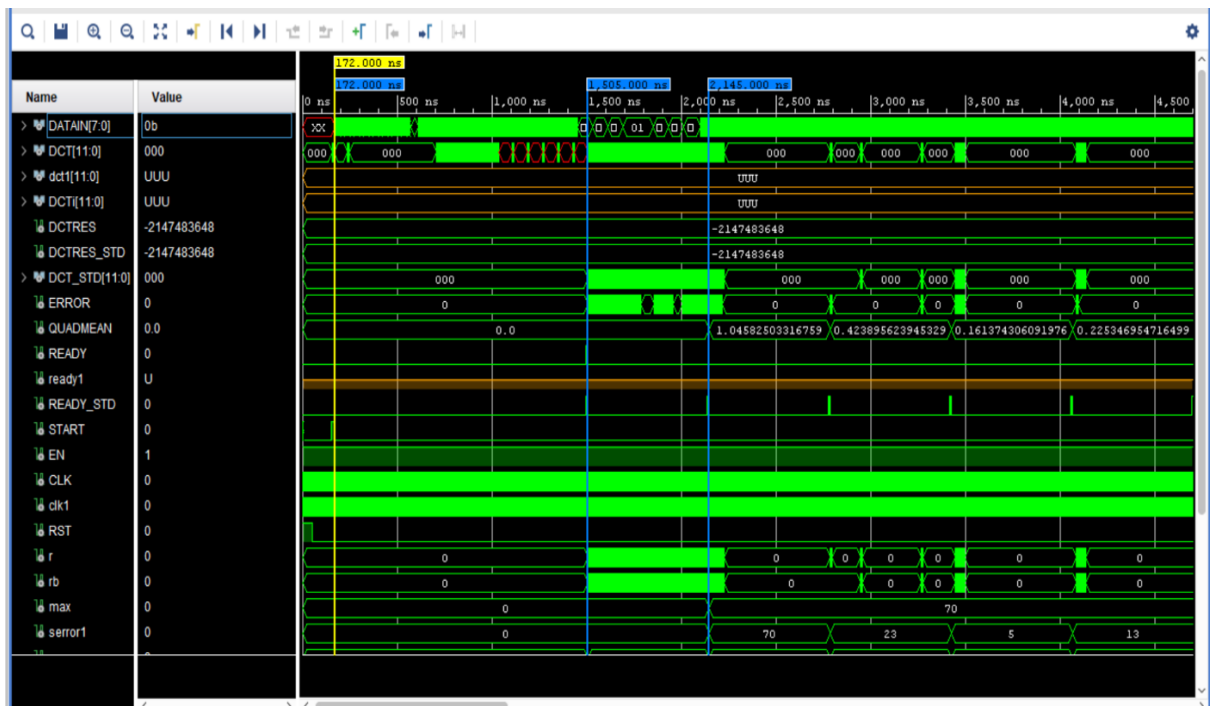
Analysis:

- DCT[11:0] : This is for Output Data
- DCT_STD[11:0] : It computes the floating-point calculations. Results are rounded to 12 bits. And it acts as standard model.
- ERROR: The difference in the output data of DCT_AAN and DCT_BEH.
- QUADMEAN: The differences in the output data of DCT_AAN and DCT_BEH are calculated. QUADMEAN is the result mean square error value for the current array.

Task Description(b): Verify the functionality of the custom IP using the provided test bench. Simulate at least for 20 μ s (step 4). What is the delay (number of clock cycles) between first data input and first data output? How many clock cycles does it take to read in one input matrix? Give the min. and max. value of mean square error for this simulation! Attach simulation snapshots to verify your findings!

Analysis:

- Delay between first data input and first data output = 133 cycles
- Clock cycles required to read input matrix = 64
- Min. root mean square error = 0
- Max. root mean square error = 1.045825033

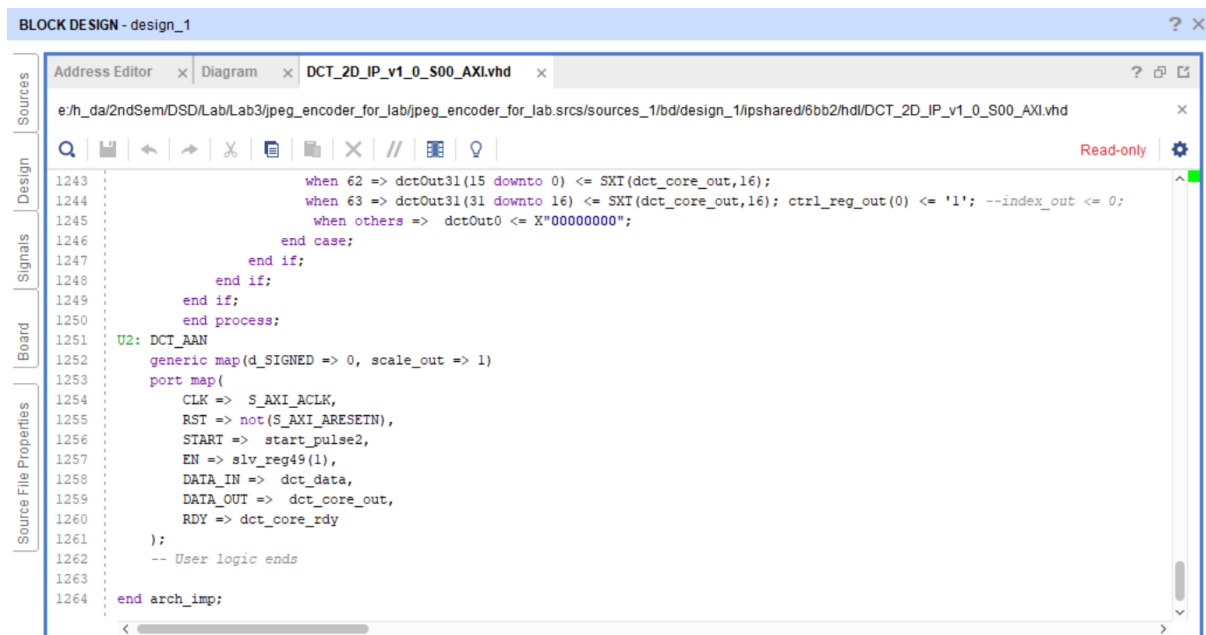


3 Task2: Integration of DCT-IP into JPEG encoder project

Task Description: Integration of the hardware custom IP into an existing JPEG encoder project by creating a custom IP on FPGA and integrate the IP into a JPEG encoder project to finally build a hardware/software-codesign.

3.1 Instantiating the DCT_AAN core

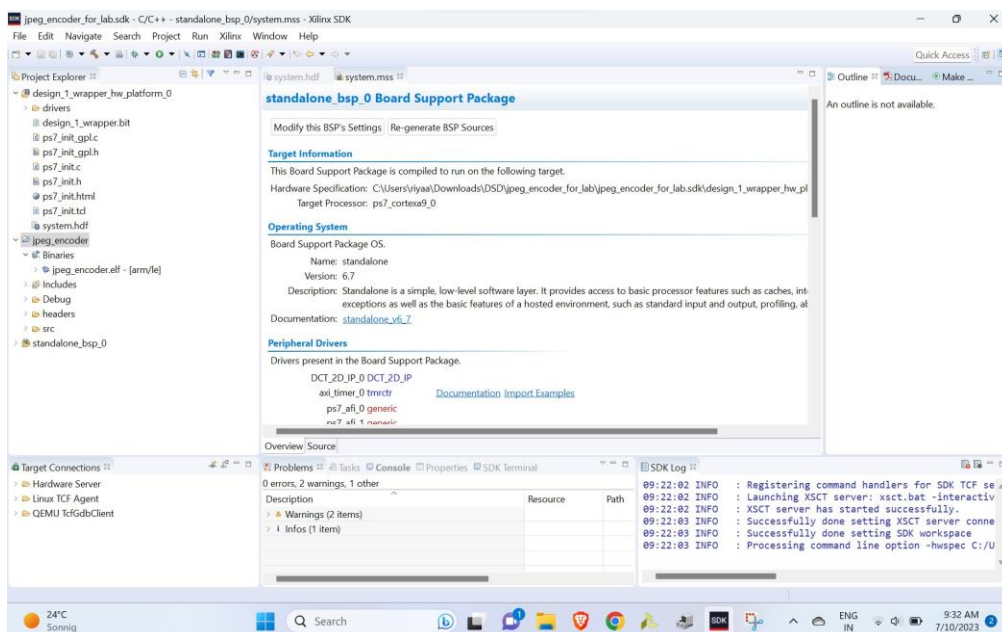
Task Description : Instantiate the DCT_AAN core. As the data handling between the IP Core and the ARM Processor via the introduced buffer is established, instantiate the DCT_AAN component within the VHDL-file „DCT_VHDL_IP_v1_0_S00_AXI.vhd”. Move to the end of the file and complete the port map section of DCT_AAN instantiation!



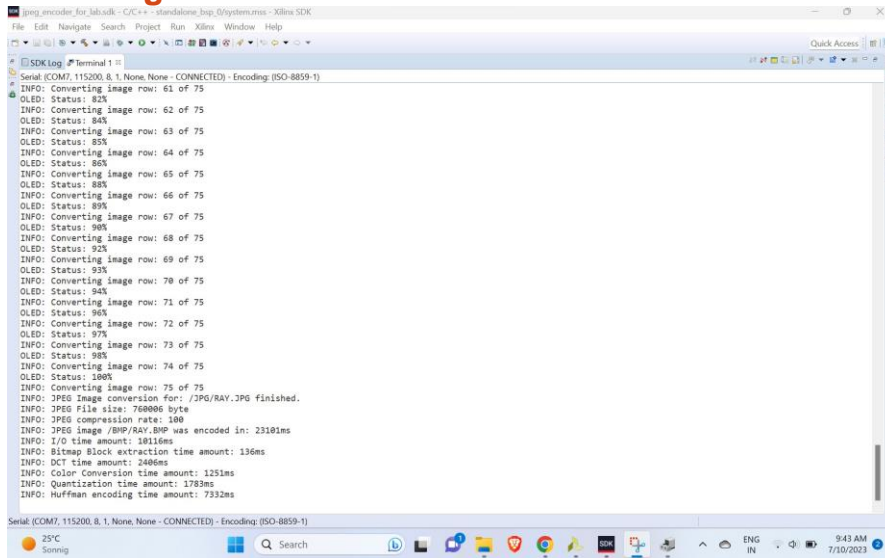
3.2 Jpeg_Encoder

Task Description: Do a screenshot of folder jpeg_encoder including *jpeg_encoder.elf* with time stamp of your windows screen!

Task Analysis:

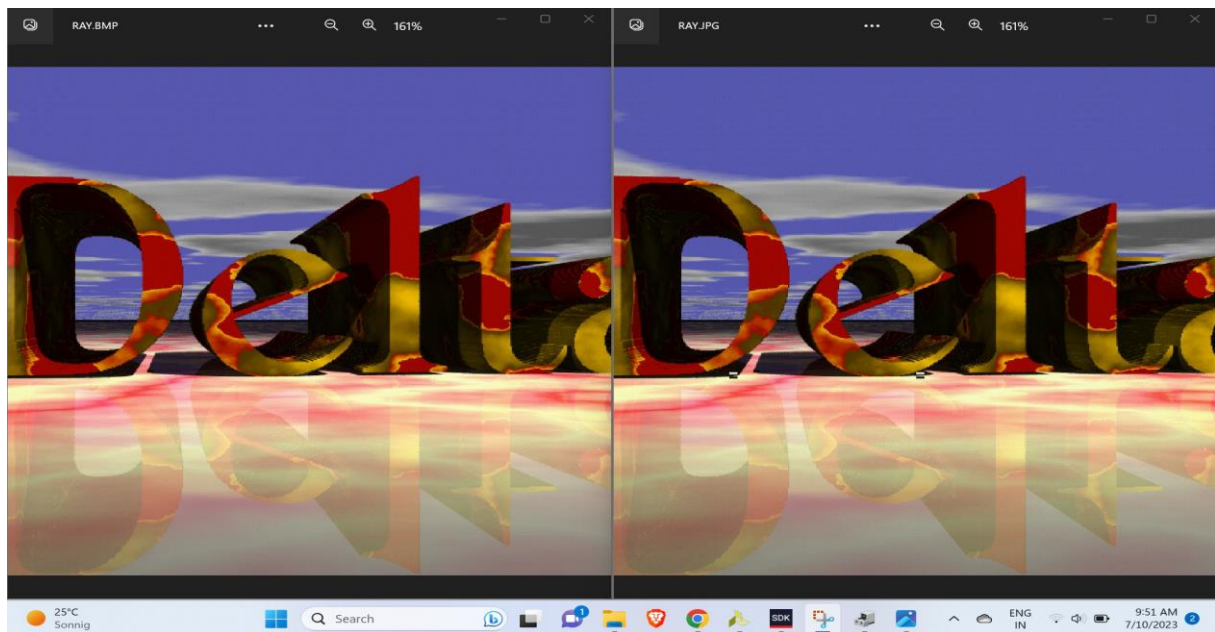


3.3 Screenshot of Statics in Terminal and compare BMP and JPEG images



```
prog: encoder for: J:\JPG - C:\C++ - standalone.jpg: 0x5d5e0000 - Xilinx SDK
Serial (COM7, 115200, 8, 1, None, None - CONNECTED) - Encoding: (ISO-8859-1)
INFO: Converting image row: 61 of 75
OLED: Status: 82%
INFO: Converting image row: 62 of 75
OLED: Status: 84%
INFO: Converting image row: 63 of 75
OLED: Status: 85%
INFO: Converting image row: 64 of 75
OLED: Status: 86%
INFO: Converting image row: 65 of 75
OLED: Status: 88%
INFO: Converting image row: 66 of 75
OLED: Status: 89%
INFO: Converting image row: 67 of 75
OLED: Status: 90%
INFO: Converting image row: 68 of 75
OLED: Status: 92%
INFO: Converting image row: 69 of 75
OLED: Status: 93%
INFO: Converting image row: 70 of 75
OLED: Status: 94%
INFO: Converting image row: 71 of 75
OLED: Status: 95%
INFO: Converting image row: 72 of 75
OLED: Status: 97%
INFO: Converting image row: 73 of 75
OLED: Status: 98%
INFO: Converting image row: 74 of 75
OLED: Status: 100%
INFO: Converting image row: 75 of 75
INFO: JPEG Image conversion for: /JPG/RAY.JPG finished.
INFO: JPEG File size: 769896 byte
INFO: JPEG compression rate: 100
INFO: JPEG image /BMP/RAY.BMP was encoded in: 23101ms
INFO: I/O time amount: 1811ms
INFO: Bitmap Block extraction time amount: 136ms
INFO: DCT time amount: 246ms
INFO: color Conversion time amount: 1251ms
INFO: Quantization time amount: 1783ms
INFO: Huffman encoding time amount: 7332ms
Serial (COM7, 115200, 8, 1, None, None - CONNECTED) - Encoding: (ISO-8859-1)
```

The size of BMP image is more than JPG image and the BMP image has more quality.



FILE NAME	JPG SIZE	BMP SIZE
BLU	4 KB	85 KB
FLAG_B24	19 KB	46 KB
RAY	742 KB	1407 KB