Lab2: Parallel Processing (Digital Audio Filter)
3 points

The parallelism and customizable architecture inherent in the FPGA architecture is ideal for high-throughput processing. Digital filters are one possible application. In this lab we are dealing with a digital audio filter implemented on the **Programmable Logic (PL)** of the SoC ZYNQ device.

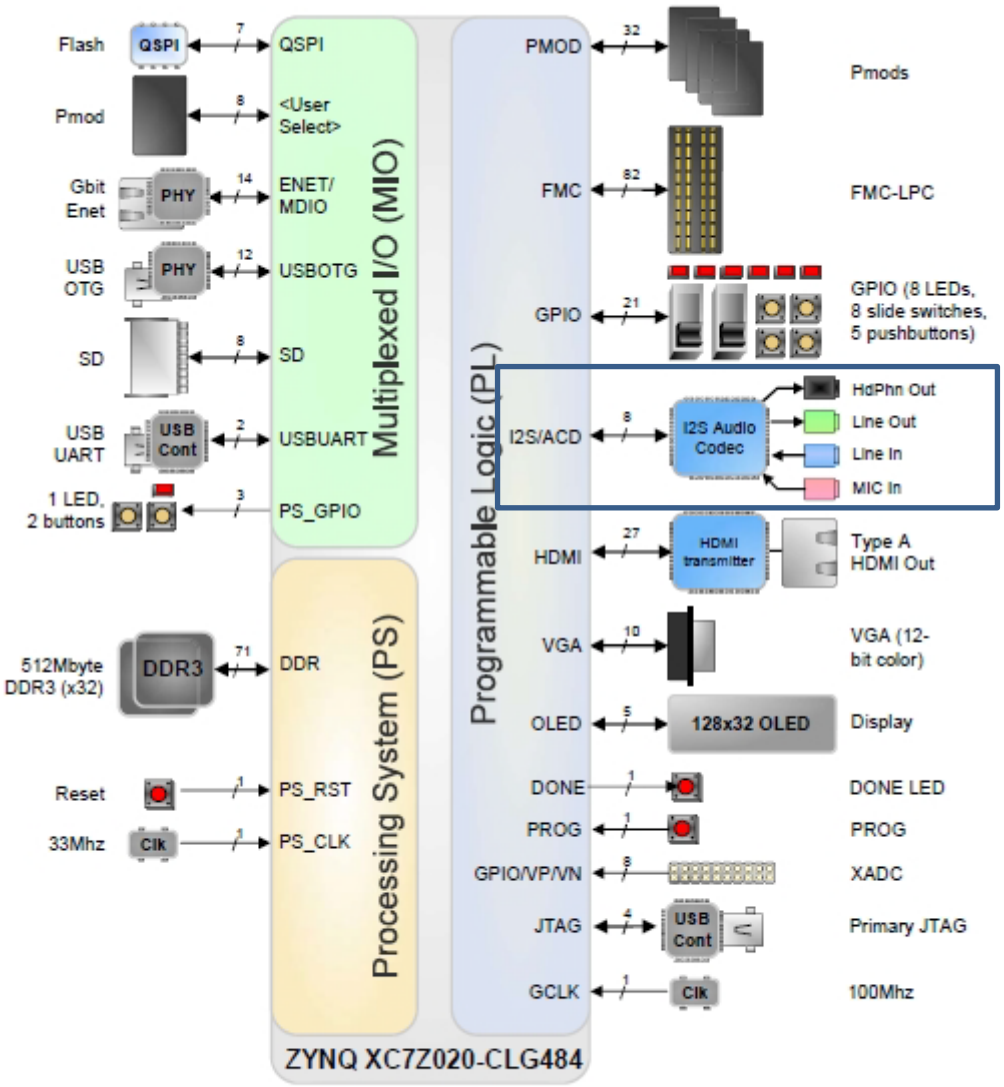


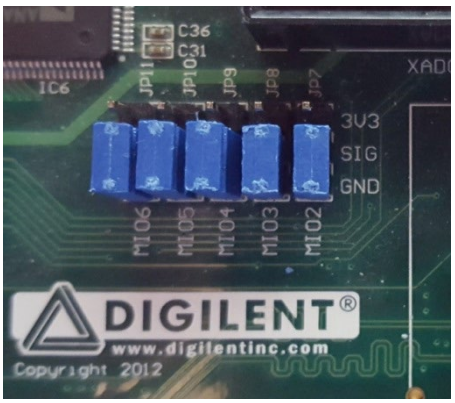
Figure 1 – ZedBoard Block Diagram

Analog input is the Line In and analog output is the Headphone. The on-board Audio Codec is used for AD und DA conversion. In this project the user can select between 3 different filters using the slides switches on ZedBoard.

1. Hardware Setup:

- ZedBoard with connected 7-segment display
- Headphone + audio source (smartphone)
- 1x USB micro cable for JTAG
- Jumper settings for using the JTAG interface

First, make sure that the jumpers **JP7-JP11** are in the JTAG position (shown below) and that the ZedBoard JTAG-Interface is connected to your computer USB port via micro-USB cable.



Connect power supply to ZedBoard, turn power switch **on**! Check if Digilent USB Device is recognized!

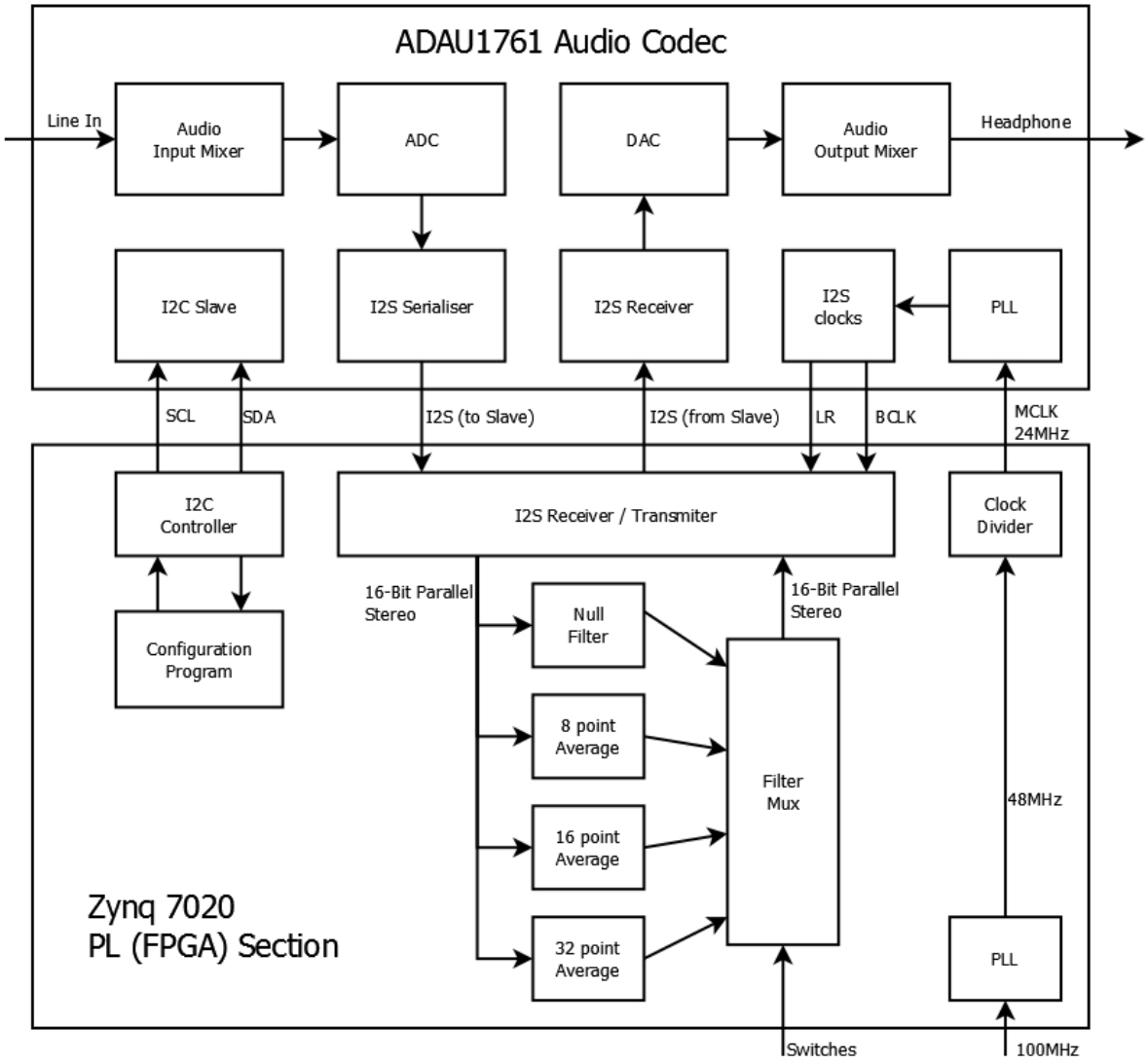
Turn power switch **off**!

2. Software Setup:

- Xilinx Vivado WebPack 2018.2.

3. Project

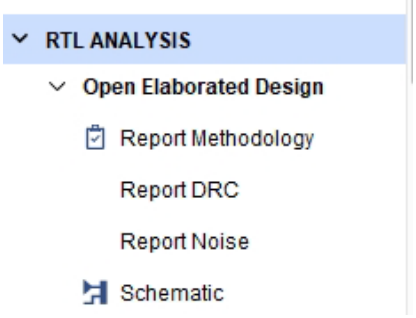
The provided open-source Vivado project file: **audio24bit**
The following block diagram describes the design:



4. Assignment

a) Explain the data format I2S for audio data exchange between Audio Codec and Zynq device! Name data signals and clock signals of this data format by studying ADAU1761 product description!

b) Open project file **audio24bit** in Vivado. Generate the RTL Schematic of the highest instance *adau1761_test.vhd*: In Flow Navigator click on **RTL ANALYSIS/Open Elaborated Design**, then click on Schematic.



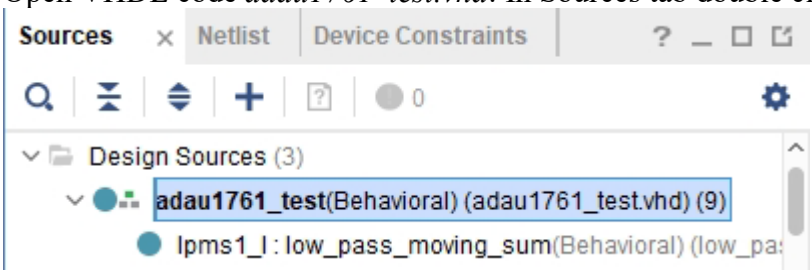
Make a screenshot of the schematic!

Answer the following questions:

- What is the purpose of the multiplexer hphone_l_i and hphone_r_i?
- What is the function of Inst_dsp_block?
- Which port is connected to the serial data output of ADC?
- Which port is connected to the serial data input of DAC?
- Which clock frequency is used for signal MCLK?
- Calculate the pre-configured sample frequency of the ADC and DAC (refer to audio codec ADAU1762 product description, chapter: clocking and sampling rates and to project source file for configuration of audio codec)!
- What is the filter length N of the three low pass filters?
- The low pass filters are running-sum FIR filter. Calculate the cut-off frequency of each filter!

c) Make a print out of the RTL schematic and explain each top level input and output!

d) Extend the functionality of the design: Display selected filter number on the attached 7-segment display. The 7-segment display is getting attached to the Pmod JA1+JB1 of ZedBoard.
Open VHDL code *adau1761_test.vhd*: In Sources tab double click on **adau1761_test**



The part of the VHDL code you need to change is already highlighted.
You also need to add I/O port settings for the communication to the Pmods.
For I/O port settings click on **I/O Ports**:

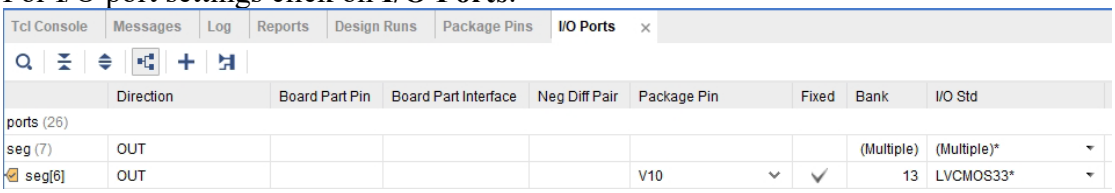
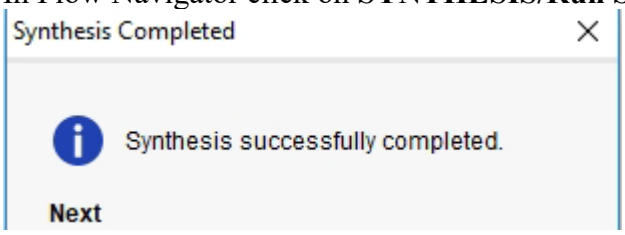


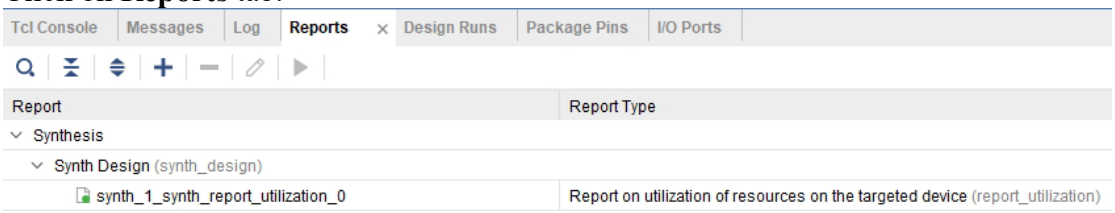
table of I/O opens, edit column **Package Pin**, **I/O Std**. for the missing ports to control 7-segment display (refer to ZedBoard user manual).

e) In Flow Navigator click on **SYNTHESIS/Run Synthesis**. Click Yes to run Synthesis.



Next: click Cancel

f) Click on **Reports** tab.



Open **Report on utilization of resources** of Synth Design.
Do research on Zynq device. What is the meaning of Slice LUTs, Slice Register, Block RAM, and DSP? Copy the table of used resources to your lab report.

g) Download the design to ZedBoard to verify the correct function of 7-segment display! For this click on **Run Implementation**. Take default settings. Then click on **Generate Bitstream**.

h) Now switch on power supply of ZedBoard. In a last step click on **Open Hardware Manager. Open Target** and **Program Device**. Take photo of 7-segment display. Connect smartphone to **Line In** and headphone to **Hdp Out**. Get implementation acknowledged by lab tutor.

Prepare before lab (send pdf-file to lab tutor):

Assignment: a) + b) + c)

Note: Send pdf-file to tutor no later than **May/29, 8pm**!

Lab report: deadline is **June/14, 8pm**!
Submit your lab report as pdf-file (team of 3 students).
Include:

1. a) + b) + c)
2. Extended VHDL model of c), table of I/O ports for 7-segment display
3. f) + h)

Reference: **ADAU1761.pdf –** Audio Codec product description
PmodSSD_manual.pdf – Digilent 7-Segment Modul Board Manual
ZedBoard_HW_UG_v2_2.pdf – ZedBoard User Guide