#### Part1: Study top level RTL design

**Task1: Describe the meaning of all output signals of HDMI\_V1!! Consider that those output signals are inputs to the HDMI transmitter ADV7511. Do research on ADV7511 of ZedBoard. Use a table format with two columns: signal name and description!**

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| **Signal Name** | **Description** |
| Data\_out [15:0] | Video Data Input. Digital input in YCbCr format. Supports typical CMOS logic levels from1.8V up to 3.3V. |
| HDMI\_CLK | Video Clock Input. Supports typical CMOS logic levels from 1.8V up to 3.3V. |
| config\_done | CEC data signal. Supports CMOS logic levels from 1.8V to 5V. |
| de | Data Enable signal input for Digital Video. Supports typical CMOS logic levels from 1.8V up to 3.3V. |
| h\_sync | Horizontal Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V. |
| v\_sync | Vertical Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V. |
| siod\_hdmi | Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8V to 3.3V. |
| sioc\_hdmi | Serial Port Data Clock input. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8V to 3.3V. |
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**Task2: The component IMG\_GENERATOR emulates the camera. Do research on OV7670 camera (data sheet). Describe each signal provided by the camera (assume a resolution setting of 640x480 and an output format of Y/Cb/Cr 4:2:2) and compare with the output ports of IMG\_GENERATOR! Use a table format with two columns: signal name and description!**

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| **Signal Name** | **Description** |
| cam\_data[7:0] | Video Data Output |
| cam\_href | HREF output |
| cam\_pclk | Pixel clock output |
| cam\_siod | SCCB serial interface data I/O. |
| cam\_vsync | Vertical sync output. |