ECN13104: Solid State Devices and Circuits

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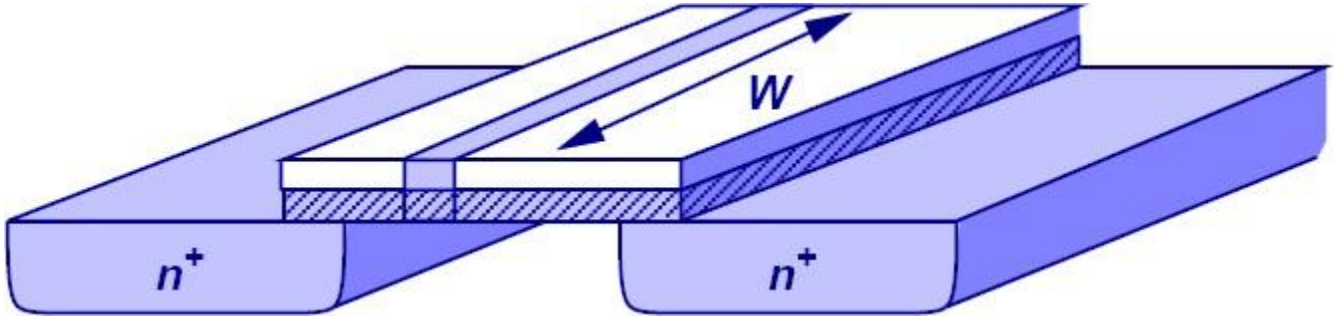
MOSFET Drain Current Equations in different regions of operations

MOSFET in ON State ($V_{GS} > V_{TH}$)



- The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.

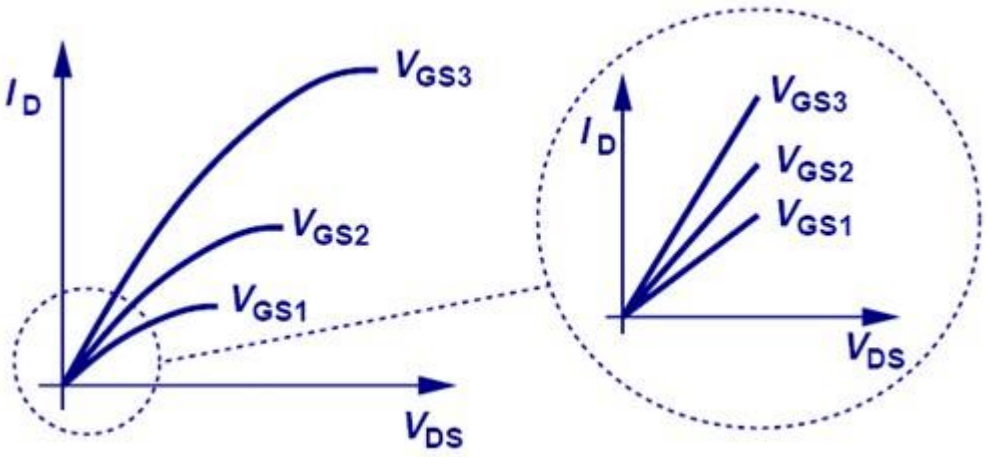
Areal inversion charge density [C/cm^2]: $$Q_{inv} = C_{ox}(V_{GS} - V_{TH})$$

- **Note that the reference voltage is the source voltage.**

In this case, V_{TH} is defined as the value of $\boldsymbol{V_{GS}}$ at which the channel surface is strongly inverted (*i.e.* $n = N_A$ at x=0, for an NMOSFET).

MOSFET as Voltage-Controlled Resistor

- For small V_{DS}, the MOSFET can be viewed as a resistor, with the channel resistance depending on the gate voltage.



$$R_{ON} = \text{resistivit y} \cdot \frac{L}{t_{inv} \cdot W} = \frac{1}{q\mu_n n_{inv}} \cdot \frac{L}{t_{inv} \cdot W}$$

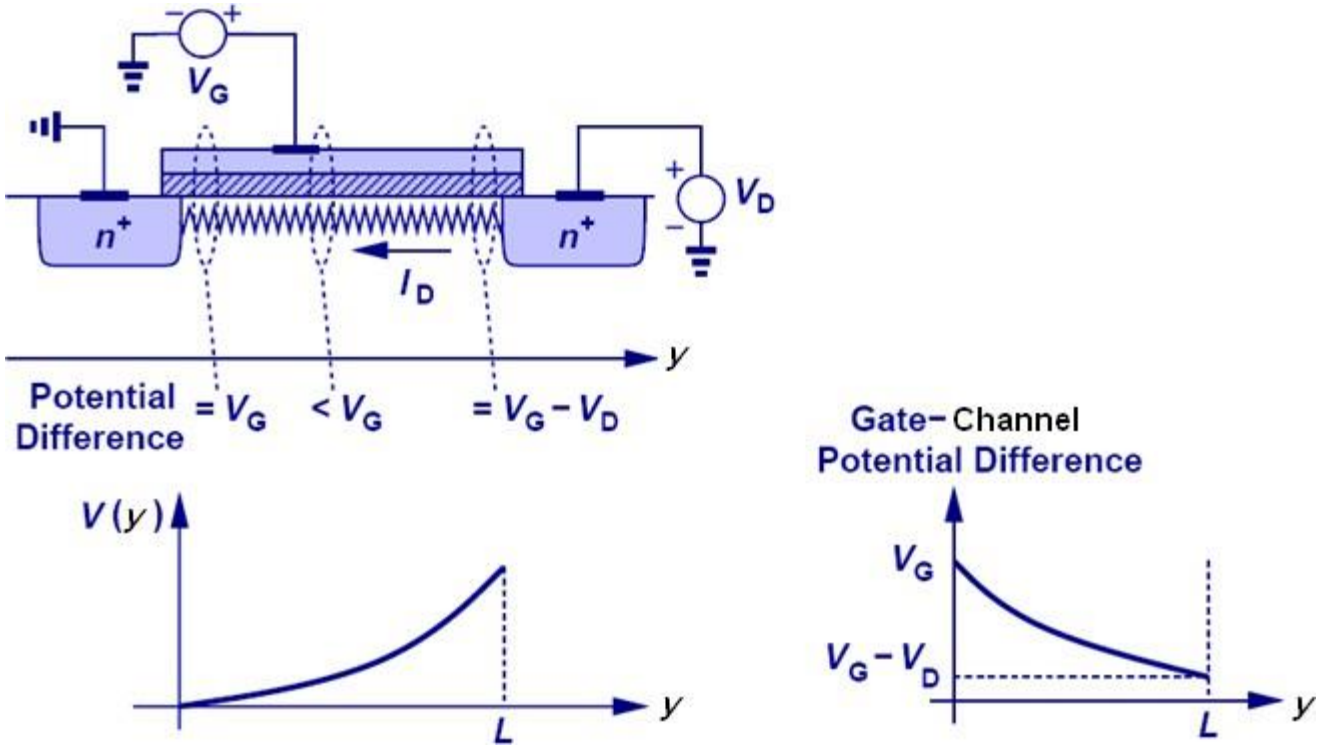
- Note that $qn_{inv} \cdot t_{inv} = Q_{inv} = C_{ox}\left(V_{GS} - V_{TH}\right)$

$$\boxed{R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)}}$$

MOSFET Channel Potential Variation

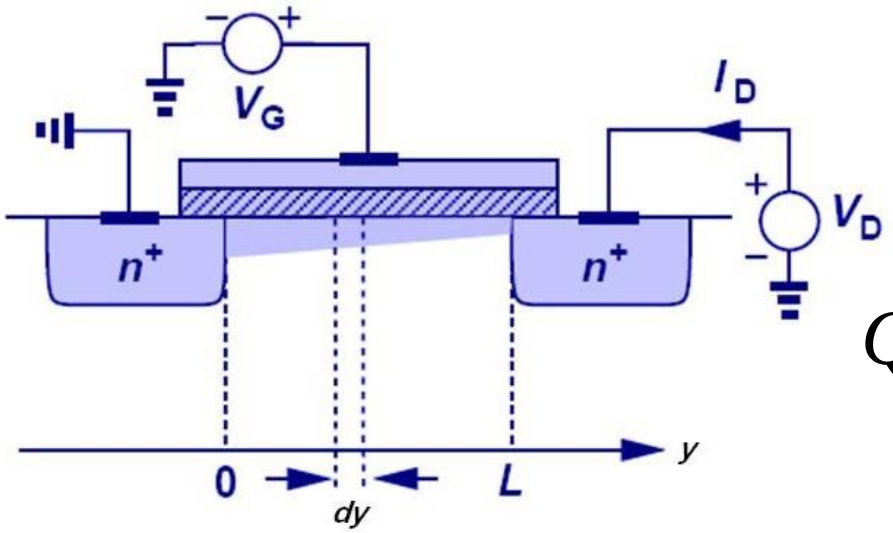
- If the drain is biased at a higher potential than the source, the channel potential increases from the source to the drain.

→The potential difference between the gate and channel decreases from the source to drain.



Charge Density along the Channel

- The channel potential varies with position along the channel:



$$Q_{inv}(y) = C_{ox}\left[V_{GS} - V_{TH} - V_C(y)\right]$$

- The current flowing in the channel is $I_D = WQ_{inv}(y) \cdot v(y)$

current is charge per unit time

- The carrier drift velocity at position *y* is $v(y) = \mu_n E = \mu_n \dfrac{dV_C(y)}{dy}$

where μ_n is the electron field-effect mobility

Drain Current, ID (for VDS<VGS-VTH)

$$I_D = WQ_{inv}(y) \cdot v(y) = WQ_{inv}(y) \cdot \mu_n \frac{dV_C(y)}{dy}$$

current is charge per unit time

Integrating from source to drain:

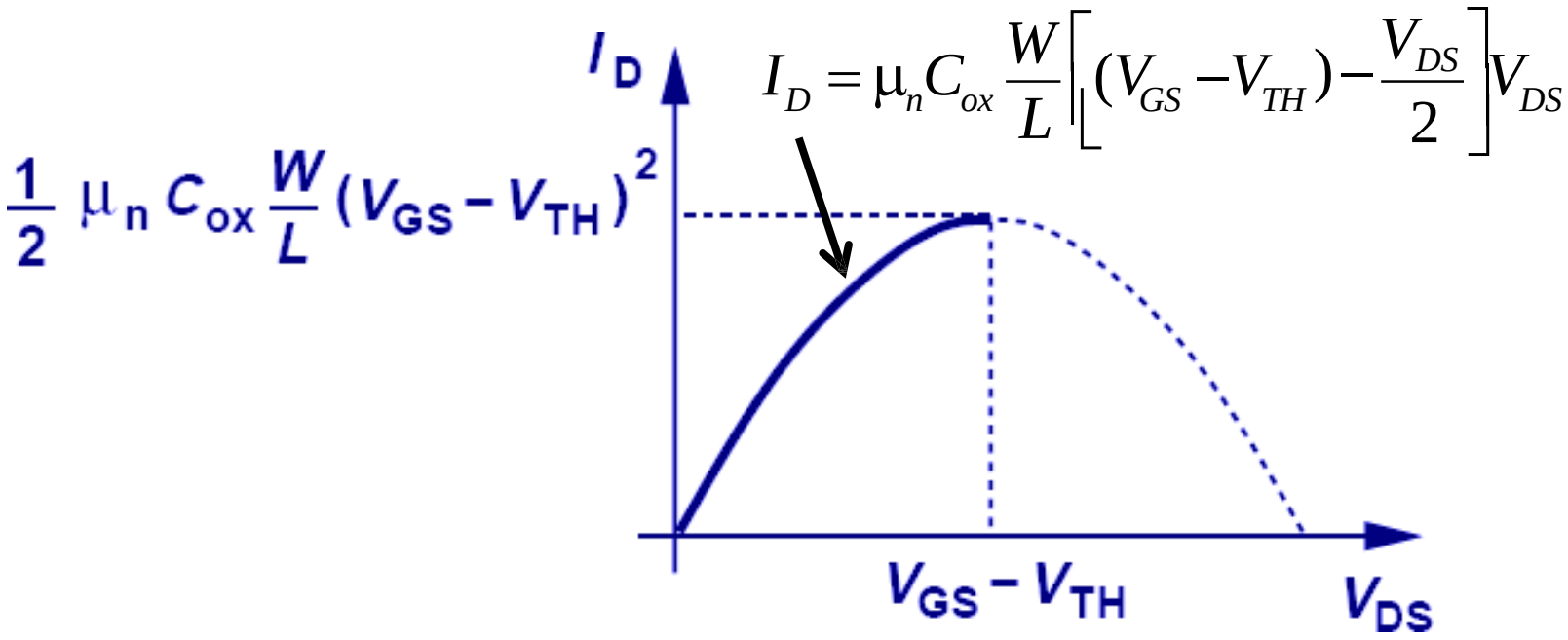
$$\int_0^L I_D dy = \int_{V_S}^{V_D} W\mu_n Q_{inv}(V_C) dV_C$$

$$I_D L = W\mu_n \int_{V_S}^{V_D} C_{ox}\left[V_{GS} - V_{TH} - V_C\right] dV_C = W\mu_n C_{ox}\left\{\left[V_{GS} - V_{TH}\right]V_{DS} - \frac{1}{2}V_{DS}^2\right\}$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}\right]V_{DS}$$

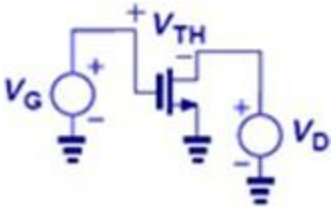
ID-VDS Characteristic

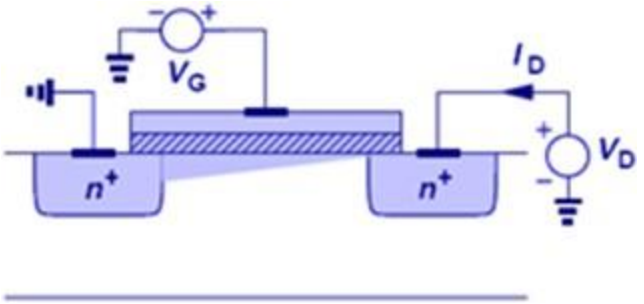
- **For a fixed value of V_{GS},** I_D is a parabolic function of V_{DS}.
- I_D reaches a maximum value at $V_{DS} = V_{GS} - V_{TH}$.



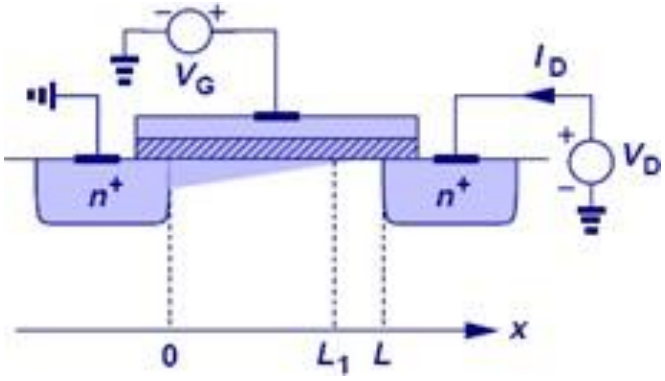
Inversion-Layer Pinch-Off ($V_{DS}>V_{GS}-V_{TH}$)

- When $V_{DS} = V_{GS}-V_{TH}$, $Q_{inv} = 0$ at the drain end of the channel.
  → The channel is "pinched-off".





- As V_{DS} increases above $V_{GS}-V_{TH}$, the pinch-off point (where $Q_{inv} = 0$) moves toward the source.
  - Note that the channel potential V_C is always equal to $V_{GS}-V_{TH}$ at the pinch-off point.
    → **The maximum voltage that can be applied across the inversion-layer channel (from source to drain) is $V_{GS}-V_{TH}$.**
    → **The drain current "saturates" at a maximum value.**

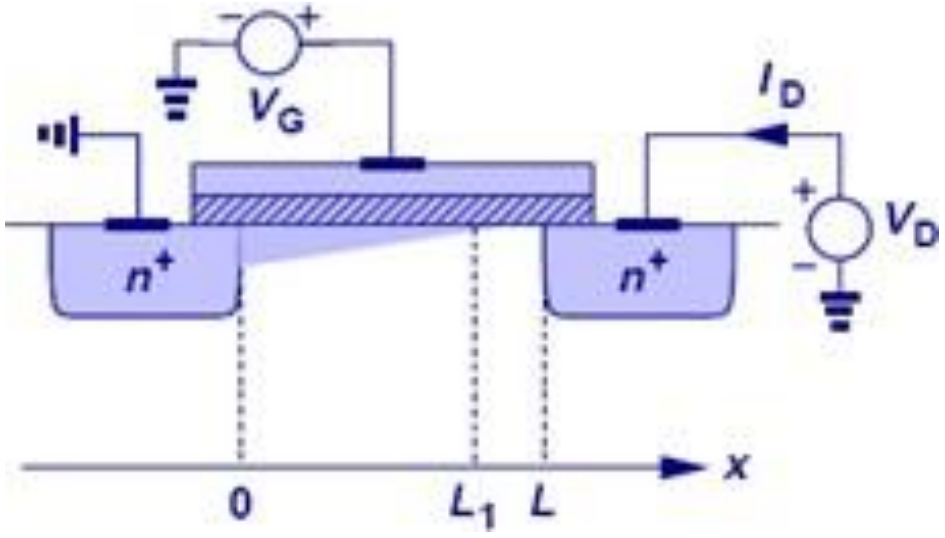


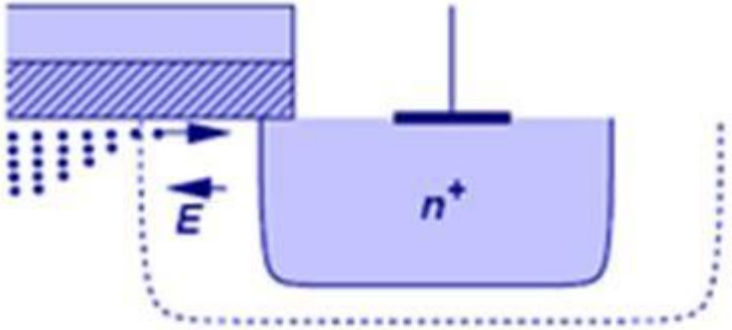
Current Flow in Pinch-Off Region

- Under the influence of the lateral electric field, carriers drift from the source (through the inversion-layer channel) toward the drain.
- A large lateral electric field exists in the pinch-off region:

$$E = \frac{V_{DS} - (V_{GS} - V_{TH})}{L - L_1}$$

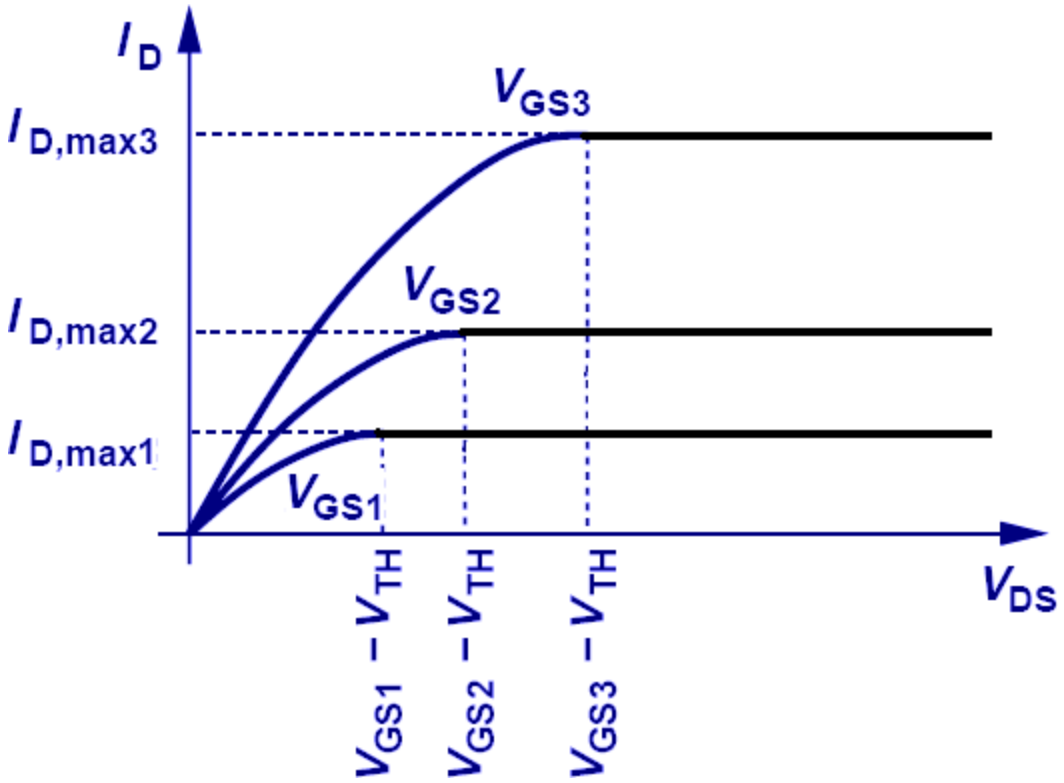
- Once carriers reach the pinch-off point, they are swept into the drain by the electric field.





Drain Current Saturation (Long-Channel MOSFET)

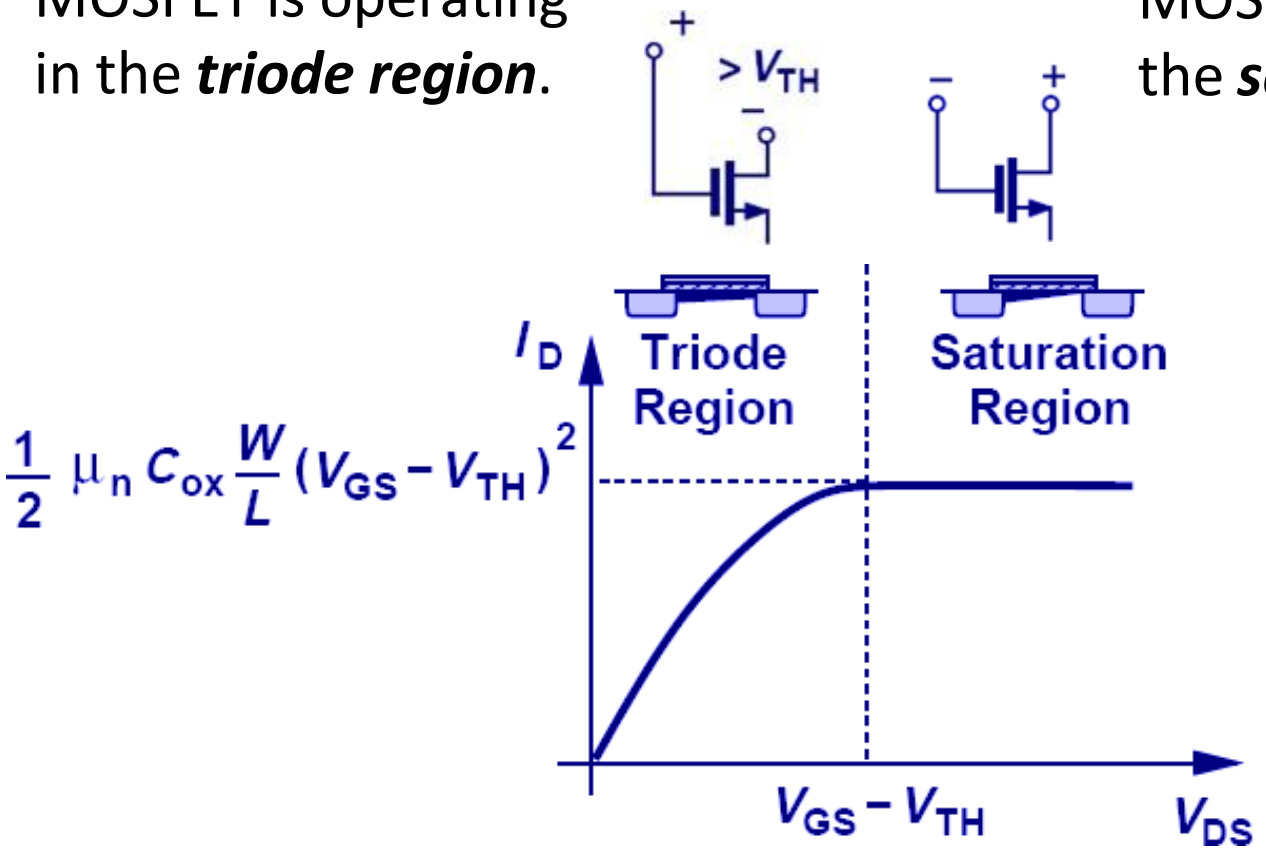
- For $V_{DS} > V_{GS}-V_{TH}$: $I_D = I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$



$$V_{D,sat} = V_{GS} - V_{TH}$$

MOSFET Regions of Operation

- When the potential difference between the gate and drain is greater than V_{TH}, the MOSFET is operating in the ***triode region***.
- When the potential difference between the gate and drain is equal to or less than V_{TH}, the MOSFET is operating in the ***saturation region***.

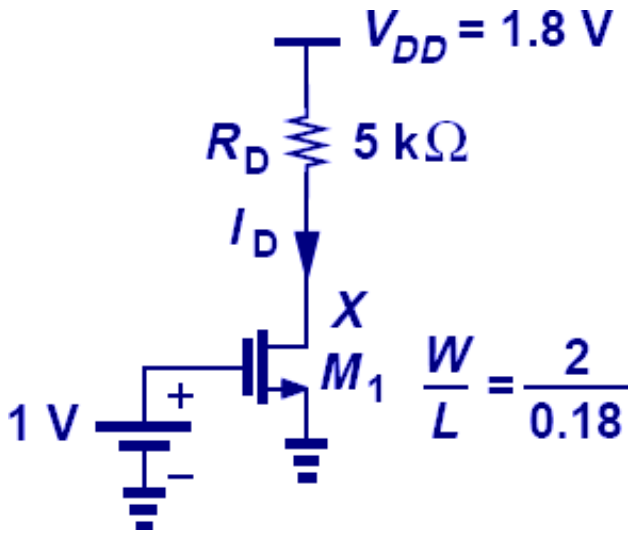


Triode or Saturation?

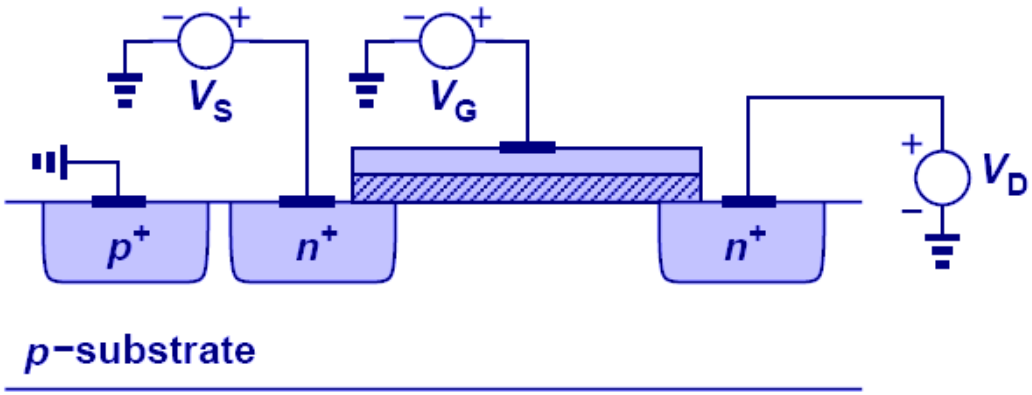
In DC circuit analysis, when the MOSFET region of operation is not known, an intelligent guess should be made; then the resulting answer should be checked against the assumption.

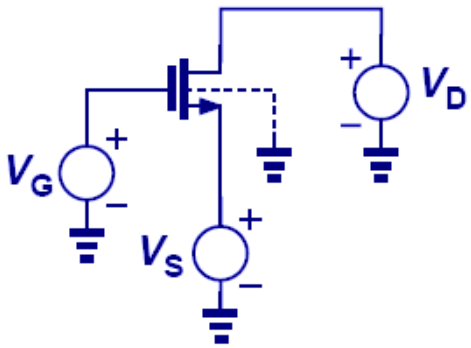
Example: Given $\mu_n C_{ox} = 100\ \mu A/V^2$, $V_{TH} = 0.4V$.

If V_G increases by 10mV, what is the change in V_D?



The Body Effect





- **V_{TH} is increased by reverse-biasing the body-source PN junction:**

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_B + V_{SB})}}{C_{ox}}$$

$$= V_{FB} + 2\phi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_B)}}{C_{ox}} - \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_B)}}{C_{ox}} + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_B + V_{SB})}}{C_{ox}}$$

$$= V_{TH0} + \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}}\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right) = V_{TH0} + \gamma\left(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B}\right)$$

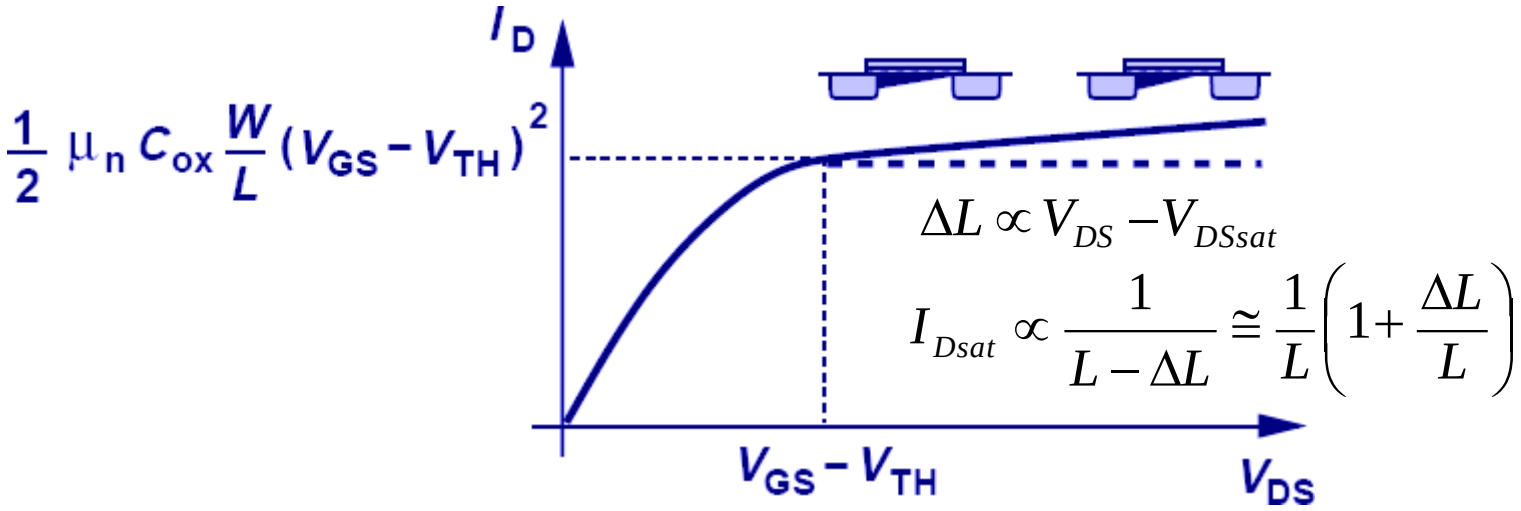
γ is the ***body effect parameter***.

Channel-Length Modulation

- The pinch-off point moves toward the source as V_{DS} increases.

→ The length of the inversion-layer channel becomes shorter with increasing V_{DS}.

→ I_D increases (slightly) with increasing V_{DS} in the saturation region of operation.



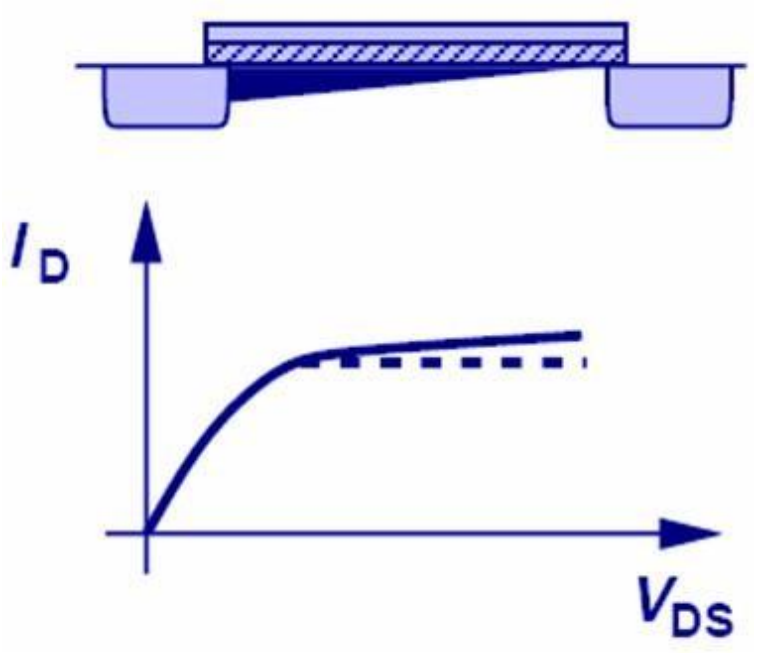
$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\lambda(V_{DS}-V_{D,sat})\right]$$

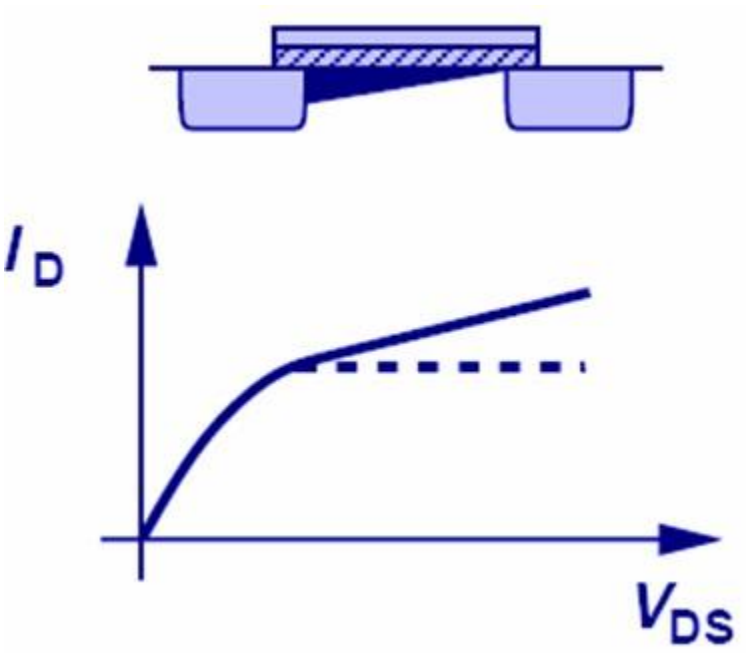
$$I_{D,sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\lambda V_{DS}\right]$$

λ is the ***channel length modulation coefficient***.

λ and L

- The effect of channel-length modulation is less for a long-channel MOSFET than for a short-channel MOSFET.



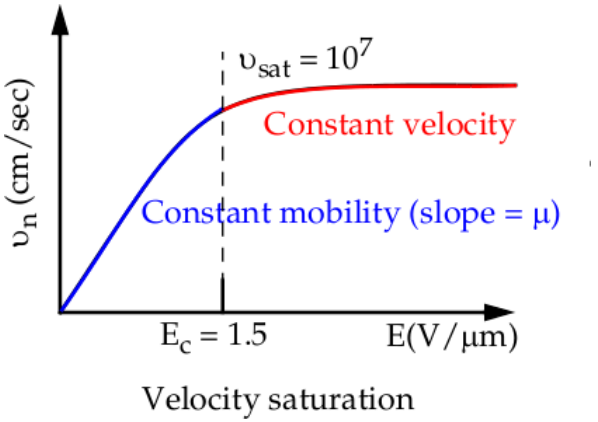


Velocity Saturation

In state-of-the-art MOSFETs, the channel is very short (<0.1μm); hence the lateral electric field is very high and carrier drift velocities can reach their saturation levels.

The electric field magnitude at which the carrier velocity saturates is $\boldsymbol{E_{sat}}$.

$$v_{sat} = \begin{cases} 8\times10^{6}\ \text{cm/s} & \text{for electrons in Si} \\ 6\times10^{6}\ \text{cm/s} & \text{for holes in Si} \end{cases}$$



Velocity saturation

Impact of Velocity Saturation

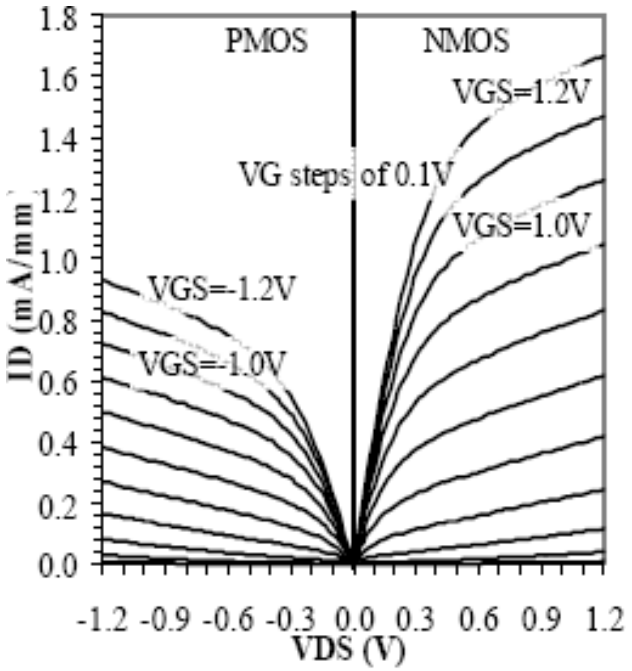
- Recall that $I_D = WQ_{inv}(y)v(y)$

- If $V_{DS} > E_{sat} \times L$, the carrier velocity will saturate and hence the drain current will saturate:

$$I_{D,sat} = WQ_{inv}v_{sat} = WC_{ox}\left(V_{GS} - V_{TH}\right)v_{sat}$$

  - **$I_{D,sat}$ is proportional to $V_{GS} - V_{TH}$ rather than $(V_{GS} - V_{TH})^2$**
  - **$I_{D,sat}$ is not dependent on L**
  - **$I_{D,sat}$ is dependent on W**

Short-Channel MOSFET I_D-V_{DS}



I_{DS}-V_{DS} for 35nm gate lengths

P. Bai et al. (Intel Corp.),
Int'l Electron Devices Meeting, 2004.

- $I_{D,sat}$ is proportional to V_{GS}-V_{TH} rather than $(V_{GS}$-$V_{TH})^2$
- $V_{D,sat}$ is smaller than V_{GS}-V_{TH}
- Channel-length modulation is apparent (?)

Drain Induced Barrier Lowering (DIBL)

- In a **short-channel MOSFET**, the source & drain regions each "support" a significant fraction of the total channel depletion charge $Q_{dep} \times W \times L$

  → **V_{TH} is lower than for a long-channel MOSFET**

- As the drain voltage increases, the reverse bias on the body-drain PN junction increases, and hence the drain depletion region widens.

  → V_{TH} decreases with increasing drain bias.

  (The barrier to carrier diffusion from the source into the channel is reduced.)

  → **I_D increases with increasing drain bias.**

NMOSFET in OFF State

- We had previously assumed that there is no channel current when $V_{GS} < V_{TH}$. This is incorrect!
- As V_{GS} is reduced (toward 0 V) below V_{TH}, the potential barrier to carrier diffusion from the source into the channel is increased. ***I_D* becomes limited by carrier diffusion** into the channel, rather than by carrier drift through the channel.

(This is similar to the case of a PN junction diode!)

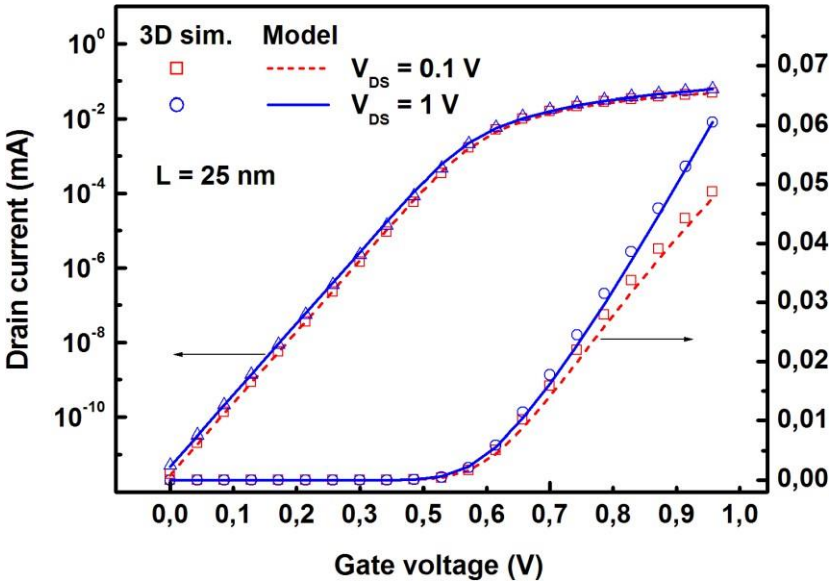
→I_D varies exponentially with the potential barrier height at the source, which varies directly with the channel potential.

Sub-Threshold Leakage Current

- Recall that, in the depletion (sub-threshold) region of operation, the channel potential is capacitively coupled to the gate potential. A change in gate voltage (ΔV_{GS}) results in a change in channel voltage (ΔV_{CS}):

$$\Delta V_{CS} = \Delta V_{GS} \times \left(\frac{C_{ox}}{C_{ox} + C_{dep}} \right) \equiv \Delta V_{GS} / m$$

- Therefore, the sub-threshold current ($I_{D,subth}$) decreases exponentially with linearly decreasing V_{GS}/m

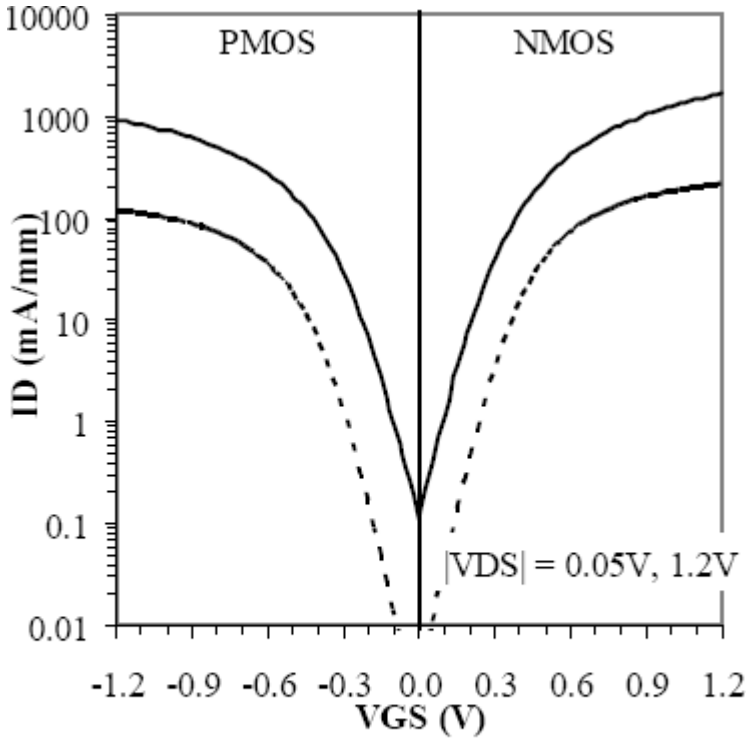


"Sub-threshold swing":

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1}$$

$$S = mV_T \ln(10) > 60\text{mV/dec}$$

Short-Channel MOSFET I_D-V_{GS}



Sub-threshold curves (I_{DS}-V_{GS}) for 35nm gate lengths

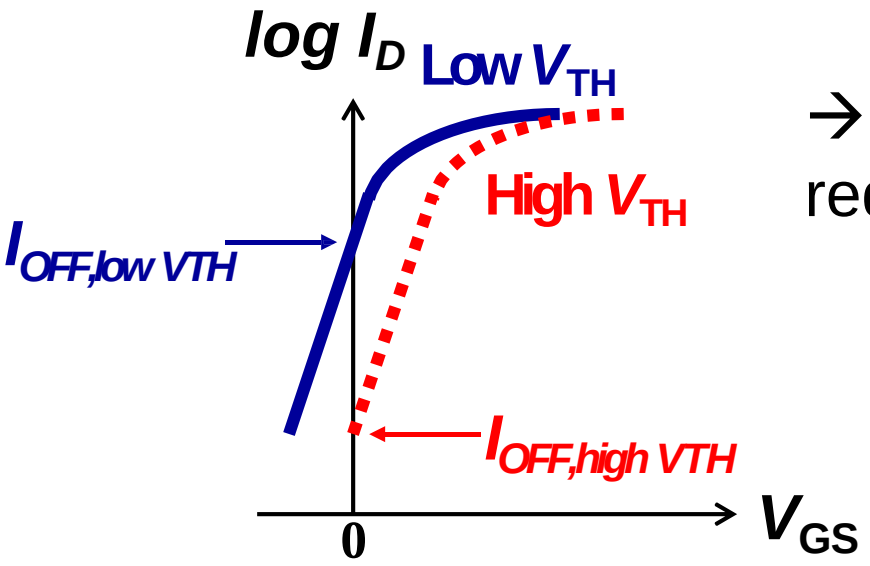
P. Bai et al. (Intel Corp.), *Int'l Electron Devices Meeting*, 2004.

V_{TH} Design Trade-Off

- Low V_{TH} is desirable for high ON-state current:

$$I_{D,sat} \propto (V_{DD} - V_{TH})^{\eta} \qquad 1 < \eta < 2$$

- But high V_{TH} is needed for low OFF-state current:

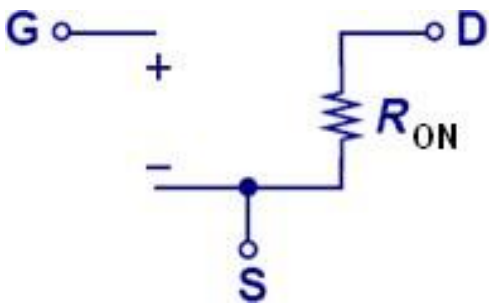


→V_{TH} cannot be reduced aggressively.

MOSFET Large-Signal Models ($V_{GS} > V_{TH}$)

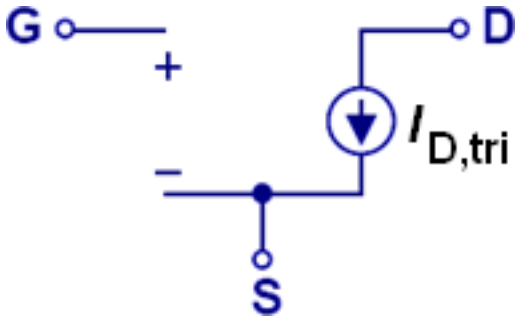
- Depending on the value of V_{DS}, the MOSFET can be represented with different large-signal models.

$V_{DS} << 2(V_{GS}-V_{TH})$



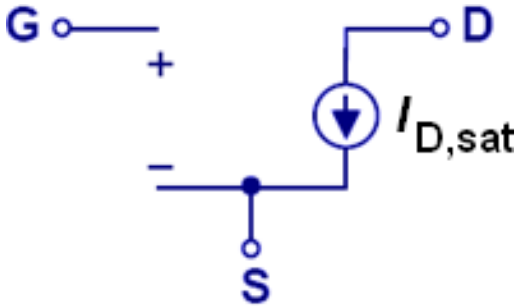
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

$V_{DS} < V_{D,sat}$



$$I_{D,tri} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}\right] V_{DS}$$

$V_{DS} > V_{D,sat}$



$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 [1 + \lambda V_{DS}]$$

or

$$I_{D,sat} = v_{sat} W C_{ox} (V_{GS} - V_{TH}) [1 + \lambda V_{DS}]$$

MOSFET Transconductance, g_m

- Transconductance (g_m) is a measure of how much the drain current changes when the gate voltage changes.

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}$$

- For amplifier applications, the MOSFET is usually operating in the saturation region.
  - **For a long-channel MOSFET:**

$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)\left\{1+\lambda V_{DS}\right\}$$

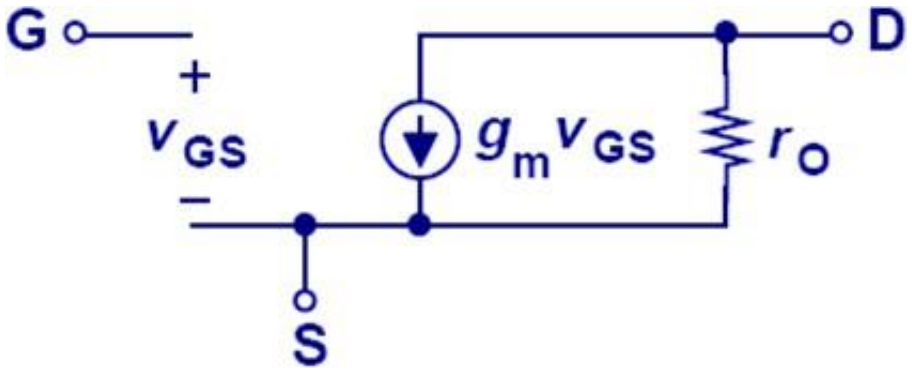
$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L}\left\{1+\lambda V_{DS}\right\} I_D}$$

  - **For a short-channel MOSFET:**

$$g_m = v_{sat} W C_{ox}\left\{1+\lambda V_{DS}\right\}$$

MOSFET Small-Signal Model (Saturation Region of Operation)

- The effect of channel-length modulation or DIBL (which cause I_D to increase linearly with V_{DS}) is modeled by the transistor output resistance, r_o.

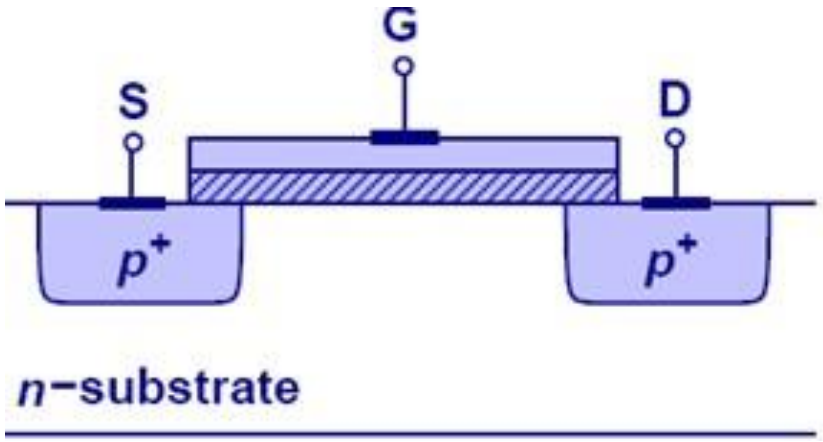


$$r_o \equiv \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\lambda I_D}$$

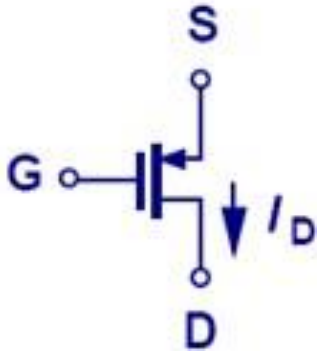
PMOS Transistor

- A p-channel MOSFET behaves similarly to an n-channel MOSFET, except the polarities for I_D and V_{GS} are reversed.

Schematic cross-section

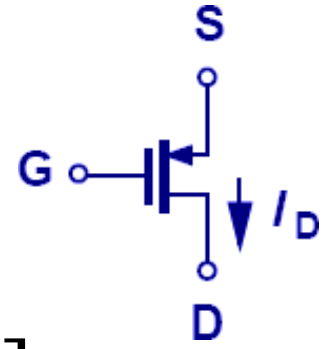


Circuit symbol



- The small-signal model for a PMOSFET is the same as that for an NMOSFET.
  - The values of g_m and r_o will be different for a PMOSFET *vs.* an NMOSFET, since mobility & saturation velocity are different for holes *vs*. electrons.

PMOS I-V Equations



- **For $|V_{DS}| < |V_{D,sat}|$:**

$$I_{D,tri} = \mu_p C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}\right] V_{DS}\left[1 - \lambda V_{DS}\right]$$

- **For $|V_{DS}| > |V_{D,sat}|$:**

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2\left[1 - \lambda V_{DS}\right]$$

for long channel

or

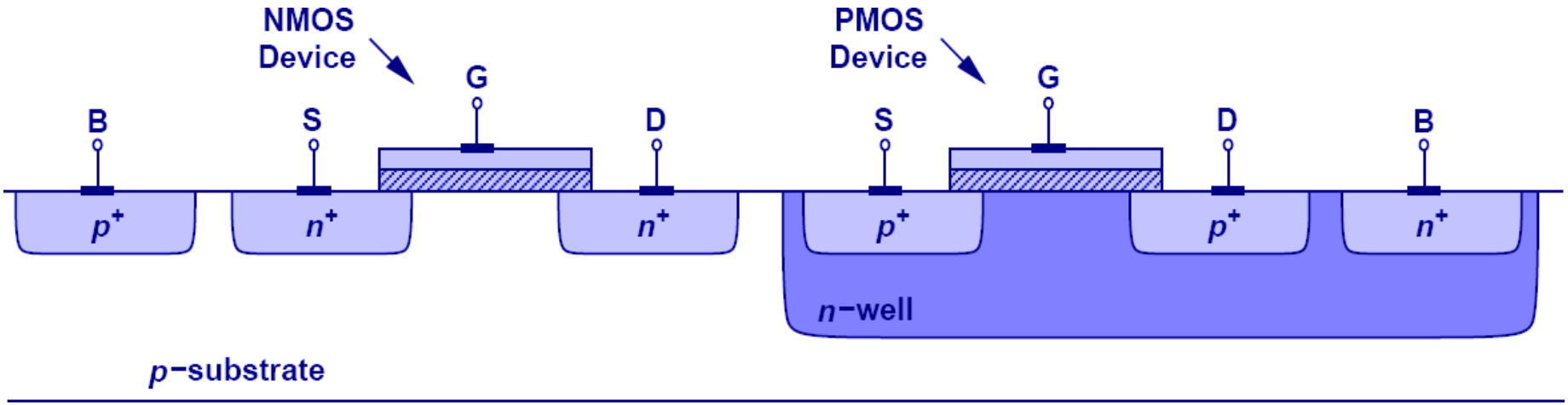
$$I_{D,sat} = -v_{sat} W C_{ox}(V_{GS} - V_{TH})\left[1 - \lambda V_{DS}\right]$$

for short channel

CMOS Technology

- It possible to form deep n-type regions (“well”) within a p-type substrate to allow PMOSFETs and NMOSFETs to be co-fabricated on a single substrate.
- This is referred to as CMOS (“Complementary MOS”) technology.

Schematic cross-section of CMOS devices



Comparison of BJT and MOSFET

- The BJT can achieve much higher g_m than a MOSFET, for a given bias current, due to its exponential *I-V* characteristic.

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
–	Voltage−Dependent Resistor

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