CALIBRE PATTERN MATCHING: PICTURE IT, MATCH IT…DONE!

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WHITEPAPER

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BACKGROUND

Human beings are visual people. From the earliest moments of our life, visual patterns are the dominant way we learn about our world. Throughout our lifespan, we react more strongly to visual stimuli than any other. Even when we speak different languages, we can communicate basic ideas via pictographs with perfect understanding.

IC layouts are visual in nature—any engineer who looks at a layout can instantly recognize transistors and wires and vias—yet we have always defined them with an esoteric textual scripting language. We define layout features by describing in text how wide and tall and long they are. We enhance these definitions by specifying the distances allowed (or not allowed) between features. This text-based, one-dimensional approach worked well enough for a fairly long time, but words have finally begun to fail us.

At today's nanometer nodes, especially at 45 nm and below, we're no longer defining relatively simple, one-dimensional length and width types of measurements. Lithography and manufacturing limitations combined with performance requirements expand the radius of influence within a design layout, so that we now find ourselves trying to describe an increasing set of combined features that are all interdependent, and sometimes multi-dimensional. Some configurations are so complex that they simply cannot be accurately (or practically) described with existing scripting languages.

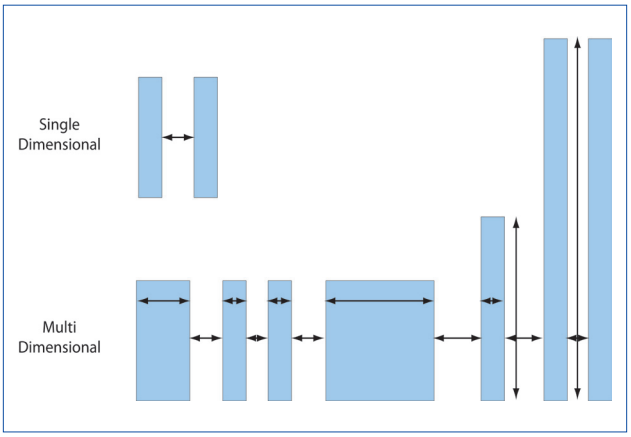

Figure 1: Design constraints and influences have spread far beyond simple length/width measurements at 45 nm and below.

Figure 1 illustrates how the focus of design rules has changed from a simple length-width type of measurement to a complex, interdependent, multi-dimensional set of variables. Not only are there more measurements in the multi-dimensional case, but all the measurements are interdependent, so the allowable range of any particular dimension depends on the values of many surrounding measurements.

Lithography presents a different set of challenges. Even in the late 1990s, feature sizes were smaller than the wavelength of light commonly used in lithography, and the gap has been growing steadily ever since. Achieving resolution at 45 nm and below has become a challenging puzzle, where systematic variability is heavily impacted by both the wafer manufacturing processes and the topological layout features themselves. As geometries shrink relative to the illumination source wavelength (Figure 2), the impact of optical effects on the wafer worsens. The constructive and destructive interference of light as it passes through the photomask and the stepper (scanner) optics can easily induce diffraction effects that distort on-chip features, or even make them disappear, rendering the integrated circuit (IC) unusable.

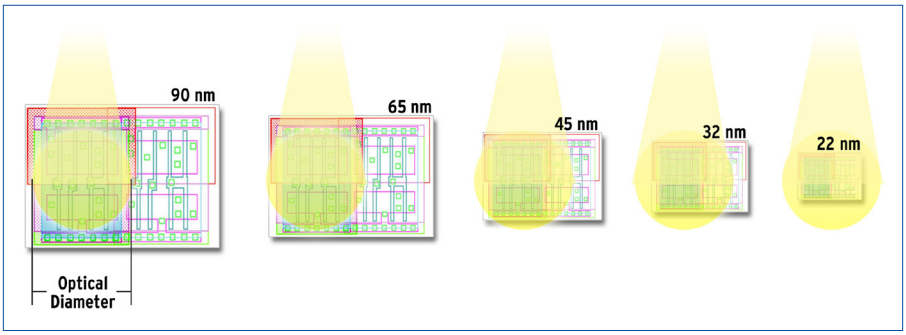

Figure 2: Feature size has been continuously shrinking node over node. At 22 nm, an entire IC standard cell design may be smaller than the optical diameter.

As a consequence, design rules are exploding in number and complexity, making design rule checking (DRC) harder and lengthier. What we have observed across the industry is that the number of physical verification checks is growing at >20% node over node—driven primarily by the growth of manufacturing process complexity. More alarming, the number of individual operations required to execute each check is also growing. The total number of operations within a physical verification deck is growing at >30% node over node. Figure 3 illustrates these growth patterns.

This runaway growth in both size and complexity has impacts throughout the IC manufacturing flow. Design rule manual developers are spending an inordinate amount of time trying to craft specialized rules that overcome manufacturing limitations and accurately satisfy the requirements of the design. Design teams must then spend even more time attempting to interpret these rules in complex rule checks that can contain hundreds of operations. A lot of valuable time and expertise is being used in an attempt to achieve congruence between the original intent of the design and its rendering as a physical implementation that can be profitably manufactured. Design teams are experiencing increased difficulty reaching physical implementation closure, longer physical verification run times, and escalating debugging difficulty and timelines.

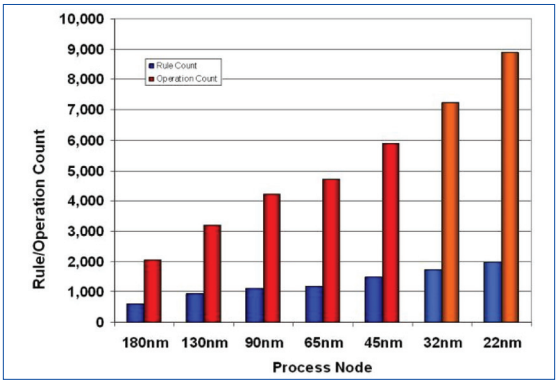

Figure 3: Growth in number and complexity of physical verification rules.

The majority of physical verification requirements are based on one simple concept: certain combinations of geometric shapes cannot be successfully manufactured with a given process. Problematic topological configurations are identified through manufacturing process simulation, failure analysis, or other verification/validation techniques. Simulations and layout analysis techniques, for example, can identify areas of concern within a particular design—features or configurations that will likely fail or negatively impact yield during manufacturing due to lithographic variability, planarity variation, or high sensitivity to random defects. Failure analysis, on the other hand, uses post-manufacture silicon testing and yield analysis techniques to identify and isolate systematic defects that appear repetitively across dies and designs.

Historically, these problematic configurations were textually defined in an engineering specification (design rule). This design rule was passed on to someone whose responsibility was to interpret the rule and write a new design rule check (using the physical verification scripting operations) that accurately represented the original pattern and design rule constraints. This design rule check would then be added to the rule decks used for physical verification. In this flow, then, these configurations are twice abstracted by the time the design rule check is implemented. Additionally, as advanced nodes are being implemented, problematic configurations are now being defined well before silicon production, generally by the teams using lithography and optical process simulations.

What we need is some efficient and accurate way to identify known problematic configurations in the physical design so they can be removed or improved before they cause failures in the manufacturing flow.

CALIBRE PATTERN MATCHING OVERVIEW

Calibre Pattern Matching allows us to return to our most basic instincts, albeit in a highly sophisticated interpretation. Try to describe even the simplest structure, say, a three-dimensional box, using only words. No two people will use the exact same words, and no two people will understand such a description in exactly the same way.

Calibre Pattern Matching allows design, manufacturing, and failure analysis teams to identify, isolate, and define specific geometric configurations (patterns) directly from a design layout. Once recognized and defined, these patterns can be added to a pattern library that can be used by the Calibre Pattern Matching engine to automatically scan designs for matching patterns. With this visual representation capability, Calibre Pattern Matching opens up a whole new way to define, manage, and process design rules, and allows designers and foundry personnel to communicate via a "language" that they both speak and comprehend fluently. The clarity and simplification achieved through Calibre Pattern Matching not only reduces the size and complexity of the rule deck, but also increases the

accuracy and precision of the DRC process.

Patterns can be identified in a variety of ways by a variety of people throughout the design, verification, and test process flows. Failure analysis groups can use pattern matching to capture configurations that repeatedly fail in manufacturing. In addition to failure geometries, however, pattern matching is also useful for any process in the design and implementation flow that attempts to predict and avoid problems. For example, pattern matching can be used for recognizing potential lithographic hotspots. Once a particular pattern has been identified as prone to lithographic distortion and/or failure, pattern matching can be used to improve runtime performance during full-chip applications (e.g., when running verification at the place and route level, pattern matching can "catch" any instantiations of the pattern that may have been introduced). By removing these configurations early in the design and implementation flow, designers can avoid the need to re-implement layouts after lithographic simulation of the full chip.

Likewise, lithography-based patterns can help OPC teams improve their process models and recipes earlier on in the design flow, thus improving the overall cycle time. Design for manufacturing (DFM) analysis can lead to the identification of problem patterns that affect manufacturability and/or performance (e.g., features affecting die planarity during chemical mechanical planarization (CMP)). Once a systematic issue that is related to a particular design feature or configuration is identified and characterized, it can be captured and added to a pattern library available to the end user.

THE CALIBRE PATTERN MATCHING PROCESS

The basic usage model for Calibre Pattern Matching is quite simple:

- Identify a pattern
- Capture the pattern, either by drawing it, "clipping" it from an existing design, or using Calibre Pattern Matching's automated capture techniques
- Add the pattern to a pattern library
- Instruct Calibre Pattern Matching to scan an IC design for any instances of the patterns in a specified pattern library

During the comparison, Calibre Pattern Matching places a pattern identifier (marker) at the site of each match. The resultant matches can then be removed, fixed, or adjusted, depending on the need of the user.

CREATING PATTERNS AND THE PATTERN LIBRARY

To understand each step of the pattern matching process, we'll walk through an example, beginning with the identification of a problem construct (Figure 4).

Problematic topological configurations are identified using the techniques described earlier in this paper. Once a systematic issue is identified and characterized, it can be captured and added to a pattern library for use downstream.

To understand how a pattern is defined and converted to a pattern library entry, we need to start by defining the elements that can be associated with a pattern. Figure 5 illustrates each of these terms.

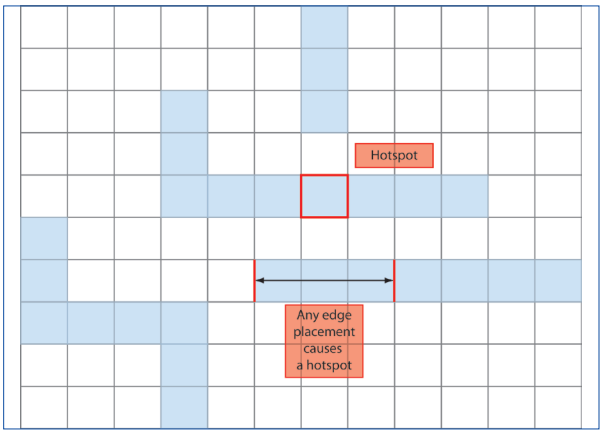

Figure 4: Illustration of a known problem configuration. This pattern causes a pinch (hotspot) due to the surrounding features (line end above, line below). If the line below ends anywhere in the "variable" region (red lines), the pinch problem will persist.

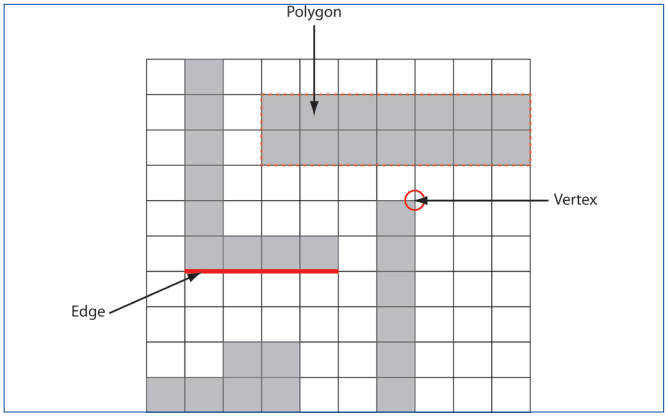

Figure 5: Elements used to define patterns.

- Pattern – consists of one or more pattern layers containing one or more polygons confined within a fixed 2-D space.
- Polygon – a set of edges that define the pattern shapes to search for
- Edge – a set of two vertexes establishing a polygonal side
- Vertex – an x-y point that is associated with any of the pattern layers

A pattern definition contains precise measurements for the combination and location of these elements. Pattern definitions also contain these specifications:

- Pattern Extent – a region bounding the pattern layers that aids in the matching process by separating the pattern geometries from the "outside world."
- Edge Tolerance – a definition of how much the edge placements are allowed to vary during the matching process.
- Pattern Marker – the output from the pattern matching operation. A pattern marker is assigned to each match between the pattern library and the design.

For individual pattern generation, all Calibre layout viewers provide an interactive pattern entry and editing environment. Using one of these viewers in conjunction with the associated Pattern Matching GUI, users can essentially "copy and paste" a problem layout pattern from an existing design into a pattern library. They can then customize the pattern as desired: specifying variation tolerances for edge placement and other pattern dimensions, better defining the extent of the pattern, or maybe enhancing the marker output.

Alternatively, Calibre Pattern Matching offers multiple ways to automatically capture and store patterns within a pattern library:

- Use an existing Calibre nmDRC or Calibre LFD result database to populate a pattern library, where all markers for a given rule check will yield its own pattern.
- Capture from a "group" layer, in which each polygon existing on the "group" layer essentially forms a new pattern within the library.
- Use the batch mode functionality to implement a more systematic, automated pattern capture flow.

The final step in the pattern library development process is to physically generate the entry that describes the pattern, or set of patterns, accurately and precisely. To complete the process, the pattern specification must be "translated" into a format that can be understood and used by the pattern matching engine to perform the library comparison. Obviously, manually translating patterns into a textual format would be difficult, time-consuming, error-prone at best, and virtually impossible for the more complex patterns of advanced nodes. Once the user is satisfied with the pattern specifications, the Calibre Pattern Library Manager is used to deliver the "ready for inclusion" code necessary for the pattern matching process.

USING CALIBRE PATTERN MATCHING

Calibre Pattern Matching makes it much easier to define or capture problem patterns. Likewise, adjusting a picture is much simpler than adjusting a detailed set of design rules. Configurations that are proven to fail often in manufacturing or that produce unacceptable performance variations can then be easily incorporated into a pattern matching library to ensure they are identified (marked) when verifying future designs.

Conversely, Calibre Pattern Matching can be also used to let designers know what patterns **can** be used. For example, a design team might use static RAM cells in digital ICs that violate a design rule for the target process, but which have been carefully designed (and proven) to be manufacturable. Including this pattern in the pattern library assures the design team that they can include this feature in their design without concern for foundry or yield issues.

Foundries and independent device manufacturers know there are certain complex layout topologies that are "sensitive" to a particular process. A foundry usually provides a Process Definition Kit to their fabless and fablite customers, in which they include detection capabilities for problematic geometric scenarios, to help designers verify the manufacturability of their designs prior to submitting them for fabrication. Extending the foundry's PDK flow to include Calibre Pattern Matching is easy, because it is fully integrated with Calibre's Standard Verification Rule Format language. This implementation can also provide the foundry with a reduced cost of ownership from a PDK development and support standpoint.

There are a multitude of design and verification challenges that can benefit from the use of Calibre Pattern Matching, including:

- Extended DRC checks
- DRC edge modification/enhancement/correction
- Pattern-driven automatic waiver flows
- Post-place and route base -to-base cell comparison
- Improved communication with failure analysis team
- Assist feature checks
- Support for metrology systems

One of the primary user groups for pattern matching technology will be those responsible for writing design rules. Calibre Pattern Matching features enable users to more easily define and manage the complex DRC checks that are critical for designs at 32 nm and below. Using pattern matching to identify difficult-to-code geometric patterns enables end users to avoid or modify these detected instances in the early stages of design implementation and verification.

For standard cell and IP designers, pattern matching can be used for base cell-to-base cell comparisons, which allows users to determine what has and has not been altered. Such comparisons can confirm that their IP has not been altered without their knowledge.

During OPC recipe development, users can employ Calibre Pattern Matching to quickly find locations where the retargeting procedure fails. Retargeting is a technique used in lithographic preprocessing to account for etching and lithographic processing effects that occur at the wafer level. Retargeting is becoming a more advanced and complicated process with each new technology node, leading to a growing need for improved verification techniques. Calibre Pattern Matching can now be integrated as a new form of fast verification at the retargeting level.

Calibre Pattern Matching is integrated with Olympus-SoC via Calibre InRoute to provide Calibre signoff quality auto-fixing and verification during design implementation. Calibre Pattern Matching can also be used in conjunction with

Calibre nmDRC and Calibre eqDRC (equation-based DRC).

There are still many other applications that can harness the power of Calibre's new Pattern Matching functionality:

- Full lithography simulation is highly accurate and fast for intellectual property. During full-chip applications, pattern matching can be added as a filtering step (as input into the simulation) to dramatically improve the speed of simulation while maintaining high accuracy.
- Association of electrical behaviors/responses with layout pattern considerations to improve functional robustness by reducing variability
- Inclusion in Design For Manufacturing (DFM) analysis leading to the identification of previously unknown problematic patterns.

BENEFITS

Incorporating Calibre Pattern Matching into your implementation, verification and manufacturing flows provides a host of benefits:

- Reducing design variability by performing physical verification checks previously difficult or impossible to perform.
- Improving overall productivity by making it easier to create and implement complex design constraints and rule checks.
- Improving communication between designers and fab/foundry by using actual patterns (rather than text-based abstractions) to create complex checks.
- Improving consistency and accuracy across flows and between teams by enabling design, manufacturing and test teams to share pattern libraries across multiple tools. Pattern libraries can be created for specific design methodologies, manufacturing processes, or other categorizations, as applicable.
- Reducing time required for rule deck development by simplifying and automating the creation of complex physical verification or design methodology checks that were previously difficult or operationally impossible to create using text-based scripting.
- Simplifying debugging by providing a direct visual comparison between actual geometries, making it much easier to understand and fix violations.
- Faster updates between manufacturing and design, enabling the quick accurate implementation of recently-identified yield-limiting patterns.

SUMMARY

The increasing difficulty reaching physical implementation closure, longer physical verification run times, and escalating debugging difficulty and timelines of advanced node designs are well-known. Calibre Pattern Matching is an extension to SVRF that simplifies complex rule checks required for advanced IC processes. Because it can be used in conjunction with a variety of Calibre products as part of a single SVRF deck—no streaming in and out, no complex flows—it can be easily incorporated into existing flows. Calibre Pattern Matching technology offers the promise of accurate, precise, and consistent definition and identification of complex configurations, reducing the time and cost needed to eliminate problematic geometries in your most advanced designs.

BIOS:

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