SRAM PHYSICAL VERIFICATION WITH CALIBRE PATTERN MATCHING

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Traditional memory verification flows can require significant resources to implement and support, but can miss critical errors known to result in manufacturing defects. A pattern-based solution that avoids costly mask re-spins can be implemented with only minor rule file edits, and is easily updated to add newly developed SRAM IP cells.

INTRODUCTION

Static random-access memory (SRAM) structures are assembled in a physical design using a set of specific intellectual property (IP) blocks that abut or overlap one another in a specific arrangement that matches the circuit specifications. These memory elements have historically been challenging to verify due to differences, smaller feature sizes, and spacing constraints deemed acceptable for memory versus traditional logic or other layout structures. At advanced nodes, SRAM verification is reaching new levels of difficulty.

Historically, the foundries develop and supply customers with SRAM libraries containing IP that is certified for both functionality and a specific process node. Any changes to these foundry-certified SRAM IP by a customer could impact yield. However, prior to 20nm, the manufacturing team could usually make adjustments during the manufacturing process to avoid any yield issues. At 16/14 nm and below, the manufacturing team now has very little margin to adjust the process, due to the physical limitations of the deep ultraviolet (DUV) lithography process used.

However, foundries provide design rules for SRAM IP to check if any violations occur in placement, so why is their use causing so many problems? The challenge in the physical verification of these memory structures is the difficulty of applying a different set of design rules to memory block elements than the rules that apply to the rest of the design, and then catching any unexpected interactions or modified cell elements. Is the structure assembled properly? Are the proper manufacturing rules being applied to the memory and the rest of the design? Did we miss anything?

LIMITATIONS OF TRADITIONAL SOLUTIONS

Various SRAM types are provided by foundries according to their processes, and it is not easy to describe all valid usages clearly and correctly. For example, can a cell be mirrored, or used with other types of SRAM? SRAM cells involve multiple layers, and contain many different geometry shapes with various dimensions, making it nearly impossible to cover all potential placement issues with design rules (Figure 1). In fact, for some floating errors that can only be seen from TOP cell, there is no way to find them with any existing design rule checking (DRC) approaches.

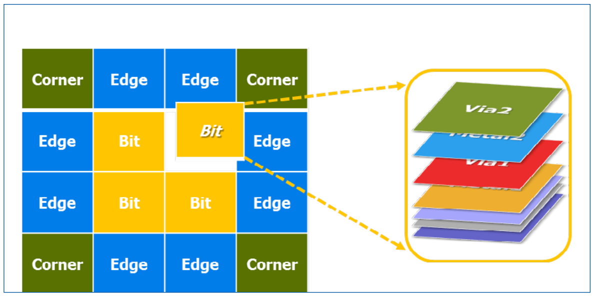


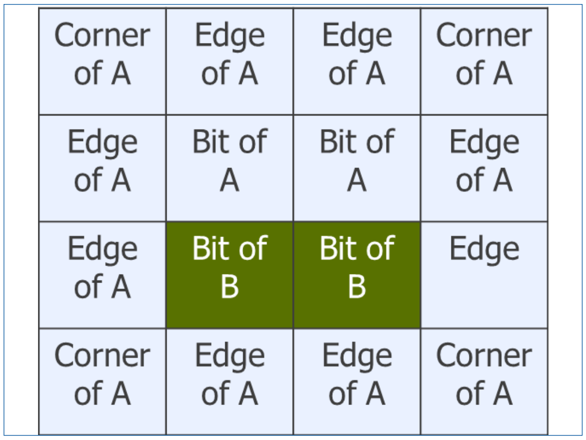
Figure 1: An SRAM block consists of multiple cells, and each cell includes multiple layers.

Over the years, many complex solutions have been developed to address this seemingly simple problem, yet each still has the potential for unintentional user error, or requires design-specific modification to the physical verification rules. One common approach is to manually add a marker layer, which is used in the physical verification rules to identify regions of the design that contain the memory blocks. Rule coders then need to write “almost” duplicate rules in their rule decks, which increases their complexity, as well as the time required to support these decks in the future.

A more significant challenge with this flow is its inability to detect IP manipulation, placement overlaps, floating shapes, or unintended interactions. All of these have the potential to cause manufacturing defects when undetected. Without a complete physical verification solution in place, mistakes in the assembly of the memory blocks or in the application of the appropriate rules to the right design data can result in catastrophic failures after manufacture.

COMMON SRAM ISSUES

Misuse of SRAM types: Because there are many SRAM types for each node, many different cells are involved. Designers may use a corner cell from type A in a SRAM block of type B, and not even realize the misuse occurred (Figure 2).



Corner of A	Edge of A	Edge of A	Corner of A
Edge of A	Bit of A	Bit of A	Edge of A
Edge of A	Bit of B	Bit of B	Edge
Corner of A	Edge of A	Edge of A	Corner of A

Figure 2: Type B cells are inadvertently misused in a type A block.

Misalignment: Placed cells are not completely aligned in a row (Figure 3). The shift may be as small as 1nm, making it very difficult to detect visually.

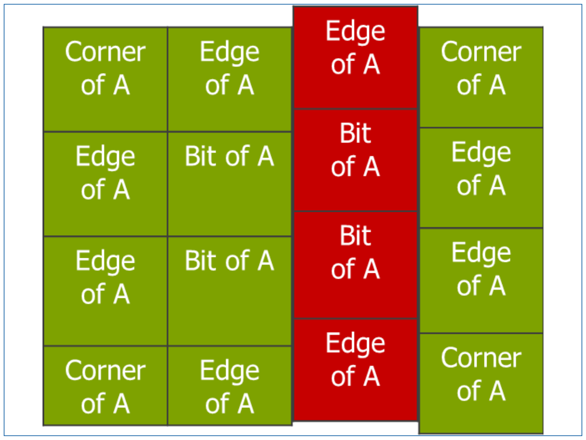


Figure 3: Misalignments can be challenging to detect.

Shape change: A design team may change the polygon shapes from the foundry-supplied SRAM cell (e.g., changing the length of vias from 70nm to 60 nm), as shown in Figure 4.

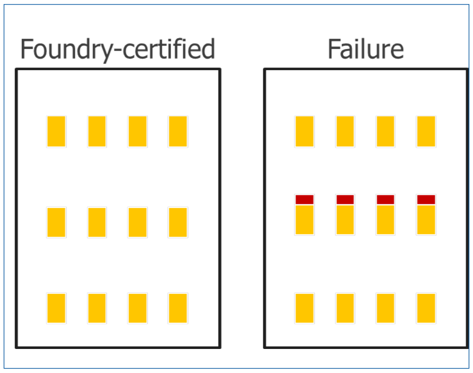


Figure 4: The length of via shapes in the middle row of the cell has been extended.

Extra/Fewer shapes: A design team may add or remove polygons in the compiled SRAM block (Figure 5).

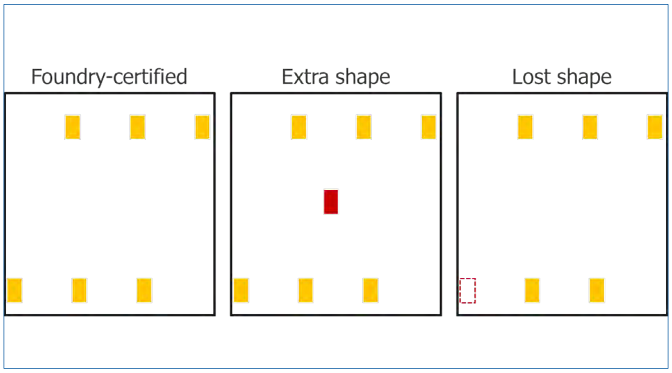


Figure 5: Polygons may be added or removed during placement.

Shape shifting: Some polygons may be shifted within the cell. This shift may be so small that it escapes detection during verification (Figure 6).

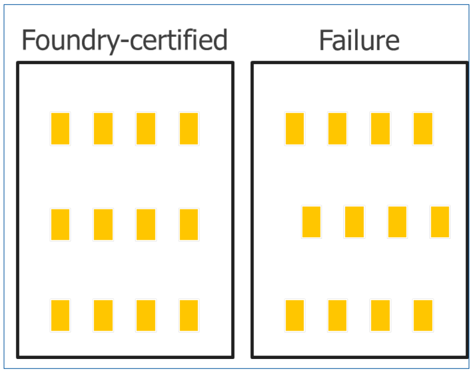


Figure 6: The via shapes in the middle row of the cell have shifted.

CALIBRE PATTERN-BASED SRAM IP VALIDATION

The Calibre Pattern Matching technology replaces existing marker-based solutions and requires only minimal Standard Verification Rule Format (SVRF) coding. Unlike traditional DRC that is dedicated to one-dimensional checks such as width and space, the Calibre Pattern Matching verification methodology can evaluate a pattern consisting of multiple polygon shapes, and check multiple layers. This solution simplifies long-term support requirements, can identify IP manipulation and external interactions, and is easy to update when new IP elements are added.

The Calibre pattern-based verification flow (Figure 7) includes four steps: pattern generation, pattern matching, error identification, and error output.

Implementing a Calibre Pattern Matching SRAM verification solution starts with pattern capture and definition:

1. Capture element and contextual patterns.
2. Verify patterns.
3. Create pattern rule in SVRF.

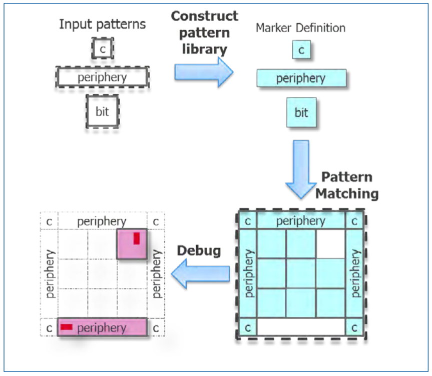


Figure 7: The general Calibre Pattern Matching process.

CAPTURE ELEMENTS AS PATTERNS

Patterns can be captured using the Calibre Pattern Matching functionality provided in the Calibre DESIGNrev™ Pattern Library Manager or through a custom batch script (Figure 8). The quality of the patterns determines how well the pattern matching flow can identify violations. At a high level, the process is to convert all standard cells to patterns. Ideally, all patterns should abut each other (like the placements in the SRAM block) without overlap. These patterns contain multiple layers, and should be generated from the TOP level to enable floating error checks.

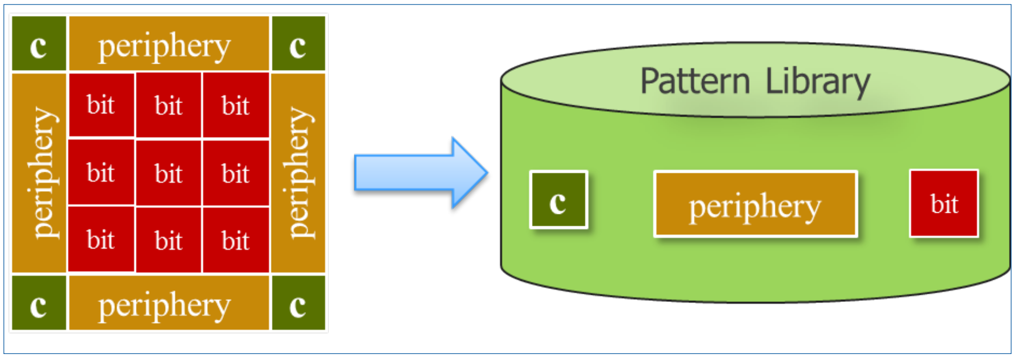


Figure 8: Each part of the SRAM IP is converted to a pattern and stored in the pattern library.

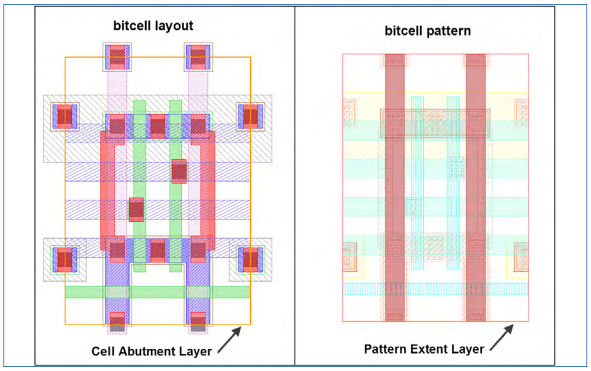


Figure 9: Abutment (marker) layer output as pattern extent.

Using an assembled SRAM block that includes all of the necessary elements, capture individual cells (such as bitcell (core), edge, top, bottom, corner, etc.) using a marker layer, and add them to the pattern library. The example in Figure 9 uses an abutment layer defined in each IP element to capture the pattern and output as the pattern marker. The abutment layer also serves as the marker layer in the design flow. This marker layer is used to identify regions for the assembled memory structure.

VERIFY PATTERN ACCURACY AGAINST LAYOUT

Compile the patterns and test using the Calibre Pattern Matching technology on an assembled SRAM memory structure (Figure 10).

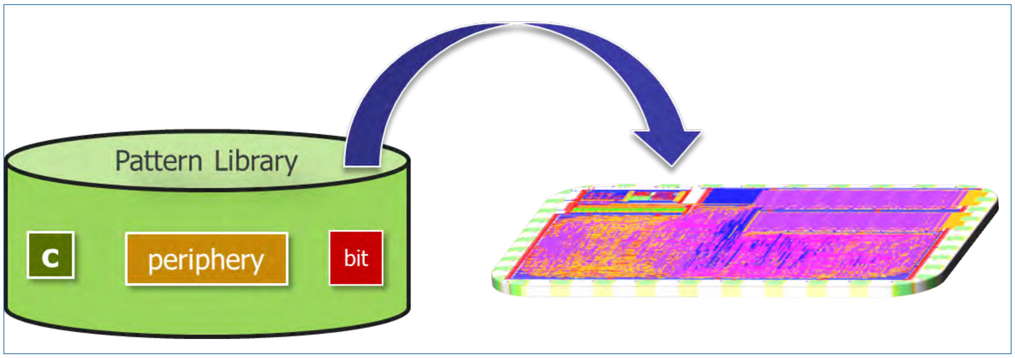


Figure 10: After each part of the SRAM IP is converted to a pattern and stored in the pattern library, it is tested against existing SRAM structures.

Output results to an ASCII database and highlight in the layout window. Regions not covered by a highlight (matched pattern) are likely due to a valid cell pattern that was not captured, or a contextual interaction that may be acceptable. Contextual interactions in the assembly can cause placed cells to fail to match the pattern due to interactions (Figure 11). If these interactions are acceptable and expected, a new pattern capturing the element in context should be added to the library.

Continue adding patterns and checking until every part of the entire memory structure matches a pattern.

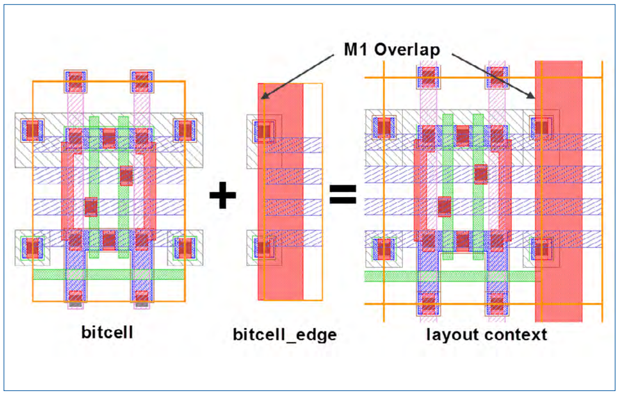


Figure 11: Unexpected contextual interaction.

CREATE PATTERN RULES

Create pattern rules in SVRF.

The typical CMACRO is used in SVRF to output positive matched patterns. However, a new rule must be created to identify IP modification, or interactions that are unacceptable (FIgure 12). Use the SRAM identification layer and the pattern output layer to output any unmatched patterns within the SRAM region. In SVRF, use a Boolean operation to output the marker layer that does NOT include the pattern output layer.

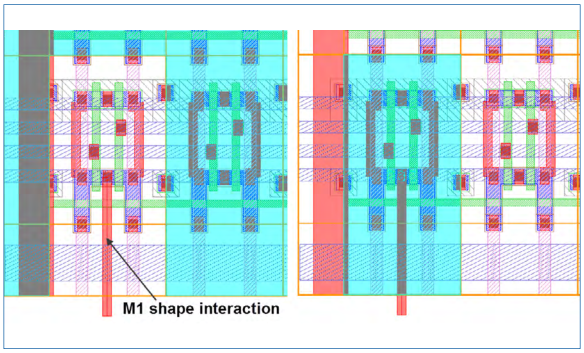


Figure 12: Positive match output (left); negative match output (right) indicates an unmatched region.

Any output error results (Figure 13) are real violations that require further analysis by a layout designer to understand why the pattern failed to match. In some cases, an additional pattern may need to be added to the pattern library.

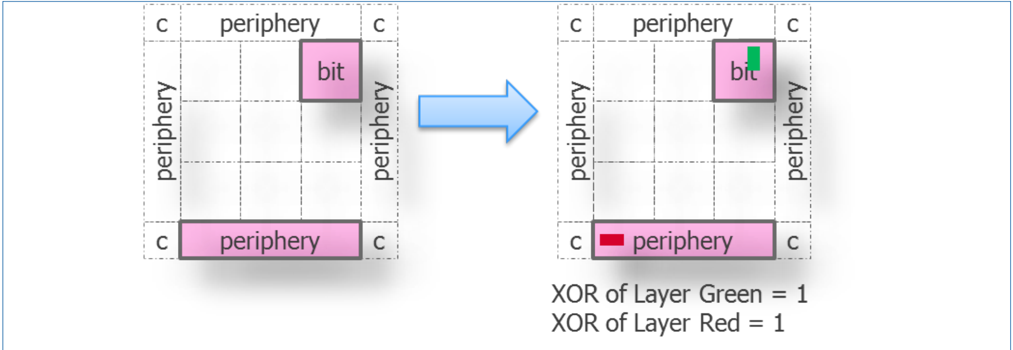


Figure 13: Pattern error output.

APPLY PATTERN MATCHING TO SRAM IP

Once the SRAM pattern library is established and verified, it can be used in your Calibre physical verification flow to automatically validate all SRAM IP placements, providing you with confidence that they have been correctly implemented in your design.

SUMMARY

The Calibre® Pattern Matching solution supplements multi-operational text-based design rule checks with an automated visual geometry capture and compare process. This visual approach is not only powerful in its ability to capture complex pattern relationships simply and quickly, but also easy to incorporate into mixed tool flows—enabling users to easily create new applications solving difficult problems such as SRAM verification. As part of the Calibre nmPlatform, Calibre Pattern Matching is used in conjunction with a wide range of other Calibre tools to solve complex layout issues with ease across design, manufacturing, and wafer test.

To learn more about the Calibre Pattern Matching solution,

go.mentor.com/Pattern_Matching

or

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