CS-403 Assignment

Q.1) Write a short note on Page Map Table. Explain Belady's Anamoly with an example.

⇒

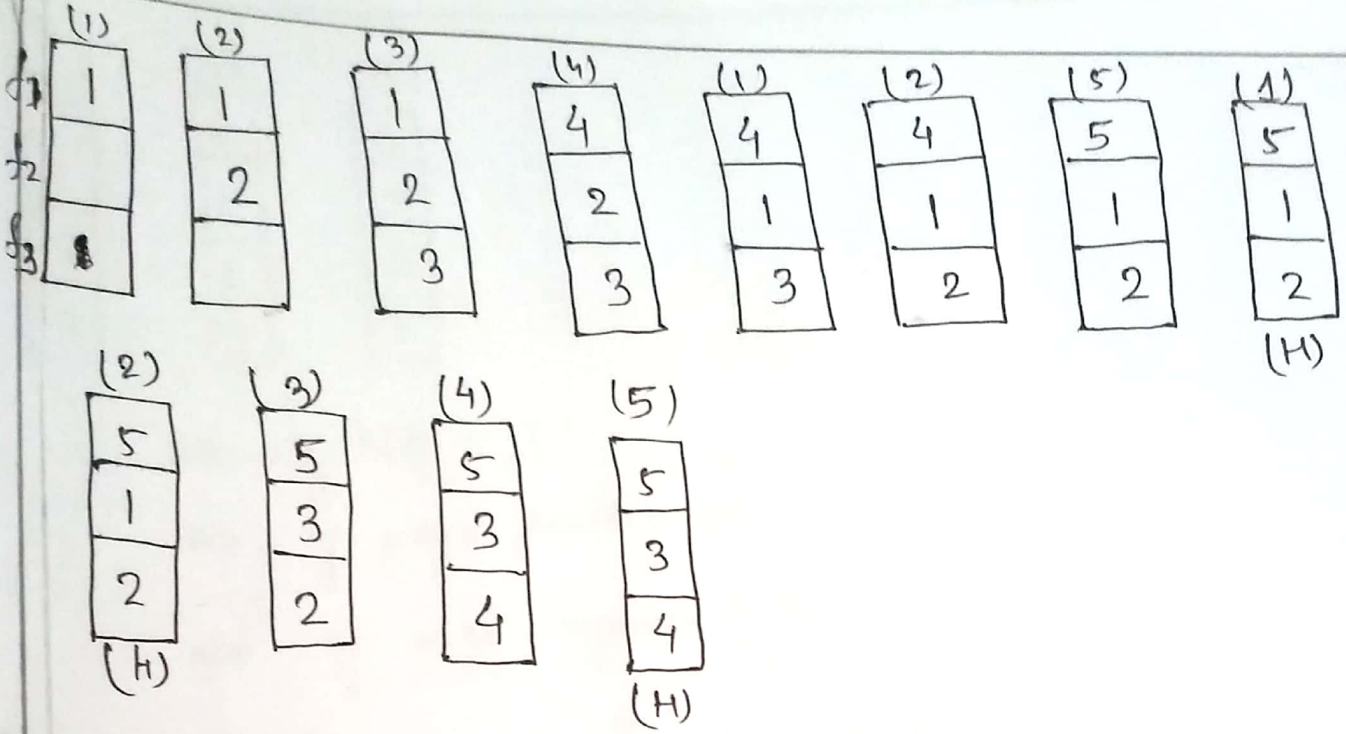
Paging is non-contiguous memory allocation method. In other words, the program is divided into small blocks elee where in main memory. In paging, the virtual address space is divided into equal size blocks called pages and the physical memory is divided into size blocks called Frames. The size of a page and and size of a frame ~~for~~ are equal.

The operating system maintains a data structure called page Table, which is used to map logical address to physical address. The page table consists of two columns for → (1) page number
(2) Frame number

Belady's Anamdy takes place only in FIFO replacement of cache. This Anamoly states that, if there is a certain string to illustrate FIFO page, replacement algorithm with no. of pages and frames, the no. of hit will not increase even when frames are increased,
This anamoly takes place only in certain reference string.

Ex- For illustrating Belady's Anamoly, we shall use the Reference string: 1 2 3 4 1 2 5 1 2 3 4

No. of frames = 3



No. of hits = 3

No. of page fault = 9

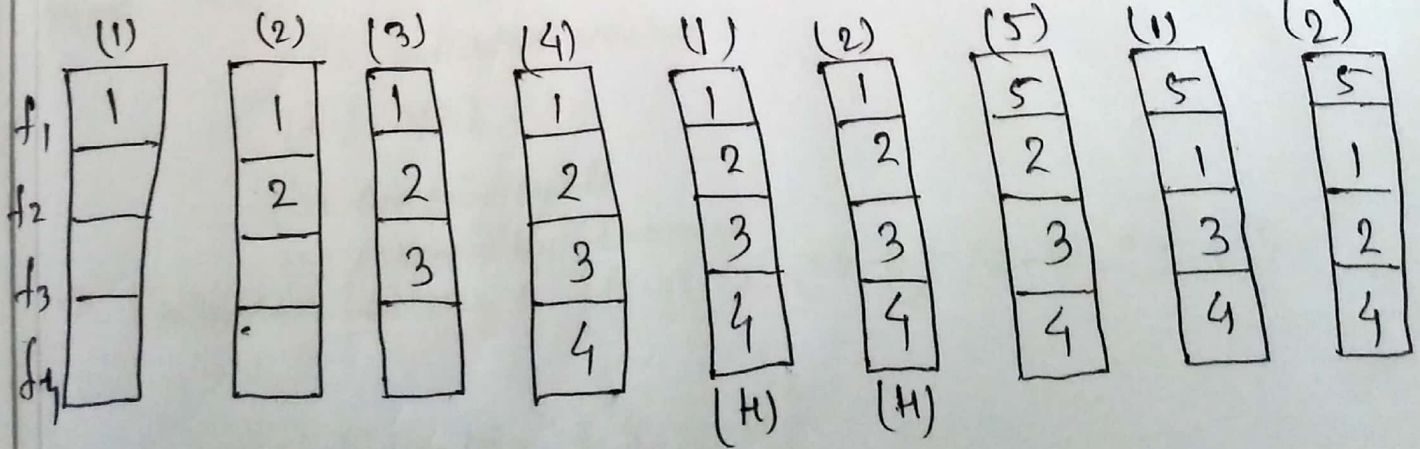
Total no. of page reference = 12

Page fault rate $= \frac{9}{12} = \frac{3}{4} = 0.75$

for pgframe = 3, Hit ratio $= \frac{3}{12} = \frac{1}{4} = 0.25$

Let the frame be increased by 1.

No. of pg. frames = 4



(3)

5
1
2
3

(4)

4
1
2
3

(5)

4
5
2
3

No. of hits = 2

No. of page fault = 10

No. of page reference = 12

for pg frame=4, Hit ratio $= \frac{2}{12} = \frac{1}{6} = 0.1667$

So here in this example, the no. of hits decreases with increase in page frame number, this is Belady's Anamoly

Q.2) Consider the following reservation table:

Stages \ Clock cycle	T_1	T_2	T_3	T_4	T_5	T_6	T_7
S_1	X		X				X
S_2				X		X	
S_3			X		X		

Forbidden

Find the (i) latency

(ii) collision vector

(iii) MAL

(iv) Greedy cycle

(v) permissible Latency

→ Forbidden Latency = {(3-1), (7-3), (7-1), (6-4), (5-3)}

∴ Forbidden Latency = {2, 4, 6}

Permissible latency = {1, 3, 5, 7}

Collision vector = $C_6\ C_5\ C_4\ C_3\ C_2\ C_1$

1 0 1 0 1 0

∴ ~~Initial~~ Collision vector = 101010

State Transition diagram =

Removing this zero

CV → 1 0 1 0 1 0

OR

RS1 → 0 1 0 1 0 1

V_1: 1 1 1 1 1 1

CV → 1 0 1 0 1 0

OR

RS3 → 0 0 0 1 0 1

V_2: 1 0 1 1 1 1

CV → 1 0 1 0 1 0

OR

RS5 → 0 0 0 0 0 1

V_3: 1 0 1 0 1 1

For V_2:

CV → 101010

RS5 → 000001

101011

For V_3:

CV → 101010

RS3 → 000101

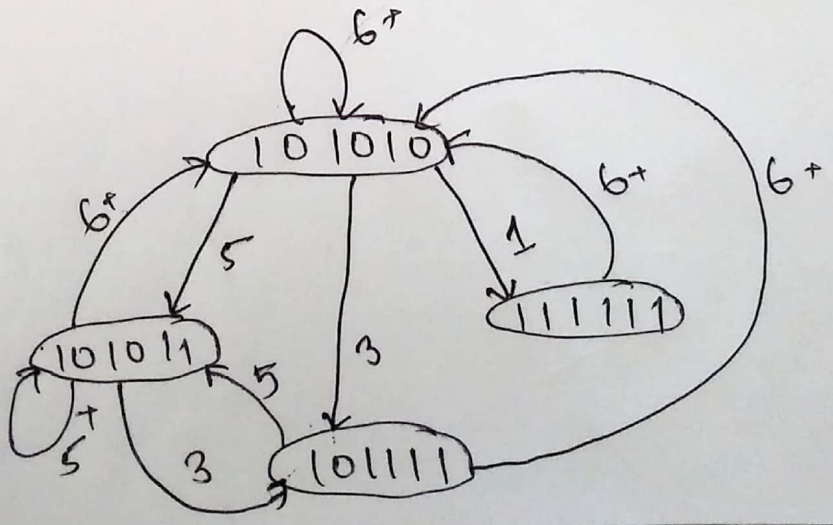
101111

CV → 101010

RS5 → 000001

101011

(Now we will stop as the repetition has started)



Latency cycle	Avg. Latency
{6}	6
{5,6}	5.5
{1,6}	3.5
{3,5}	4
{5}	5
{3,5,5}	6.5
{3,6}	4.5
{5,5,6}	8
{3,5,6}	7
{3,5,5,6}	9.5

∴ Minimum Avg. Latency (MAL = 3.5

Greedy cycle = {1,6}

Q.3) What is Hazard in pipeline? Explain the arithmetic and instruction pipeline. Explain the flynn's classification.

→ Pipeline Hazards are situations the prevent the next instruction in the instruction stream from executing during its designated clock cycle.

* Pipeline can be classified into three types -

(i) Arithmetic Pipeline
(ii) Instruction Pipeline
(iii) Processor Pipeline

Arithmetic Pipeline

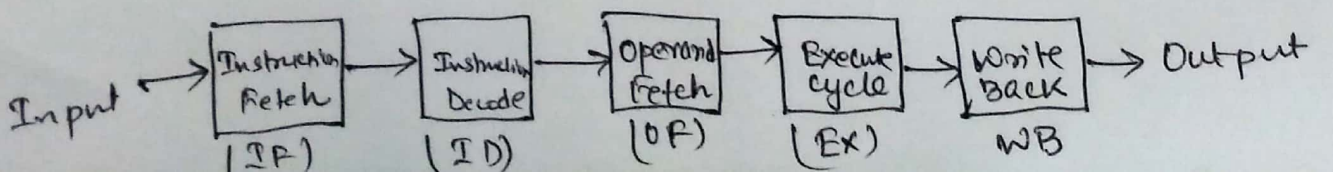
This pipeline divides an arithmetic operation such as a multiply, into multiple arithmetic steps each of which is executed one by one in different arithmetic stages in the ALU.

Examples- 4-stage Pipeline used in Star-100

Instruction Pipeline

The ~~instruction~~ execution of a stream of instructions can be pipelined by overlapping the execution of the current instructions with the fetch, decode and operand fetch of subsequent instructions. All high performance computers are now equipped with this pipeline.

A typical instruction pipeline is divided into five stages as shown below :-



Flynn's classification

Flynn used the concept of data stream and instruction where a data stream is defined as a sequence of data including input, temporary result, particle data. An instruction stream is a sequence of instruction executed by the machine.

Flynn's classification is divided into 4 types:

(i) SISD → Single instruction single Data

(ii) SIMD → Single instruction multiple data

(iii) MIMD → multiple instruction multiple data

(iv) MISD → multiple instruction single data

(5) Find RAW, WAR, WAW for following instructions

Sol:

I1: ADD R5, R0, R1
I2: MUL R6, R2, R5
I3: SUB R5, R3, R6

ADD

⇒ R5 ← R0+R1
R6 ← R2*R5
R5 ← R3−R6

RAW
I1 → I2
I2 → I3

WAR
I2 → I3

WAW
I1 → I3

(4) State the importance of Amdhal's law. If a CPU is improved by 20% and 30% jobs are CPU bound, then calculate the total improvement of the system.

→ It is used to find the maximum of overall improvement possible by improving particular part of the system.

$$\text{Speedup}(N) = \frac{1}{(1-p) + p/n}$$

where (p) → parallel portion
n → factor
1−p → sequential portion.

$$N = \frac{1}{1 - 0.3 + \frac{0.30}{1.10}} = \frac{1}{0.7 + \frac{3}{11}} = 1.028$$

$$\text{improvement} = (1.028 - 1) \times 100\ \%$$

$$= 2.8\ \%.$$