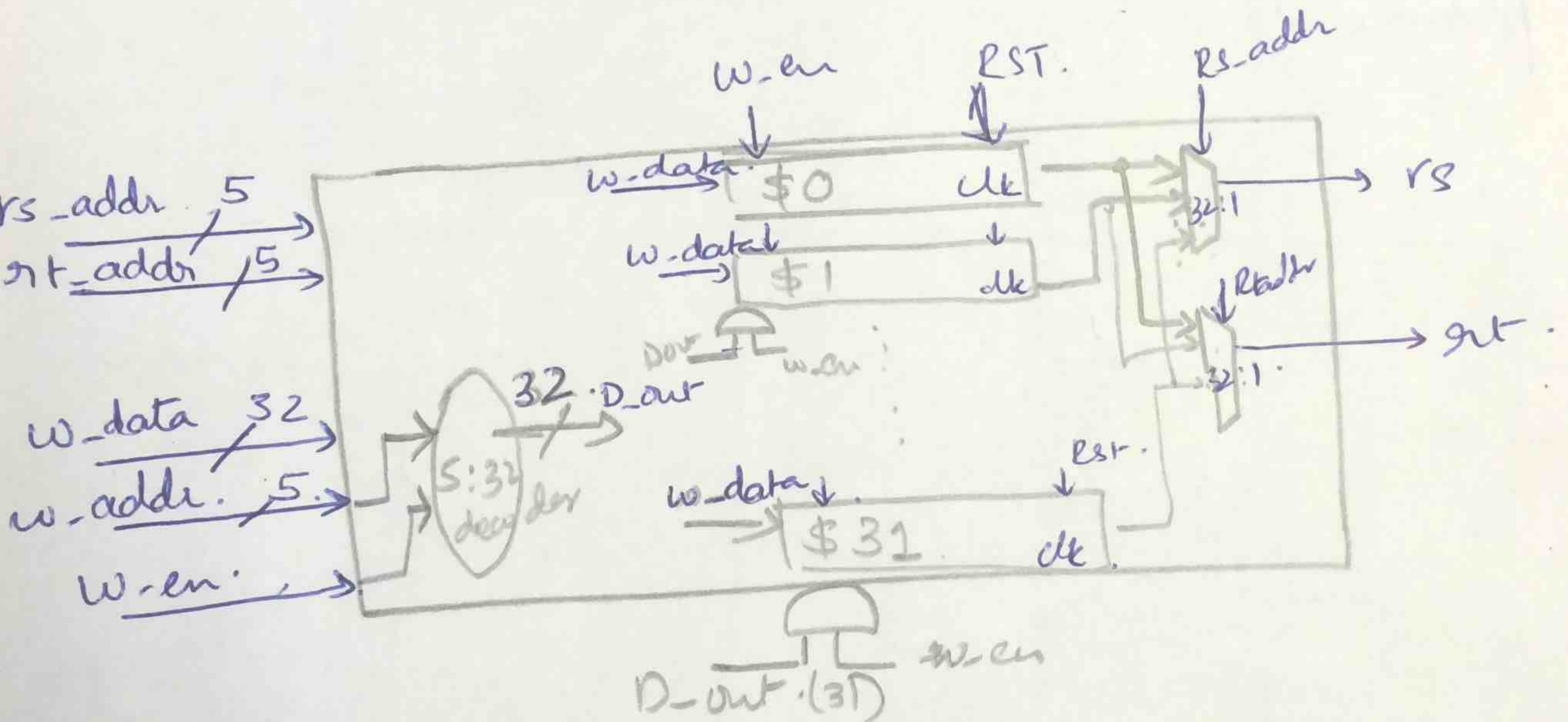


Souparni Agnihotri.

Group - J3 - Souparni Agnihotri
Fahmida Joyti
Christopher Kelly.

I am at a level of 7 comfort with VHDL

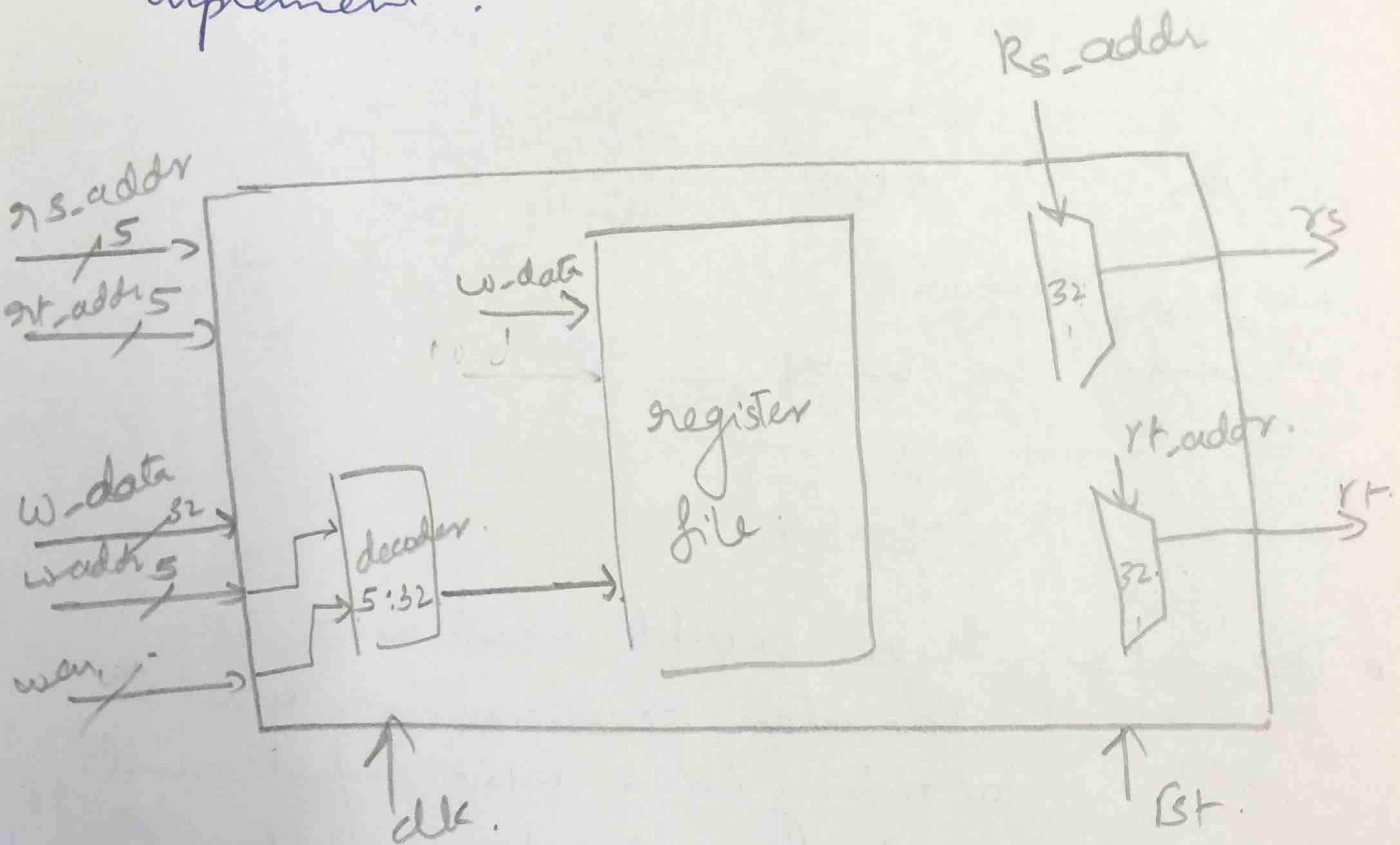
• REGISTER FILE.



- **Decoder** :- We would need a 5:32 decoder because we would be taking in a 5 bit input and will get a 32 bit output.

• 32:1 Multiplexer:-

I am using an array to store the 32 bit inputs and will access each input for the corresponding select. I feel like that design would be easier to implement.



MIPS PROCESSOR

