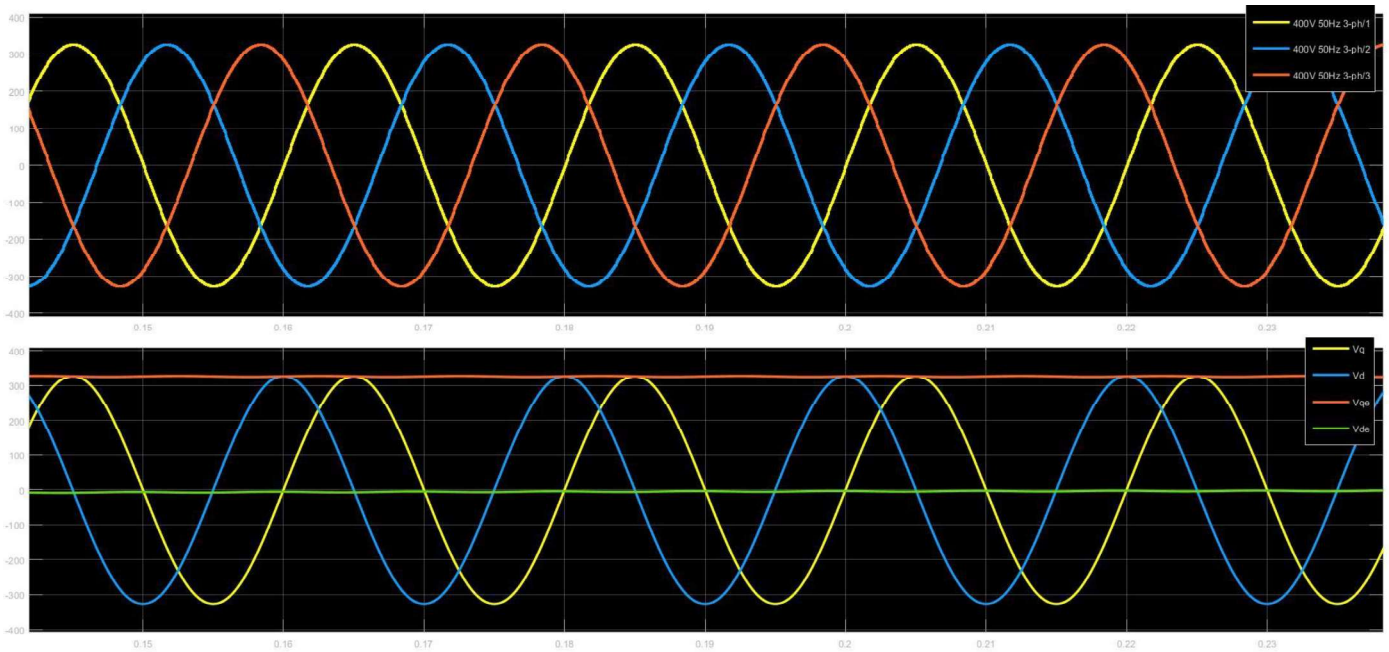
1. **Implement a 3ϕ PLL with following input voltages (400V, 50Hz fundamental):**
   a) **Balanced sinusoids.**
   b) **Unbalanced sinusoids.**
   c) **Fundamental + 20% 5th harmonic.**

Solution:

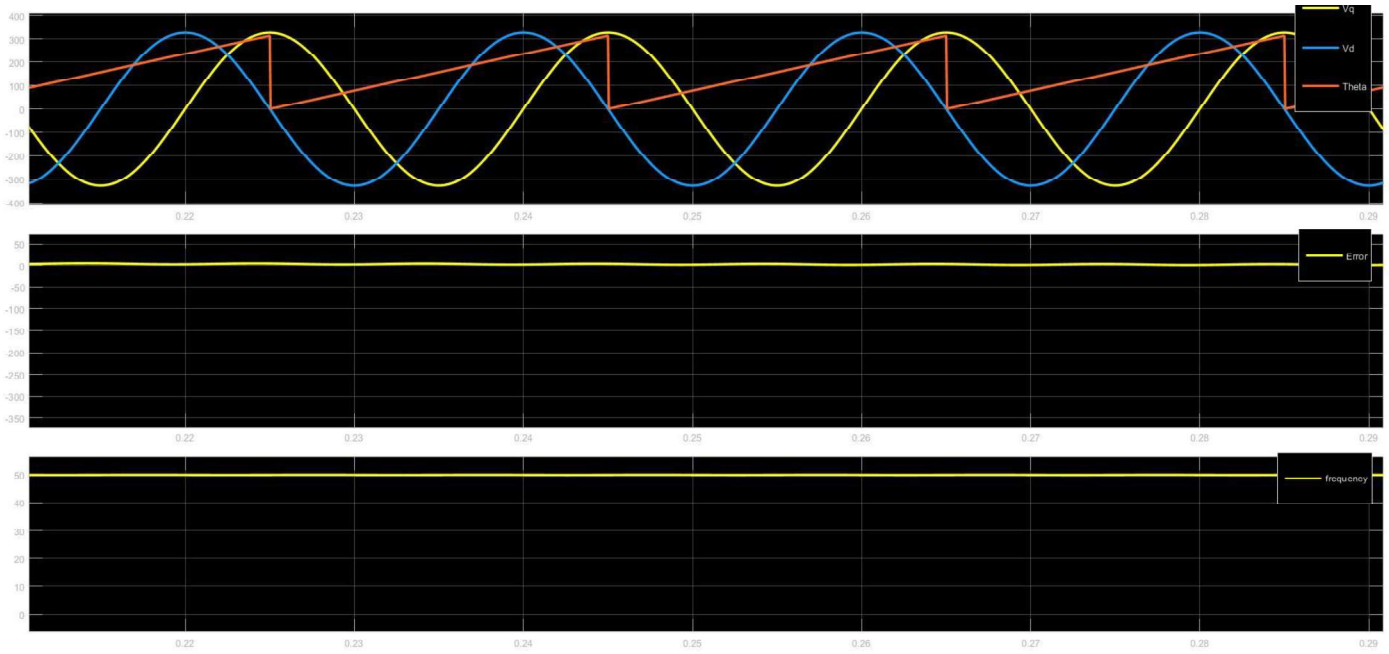
The three phase PLL has been implemented using Matlab Simulink as shown below:

Part a)

Observations taken under balanced condition:-



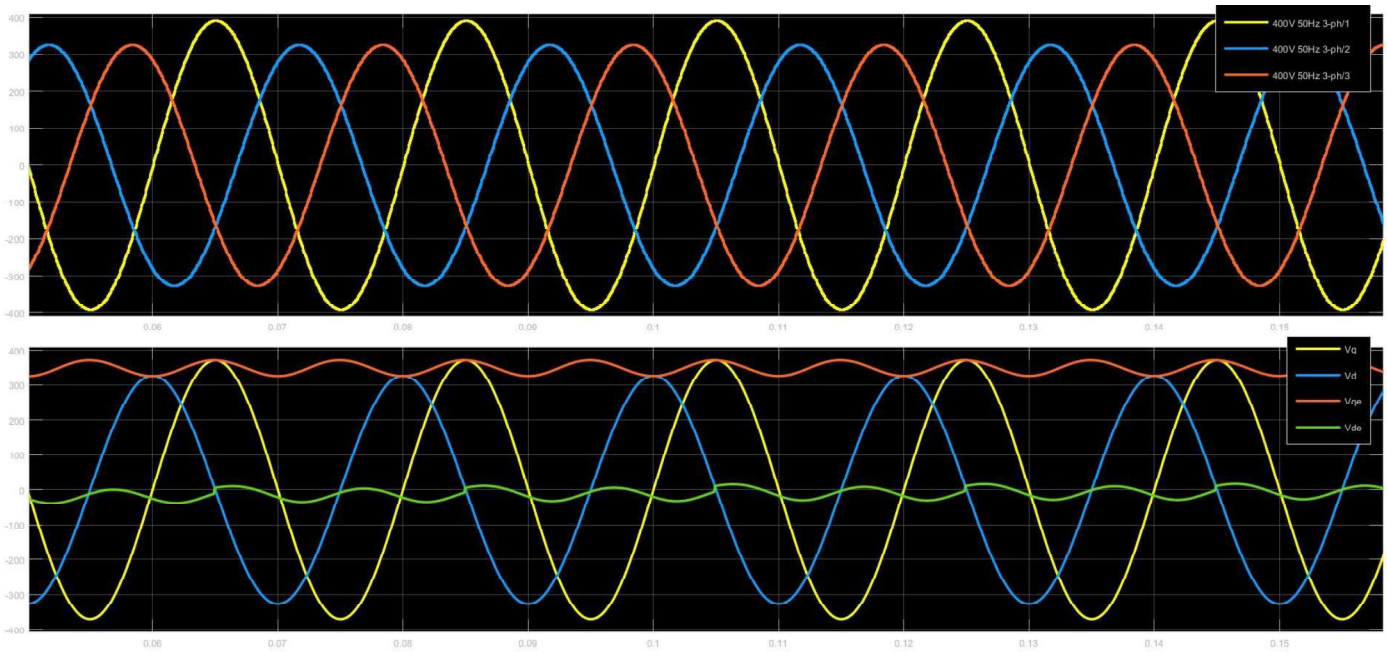
Above figure depicts the three phase input and the Vq-Vd transformations under rotating frame.



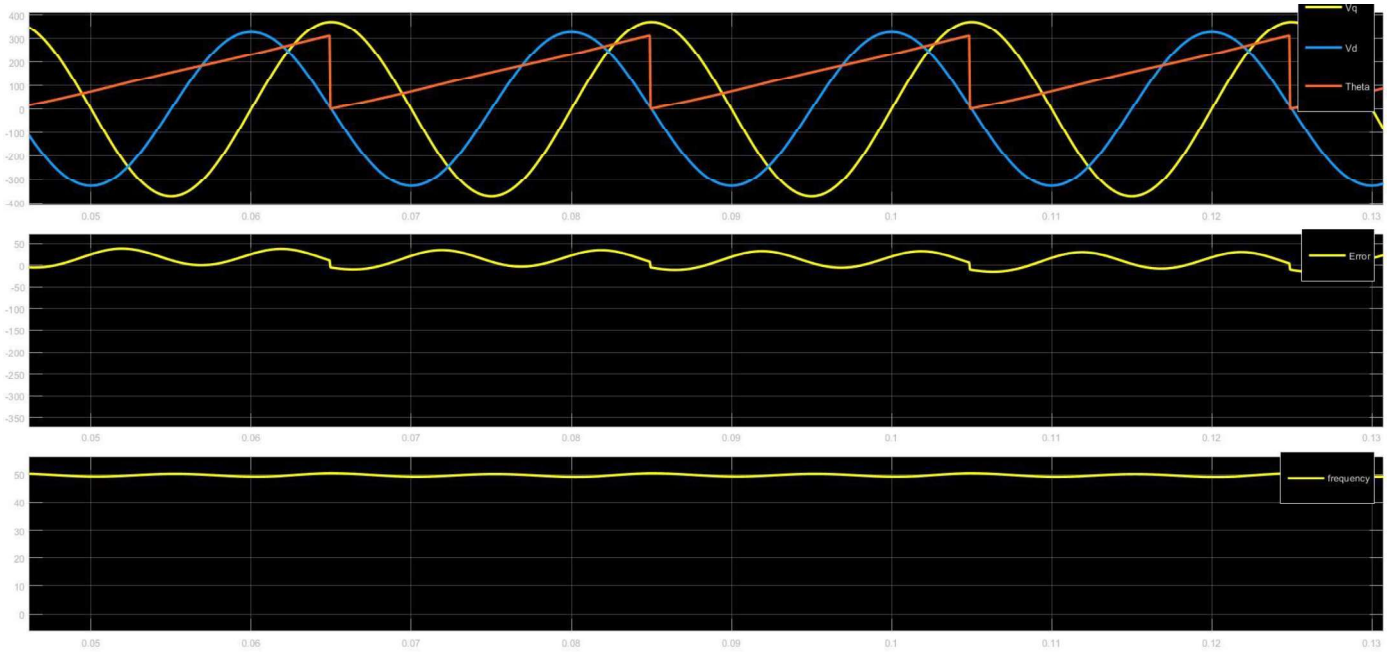
For the balanced system the error, frequency and the theta are observed as above.

Part b)

Observations taken under unbalanced condition(a phase has magnitude of 120%):-



Above figure depicts the three phase input and the Vq-Vd transformations under rotating frame.



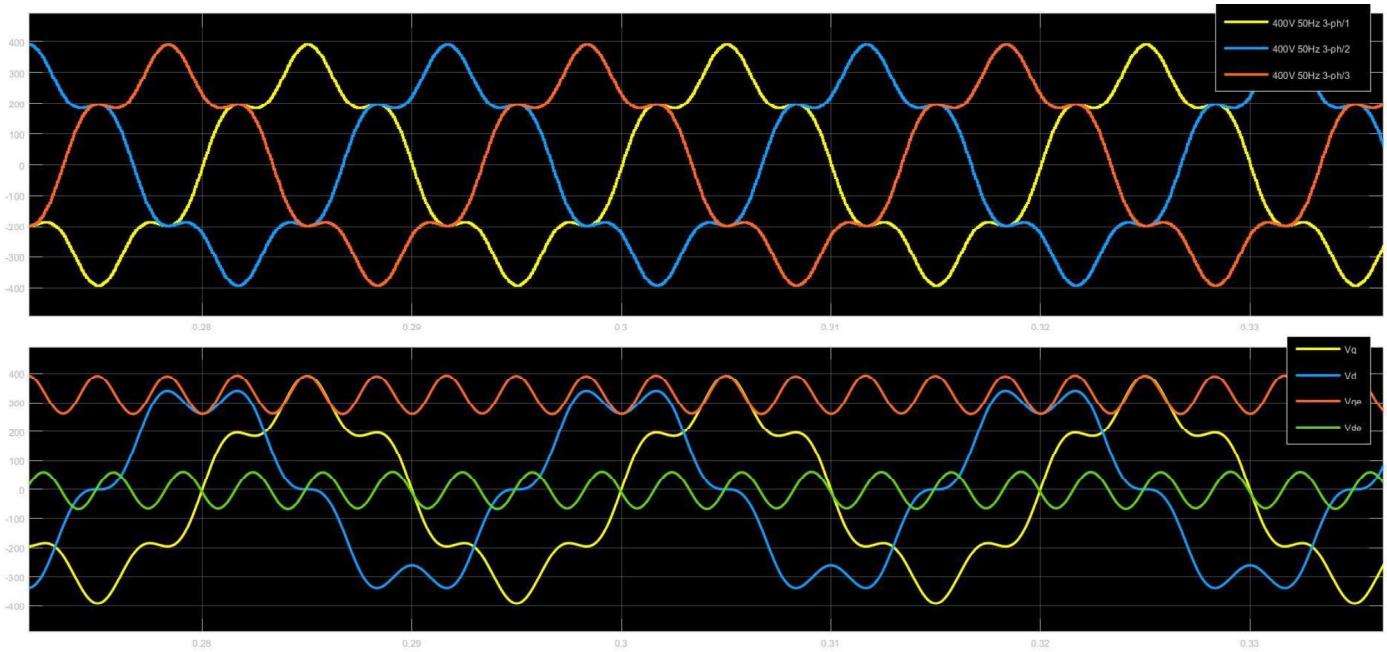
For the unbalanced system the error, frequency and the theta are observed as above.

Conclusions:

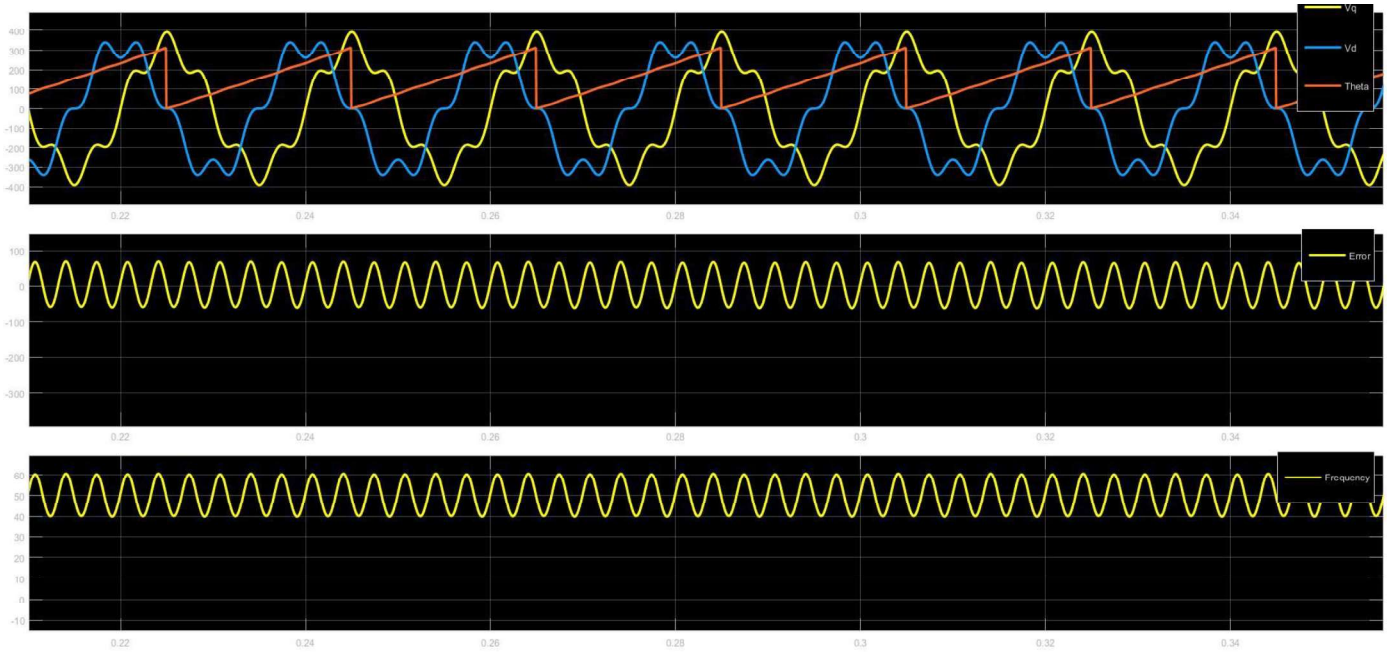
As a result of unbalance, negative sequence component introduces which leads to the induction of 2^{nd} harmonic frequency in the Vde and Vqe.

Part c)

1.Observations taken with input having Fundamental + 20% 5th harmonic without filter:



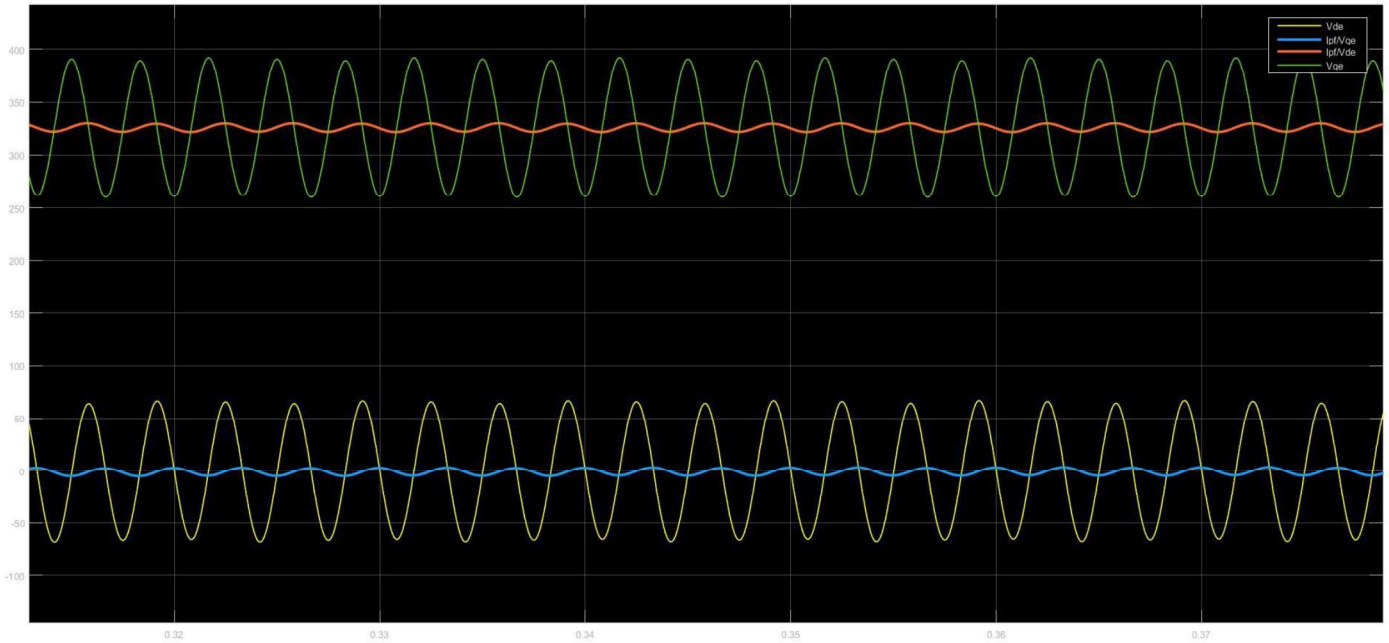
Above figure depicts the three phase input and the Vq-Vd transformations under rotating frame.



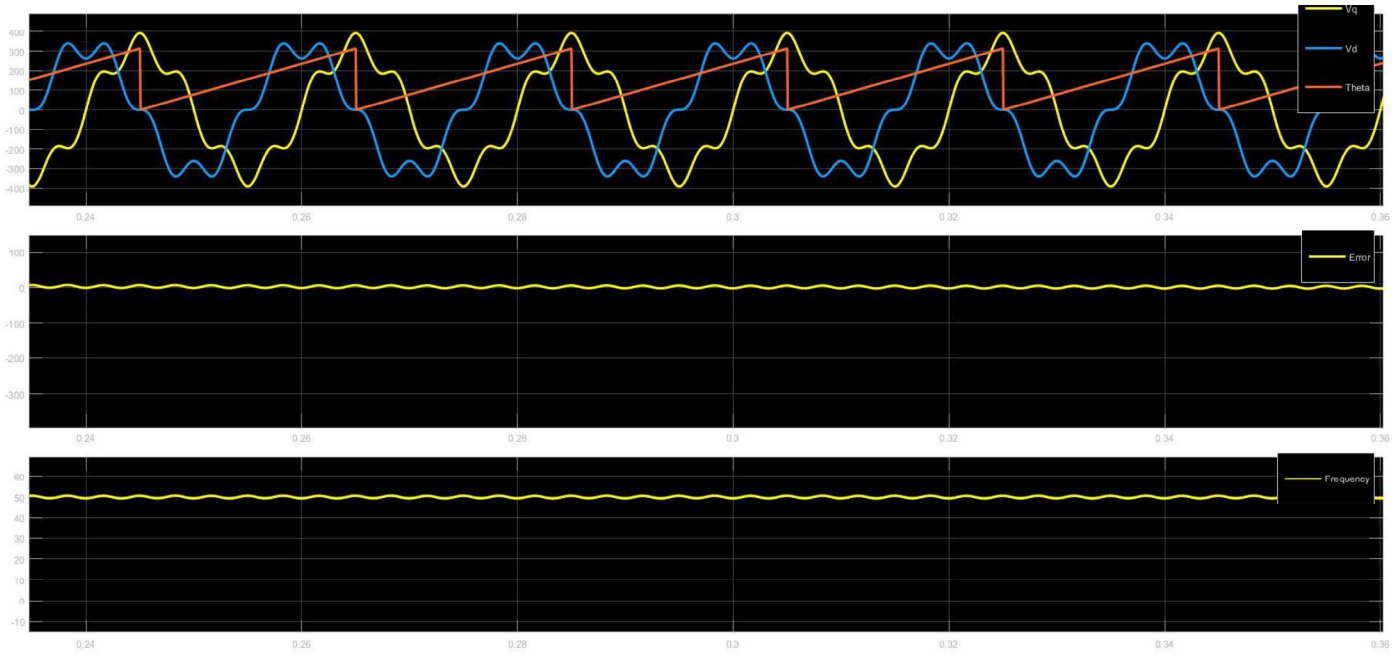
For the system with 5th harmonic the error, frequency and the theta are observed as above.

2. **Simulate part (c) of above question with ac side filter and dc side filter separately. Explain the differences observed in the PLL output waveform.**

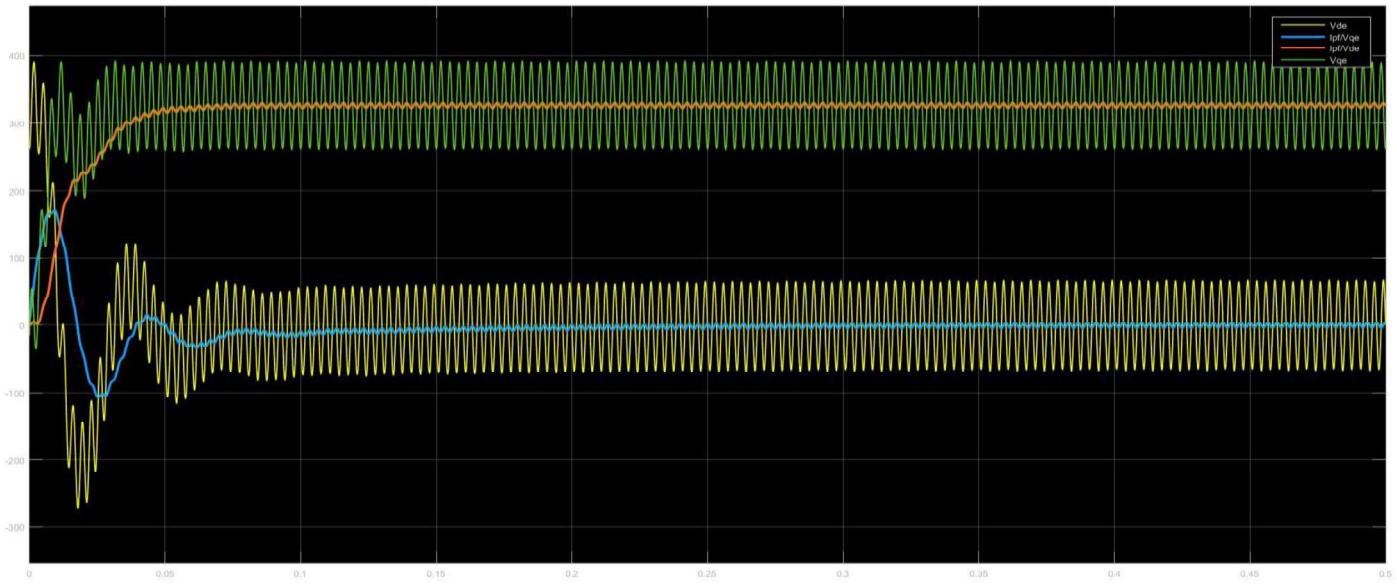
2.Observations taken with input having Fundamental + 20% 5th harmonic with filter on DC side:



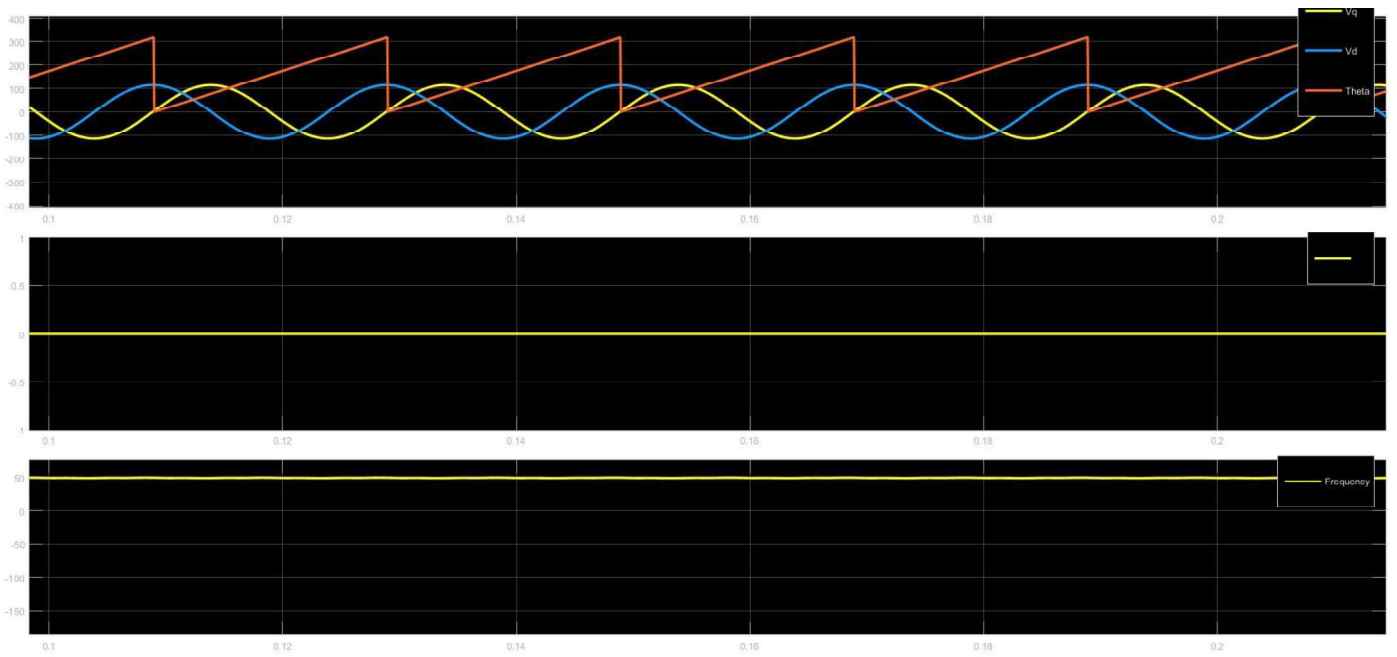
Above figure depicts the Vq-Vd transformations under rotating frame.



For the system with 5th harmonic the error, frequency and the theta are observed as above with dc side filter.



Graph shows the transients of Vq-Vd with dc side filter .



For the system with 5th harmonic the error, frequency and the theta are observed as above with ac side filter.

Observations:

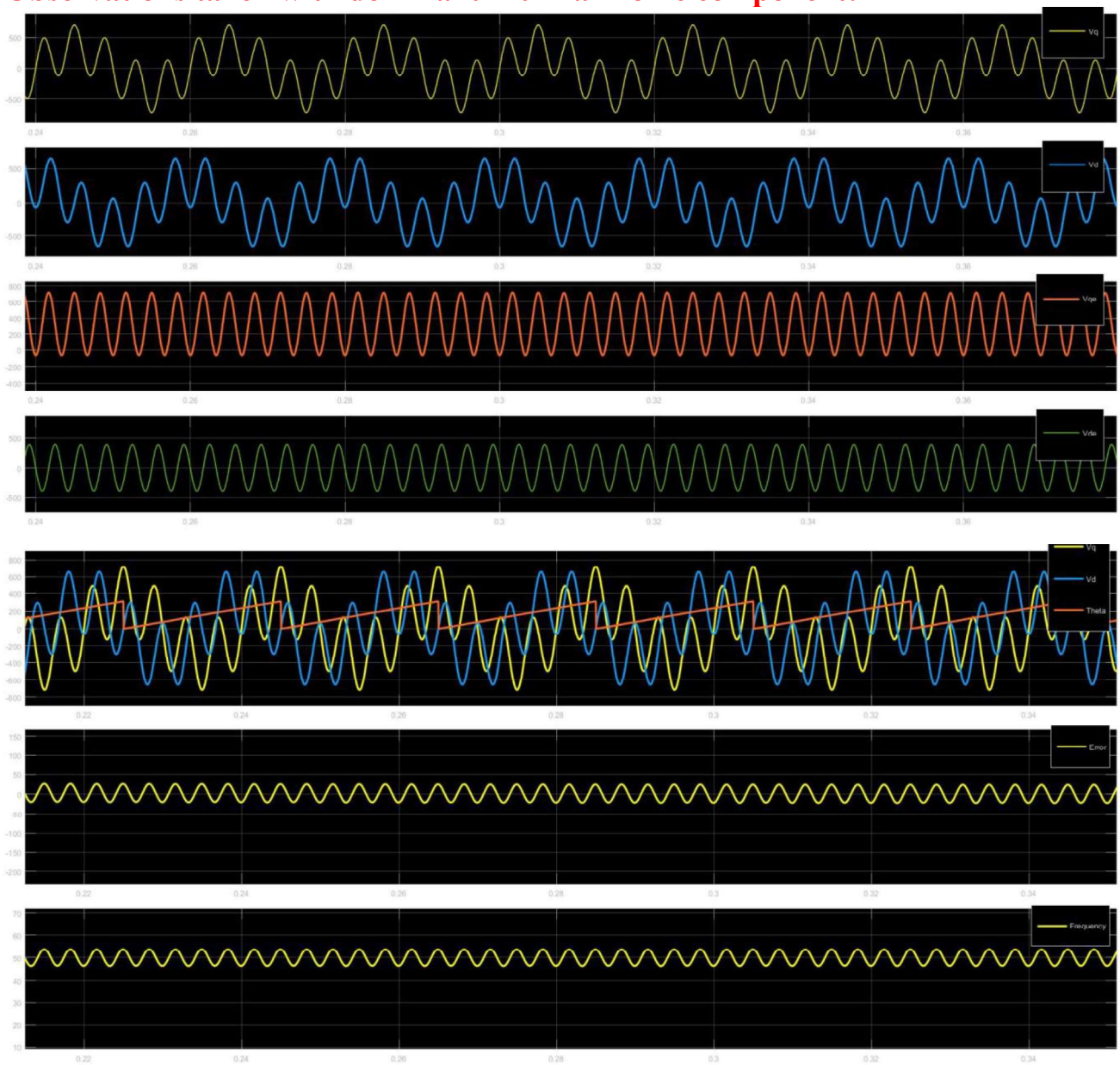
With filter the oscillations in the Vd is damped by proper design of filter.

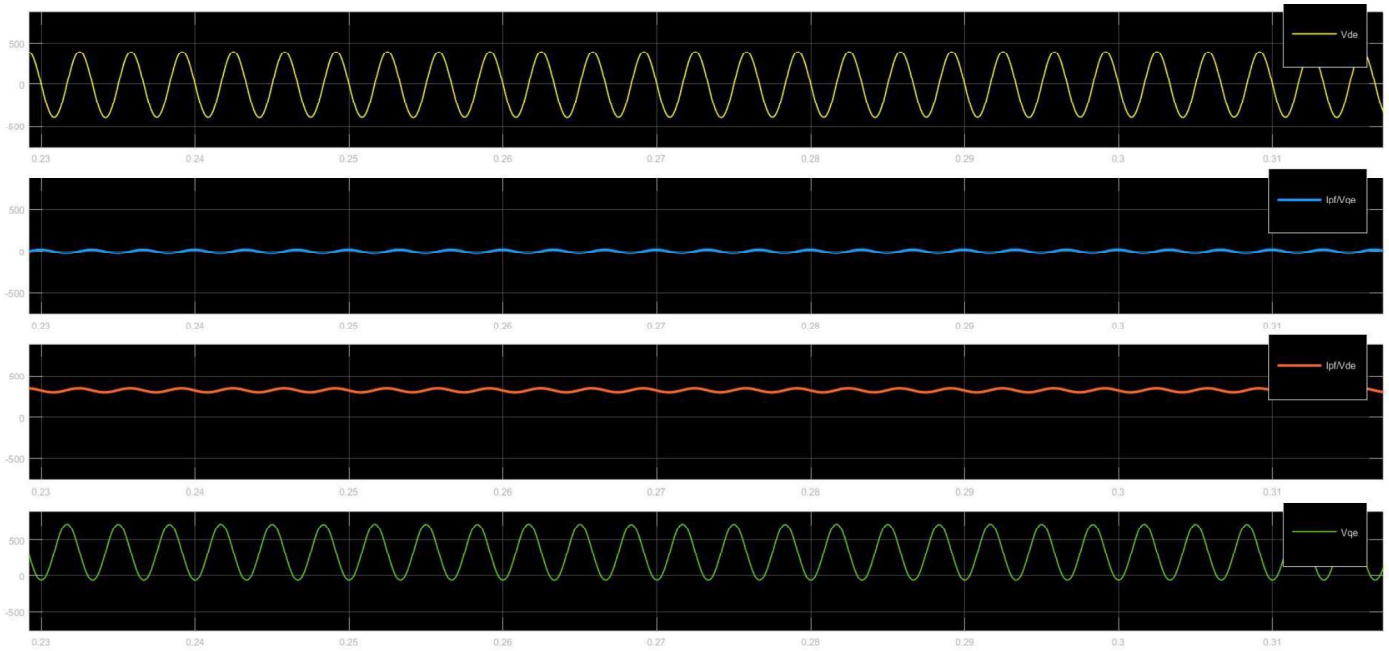
With filter on AC side it is observed that the analog filter design would result in large LC values. However it is locking at 50Hz as the desired result.

3. **In simulation with harmonics and having no filter, change magnitude of 5th harmonic to be greater than magnitude of fundamental component. Observe and comment on various waveforms.**

Solution:

Observations taken with dominant fifth harmonic component:





Observations: The PLL locked at 50 Hz only which was the fundamental component irrespective of dominating fifth harmonic.

4. **Implement a 1ϕ PLL for a pure sinusoidal voltage input (230V, 50Hz).**

Solution: