Understanding Logical Effort

Using ngspice, designing a minimum sized CMOS inverter such that the rise time and fall time are equal for a load capacitance of 0.1pF.
(We shall use the time taken to traverse from 10% to 90% of the transient as the rise/fall delay).
The n channel transistor W is 0.6μm and L is 0.4μm. Channel length of p channel transistor should also be 0.4μm. Adjust the width of the p channel transistor to get equal rise and fall times.
For this process, we shall take V_{DD} to be 3.3V.

CMOS inverter such that the rise time and fall time are equal for a load capacitance of 0.1pF.

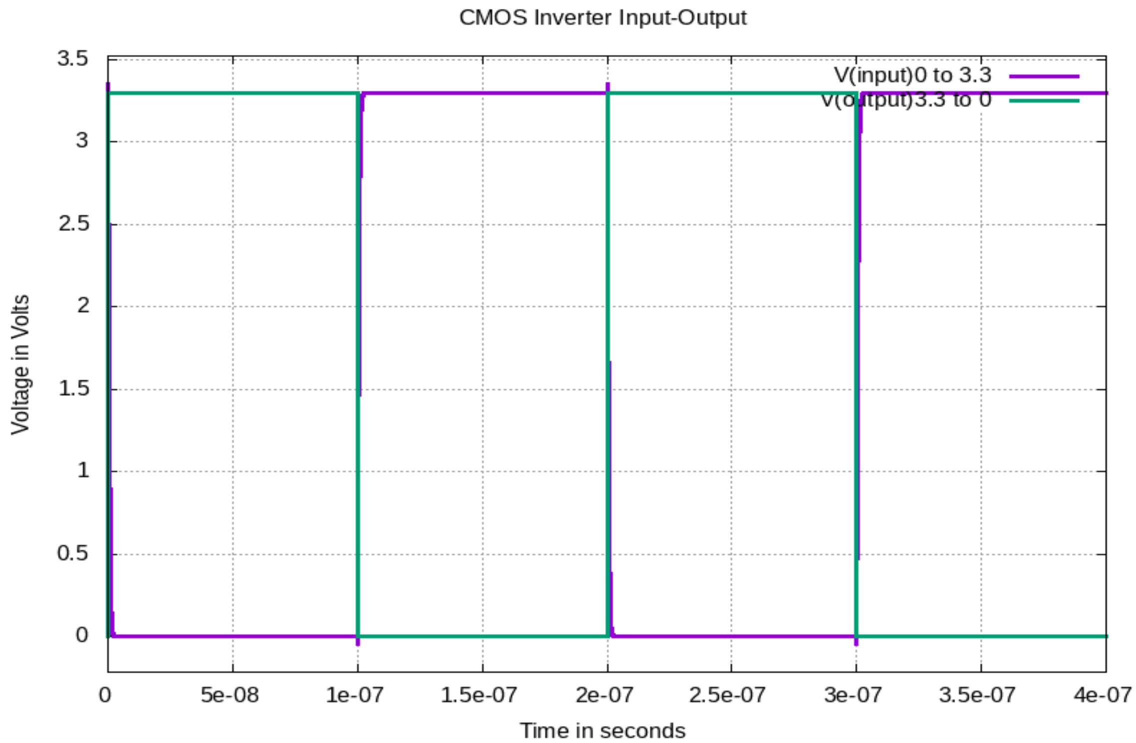
Let λ=90n,
L min = 2λ
Source Area = Drain area = W × 4λ = 2 × W × L min .
Source Perim. = Drain Perim. = 2(W + 4λ) = 2(W + 2L min)

The n channel transistor W is 0.6μm and L is 0.4μm. Channel length of p channel transistor is also 0.4μm. Adjusting the width of the p channel transistor to get equal rise and fall times.
Width turns out to be 1.55795μm.

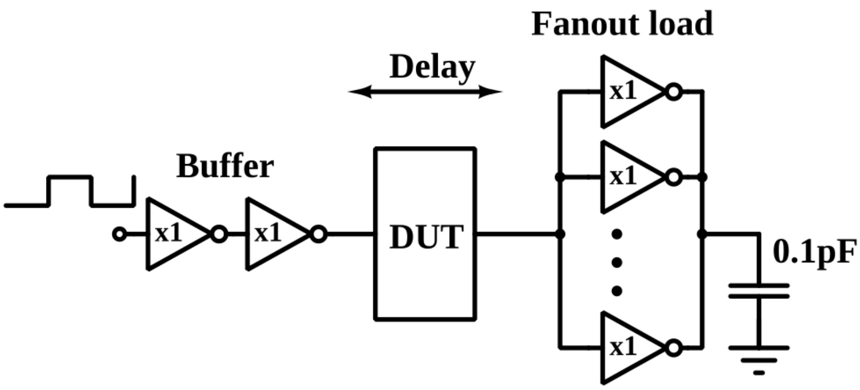
After measurements for transient analysis, rise time turned out to be 1.063718 nsec and fall time was 1.063717 nsec. Where time taken to traverse from 10% to 90% of the transient is considered as the rise/fall delay.

Also, the Inverter delay measured between 50% positions i.e. 1.65V on the transients at the input and output is .5774116 nsec.

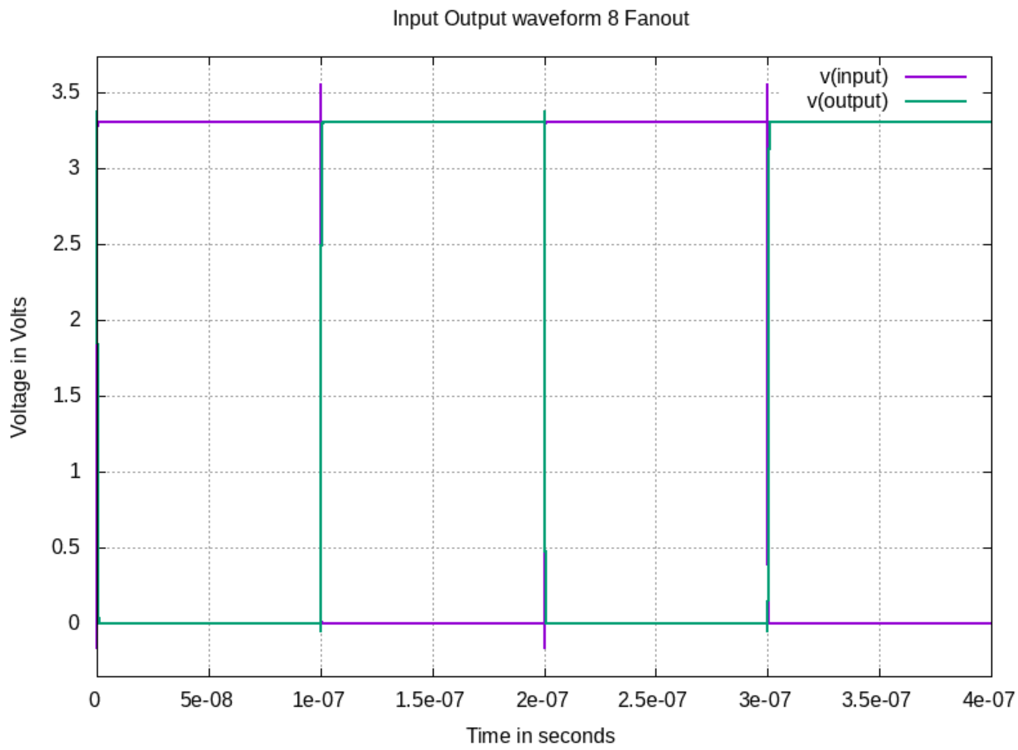
Minimun size Inverter with 0.1pf load.



Loading the DUT with 1, 2, 3, . . . 8 inverters.



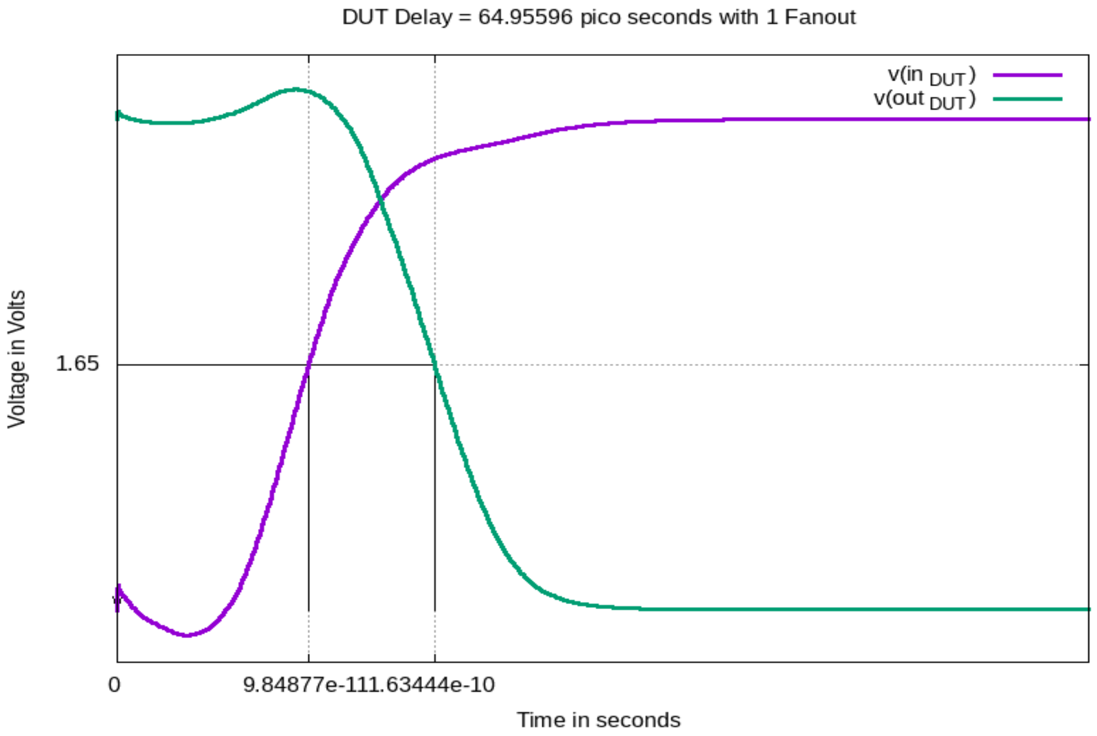
DUT input output waveform

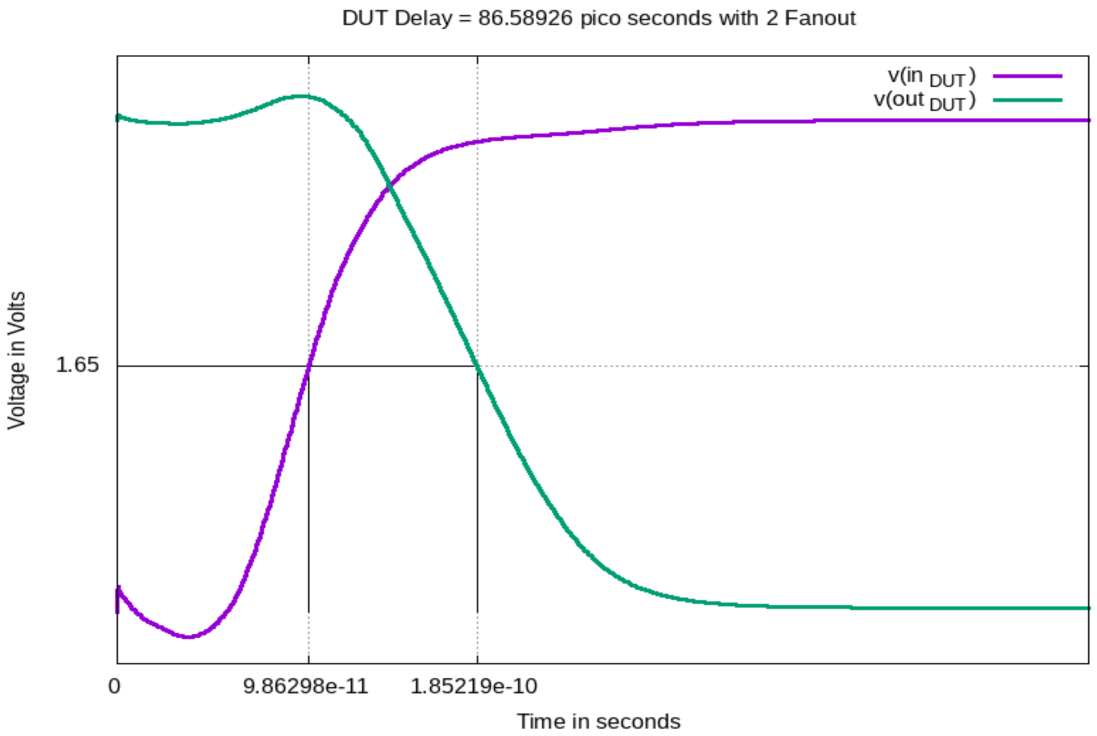


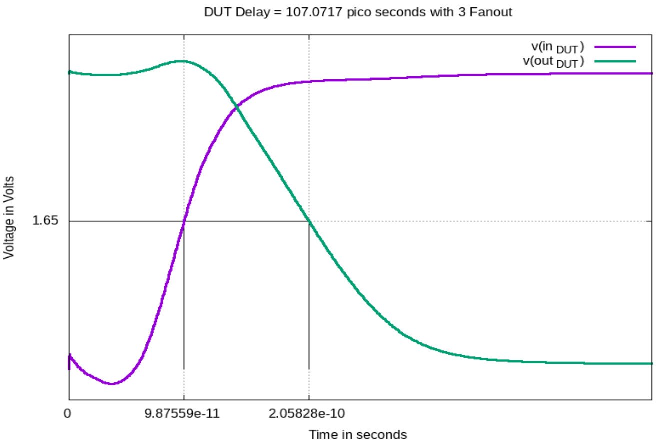
Observations:

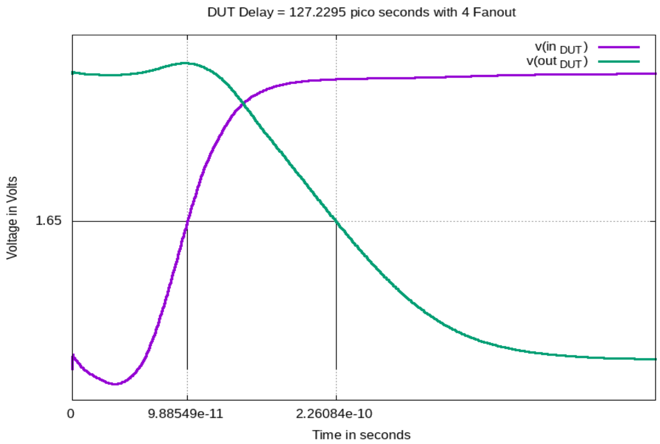
Measurements for Transient Analysis 1 Fanout Load inverter (in seconds)	
Rise time for output capacitor	= 1.066423e-09
Fall time for output capacitor	= 1.067839e-09
Rise time for DUT output	= 7.692229e-11
Fall time for DUT output	= 7.361886e-11
Delay by DUT	= 6.495596e-11
Measurements for Transient Analysis 2 Fanout Load inverter (in seconds)	
Rise time for output capacitor	= 5.527538e-10
Fall time for output capacitor	= 5.540146e-10
Rise time for DUT output	= 1.141917e-10
Fall time for DUT output	= 1.116567e-10
Delay by DUT	= 8.658926e-11
Measurements for Transient Analysis 3 Fanout Load inverter	
Rise time for output capacitor	= 3.898961e-10
Fall time for output capacitor	= 3.909244e-10
Rise time for DUT output	= 1.557521e-10
Fall time for DUT output	= 1.532822e-10
Delay by DUT	= 1.070717e-10
Measurements for Transient Analysis 4 Fanout Load inverter	
Rise time for output capacitor	= 3.167560e-10
Fall time for output capacitor	= 3.173368e-10
Rise time for DUT output	= 2.039521e-10
Fall time for DUT output	= 2.009512e-10
Delay by DUT	= 1.272295e-10
Measurements for Transient Analysis 5 Fanout Load inverter	
Rise time for output capacitor	= 2.796501e-10
Fall time for output capacitor	= 2.797147e-10
Rise time for DUT output	= 2.643911e-10
Fall time for DUT output	= 2.584323e-10
Delay by DUT	= 1.474070e-10
Measurements for Transient Analysis 6 Fanout Load inverter	
Rise time for output capacitor	= 2.602525e-10
Fall time for output capacitor	= 2.595680e-10
Rise time for DUT output	= 3.534234e-10
Fall time for DUT output	= 3.311610e-10
Delay by DUT	= 1.677488e-10
Measurements for Transient Analysis 7 Fanout Load inverter	
Rise time for output capacitor	= 2.499899e-10
Fall time for output capacitor	= 2.484970e-10
Rise time for DUT output	= 4.344415e-10
Fall time for DUT output	= 4.126067e-10
Delay by DUT	= 1.883176e-10
Measurements for Transient Analysis 8 Fanout Load inverter	
Rise time for output capacitor	= 2.459695e-10
Fall time for output capacitor	= 2.438730e-10
Rise time for DUT output	= 4.830160e-10
Fall time for DUT output	= 4.686080e-10
Delay by DUT	= 2.090897e-10

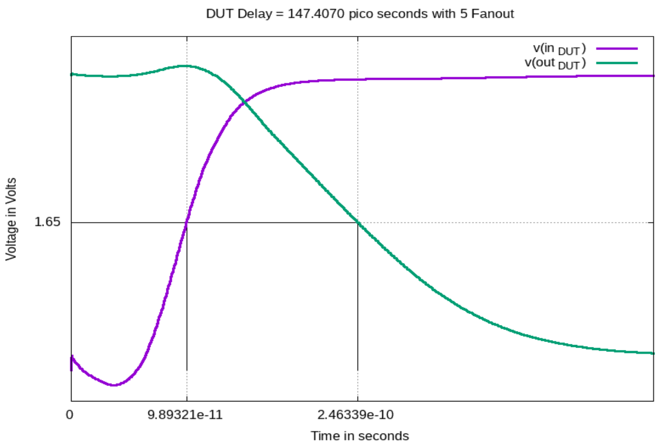
Input-Output Delay Characteristcis of DUT

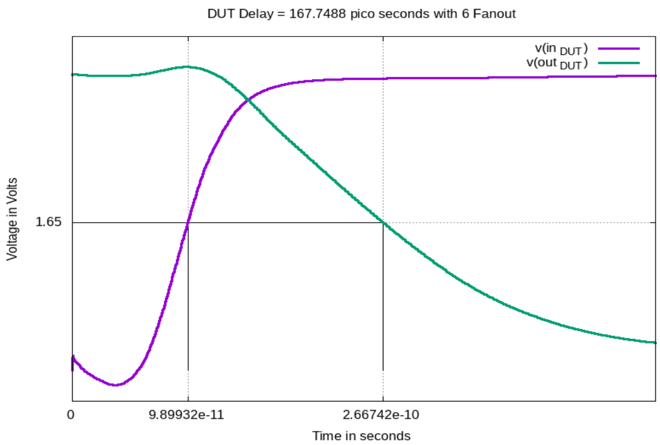


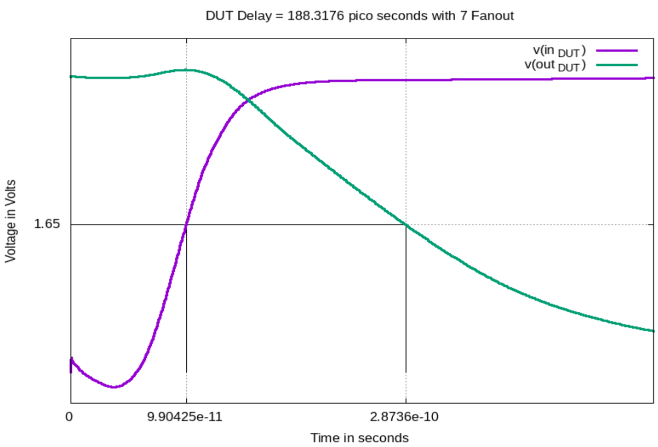


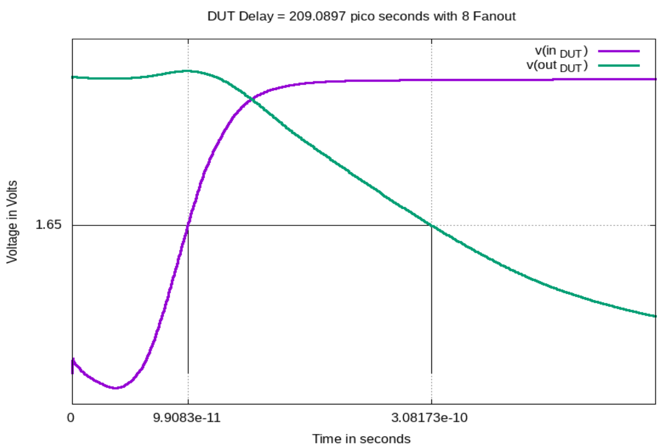

DUT Delay = 107.0717 pico seconds with 3 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.87559e-11
2.05828e-10
Time in seconds


DUT Delay = 127.2295 pico seconds with 4 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.88549e-11
2.26084e-10
Time in seconds


DUT Delay = 147.4070 pico seconds with 5 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.89321e-11
2.46339e-10
Time in seconds

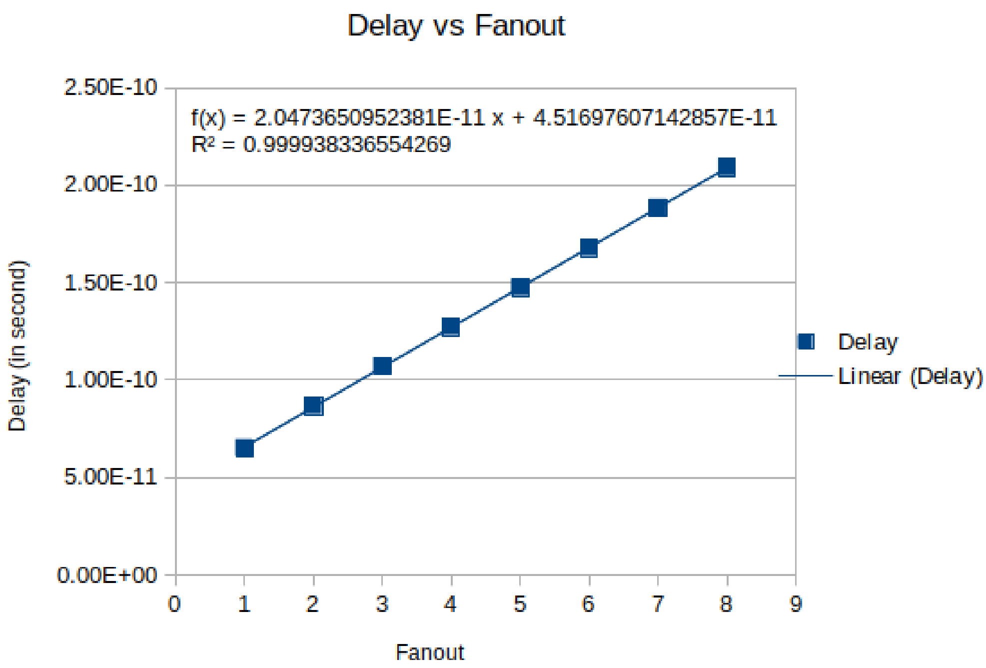

DUT Delay = 167.7488 pico seconds with 6 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.89932e-11
2.66742e-10
Time in seconds


DUT Delay = 188.3176 pico seconds with 7 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.90425e-11
2.8736e-10
Time in seconds


DUT Delay = 209.0897 pico seconds with 8 Fanout
v(in DUT)
v(out DUT)
Voltage in Volts
1.65
0
9.9083e-11
3.08173e-10
Time in seconds

Plotting Fanout vs Delay of DUT,

FANOUT	Delay (in pico seconds)
1	64.95596
2	86.58926
3	107.0717
4	127.2295
5	147.407
6	167.7488
7	188.3176
8	209.0897



Evaluating τ and p_{inv}

From graph

$p_{inv}\tau = 4.51697607142857 \times 10^{-11}$

where,

$\tau = 2.04736509523811 \times 10^{-11}$

So,

$p_{inv} = 4.51697607142857 \times 10^{-11} / 2.04736509523811 \times 10^{-11}$

$p_{inv} = 2.216872509103$