

# Cache Coherence Protocol using SystemC

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## Details:

The code submitted is not 100% functional. However, the code contains pseudo code for the logic and contains the primary function calls.

## Explanation:

**Snooping:** In this thread (line 185), the cache snoops if there is a signal on the bus that is not generated by itself (line 194). Followed by a check which checks if a cache block is present inside its cache and is valid (line 204). If the cache block is valid, then we check if the port signal is a read or write.

In case of read, we update the value of the valid cache block onto the data bus for the CPU and updated its age for the replacement policy.

In case of a write, we simply invalidate the cache block since it is being written by the CPU to some other cache.

**Cache:** In the cache execute thread (line 230), we simply just call the bus interface read/write signals to provide the bus signals for all caches in case of a miss.

In case of write miss, we simply send the bus signal containing the current cache id, the address and the data that is being written (line 272).

In case of read miss, we first set the data port to a known value and wait for certain cycles allowing other caches to check if there is cache hit. If so, then the other cache returns the data on the data port. If no caches have the cache block, then we request the memory to provide the value (line 304).