

# Cache simulator using SystemC

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## Requirements:

Cache size = 32 KB

Cache line size = 32 Bytes

Cache ways = 8

## Calculations:

Byte offset bits =  $\log_2(\text{Cache line size}) = \log_2(32) = \mathbf{5 \text{ bits}}$

Index bits =  $\log_2(\text{Cache size} / (\text{Cache line size} * \text{Cache ways}))$

$= \log_2(32K / (32 * 8)) = \mathbf{7 \text{ bits}}$

Tag bits = Address bits – Index bits – Byte offset bits =  $32 - 7 - 5 = \mathbf{20 \text{ bits}}$

## Results:

Tracefiles	CPU	Reads	Read Hits	Read Misses	Writes	Write Hits	Write Misses	Hit Rate	Execution time (ns)
dbg	0	40	19	21	60	29	31	48.000	2259
rnd	0	33031	18662	14369	32505	18308	14197	56.411	1534940
fft	0	86298	7282	79016	43195	10990	32205	14.110	8074286

## Screenshots:

1. dbg\_pl

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU    Reads  RHit   RMiss  Writes  WHit   WMiss  Hitrate
0      40      19     21     60      29     31     48.000000
```

2. rnd\_pl

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU    Reads  RHit   RMiss  Writes  WHit   WMiss  Hitrate
0      33031  18662  14369  32505  18308  14197  56.411743
```

3. fft\_pl

```
Info: /OSCI/SystemC: Simulation stopped by user.
CPU    Reads  RHit   RMiss  Writes  WHit   WMiss  Hitrate
0      86298  7282   79016  43195  10990  32205  14.110415
```