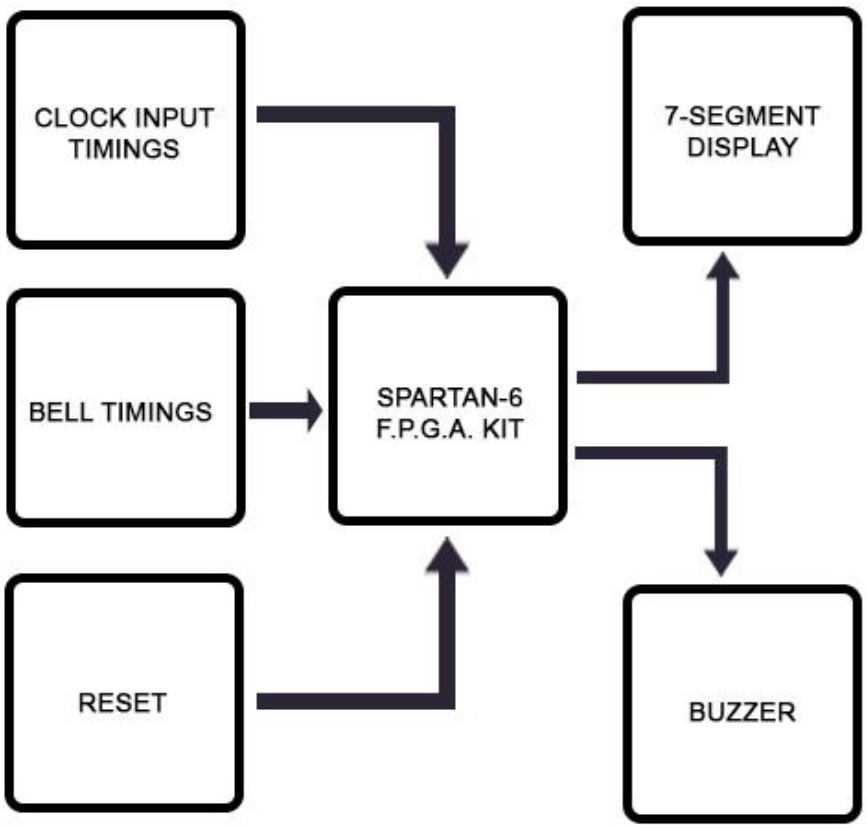
COLLEGE BELL SYSTEM USING FPGA

INTRODUCTION

Educational institutes like colleges, universities and schools have various periods and classes throughout the day. To indicate the end of each class and the start of each period a bell is used. This bell is usually rung by a person after each hour. However this bell might not be accurate all the time. So we propose a system to automate this process. The primary objective of designing this project is to reduce human intervention for the purpose of manual switching operation of a bell, thus increasing the accuracy. Our system is designed in such a way that it is exactly dependent on real time clock and the switching of the bell is controlled automatically.

BLOCK DIAGRAM



Clock Input Timings:

The Spartan 6 FPGA kit has an inbuilt clock of 4Mhz.The time period will be inversely proportional, i.e. 0.25us. So we design a clock with time period 1s, to match with the real time. The input timings to start the clock are also given.

Bell Timings:

The values of time at which the bell should ring and the duration of the bell is also decided and given as input (i.e. for every hour from 9:00am to 4:00 pm).

Reset:

A reset switch is used to reset all time values to zero. Active high reset is used.

F.P.G.A. kit:

The FPGA kit converts the Verilog Behavioral code into Switch level which is used to implement into the hardware devices such as LED, Buzzer, Dip switch, LCD display etc..

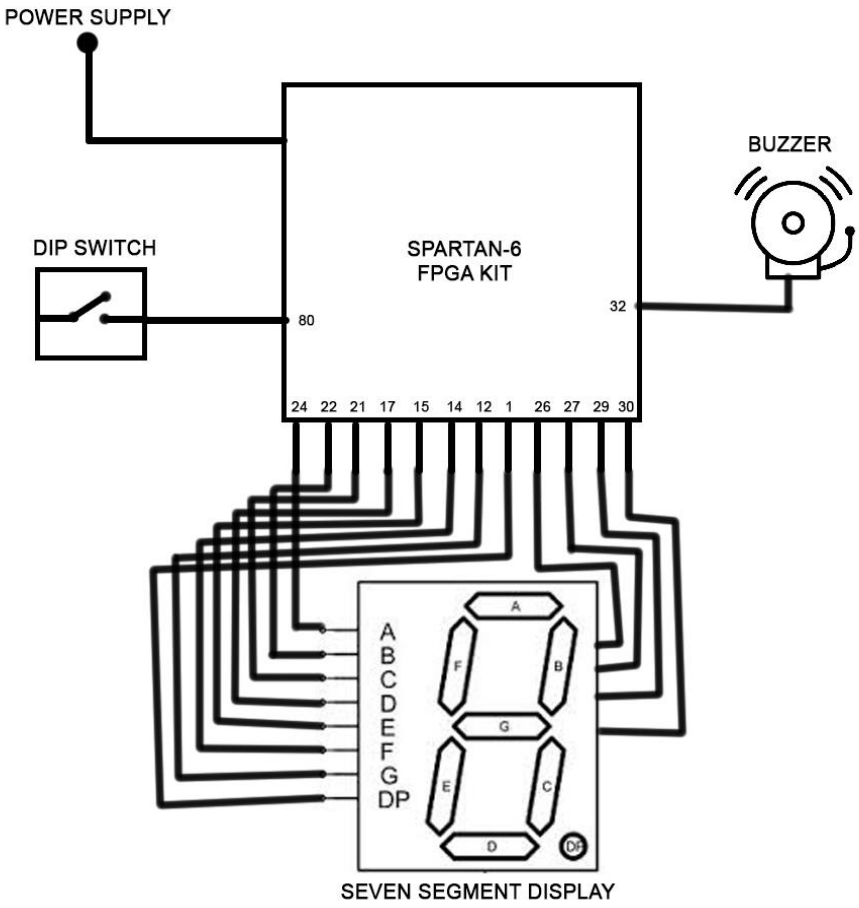
Seven Segment Display:

A Seven Segment Display is used to display the hours and minutes of the clock. A Verilog code is used to convert the binary values of the clock to Seven Segment Display.

Buzzer:

The Buzzer is used as a bell. When the clock reaches the desired value (i.e. every hour from 9:00 am to 4:00pm in the current code) it will causes the bell to ring for a desired duration**.**

CIRCUIT DESIGN



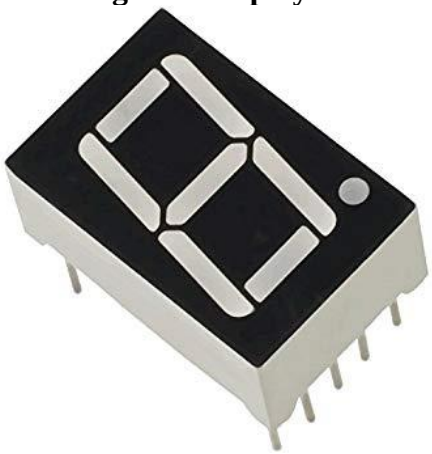
Component Description

SL. No	Name	Description
1	Spartan-6 FPGA kit	Used for implementing the Verilog code.
2	Seven Segment Display	Used to display the time.
3	Dip Switch	Used as a reset switch.
4	Buzzer	Used as a bell.

Spartan-6 FPGA kit:

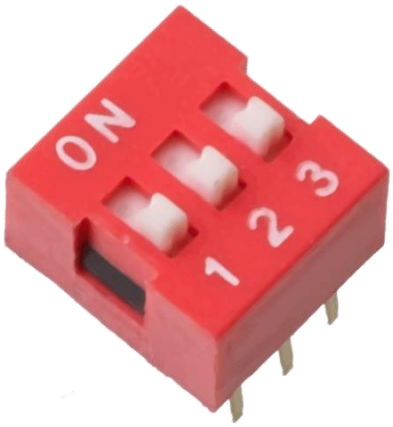
Spartan 6 FPGA Development board is the feature rich development board with Spartan 6 FPGA, SPI FLASH, ADC, DAC, LCD, 7 segment Display, Wi-Fi and Bluetooth. The Board also provides additional interface like CMOS Camera and TFT Display at the expansion connectors.

Seven Segment Display



The common cathode seven segment displays have the cathode of the LEDs connected together and so the logic “1” should be given to the common cathode and Logic “0” should be given to the corresponding anode in order to display the numerical value.

Dip Switch



DIP switches are most common used in electronic circuits for digital input of ON/OFF states. They allow control over current flow in a circuit.

Buzzer

A buzzer is a small yet efficient component to add sound features to our project/system. It is very small and compact 3-pin structure hence can be easily used on breadboard. This buzzer can be used by simply powering it using a DC power supply ranging from 1.25V to 3.3V.

WORKING PRINCIPLE

Clock generation:

The Spartan-6 FPGA kit has a 4MHz internal clock. A Verilog code designed to generate a 1Hz clock using this 4MHz and clock division concept, so as to generate a time of 1s which matches the real world timing.

Time generation:

Using this 1Hz clock seconds, minutes and hours are incremented. A 24-hour format is chosen. At every negative edge of this clock, the seconds gets incremented. After 59 seconds, the minutes start incrementing and after 59 minutes, hours start incrementing. After 23 hours, 59 minutes and 59 seconds, the time is set back to 0 and seconds start incrementing again. All variables keep incrementing continuously. The initial value of all variables can be changes so as to start the clock from a particular time. The reset switch is used to reset all time values to zero.

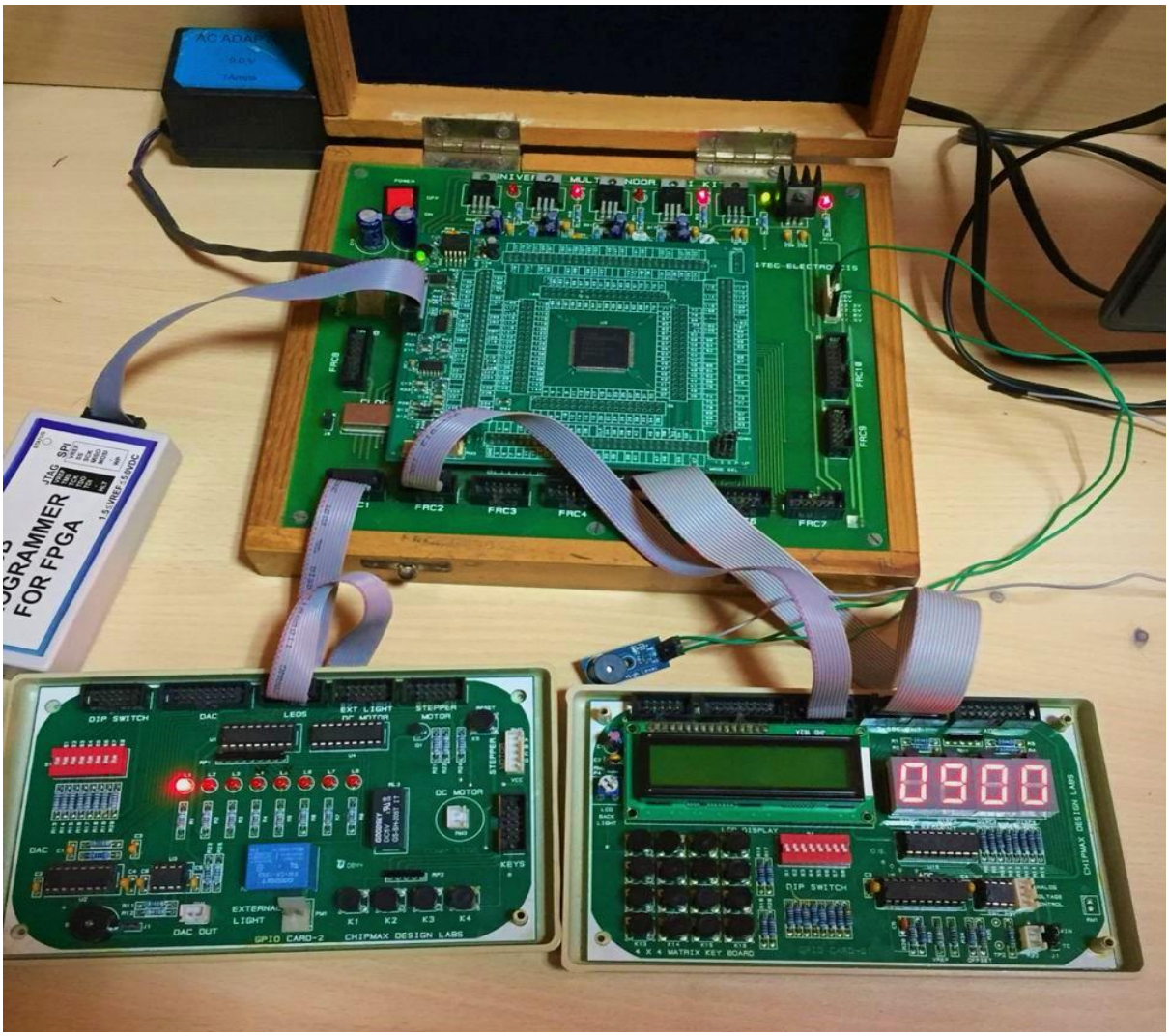
Bell time settings:

The bell timings are set to ring only from 9:00 hours to 16:00 hours. There are a total of 8 bell rings. The first being at 9:00 hours indicating the start of college day, the next bell rings are at 10:00 hours, 11:00 hours, 12:00 hours, 13:00 hours, 14:00 hours, 15:00 hours respectively. The

last bell ring is at 16:00 hours indicating the end of the college day. The first and the last bell rings for 8 seconds each and the bells in between ring for 5 seconds each.

The current value of time is given as initial condition to the clock and switched on. The clock and bell works according to the conditions mentioned.

RESULT



The college Bell System is implemented and outputs are verified.

This project can be further improved by displaying the seconds and by designing a provision for manual input of time to the clock.