



MINI-PROJECT

ON

Monostable multivibrator using IC 555

A PROJECT REPORT Submitted

TO

GONDWANA UNIVERSITY, GADCHIROLI By

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In partial fulfilment for the award of the degree of
BACHELOR OF ENGINEERING IN ELECTRONICS &
TELECOMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project title
Monostable multivibrator by using IC 555
has been carried out by the Team under my guidance in
partial fulfilment of the degree of Bachelor of
engineering in Electronics & Telecommunication
Engineering of Gondwana University, Gadchiroli during
the academic year 2024-2025

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Place :- Chandrapur

Date:

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Component List

| Sr. No. | Component | Value | Quantity |
|---------|------------------|--------------|-------------|
| 1 | Resistor | 10 kOhm | 3 |
| 2 | Resistor | 4.7 kOhm | 1 |
| 3 | Capacitor | 470 μ F | 1 |
| 4 | Capacitor | 1000 μ F | 1 |
| 5 | Capacitor | 10 nF | 1 |
| 6 | Resistor | 1 kOhm | 1 |
| 7 | LM555 (IC555) | - | 1 |
| 8 | Banana Clips | - | 10 |
| 9 | Patch Cords | - | As required |
| 10 | Push Button | - | 1 |
| 11 | LED | - | 1 |
| 12 | Connecting Wires | - | As required |

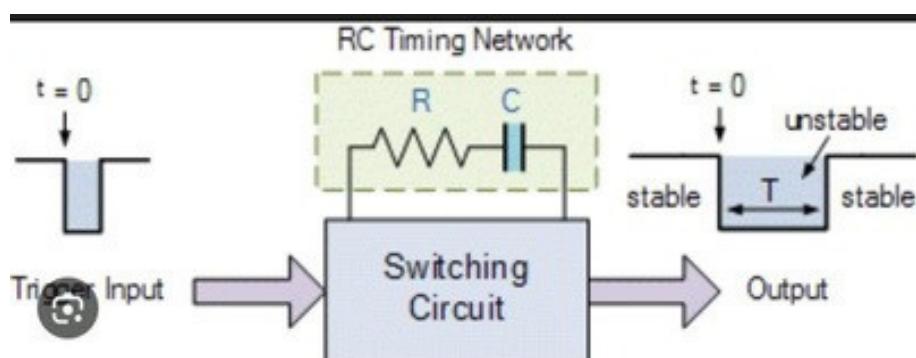
Title:-

Monostable multivibrator by using IC 555.

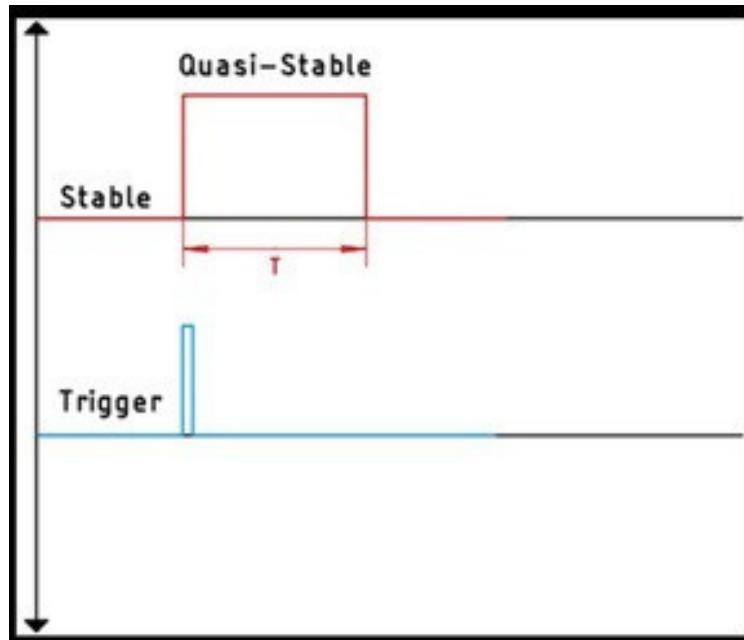
Objective:-

The objective is to design a monostable multivibrator using IC 555 to generate a single output pulse of specific duration in response to a trigger signal.

Abstract:

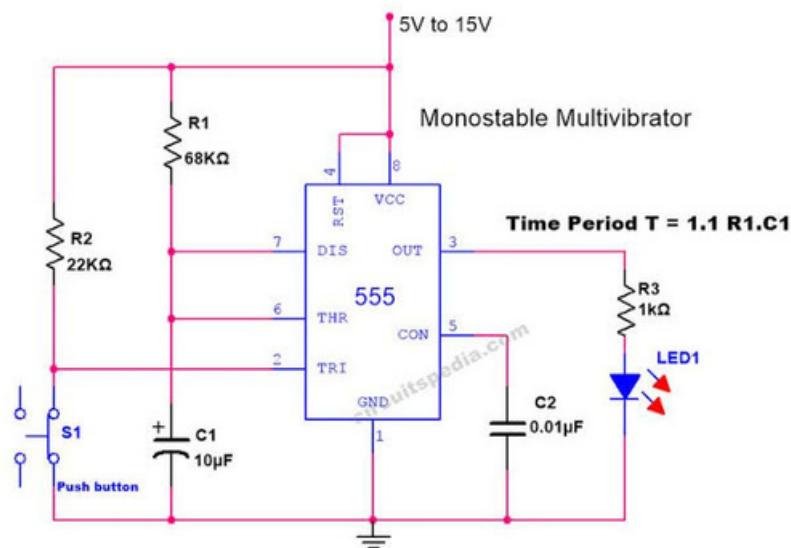


A **monostable multivibrator** using the IC 555 timer, like the one made with an op-amp, has only one stable state, and the other state is a quasi-stable state. When triggered, the 555 timer switches from its stable state to the quasi-stable state for a fixed time period determined by external components. After this time, it automatically returns to the stable state.



Img src: [electronics circuits](#)

Monostable multivibrator with IC 555



Img Source: [electronics tutorial](#)

Working:

In its stable state, the output of the 555 is low (0V). When a trigger pulse is applied, it changes to high (1) for a set time duration, then returns to the low state.

The time period for which the output stays high is determined by a resistor and capacitor connected externally to the timer, similar to the op-amp-based design.

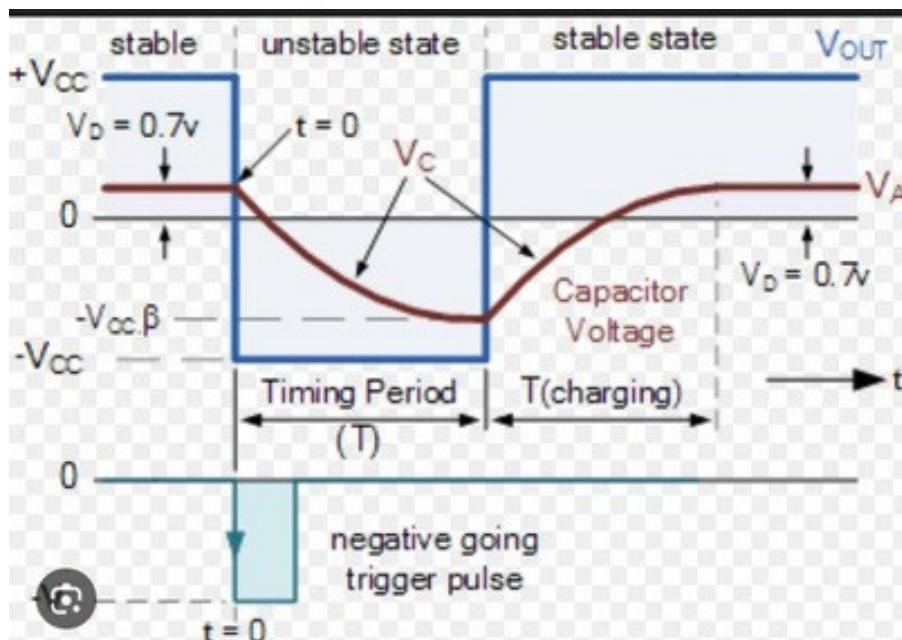
Circuit Description:

IC 555: The heart of the circuit, operating in monostable mode.

Resistor (R): Determines the time constant along with the capacitor.

Capacitor (C): Works with the resistor to set the time duration for which the output remains in the quasi-stable state.

Trigger Pulse: A negative pulse applied at the trigger input (pin 2) to initiate the state change.



Img src: [electronics tutorial](#)

Circuit Operation:

- Initially, the output of the 555 IC is LOW.
- When a negative trigger pulse is applied to pin 2 (trigger pin), the output goes HIGH.
- The capacitor (C) starts charging through the resistor (R).
- The output stays HIGH until the capacitor voltage reaches $2/3$ of the supply voltage (determined by the internal comparators of the IC 555).
- Once this threshold is reached, the output returns to LOW, and the circuit resets, waiting for the next trigger pulse.

Time Period Calculation:

The time for which the output remains HIGH is determined by the resistor and capacitor values, and the time period (T) is given by:

$$T = 1.1 \times R \times C$$

Where:

T is the time duration of the output pulse (in seconds),
R is the resistance (in ohms),
C is the capacitance (in farads).

For example, if you use a resistor of 10 k Ω and a capacitor of 100 μ F, the time period would be:

$$T = 1.1 \times 10,000 \times 100 \times 10^{-6}$$

$$T = 1.1 \text{ seconds}$$

Calculation

Case 1: $R_1 = 10\text{kohm}$. $C_1 = 470 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 10 \times 10^3 \times 470 \times 10^{-6}$$

$$T = 5.14 \text{ seconds}$$

Case 2: $R_1 = 10\text{kohm}$. $C_1 = 1000 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 10 \times 10^3 \times 1000 \times 10^{-6}$$

$$T = 11 \text{ seconds}$$

Case 3: $R_1 = 20\text{kohm}$. $C_1 = 470 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 20 \times 10^3 \times 470 \times 10^{-6}$$

$$T = 10.34 \text{ seconds}$$

Case 4: $R_1 = 20\text{kohm}$. $C_1 = 1000 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 20 \times 10^3 \times 1000 \times 10^{-6}$$

$$T = 22 \text{ seconds}$$

Case 5: $R_1 = 4.7 \text{ k ohm}$. $C_1 = 470 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 4.7 \times 10^3 \times 470 \times 10^{-6}$$

$$T = 2.429 \text{ seconds}$$

Case 6: $R_1 = 4.7 \text{ k ohm}$. $C_1 = 1000 \text{ micro F}$

$$T = 1.1 \times R_1 \times C_1$$

$$T = 1.1 \times 4.7 \times 10^3 \times 1000 \times 10^{-6}$$

$$T = 5.17 \text{ seconds}$$

Advantages: -

Ease of Use: The IC 555 is easy to set up in monostable mode with minimal components.

Stable Operation: Provides reliable output timing for a range of applications.

Cost-Effective: Low-cost components make it accessible for many designs.

Disadvantages: -

Limited Timing Range: Large resistors or capacitors are required for long durations.

Temperature Sensitivity: Like other RC-based circuits, component values can drift with temperature changes, affecting timing accuracy.

Trigger Sensitivity: The trigger pulse must be shorter than the output pulse for proper operation.

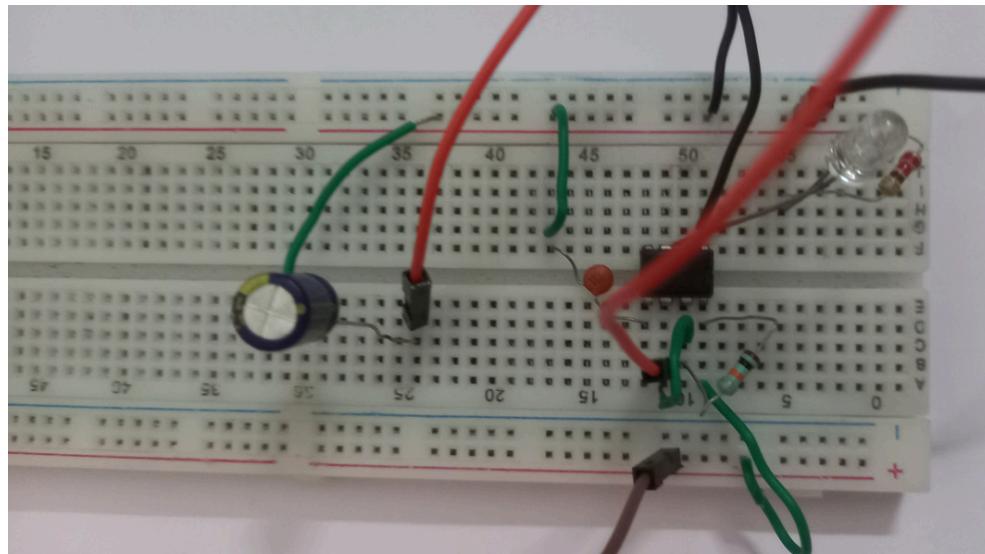
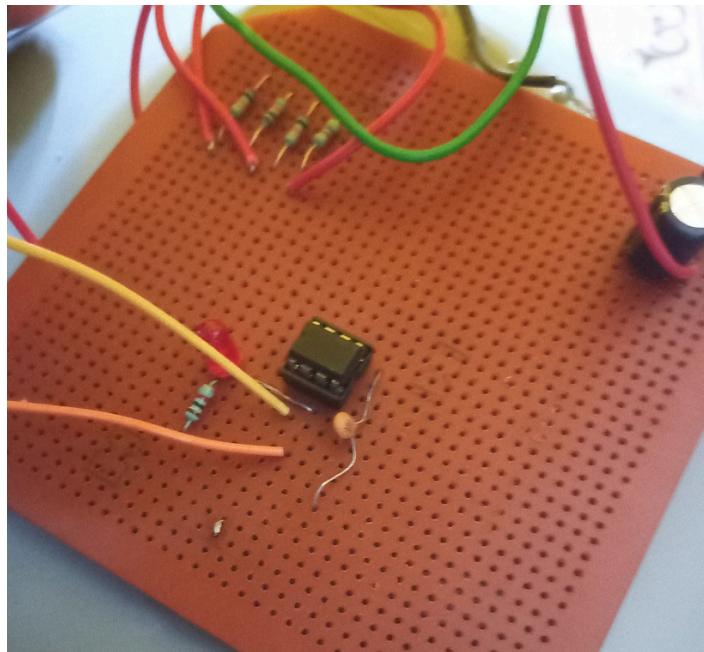
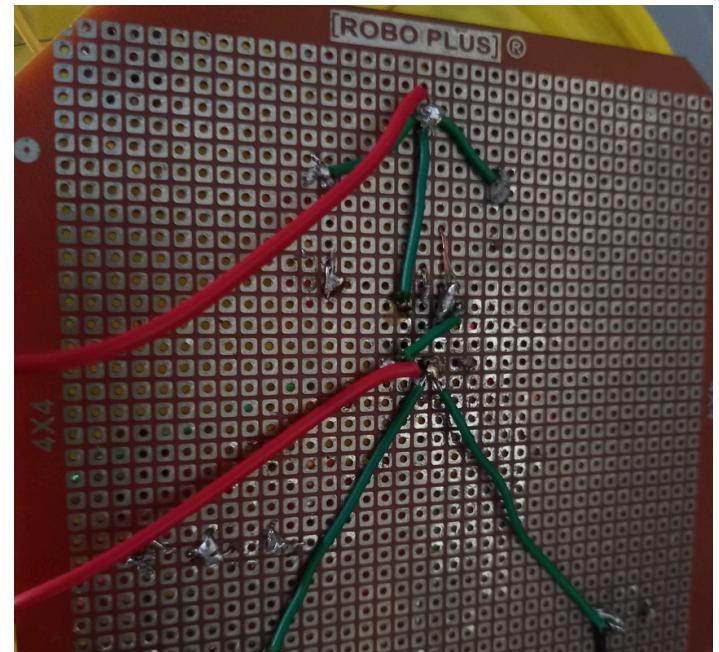


Fig.Circuit design on Breadboard



**fig. Zero PCB Circuit design
(Front side)**



**fig. Zero PCB Circuit design
(back side)**

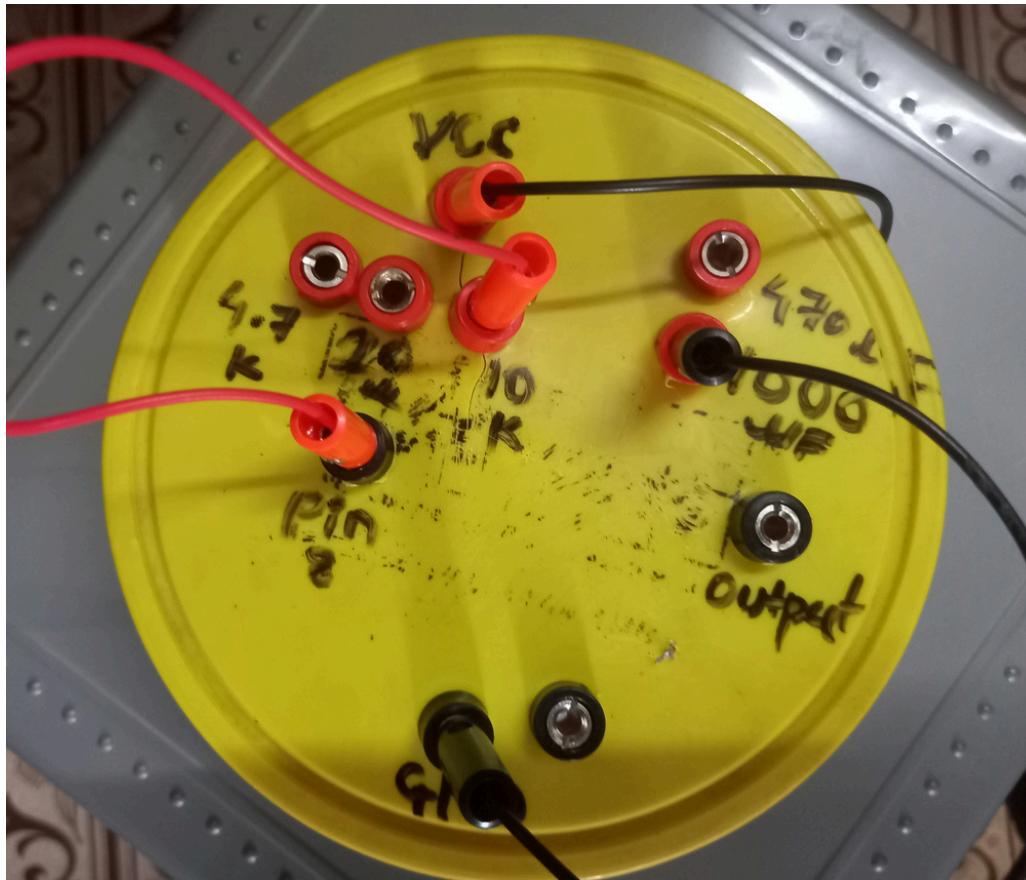


Fig. Overall project kit.

Application: -

Timers: Can be used as timers in various circuits where a delayed output is needed.

Pulse Generation: Used to generate pulses of specific width in digital circuits.

Debouncing Switches: Removes unwanted noise and false triggering caused by mechanical switch bouncing.

Reference:

Books:

1. “555 Timer Applications” by Forrest M. Mims
2. “Practical Electronics for Inventors” by Paul Scherz

Websites:

1. <https://circuitdigest.com/electronic-circuits/555-timer-monostable-multivibrator-circuit>
2. https://www.electronics-tutorials.ws/waveforms/555_timer.html

LM555 Timer

1 Features

- Direct Replacement for SE555/NE555
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output
- Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

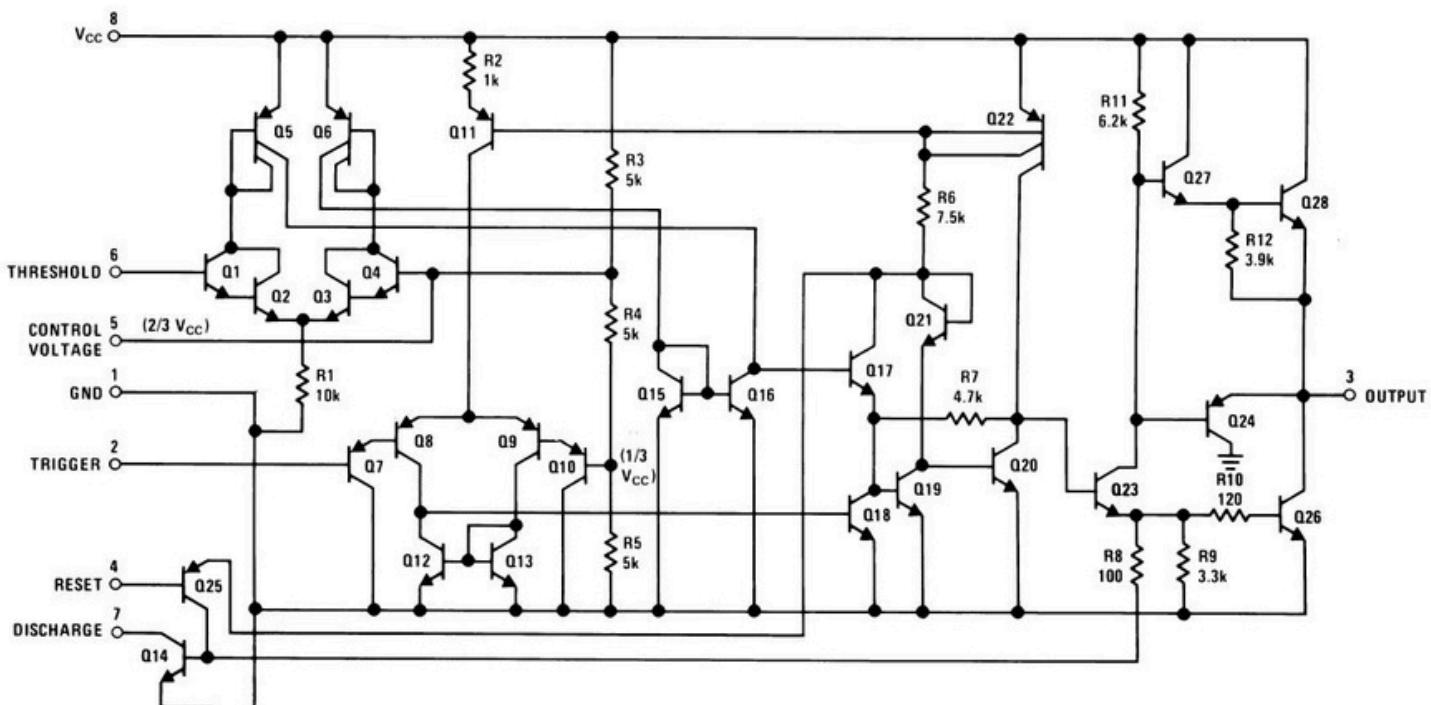
The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| LM555 | SOIC (8) | 4.90 mm x 3.91 mm |
| | PDIP (8) | 9.81 mm x 6.35 mm |
| | VSSOP (8) | 3.00 mm x 3.00 mm |

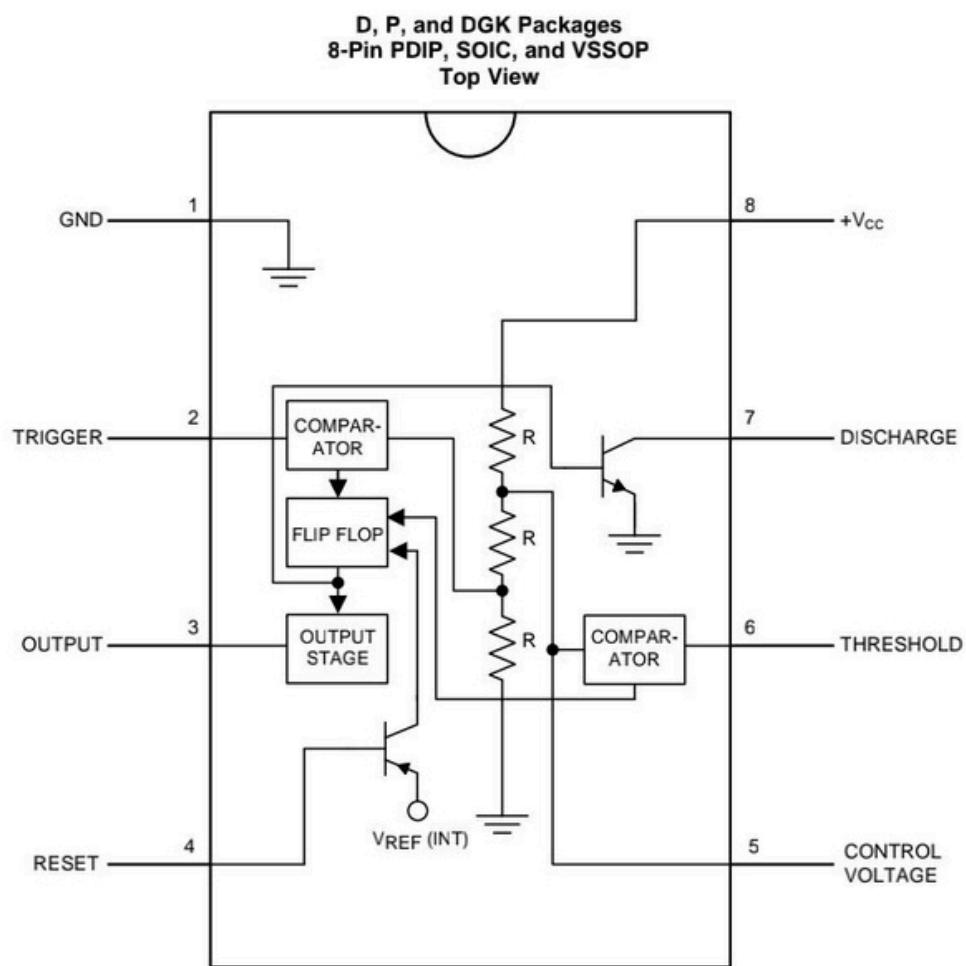
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|---|
| NO. | NAME | | |
| 5 | Control Voltage | I | Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform |
| 7 | Discharge | I | Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage |
| 1 | GND | O | Ground reference voltage |
| 3 | Output | O | Output driven waveform |
| 4 | Reset | I | Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering |
| 6 | Threshold | I | Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop |
| 2 | Trigger | I | Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin |
| 8 | V ⁺ | I | Supply voltage with respect to GND |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | | | MIN | MAX | UNIT |
|---------------------------------------|---|--------------------------|------|-----|------|
| Power Dissipation ⁽³⁾ | LM555CM, LM555CN ⁽⁴⁾ | | 1180 | | mW |
| | LM555CMM | | 613 | | mW |
| Soldering Information | PDIP Package | Soldering (10 Seconds) | 260 | | °C |
| | Small Outline Packages (SOIC and VSSOP) | Vapor Phase (60 Seconds) | 215 | | °C |
| | | Infrared (15 Seconds) | 220 | | °C |
| Storage temperature, T_{sig} | | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) For operating at elevated temperatures the device must be derated above 25°C based on a 150°C maximum junction temperature and a thermal resistance of 106°C/W (PDIP), 170°C/W (SOIC-8), and 204°C/W (VSSOP) junction to ambient.
- (4) Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-----------------------|
| $V_{(\text{ESD})}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±500 ⁽²⁾ V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The ESD information listed is for the SOIC package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------------------|--|-----|-----|------|
| Supply Voltage | | | 18 | V |
| Temperature, T_A | | 0 | 70 | °C |
| Operating junction temperature, T_J | | | 70 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | LM555 | | | UNIT |
|---|--------|------|-------|------|
| | PDIP | SOIC | VSSOP | |
| | 8 PINS | | | |
| $R_{\text{θJA}}$ Junction-to-ambient thermal resistance | 106 | 170 | 204 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ to 15 V , unless otherwise specified)⁽¹⁾⁽²⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|-----|--------|------|-----------------------|
| Supply Voltage | | 4.5 | | 16 | V |
| Supply Current | $V_{CC} = 5\text{ V}$, $R_L = \infty$ | | 3 | 6 | mA |
| | $V_{CC} = 15\text{ V}$, $R_L = \infty$ (Low State) ⁽³⁾ | | 10 | 15 | |
| Timing Error, Monostable | | | | | |
| Initial Accuracy | | | 1 % | | |
| Drift with Temperature | $R_A = 1\text{ k}$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$, ⁽⁴⁾ | | 50 | | ppm/ $^\circ\text{C}$ |
| Accuracy over Temperature | | | 1.5 % | | |
| Drift with Supply | | | 0.1 % | | V |
| Timing Error, Astable | | | | | |
| Initial Accuracy | | | 2.25 | | |
| Drift with Temperature | $R_A, R_B = 1\text{ k}$ to $100\text{ k}\Omega$, $C = 0.1\text{ }\mu\text{F}$, ⁽⁴⁾ | | 150 | | ppm/ $^\circ\text{C}$ |
| Accuracy over Temperature | | | 3.0% | | |
| Drift with Supply | | | 0.30 % | | V |
| Threshold Voltage | | | 0.667 | | $\times V_{CC}$ |
| Trigger Voltage | $V_{CC} = 15\text{ V}$ | | 5 | | V |
| | $V_{CC} = 5\text{ V}$ | | 1.67 | | V |
| Trigger Current | | | 0.5 | 0.9 | μA |
| Reset Voltage | | 0.4 | 0.5 | 1 | V |
| Reset Current | | | 0.1 | 0.4 | mA |
| Threshold Current | (5) | | 0.1 | 0.25 | μA |
| Control Voltage Level | $V_{CC} = 15\text{ V}$ | 9 | 10 | 11 | V |
| | $V_{CC} = 5\text{ V}$ | 2.6 | 3.33 | 4 | |
| Pin 7 Leakage Output High | | | 1 | 100 | nA |
| Pin 7 Sat ⁽⁶⁾ | | | | | |
| Output Low | $V_{CC} = 15\text{ V}$, $I_7 = 15\text{ mA}$ | | 180 | | mV |
| Output Low | $V_{CC} = 4.5\text{ V}$, $I_7 = 4.5\text{ mA}$ | | 80 | 200 | mV |
| Output Voltage Drop (Low) | $V_{CC} = 15\text{ V}$ | | | | |
| | $I_{SINK} = 10\text{ mA}$ | | 0.1 | 0.25 | V |
| | $I_{SINK} = 50\text{ mA}$ | | 0.4 | 0.75 | V |
| | $I_{SINK} = 100\text{ mA}$ | | 2 | 2.5 | V |
| | $I_{SINK} = 200\text{ mA}$ | | 2.5 | | V |
| | $V_{CC} = 5\text{ V}$ | | | | |
| | $I_{SINK} = 8\text{ mA}$ | | | | V |
| | $I_{SINK} = 5\text{ mA}$ | | 0.25 | 0.35 | V |

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Recommended Operating Conditions** indicate conditions for which the device is functional, but do not ensure specific performance limits. **Electrical Characteristics** state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the **Recommended Operating Conditions**. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(3) Supply current when output high typically 1 mA less at $V_{CC} = 5\text{ V}$.

(4) Tested at $V_{CC} = 5\text{ V}$ and $V_{CC} = 15\text{ V}$.

(5) This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total ($R_A + R_B$) is $20\text{ M}\Omega$.

(6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Electrical Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ to 15 V , unless otherwise specified)⁽¹⁾⁽²⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|-------|------|-----|------|
| Output Voltage Drop (High) | $I_{SOURCE} = 200\text{ mA}$, $V_{CC} = 15\text{ V}$ | | 12.5 | | V |
| | $I_{SOURCE} = 100\text{ mA}$, $V_{CC} = 15\text{ V}$ | 12.75 | 13.3 | | V |
| | $V_{CC} = 5\text{ V}$ | 2.75 | 3.3 | | V |
| Rise Time of Output | | | 100 | | ns |
| Fall Time of Output | | | 100 | | ns |

6.6 Typical Characteristics

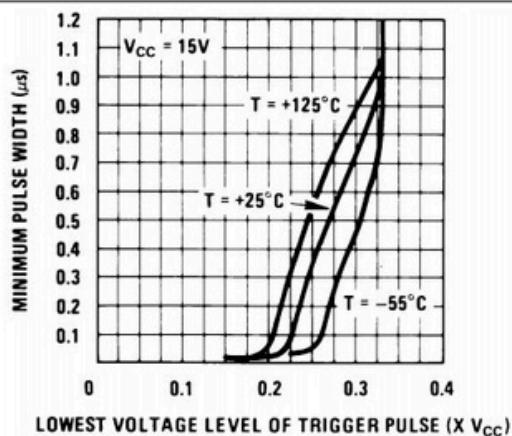


Figure 1. Minimum Pulse Width Required For Triggering

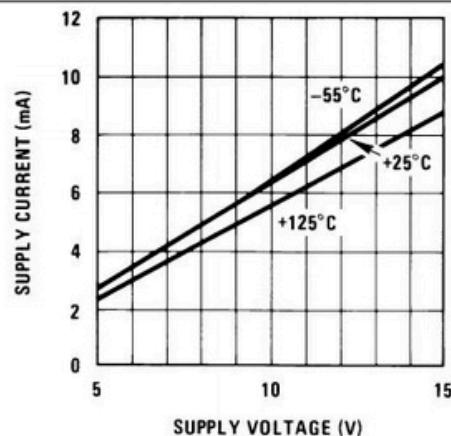


Figure 2. Supply Current vs. Supply Voltage

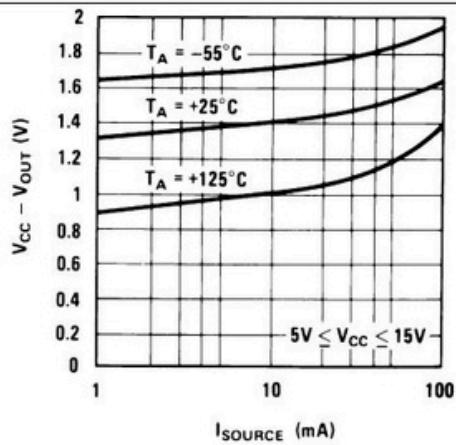


Figure 3. High Output Voltage vs. Output Source Current

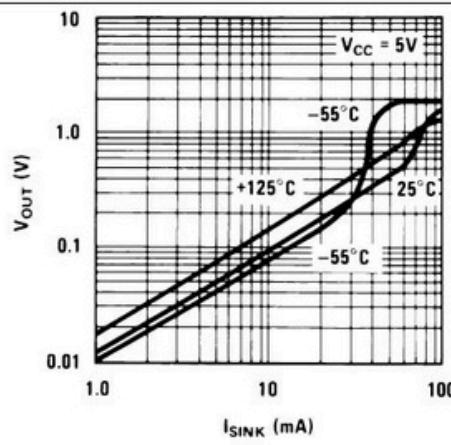


Figure 4. Low Output Voltage vs. Output Sink Current

Typical Characteristics (continued)

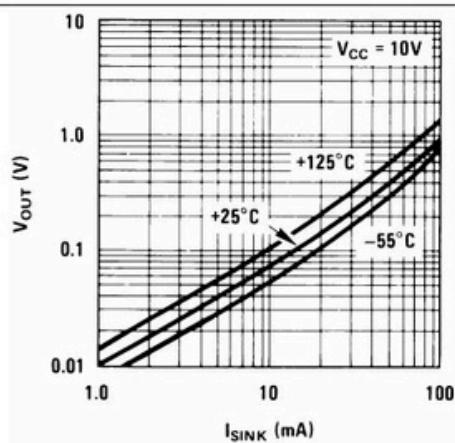


Figure 5. Low Output Voltage vs. Output Sink Current

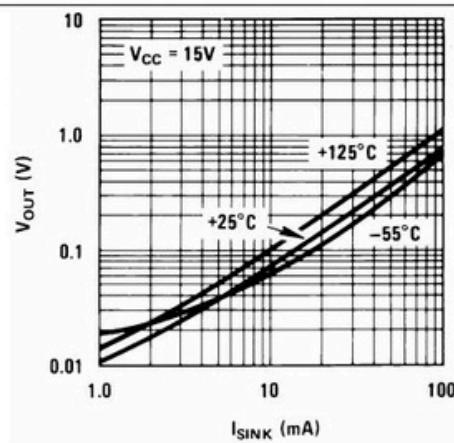


Figure 6. Low Output Voltage vs. Output Sink Current

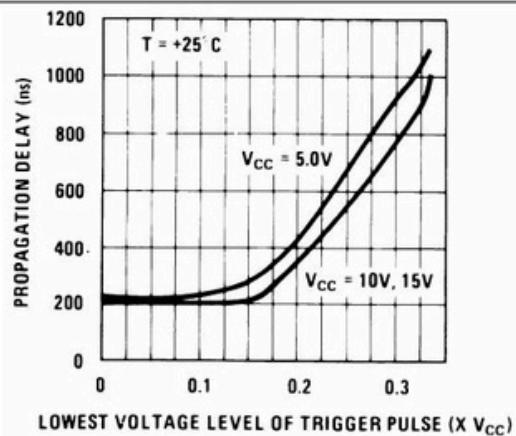


Figure 7. Output Propagation Delay vs. Voltage Level of Trigger Pulse

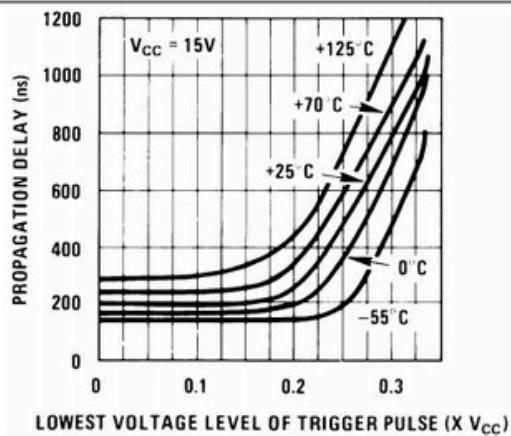


Figure 8. Output Propagation Delay vs. Voltage Level of Trigger Pulse

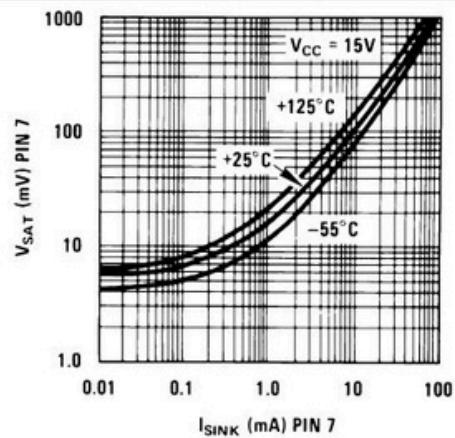


Figure 9. Discharge Transistor (Pin 7) Voltage vs. Sink Current

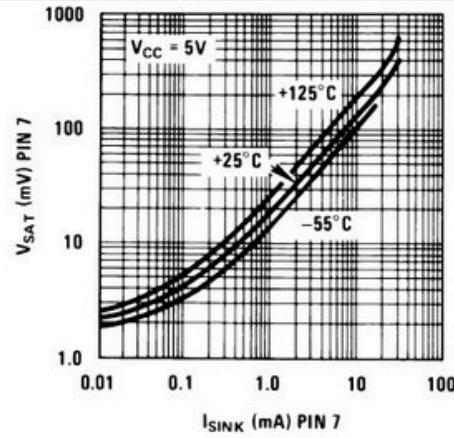


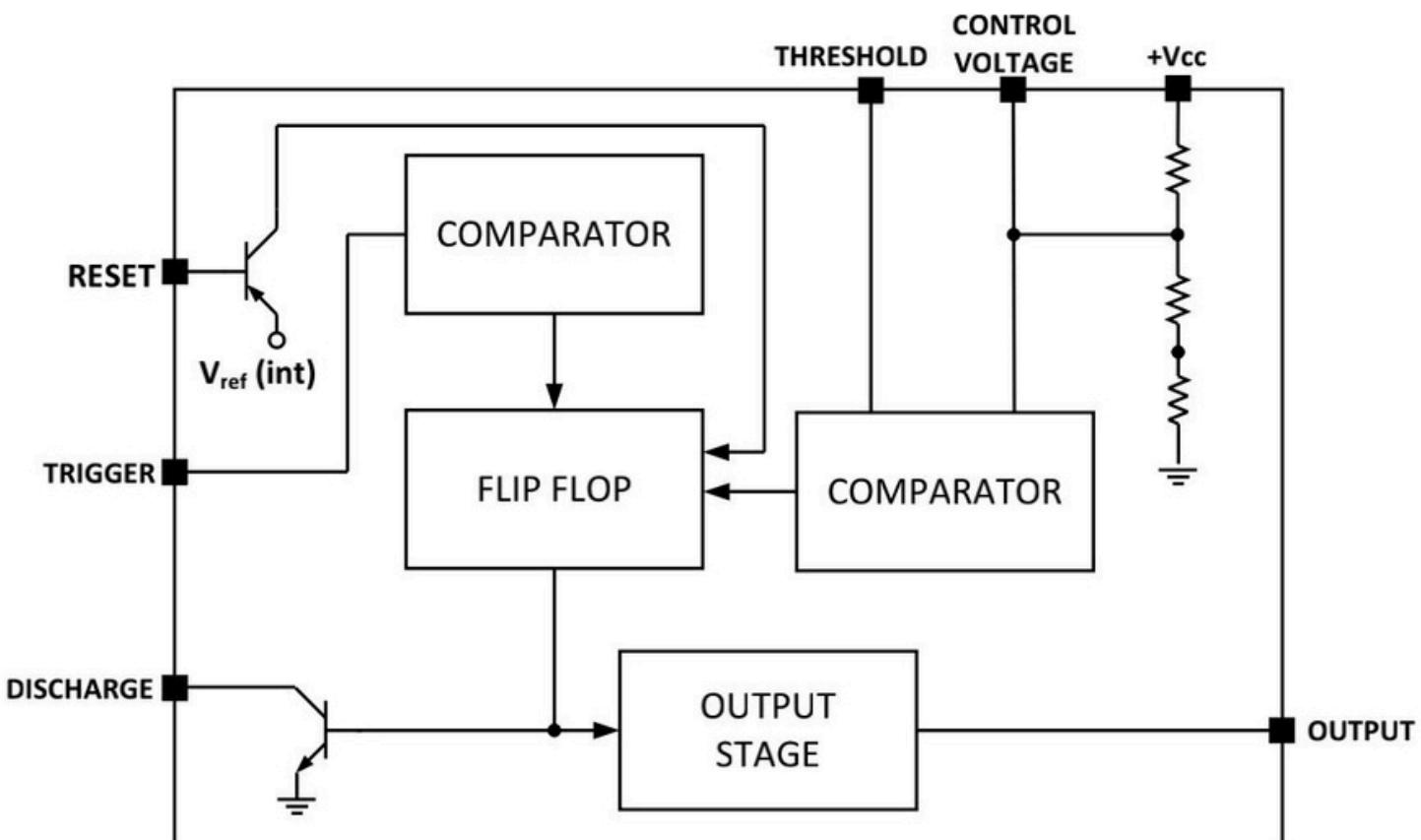
Figure 10. Discharge Transistor (Pin 7) Voltage vs. Sink Current

7 Detailed Description

7.1 Overview

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits. The LM555 are available in 8-pin PDIP, SOIC, and VSSOP packages and is a direct replacement for SE555/NE555.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Direct Replacement for SE555/NE555

The LM555 timer is a direct replacement for SE555 and NE555. It is pin-to-pin compatible so that no schematic or layout changes are necessary. The LM555 come in an 8-pin PDIP, SOIC, and VSSOP package.

7.3.2 Timing From Microseconds Through Hours

The LM555 has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C value used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.3.3 Operates in Both Astable and Monostable Mode

The LM555 can operate in both astable and monostable mode depending on the application requirements.

- **Monostable mode:** The LM555 timer acts as a “one-shot” pulse generator. The pulse begins when the LM555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the

Feature Description (continued)

capacitor equals $2/3$ of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.

- Astable (free-running) mode: The LM555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of R_A , R_B , and C .

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 11). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

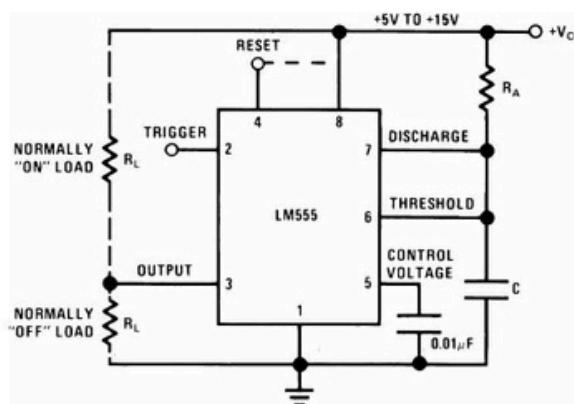


Figure 11. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_A C$, at the end of which time the voltage equals $2/3 V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 12 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC} = 5$ V
TIME = 0.1 ms/DIV.
 $R_A = 9.1$ kΩ
 $C = 0.01$ μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Figure 12. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10 \mu s$ before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, TI recommends connecting the Reset pin to V_{CC} to avoid any possibility of false triggering.

Device Functional Modes (continued)

Figure 13 is a nomograph for easy determination of R, C values for various time delays.

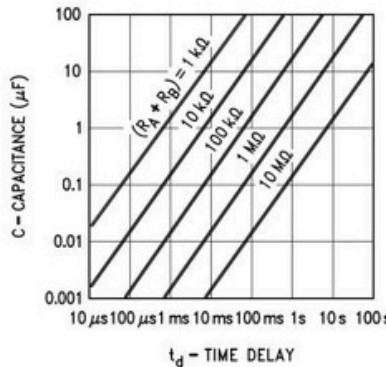


Figure 13. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of these two resistors.

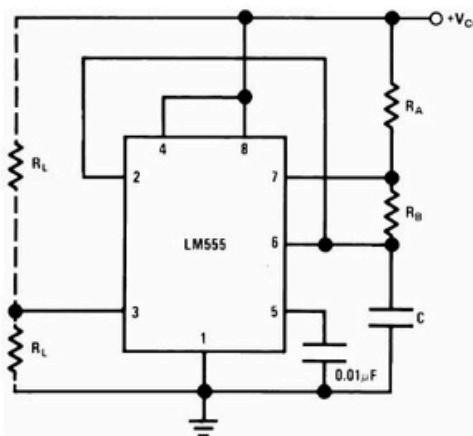


Figure 14. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 15 shows the waveforms generated in this mode of operation.

9 Power Supply Recommendations

The LM555 requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 μ F in parallel with a 1- μ F electrolytic capacitor. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM555. The 0.1- μ F capacitor in parallel with a 1- μ F electrolytic capacitor should be as close as possible to the LM555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01- μ F bypass capacitor for control voltage pin
- C3 – 0.1- μ F bypass ceramic capacitor
- C4 – 1- μ F electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

10.2 Layout Example

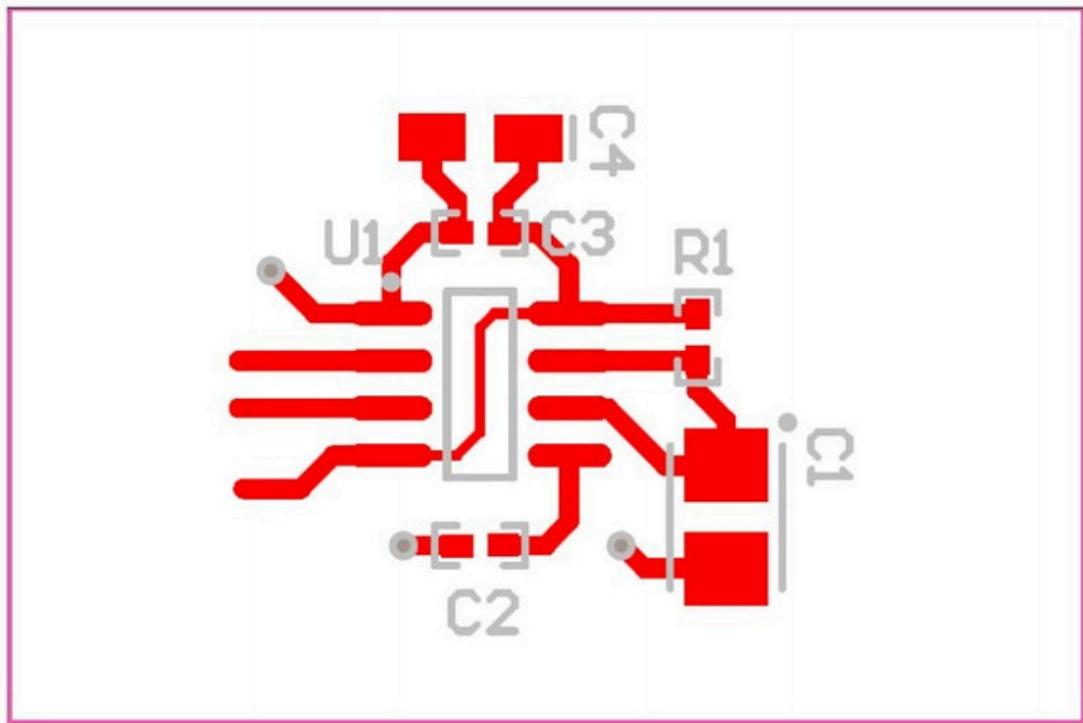


Figure 20. Layout Example

| ckage Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) |
|------------|-----------------|------|-------------|--------------|--------------------------------|--------------------|--------------|
| SOIC | D | 8 | 95 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 |
| VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 |
| VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 |
| SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 |
| PDIP | P | 8 | 40 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | 0 to 70 |

lows:

designs.

be discontinued, and a lifetime-buy period is in effect.

ce is in production to support existing customers, but TI does not recommend using this part in a new design.

ot in production. Samples may or may not be available.

of the device.

ctor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the required materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead

an products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold requirement.

level rating according to the JEDEC industry standard classifications, and peak solder temperature.

s to the logo, the lot trace code information, or the environmental category on the device.

eses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is inden
ent the entire Device Marking for that device.

may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material column width.