CS & IT ENGINEERING

Operating System

Memory Management

DPP 06 (Discussion Notes)

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Q.1 A computer system has a physical address of 128 bits and a page size of 32 KB. Each page table entry contains 4 valid and 2 dirty bits along with the translation bits. If the maximum size of the page table of a process is 60MB. Calculate the size of logical address space supported by the system (in GB)?

[MCQ]

A. 512

B. 32

C. 128

D. 64

$P.A = 128 \text{ bits}$

$P.S = 32 kB \ (15 \text{ bits})$

$P.T.E = 4 + 2 + \text{Frame bits}$

Page Table size $= 60MB$

No. of frames $\Rightarrow \dfrac{2^{128}}{2^{15}} \Rightarrow 2^{113}$

Frame bits $\Rightarrow \log_2 2^{113} \Rightarrow 113 \text{ bits}$

$P.T.E \Rightarrow 4 + 2 + 113$

$\Rightarrow 119 \text{ bits}$

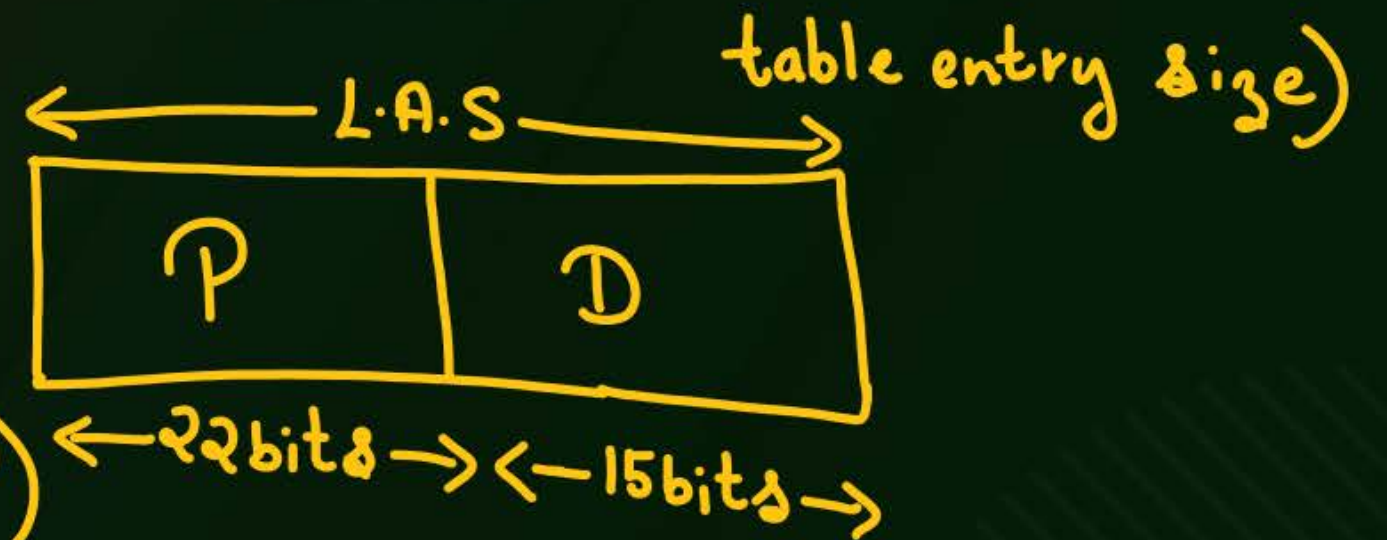$\Rightarrow \left(\dfrac{119}{8}\right) \text{Bytes}$

$$\left\lceil \frac{119}{8} \right\rceil \Rightarrow \left\lceil 14.875 \right\rceil \Rightarrow 15 \text{ Bytes}$$

Page Table size $\Rightarrow$ No. of pages (Page Table enteries) $*$ P.T.E (page table entry size)
$$[P]$$

$$60 \text{MB} \Rightarrow P * 15 \text{B}$$

$$P \Rightarrow \frac{\overset{4}{60\text{MB}}}{\cancel{15}\cancel{B}} \Rightarrow 4\text{M} \left(2^2 * 2^{20} \right)$$

$$L.A = 4\text{M} * 32\text{kB} \Rightarrow 128 * 2^{30} \text{B} \Rightarrow 128\text{GB}$$

L.A.S

P	D

$\leftarrow$ 22bits $\rightarrow$ $\leftarrow$ 15bits $\rightarrow$

Q.2 Consider a system with 512 KB page size and each page table entry requires 8 bytes. The level of paging required to map a 30bit logical address if every page table fits into a single page are

$$\text{Given:-} \quad P.S = 512\,KB \left(2^{9} * 2^{10}B = 2^{19}B \right)$$

$$P.T.E = 8\,Bytes \left(2^{3}B \right)$$

$$L.A.S = 30\,bits$$

$$\boxed{1K = 1024}$$

$$\textcircled{1}$$

$$I^{st} \text{ Level Page Table :}$$

1. No. of pages $\Rightarrow \dfrac{2^{30}}{2^{19}} \Rightarrow 2^{11} \; (2k)$

2. Page Table Size $\Rightarrow$ No. of pages $*$ P.T.E

Page Table Size $\Rightarrow 2^{11} * 2^3$ Bytes

$\Rightarrow 2^{14}$ Bytes $(16\,KB)$

$$\left(\begin{array}{c} 16KB \\ I^{st} \text{ level page} \\ \text{table} \end{array} \right) < \left(\begin{array}{c} 512\,KB \\ \text{Page Size (P.S)} \end{array} \right)$$

Q.3

A computer system implements a 36 bits virtual address. Page size to 64KB and the size of physical memory is 34 bits. The approximate size of page table in the system is _____3_____ MB.

[Assume memory is byte addressable]

[NAT]

Given:- $L.A.S = 36\ bits$

$P.S = 64KB\ (2^{16}\ B)$

$P.A.S = 34\ bits$

No. of pages $\Rightarrow \dfrac{L.A}{P.S}$

$\Rightarrow \dfrac{2^{36}}{2^{16}} \Rightarrow 2^{20} = 1M$

No. of frames $\Rightarrow \dfrac{P.A}{P.S}$

$$\text{No. of frames} \Rightarrow \frac{2^{34}}{2^{16}} \Rightarrow 2^{18} \Rightarrow 256K$$

$$\log_2 2^{18} \text{ bits} = 18 \text{ bits}$$

$$\text{P.T.E} \Rightarrow \left\lceil \frac{18}{8} \right\rceil \Rightarrow \lceil 2.2 \rceil = 3 \text{ Bytes}$$

Page Table Size = No. of pages * P.T.E Size

$$\Rightarrow \quad 2^{20} \ * \ 3 \, Bytes$$

$$\Rightarrow \quad 3 * 2^{20} \, Bytes$$

$$\Rightarrow \quad 3 MBytes$$

Q.4

If page size is 4096 Bytes, in a paging system. A process needs 20 frames. What is the maximum possible internal fragmentation size_____.
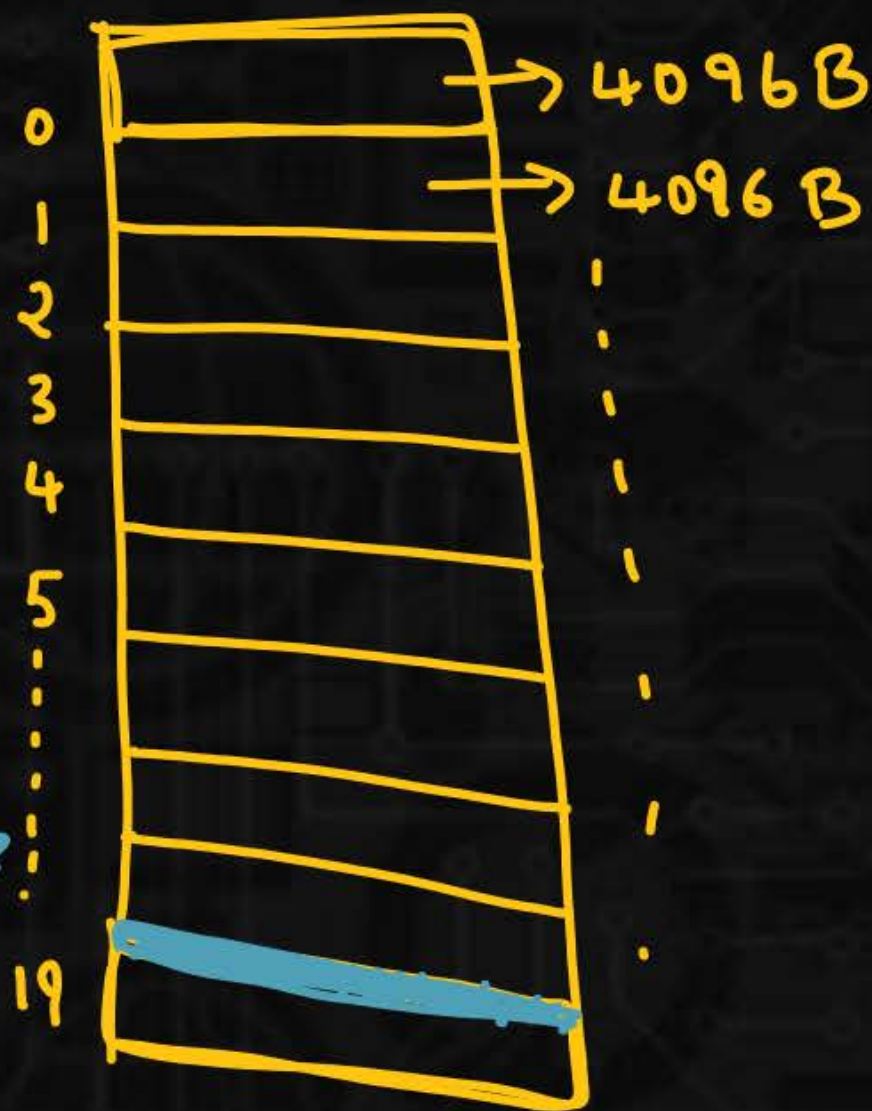
[MCQ]

A. 4096 byts

B. 4095 Bytes

C. 2048 Bytes

D. No internal fragmentation

Given: Page size = 4096 Bytes

Process requires = 20 frame

$19^* 4096 \text{ Bytes} + 1B$

$4096 \text{ Bytes} - 1 \text{ Byte}$

$\Rightarrow 4095 \text{ Bytes}$

0 → 4096 B

1 → 4096 B

2

3

4

5

19

Q.5

Consider a virtual address space of eight pages of 2048 words each mapped onto a physical memory of 32 frames. How many bits are there in the logical address.
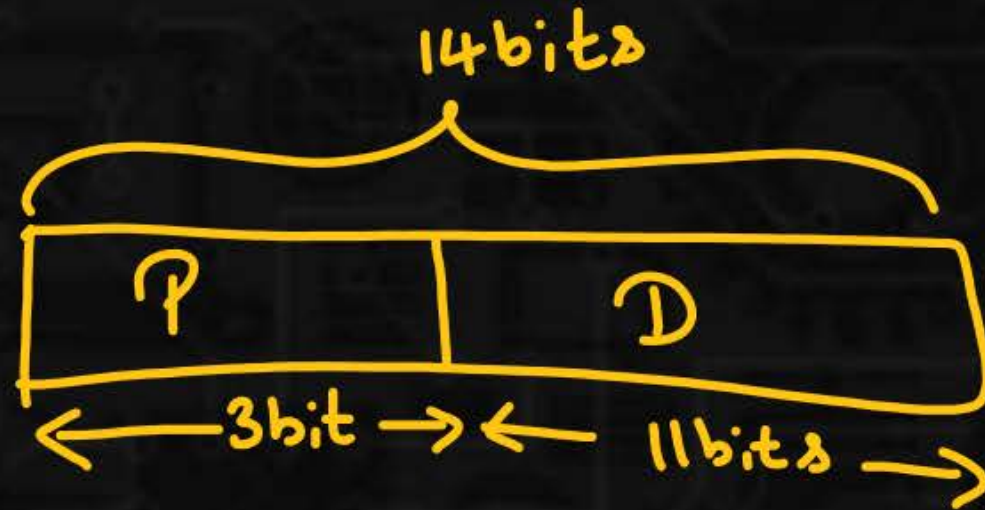
[MCQ]

A. 13

B. 14

C. 10

D. 11

14 bits

P	D

← 3 bit → ← 11 bits →

$8 \text{ pages} \Rightarrow 2^3 \text{ pages}$

$\text{Size of each page} = 2048$

$\log_2 2048 \Rightarrow \log_2 2^{11} \Rightarrow 11 \text{ bits}$

Q.6 Consider a virtual memory system with physical memory of 8GB. A page size of 8KB and 46-bit virtual address. Assume every page table exactly fits into a single page. If page table entry size is 4 bytes the how many levels of page tables would be required?

[NAT]

Given:-

$P.A = 8GB = 2^{33}$ Bytes

$P.S = 8KB = 2^{13}$ Bytes

$V.A = 46 bits$

$P.T.E = 4 Bytes$

I^{st} Level Page Table: **(3)**

No. of pages $\Rightarrow \dfrac{2^{46}}{2^{13}} = 2^{33}$ pages

$P.T.S_1 \Rightarrow 2^{33} * P.T.E$

$\Rightarrow 2^{33} * 4 Bytes$

$\Rightarrow 2^{35} B = 2^5 * 2^{30} B$

$\Rightarrow 32 GB$

IInd level Page Table :-

No. of pages $\Rightarrow \dfrac{2^{35}}{2^{13}} \Rightarrow 2^{22}$ pages

P.T.S$_2$ $\Rightarrow 2^{22} *$ P.T.E

$\Rightarrow 2^{22} * 4$ Bytes

$\Rightarrow 2^{24}$ B $= 2^4 * 2^{20}$ Bytes

$= \underline{16 MB}$

IIIrd level page Table :-

No. of pages $= \dfrac{2^{24}}{2^{13}} = 2^{11}$

P.T.S$_3$ $\Rightarrow 2^{11} *$ P.T.E

$\Rightarrow 2^{11} * 4$ Bytes

$\Rightarrow 2^{13}$ Bytes.

$\Rightarrow \underline{8 kB}$

Q.7 Consider the following statements:

I. Overlays are used to increase the size of physical memory. *False*

II. The size of virtual memory depends on the size of main memory. *False.*

III. Aging is used to keep track of number of times a page is referenced. *False*

How many of the above are correct statements?

[NAT]

0

A processor can support a maximum memory of 8 GB, where the memory is word addressable (each word consists 4 bytes). The size of address bus of the process is at least __31__ bits.

[NAT]

Memory Size $\Rightarrow$ 8 GB

$$\log_2 2^{31} \Rightarrow 31 \text{ bits}$$

1 word = 4 Bytes

$$8 GB \Rightarrow 2G * \underline{4B} (1 \text{ word})$$

$$\Rightarrow 2^{31} * 2^2 B$$

Q.9 Which of the following statement is/are correct regarding paging?

[MSQ]

A,C

A. Paging helps solve the issue external fragmentation *True.*

B. Page size has <u>no</u> impact on internal fragmentation *False*

C. Paging incurs memory overheads. *True.*

D. Multi-level paging is necessary to support pages of different sizes. *False.*

Q.10 What is basic objective of hierarchical paging?

Multilevel paging

[MCQ]

A. Reduce Internal fragmentation.

B. Reduce External fragmentation.

C. To reduce context -switch overhead. ✗

D. Reduce page table size overhead in memory. ✓