CS & IT ENGINEERING

Operating Systems

Memory Management

Lecture No. 8

By- Dr. Khaleel Khan Sir

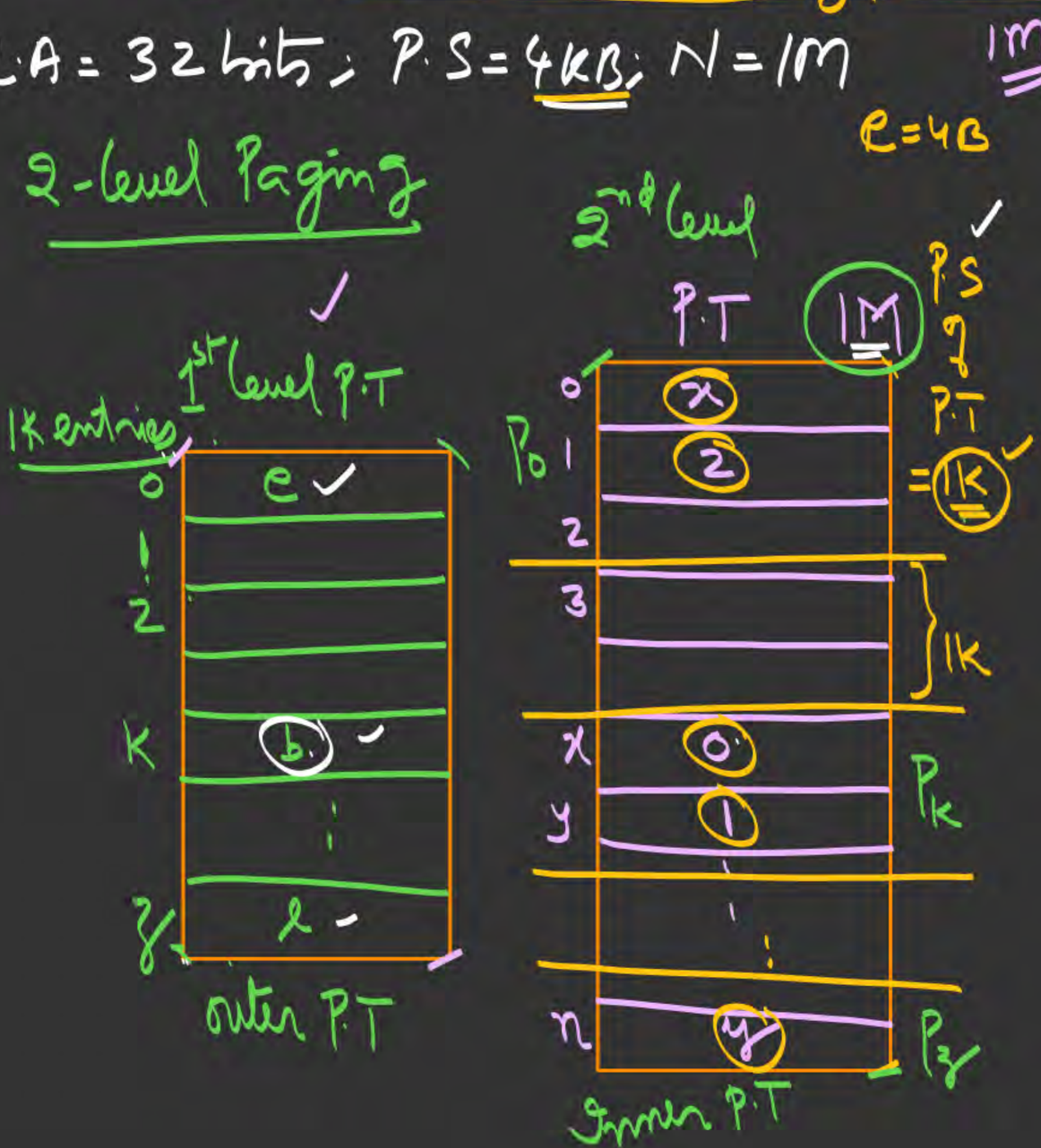
- Multi-Level Paging
- Segmentation
- Problem Solving

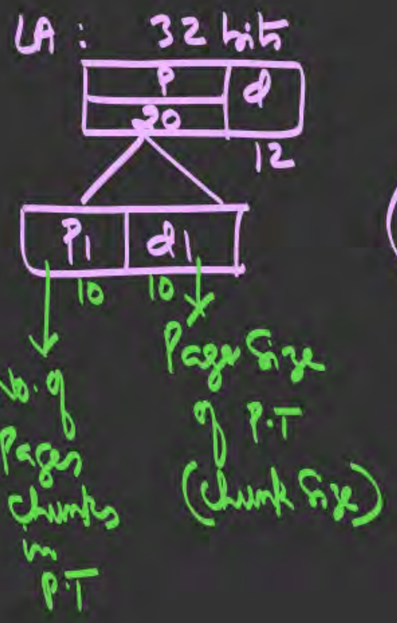
1K + 3K = 4K

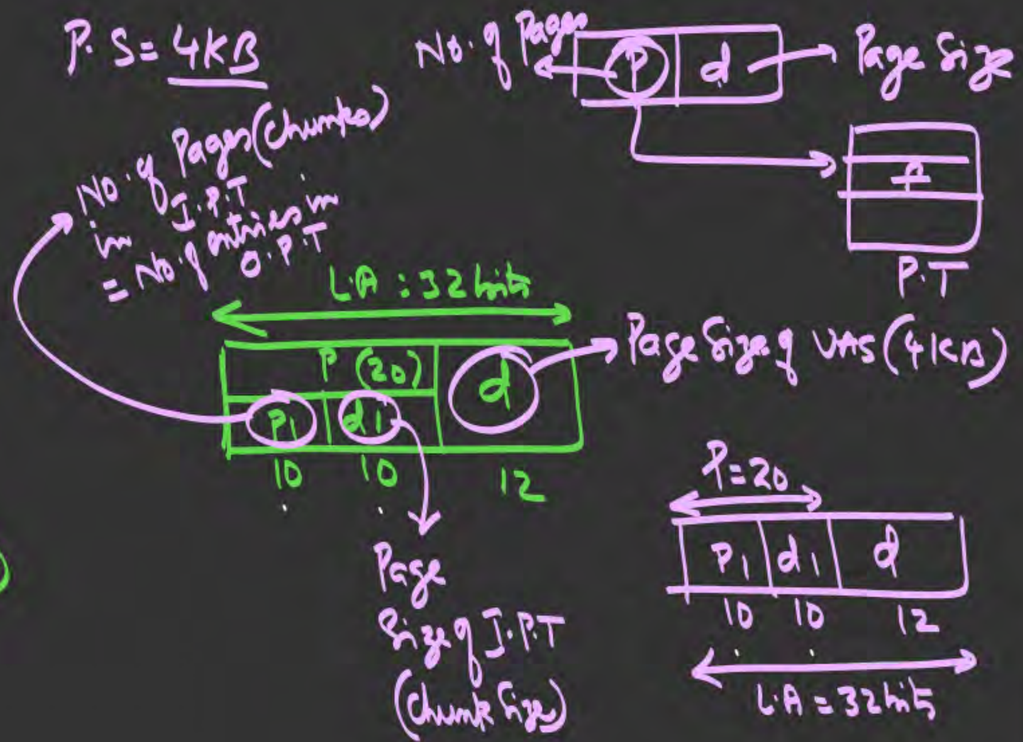
Multi-Level Paging / Hierarchical Paging / Tree-level

LA = 32 bits; PS = 4KB; N = 1M

2-level Paging

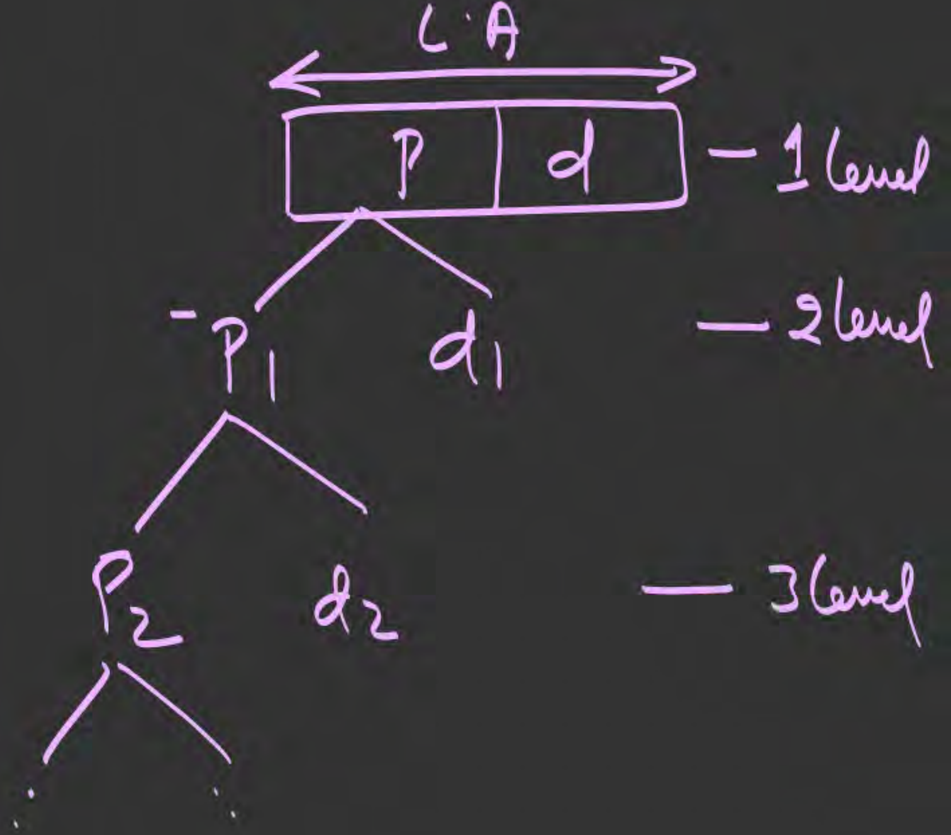



LA : 32 bits
p
d
20
12
p1
d1
10
10
No. of Pages chunks in P.T
Page Size of P.T (chunk size)


P.S = 4KB
No. of Pages (chunks) in I.P.T = No. of entries in O.P.T
LA : 32 bits
p (20)
d
p1
d1
10
10
12
Page Size of UMS (4KB)
Page Size of I.P.T (chunk size)

No. of Pages
p
d
Page Size
P.T

P=20
p1
d1
d
10
10
12
LA = 32 bits

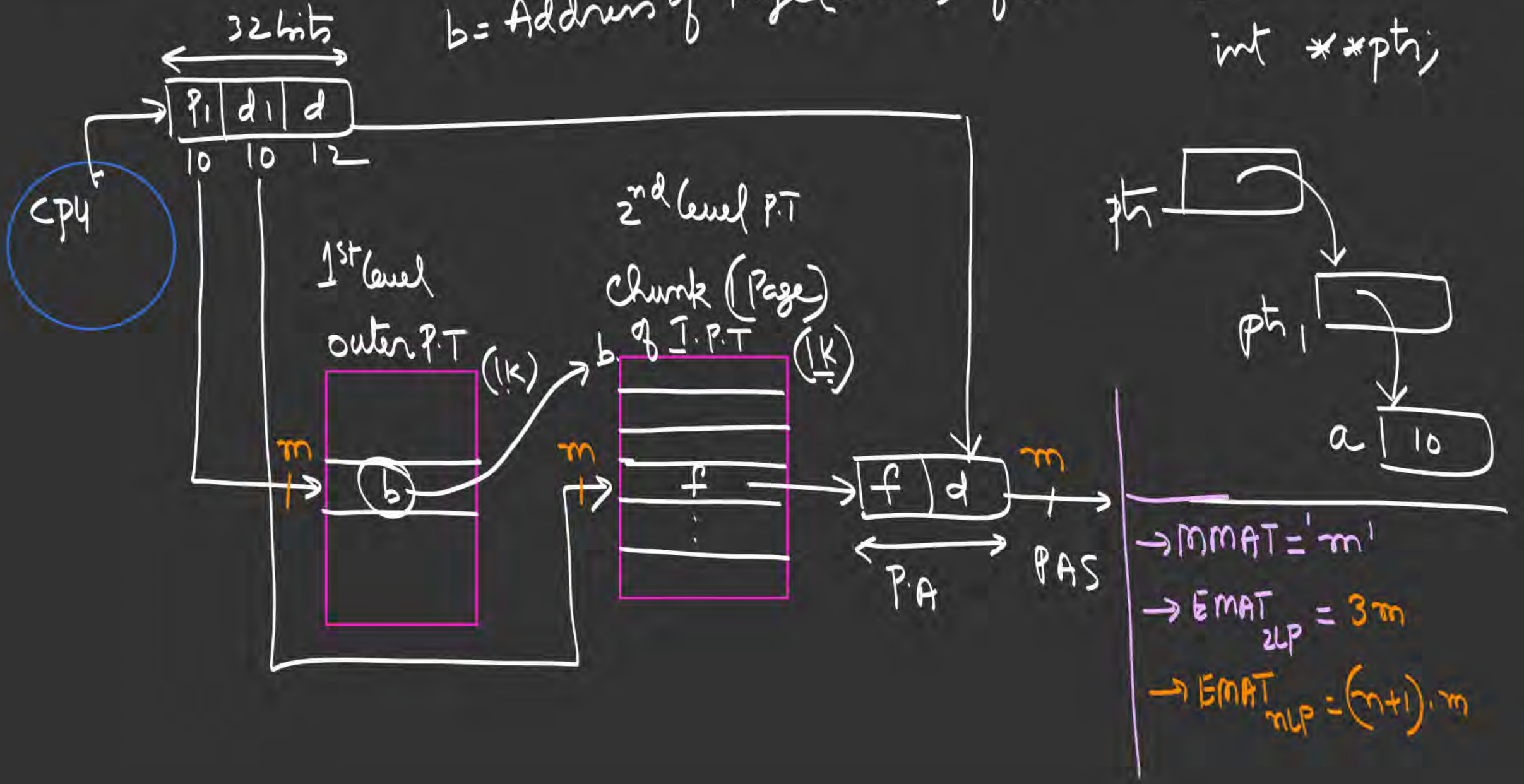

L.A
p
d
— 1 level
p1
d1
— 2 level
p2
d2
— 3 level

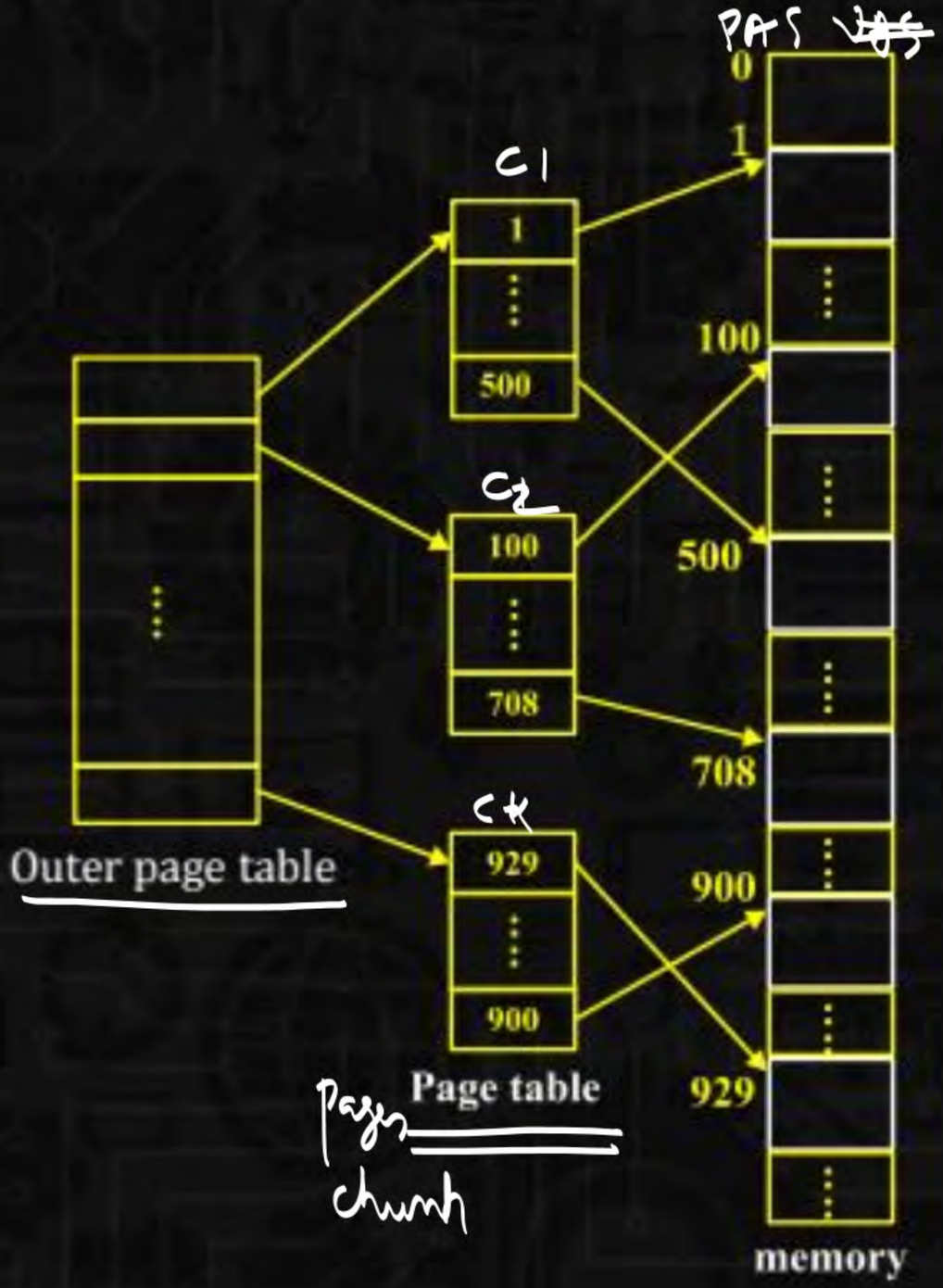
L.A: 32 bits; P.S = 4KB;

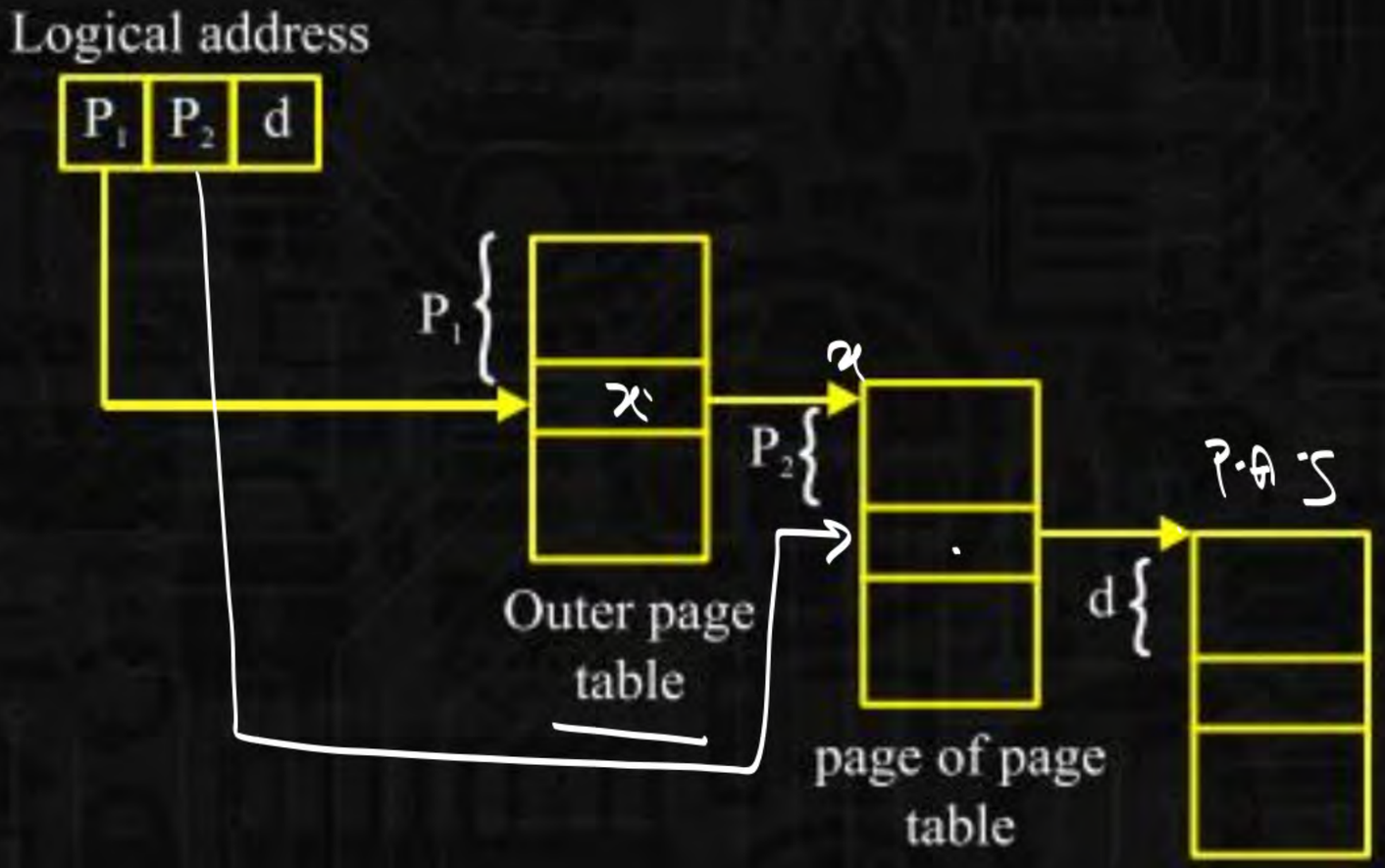
b = Address of Page (Chunk) of I.P.T

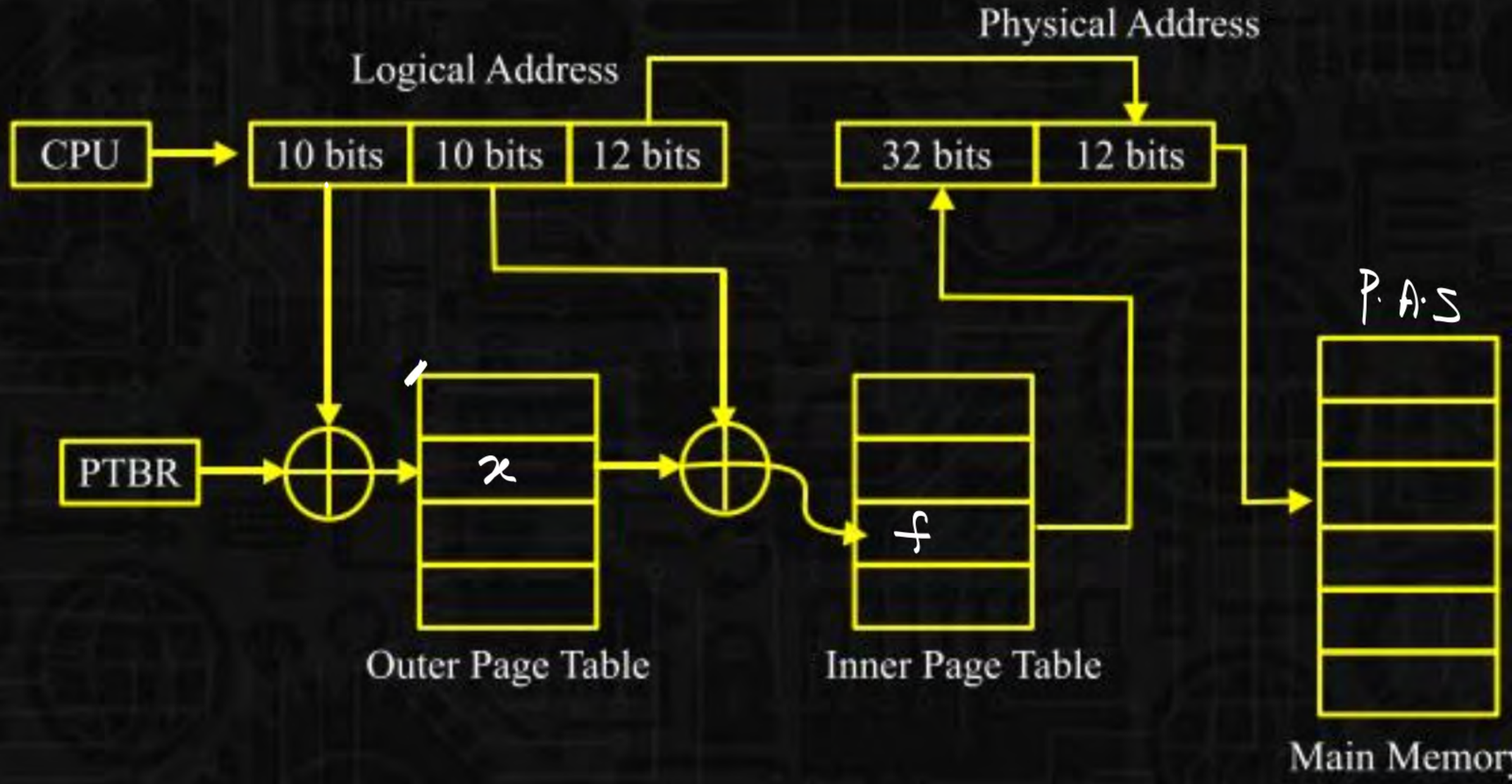
Perf:

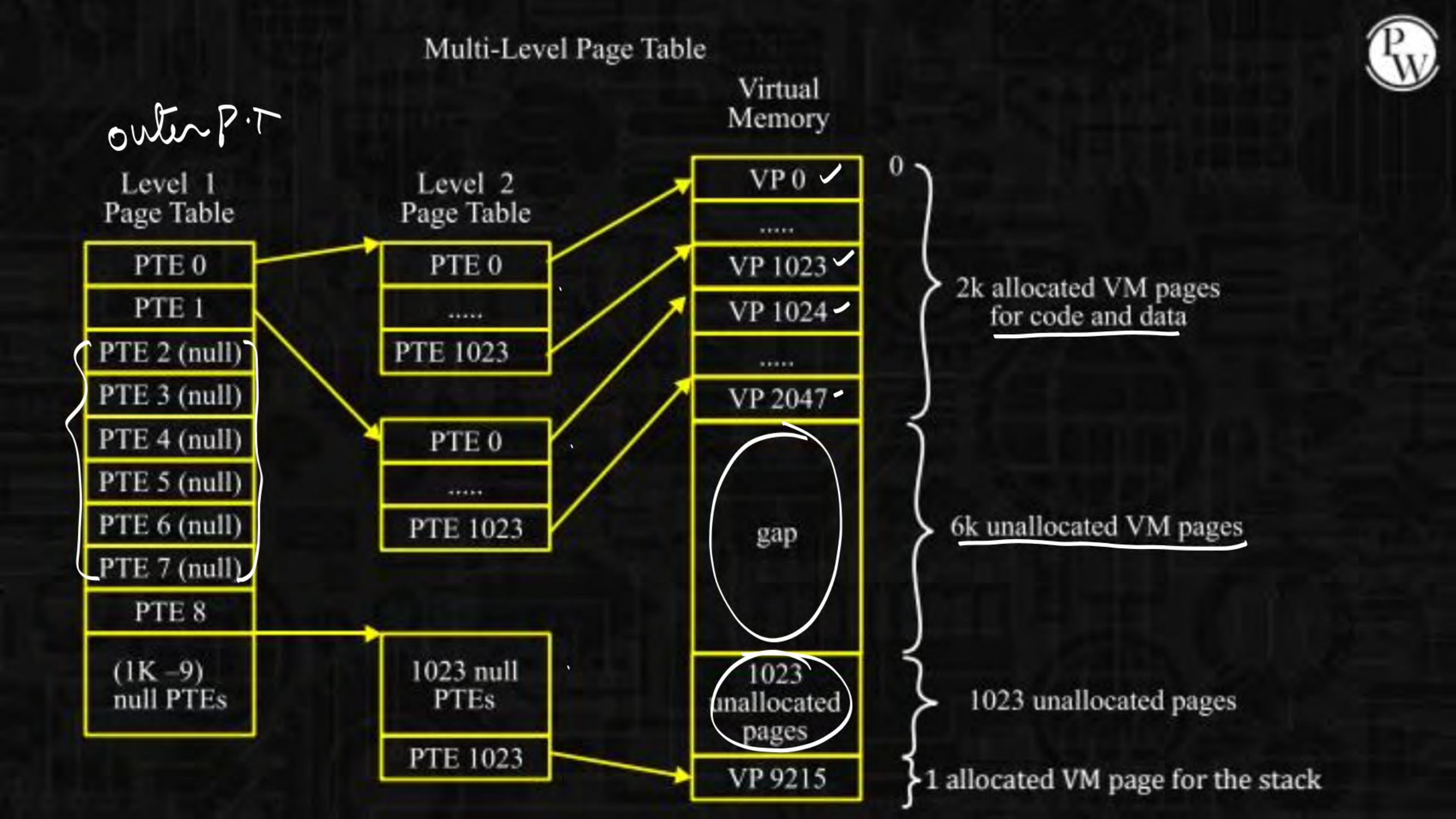
int **pth;



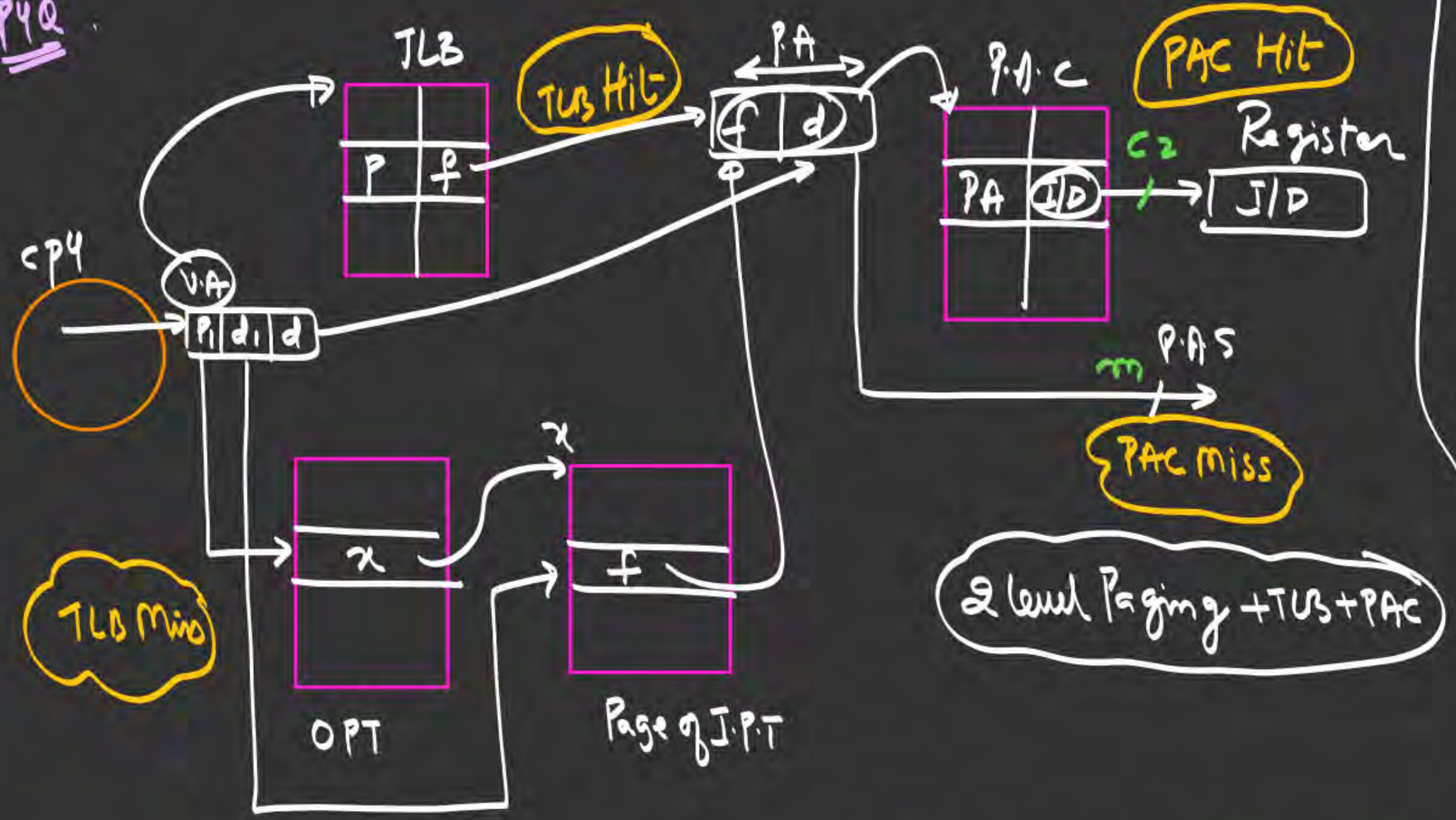

PAS
0
1
100
500
708
900
929
memory
C1
1
500
C2
100
708
Ck
929
900
Outer page table
Page table
Pages
chunk


Logical address
P1
P2
d
Outer page table
page of page table
P.A.S


Physical Address
Logical Address
CPU
10 bits
10 bits
12 bits
32 bits
12 bits
P.A.S
PTBR
x
f
Outer Page Table
Inner Page Table
Main Memory


Multi-Level Page Table
outer P.T
Level 1
Page Table
Level 2
Page Table
Virtual
Memory
PTE 0
PTE 1
PTE 2 (null)
PTE 3 (null)
PTE 4 (null)
PTE 5 (null)
PTE 6 (null)
PTE 7 (null)
PTE 8
(1K –9)
null PTEs
PTE 0
.....
PTE 1023
PTE 0
.....
PTE 1023
1023 null
PTEs
PTE 1023
VP 0
.....
VP 1023
VP 1024
.....
VP 2047
gap
1023
unallocated
pages
VP 9215
0
2k allocated VM pages
for code and data
6k unallocated VM pages
1023 unallocated pages
1 allocated VM page for the stack

P4Q



→ MMAT = m

→ TLB AT = c_1

→ TLB Hit ratio = x_1

→ PAC AT = c_2

→ PAC Hit ratio = x_2

$$EMAT_{2LP} = x_1\left[c_1 + x_2c_2 + (1-x_2)(c_2+m)\right] + (1-x_1)\left[c_1 + \underline{m+m} + x_2c_2 + (1-x_2)(c_2+m)\right]$$

Q. In the context of operating systems, which of the following statements is/are correct with respect to paging?

MSQ

A. Page size has no impact on internal fragmentation.

B. Paging helps solve the issue of external fragmentation.

C. Paging incurs memory overheads (Space (PT's))

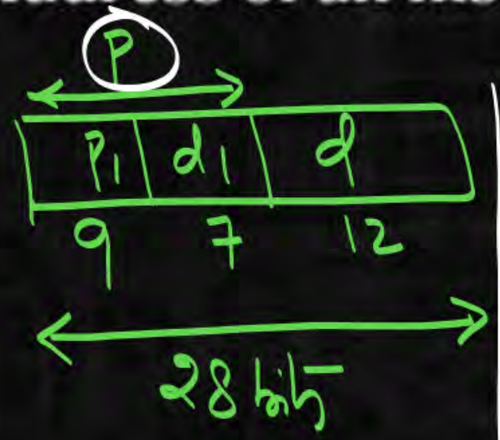
D. Multi-level paging is necessary to support pages of different sizes

(B & C)

Q. Consider a System using 2 Level Paging Architecture. The Top level 9 bits of the Virtual Address are used to index into the outer Page Table. The next 7 bits of the Address are used to index into next level Page Table. If the size of Virtual Address is 28 bits. Then

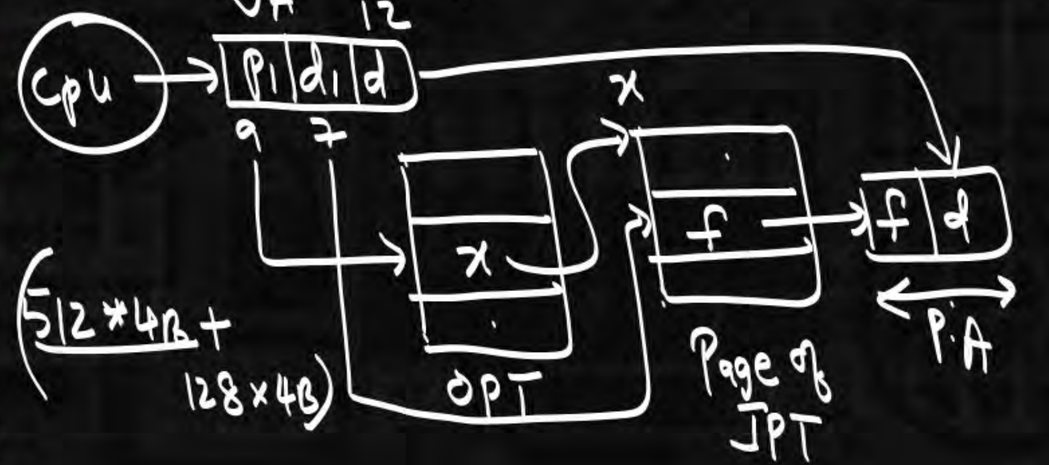
(i) How large are the Pages and How many are there in Virtual Address Space?

(ii) If P.T.E at both levels is 32 bits in size then what is the Space Overhead needed to translate Virtual Address to Physical Address of an Instruction or Data Unit?



(2KB + 512B)
(2.5KB)

d ~ P.S of VAS = 2^{12} = 4KB

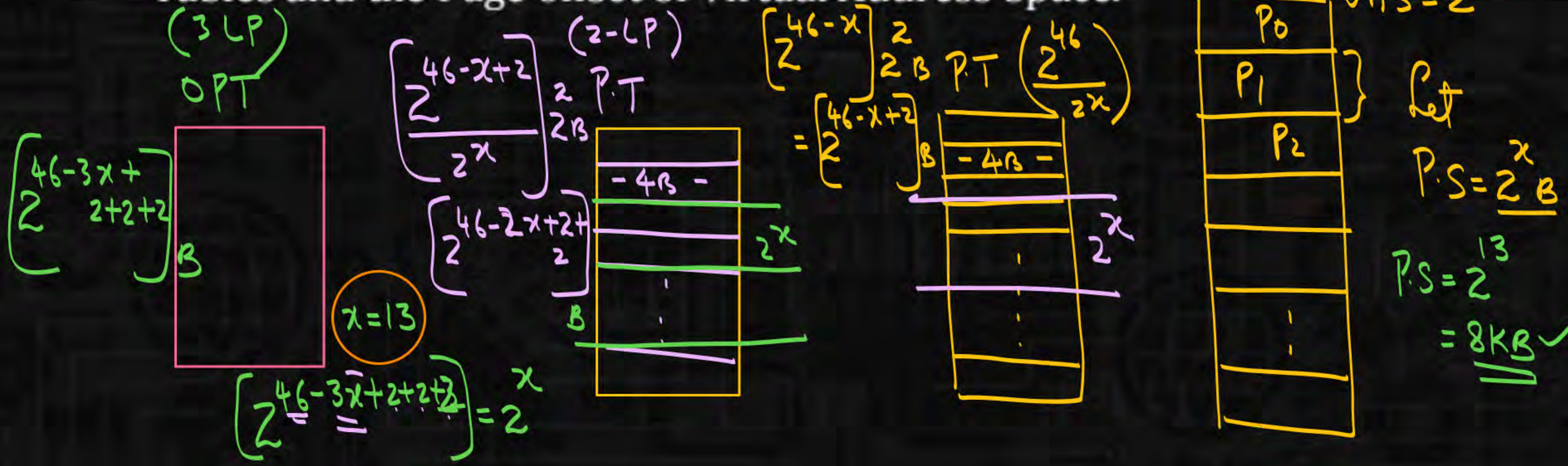


P ~ No. of Pages in VAS

$N = 2^{16} = 64K$

Q. *

Consider a Computer System using 3 Level Paging Architecture with a uniform Page Size at all levels of Paging. The size of Virtual Address is 46 bits. Page Table Entries at all levels of Paging is 32 bits. What must be the Page Size in Bytes such that the Outer Page Table exactly fits in one frame of Memory. Assume Page Size is power of 2 in Bytes. Show the Virtual Address format indicating the number of bits required to access all the three levels of Page Tables and the Page offset of Virtual Address Space.



Let VAS $= 2^S$ Bytes VA $= S$ bits

PS $= 2^x$ Bytes

PTE $= 2^c$ Bytes

No. of levels of Paging $= 'l'$

Size of outer P.T $= 2^{S-lx+lc}$ Bytes

$= \left(\frac{2^S}{2^x}\right) \cdot 2^c = \left[2^{S-x+c}\right]$

VA = 46 bits

PTE = 4 Bytes

PS $= 2^x$ By

$l = 3$ $\rightarrow$ $2^{13} = 8$KB

$OPT = 2^x$

LA = 46 bits

P_1	P_2	P_3	d
y	y	y	x

$\left(2^y\right)$ 4B

$3y + x = 46$ — (1)

$OPT = \left(2^y\right)$ 4B

$x = y + 2$ — (2)

$x = 13$

$= 2^{y+2}$ By $= 2^x$ By

$3y + y + 2 = 46$

$4y = 44$

$\therefore y = 11$

Q

Consider a Computer System with 57 bit Virtual Addressing, Using Multi-Level Tree Structured Page Tables with L Levels for Virtual to Physical Address Translation. Page size is 4KB and Page Table Entry is of 8 Bytes at all levels.

The value of L is _____.

GATE 2023

VA = 57 bits

No. of Levels = 'L'

P.S = 4KB ✓

PTE = 8B

No. of entries that Can be Stored in one Page $= \frac{4KB}{8B} = \frac{2^{12}}{2^3} = 2^9 = 512$

$$OPT = \left\lceil \frac{57 - L \cdot 12 + L \cdot 3}{2} \right\rceil By$$

$$= \left\lceil \frac{57 - 12L + 3L}{2} \right\rceil = 2^{12} B$$

$$57 - 9L = 12$$

$$L = 5$$ ✓

OPT = 1 Page/Frame

OPT = 4KB

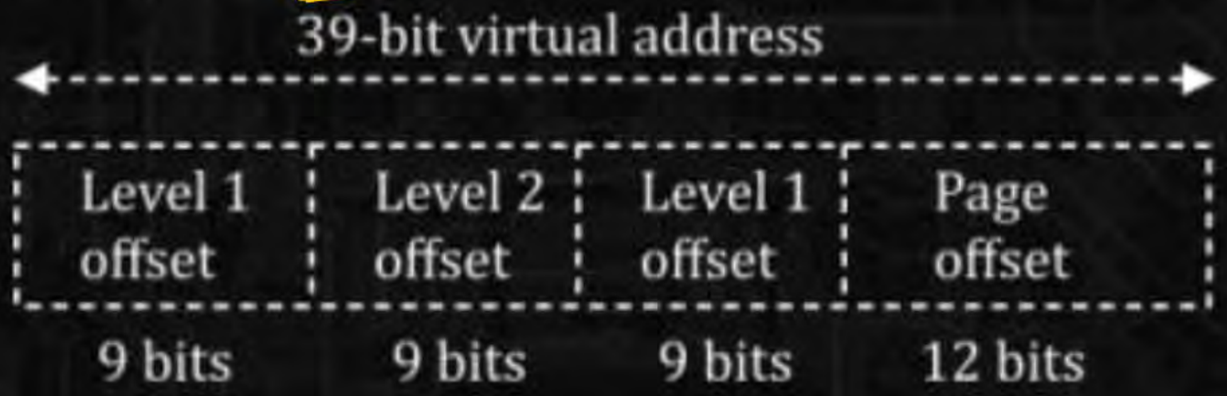
2^{12}

VA: 57 bits ✓

9. L = 45

$L = \frac{45}{9} = 5$

Q. Consider a three-level page table to translate a 39-bit virtual address to a physical address as shown below.



$2^{GB} = 31$ bit

The page size is 4KB (1KB = 2^{10} bytes) and page table entry size at every level is 8 bytes. A process P is currently using 2GB (1GB = 2^{30} bytes) virtual memory which is mapped to 2 GB of physical memory, The minimum amount of memory required for the page table of P across all levels is____ KB.

(OPT + 2nd level PT + 3rd level P.T)

4 = 100

00100

0100

V.A.S = 64 KB

Text = S_1 B

Data = S_2 B

Stack = S_3 B

P.S = ? 2^x

$VAS = \left(2^{16-x}\right)$

Text :-

Data =

Stack =

Ans: 512 B

Hint: <Internal Frag.>


THANK YOU GW
SOLDIERS !