Assignment VII

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I. Introduction

In this assignment, we have build-up a code generator which takes 3-address code as input and produces target code as per RISC V. In the RISC architecture, the size of ISA is small enough and complex arithmetic/logical operations are not included in this, hence, in our code generator we have implemented the algorithm which can generate codes for these missing operations. Furthermore our task was to count the usage of individual registers inside the basic block and print it. For each basic block, we have sorted the registers in non-increasing order and printed them. Also we have found out and printed any false dependency that can be solved by register renaming.

II. Implementation

A. Important Points

- The entire code works in two pass.
- In first pass, we collect the information about the basic blocks which has a goto associated with it.
- In second pass, we convert it into actual three code including the labels colected in first pass.

B. Structure Used

- Array of Strings: Contains information about the labels.
- Counter for keeping track of registers.

III. Code Analysis

NOTE: We have assumed that we are having infinite number of registers.

A. Robustness

The code is robust in nature, changing the input following the format will not produce unexpected results. It will be able to handle them.

B. Correctness

The generation of three address codes follows the RISC V architecture and always follows it's standards.

IV. COMPLETE ANALYSIS

Now we have completed all stages of compiling a program.

A. Lexical Analysis

B. Syntax Analysis

C. Semantic Analysis

D. Code Generation Phase