Pixel Front End Driver Supervisor

Version: 3.0
Date: Thu, 11 Jan 2007 14:14:53 GMT

Halted

Finite State Machine

Current State Halted	FED Address Map Filename FED Configuration Filename			
Configure	Halt	Pause	Resume	Start

Low Level Commands

Reload Firmware

ReloadFirmware

Channel Offset

Channel	Capacitor Adjust	Input Offset	Output Offset	Offset DAC
1	0	0	0	

ChannelOffsets

Control and Mode Registers

Control Registers

Transparent Mode (•) Disable ( ) Enable
Transparent Gate Start by ( ) L1A (•) VME or EFT (OPTO Module)
Use simulated test-DAC (•) Disable ( ) Enable
Event number generated by ( ) TTC (•) VME
L1A triggers from TTCrx (•) Disable ( ) Enable
EFT Signals from the OPTO Module (•) Disable ( ) Enable
TTSReady (•) Disable ( ) Enable
TTSError (•) Disable ( ) Enable
OUTofSYN (•) Disable ( ) Enable

Mode Registers

S-Link ( ) Disable (•) Enable
Write Spy Memory ( ) Disable (•) Enable
S-Link (•) Let it be, or ( ) Reset

SetControlRegister

Reading FIFO

Read

- Spy FIFO 1 ○
- Spy FIFO 2 Normal Mode ○
- Spy FIFO 3 Normal Mode ◉

Ship Spy FIFO data to

- Screen ◉
- RUBuilder ○
- File ○

ReadFIFO

Enable FIFO 3

EnableFIFO3

Clock Phases and Delays

Channel 1 Phase 0 Delay 0 SetPhasesDelays