XDAQ

PixelSupervisorGUI

Version: 3.0
Date: Mon, 14 Aug 2006 23:55:08 GMT

Halted

Finite State Machine

- (•) Manual
  - Configuration file for the FED [ ] [Browse...]
  - Transparent Mode (•) Disable ( ) Enable
  - Transparent Gate Start by ( ) L1A (•) VME or EFT (OPTO Module)
  - Use simulated test-DAC (•) Disable ( ) Enable
  - Event number generated by ( ) TTC (•) VME
  - L1A triggers from TTCrx (•) Disable ( ) Enable
  - EFT Signals from the OPTO Module (•) Disable ( ) Enable
  - TTSReady (•) Disable ( ) Enable
  - TTSError (•) Disable ( ) Enable
  - OUTofSYN (•) Disable ( ) Enable
  - S-Link ( ) Disable (•) Enable
  - Write Spy Memory ( ) Disable (•) Enable
  - S-Link (•) Let it be, or ( ) Reset
  - Use Spy FIFO 1 ( ), 2 ( ), or 3 (•)
  - Ship Spy FIFO data to (•) RUBuilder, ( ) File, or ( ) Screen
    RUBuilder
- ( ) Calibration
- ( ) Physics

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Configure	Halt	Initialise	Pause	Resume	Start