Assignment No. 1

CS666: Hardware Security for Internet of Things

1 Questions

1. Design a Verilog module for the 1-bit full adder that should have three inputs: A, B, and Cin (carry-in), and two outputs: Sum and Cout (carry-out). Now, using instanciation of the 1-bit full adder module, design a 8-bit full adder that should have three inputs: A (8-bit input), B (8-bit input), and Cin (1-bit carry-in), and two outputs: Sum (8-bit output) and Cout (1-bit carry-out).

2. Write a Verilog module for 4-bit multiplication? The module should have two 4-bit inputs, A and B, and produce an 8-bit product, P. The computational workflow is shown in Figure 1. Firstly, generate a partial product matrix with dimensions of 4x8. Then, compress the matrix to a 2x8 matrix using a 1-bit full adder module that was designed earlier. Finally, generate the final result using an 8-bit adder module that was also designed earlier.

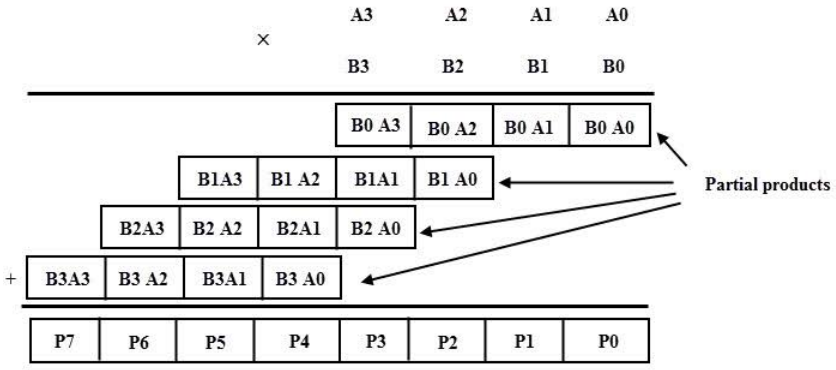

Figure 1: Computation workflow of 4-bit multiplication

3. Write a Verilog code for a 4-bit forward counting synchronous Johnson counter with a one-bit reset signal. The Johnson counter is a type of shift register that cycles through a sequence of 2^n states. In this case, the 4-bit counter will produce 16 states, each represented by a unique 4-bit binary pattern. Additionally, the counter should be able to reset to its initial state when a one-bit reset signal is asserted. The input consists of two signals 1. clock; 2. reset signal; and the output is a 4-bit value representing the state of the counter at a particular state.