CSE 332: Operating Systems
Fall 2024
Quiz 4 (Set B)

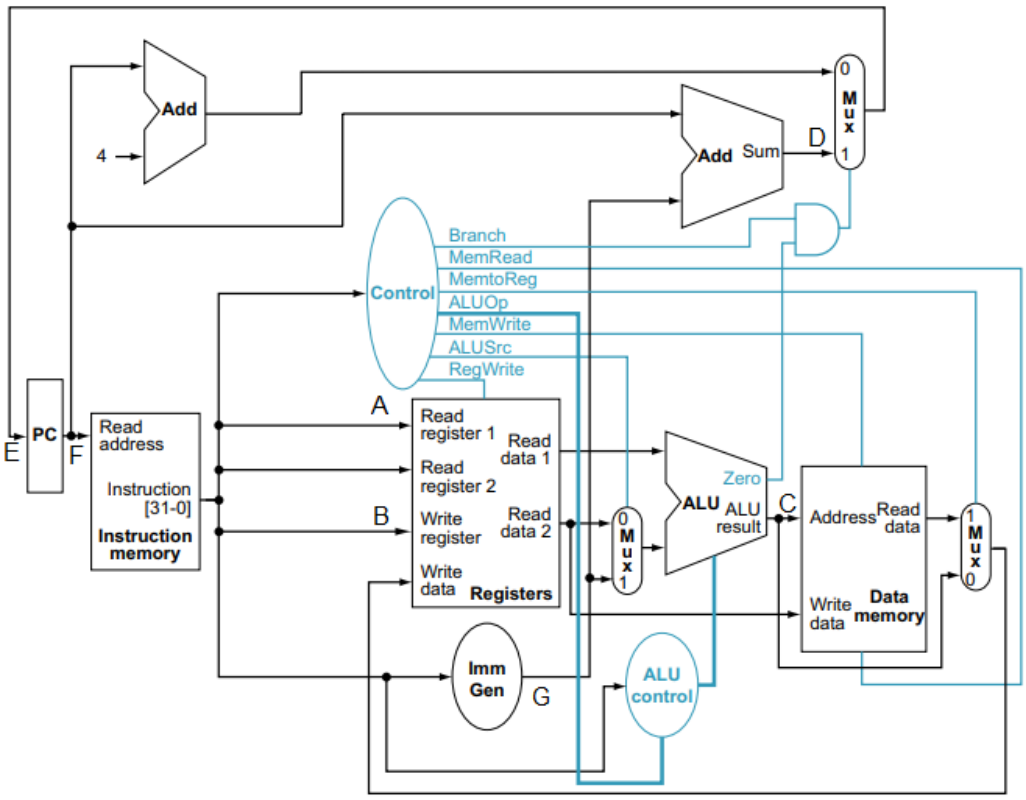

Figure 1: Non-Pipelined Datapath

Question 1: 10 Marks

Refer to the single-cycle datapath shown in Figure 1. The instruction being currently executed is `add x3, x1, x2`, fetched from address 0xFFFAB200. Place tick marks in the following table to show which stages are active the given instruction. Assume x1 = 30, x2 = 40.

Stages	**IF**	**ID**	**EX**	**MEM**	**WB**
Active					

Complete the following table:

Data	Value
A	
B	
C	
E	
F	
G	
Branch	
MemRead	
MemtoReg	
ALUSrc	
RegWrite	

Question 2: 10 Marks

Consider the following specifications for a **pipelined** RISC-V CPU **without forwarding**:

Stage	IF	ID	EX	MEM	WB
Time (ps)	200	100	250	200	100

The following instructions are executed in order:

1. `add x3, x4, x2`
2. `add x5, x6, x1`
3. `lw x1, 24(x5)`
4. `add x9, x1, x15`

Calculate the **total time** required to execute these instructions, **ensuring no data hazard occurs**. Hint: you should start by trying to calculate the clock period. A clock cycle diagram of the instruction sequence should help you reach your answer.

Question 3: 5 Marks

funct7	**rs2**	**rs1**	**funct3**	**rd**	**opcode**
0100000	5 bits	5 bits	000	5 bits	0110011

Table 1: R-type Instruction Format

imm[11]	**imm[9:4]**	**rs2**	**rs1**	**funct3**	**imm[3:0]**	**imm[10]**	**opcode**
1 bit	6 bits	5 bits	5 bits	3 bits	4 bits	1 bit	7 bits

Table 2: SB-type Instruction Format

Suppose you have fetched the instruction `sub x9, x4, x4` from the address 0x00F0A0B0 in a faulty version of the non-pipelined RISC-V CPU (Figure 1), where the branch control signal is permanently switched to 1. A fault in the immediate generation unit makes it consider every instruction it faces as a SB-type instruction. Calculate the address of the next instruction fetched from the instruction memory. Some necessary information has been provided for you in Tables 1 and 2.