CSE 340: Computer Architecture
Fall 2024
Quiz 2 (Set A)

Name:
ID: **Section:**

Question 1: Multiple Choice (10 marks)

Please place a cross (×) across the **correct** box. In case of an incorrect answer cleanly strike out the cross (✳) and mark your new answer. You can change your answer **only once**.

1. The register `x9` initially contains 71, and `x10` contains 3. What will be stored in `x9` after the operation `srl x9, x9, x10`?
   - ☐ 68
   - ☐ 142
   - ☐ 17
   - ☐ 8
2. Registers across RISC-V instruction formats are named `rs1`, `rs2` and `rd`. For the operation `sd x9, 96(x22)`, choose the correct answer.
   - ☐ `rd` is set to 9, `rs1` is set to 22.
   - ☐ `rs1` is set to 96, `rd` is set to 9.
   - ☐ `rs1` is set to 22, `rs2` is set to 9.
   - ☐ `rd` is set to 96, `rs1` is set to 22.
3. The registers `r9`, `r10` and `r11` contain the numbers 31, 15, and 20 respectively. What will be stored in `x9` after the operation `xor x9, x10, x11`?
   - ☐ 27
   - ☐ 25
   - ☐ 29
   - ☐ 35
4. What will be placed in the `immediate` field for the instruction `addi x9, x9, -12`?
   - ☐ 0000 0000 1100
   - ☐ 1111 1110 1010
   - ☐ 1111 1111 0100
   - ☐ 0000 0000 1011
5. How long is a RISC-V instruction in bits?
   - ☐ 8 bits
   - ☐ 16 bits
   - ☐ 32 bits
   - ☐ 64 bits

Question 2 (10 marks)

Write the binary encodings of the following RISC-V instructions. Mention the different sections of the code and their names. The following table has been provided for reference.

1. `add x10, x19, x21`
2. `ld x13, 64(x20)`
3. `sd x11, 32(x19)`
4. `or x16, x18, x23`

Instruction	funct3	funct7	opcode
add	000	0000000	0110011
ld	011	-	0000011
sd	011	-	0100011
or	110	0000000	0110011

Question 3: Bonus (3 marks)

Store the 32-bit number 0000 0000 1110 1010 0110 0100 0101 0110 in the register `x10`.