CSE 340: Computer Architecture
Fall 2024
Quiz 2 (Set B)

Name:
ID: **Section:**

Question 1: Multiple Choice (10 marks)

Please place a cross (×) across the **correct** box. In case of an incorrect answer cleanly strike out the cross (✗) and mark your new answer. You can change your answer **only once**.

1. How long is a RISC-V instruction in bits?
   - ☐ 8 bits
   - ☐ 16 bits
   - ☐ 32 bits
   - ☐ 64 bits

2. The registers `r9`, `r10` and `r11` contain the numbers 31, 15, and 20 respectively. What will be stored in `x9` after the operation `and x9, x10, x11`?
   - ☐ 8
   - ☐ 4
   - ☐ 20
   - ☐ 12

3. The register `x9` initially contains 71, and `x10` contains 2. What will be stored in `x9` after the operation `srl x9, x9, x10`?
   - ☐ 68
   - ☐ 17
   - ☐ 35
   - ☐ 2

4. Registers across RISC-V instruction formats are named `rs1`, `rs2` and `rd`. For the operation `sd x11, 64(x20)`, choose the correct answer.
   - ☐ `rs1` is set to 20, `rs2` is set to 11.
   - ☐ `rs1` is set to 64, `rd` is set to 11.
   - ☐ `rd` is set to 64, `rs1` is set to 20.
   - ☐ `rd` is set to 11, `rs1` is set to 20.

5. What will be placed in the `immediate` field for the instruction `addi x9, x9, -16`?
   - ☐ 0000 0001 1100
   - ☐ 0000 0001 0000
   - ☐ 1111 1111 0000
   - ☐ 1111 1110 1000

Question 2 (10 marks)

Write the binary encodings of the following RISC-V instructions. Mention the different sections of the code and their names. The following table has been provided for reference.

1. `ld x17, 56(x27)`
2. `sub x10, x19, x21`
3. `and x16, x18, x23`
4. `sd x11, 32(x19)`

Instruction	funct3	funct7	opcode
sub	000	0100000	0110011
ld	011	-	0000011
sd	011	-	0100011
and	111	0000000	0110011

Question 3: Bonus (3 marks)

Store the 32-bit number 0000 0000 1010 1010 0100 0101 0110 1011 in the register `x10`.