CSE 332: Operating Systems

Fall 2024

Quiz 4 (Set A)

Showvik

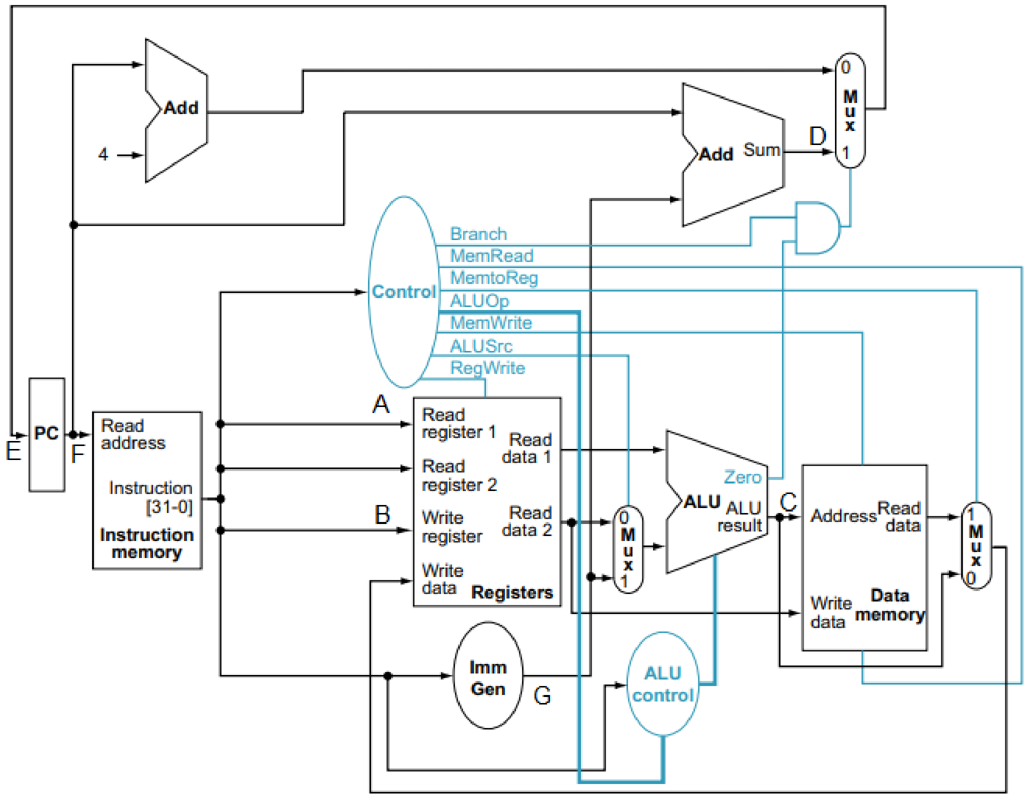


Figure 1: Non-Pipelined Datapath

Question 1: 10 Marks

Refer to the single-cycle datapath shown in Figure 1. The instruction being currently executed is `lw x5, 120(x23)`, fetched from address 0xA010B120. Place tick marks in the following table to show which stages are active the given instruction. Assume x5 = 100, x23 = 150.

Stages	IF	ID	EX	MEM	WB
Active	✓	✓	✓	✓	✓

(all active for load)

Complete the following table:

Data	Value
A	23
B	5
C	270
E	0xA010B124
F	0xA010B120
G	120
Branch	0
MemRead	1
MemtoReg	1
ALUSrc	1
RegWrite	1

Question 2: 10 Marks

Consider the following specifications for a **pipelined** RISC-V CPU **without forwarding**:

Stage	IF	ID	EX	MEM	WB
Time (ps)	200	100	400	200	100

The following instructions are executed in order:

1. `add x5, x4, x2`
2. `add x3, x6, x1`
3. `lw x1, 24(x5)`
4. `add x9, x1, x15`

Calculate the **total time** required to execute these instructions, **ensuring no data hazard occurs**. Hint: you should start by trying to calculate the clock period. A clock cycle diagram of the instruction sequence should help you reach your answer.

Question 3: 5 Marks

funct7	rs2	rs1	funct3	rd	opcode
0100000	5 bits	5 bits	000	5 bits	0110011

Table 1: R-type Instruction Format

imm[11]	imm[9:4]	rs2	rs1	funct3	imm[3:0]	imm[10]	opcode
1 bit	6 bits	5 bits	5 bits	3 bits	4 bits	1 bit	1100011

Table 2: SB-type Instruction Format

Suppose you have fetched the instruction `sub x5, x2, x2` from the address 0x00A1B0C0 in a faulty version of the non-pipelined RISC-V CPU (Figure 1), where the branch control signal is permanently switched to 1. A fault in the immediate generation unit makes it consider every instruction it faces as a SB-type instruction. Calculate the address of the next instruction fetched from the instruction memory. Some necessary information has been provided for you in Tables 1 and 2.

2. clock = 400ps

sequence:

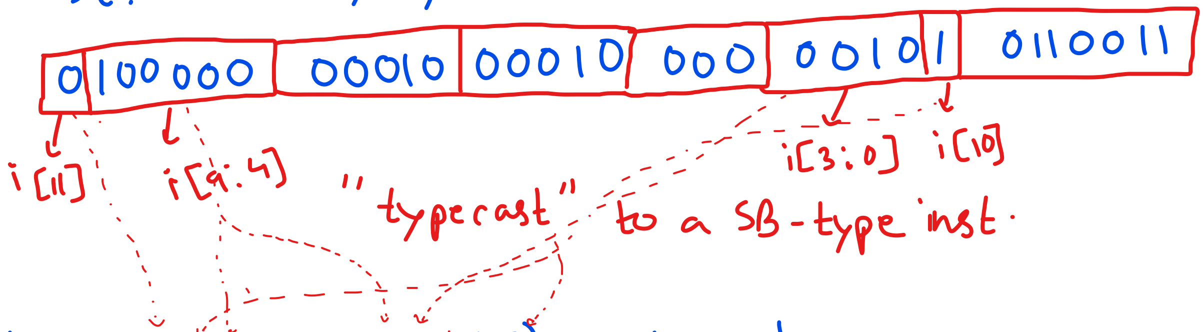
	1	2	3	4	5	6	7	8	9	10	11
1. add	IF	ID	EX	MEM	WB (i)						
2. add		IF	ID	EX	MEM	WB					
			☁	☁	☁ (ii)	☁	☁				
3. lw				IF	ID (ii)	EX	MEM	WB (iii)			
					☁	☁	☁	☁	☁		
						☁	☁	☁	☁	☁	
4. add							IF	ID (iv)	EX	MEM	WB

← added to line up (i) and (ii)

← added to line up (iii) and (iv)

Total = 11×400 = 4400ps

3. inst: sub $\overset{rd}{x5}, \overset{rs1}{x2}, \overset{rs2}{x2}$



$$imm = (0\,1\,100000\,0010)_2 = (1538)_{10}$$

reconstructed from inst.

sub x5, x2, x2 will always cause zero flag to turn on

branch flag also switched to 1.

if CPU treats it as a SB-type (beq), then

$$\begin{aligned} target &= curr + imm \times 2 \\ &= 0x00A1B0C0 + (1538)_{10} \times 2 \\ &= 0x00A1BCC4 \end{aligned}$$