CSE 340: Computer Architecture
Fall 2024
Quiz 1 (Set B)

Name:
ID: **Section:**

Question 1 (12 marks)

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C and D). You have two processors P1 and P2, where P1 has a clock rate of 3.0 GHz, and CPIs of 2, 1, 3 and 3 (for classes A, B, C and D respectively), and P2 has a clock rate of 3.0 GHz, and CPIs of 1, 2, 3 and 1 similarly.

(a) Given a program with 1×10^6 instructions with 10% from class A, 20% from B, 50% from C, and 20% from D, which processor is faster? (8)

(b) Find the clock cycles required in both cases. (4)

Question 2 (8 marks)

Convert the following C code into RISC-V instructions:

(a)
```
e = a - (b - c) - d
```

a, b, c and d are in registers x19, x20, x21, x22 respectively, and e is stored in x23. (4)

(b)
```
A[16] = h + A[8]
```

Given, A is an array of **words**, the base address of A is stored in x21, and h is stored in x22. You can use x9 as a temporary register. (4)