SPARKONICS - IIT Patna ©

Home-Plug

ADC - simulation

Simulation is done in matlab 2024r_a © owned by mathworks.com
The main framework used is simscape and simulink blocks

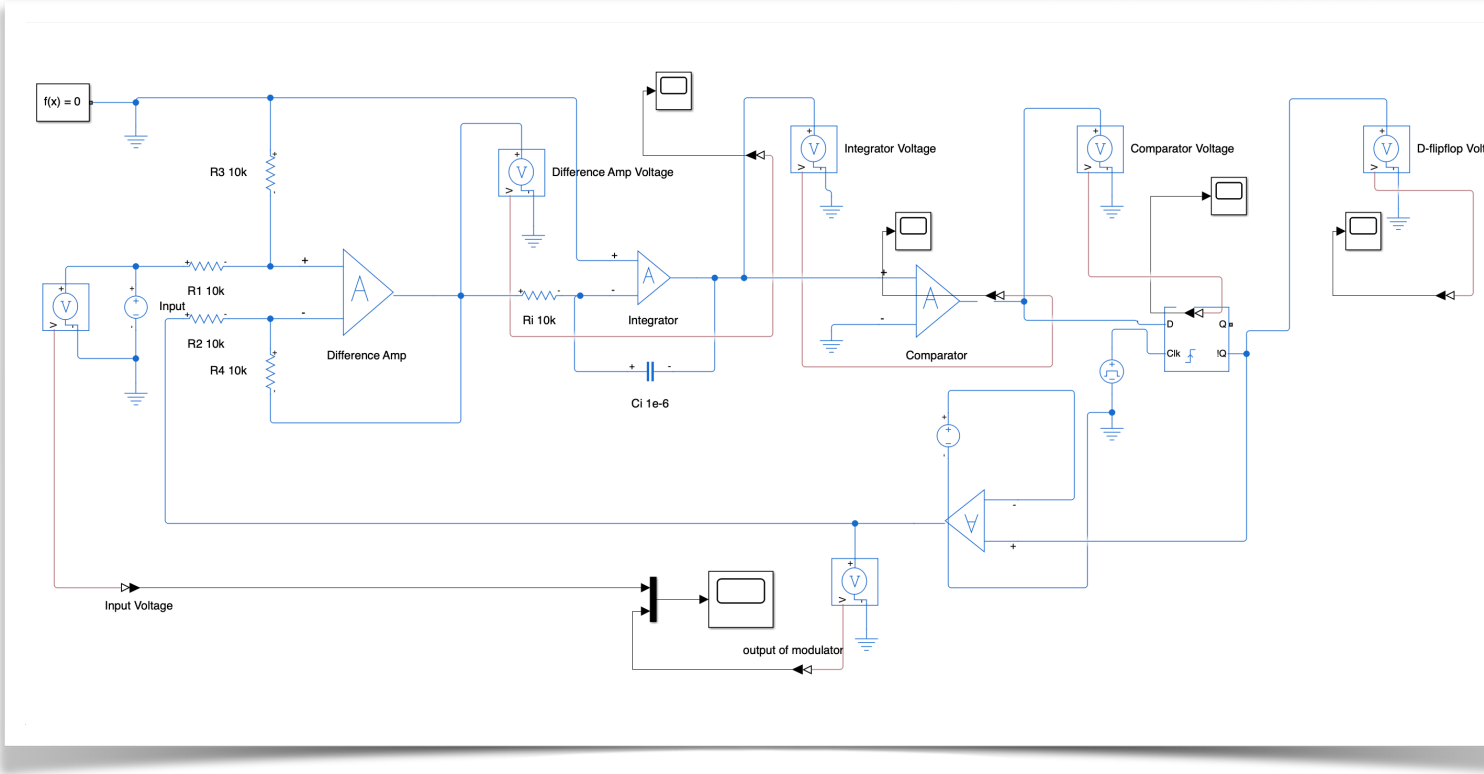
Components Used :

S.NO	Component	Framework	Use	Value
1	Voltage Source	Simscape/electrical	Giving Input Voltage	5V - Peak to Peak 60Hz
2	Finite Gain OpAmp	Simscape/electrical	Difference Amplifier	15 Vmax 15 Vmin Gain 1
3	Finite Gain OpAmp	Simscape/electrical	Integrator	15 Vmax 15 Vmin Resistor 10Kohm Capacitor 1.667e-6
4	Finite Gain OpAmp	Simscape/electrical	Comparator	Vmax 5 Vmin 0 Compares with Zero(Inverting)
5	D-Flip Flop	Simscape/electrical	As a multiplier block	CLK given defines the Oversampling Frequency
6	Finite Gain OpAmp	Simscape/electrical	Comparator	Vmax 5 Vmin -5 Compares with 1V(Inverting)
7	Feedback	6(S.No) component output is fed into difference amplifier of 2(S.No) at Inverting terminal while Input Signal is given at Non-Inverting Signal	To make the bit stream output from d-flip flop average to actual value with least bit of quantisation error	
8	Scope	Simulink	To observe the signals in 2d View	
9	Voltage Sensor	Simscape/electrical	To measure the voltage of across components	

S.NO	Component	Framework	Use	Value
10	Controlled Voltage Sensor	Simscape/electrical	To measure the voltage of simulink components, and feed it to simscape components as input	
11	Electrical Reference	Simscape/electrical	To make a line ground	
12	Ps-simulink convertor	Simscape/electrical	To convert an simscape signal into simulink signal	
13	Simulink-ps convertor	Simscape/electrical	To convert simulink signal to simscape signal	

Simulink Simulation of Sigma Delta Modulator:

Sigma-Delta Modulator



Simulation Done in Matlab

1. The Sigma Delta Modulator working is a unique ADC which converts a signal into a bit of streams comprised of ones and zeros
2. To understand better visit this link : https://www.analog.com/en/resources/interactive-design-tools/sigma-delta-adc-tutorial.html
3. I would say that the important aspects that has to remembered is the clock frequency which is set to the D-Flip Flop

The importance of D-Flip FLop

4. D-Flip Flop is placed after the first comparator, its inputs are the output of the first comparator and a pulse(Clock)
5. D-Flip Flop is responsible for the stream of bits, the outputs of the Flip flop are stream of bits with varied width and uneven spacing
6. When you take the mean of a range of stream of bits you get a quantised output
7. The clock frequency (i.e: pulse generator frequency) is the Oversampler which gives use the extreme sampled version of the input signal, which later will be converted to digital output
8. The Clock frequency is given by the equation

Clock Frequency (Fclk) = OSR * 2 * Input Frequency(Fin)

9. Here Important terms like OSR, comes into picture which stands for Over Sampling Ratio and 2*Fin which is the minimum nyquist frequency.
10. The product of OSR and Nyquist Frequency gives us the Clk Frequency
11. Now, in our simulation I have found that a minimum OSR of 50 and for better results an OSR of 1000 are required
12. The input signal we have taken is 5v(Peak-to-peak) and Frequency of 60Hz, which means a frequency of 6Khz to 60Khz are optimal

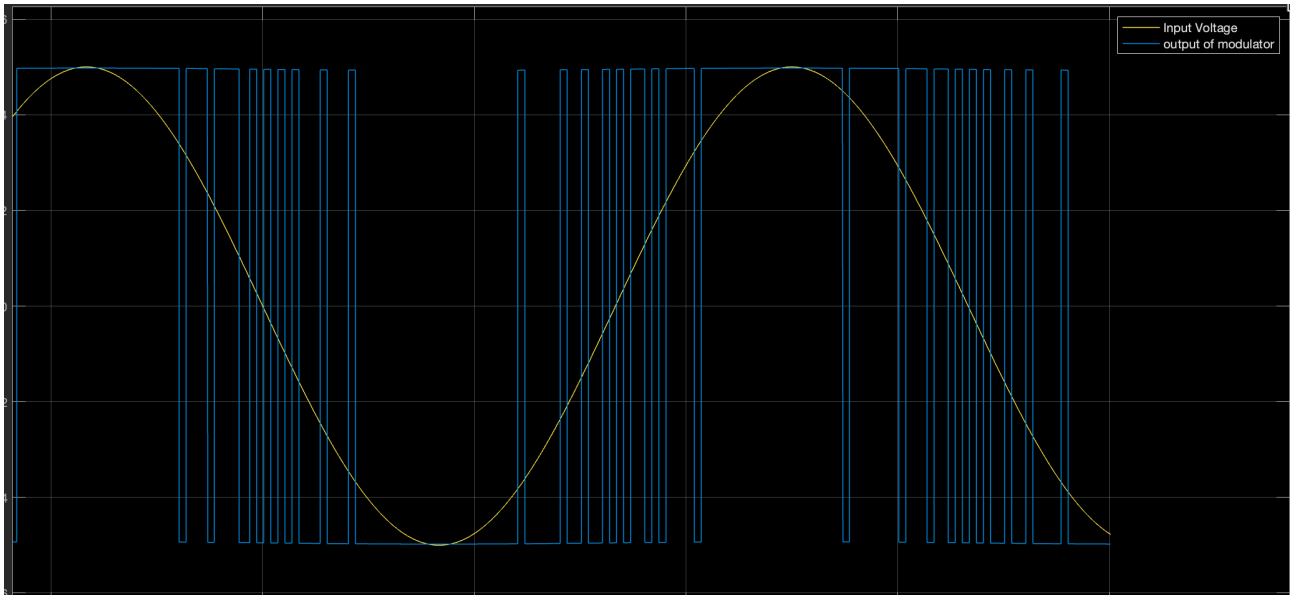
Simulink Results :

The input signal Voltage is 5V(peak-peak) and frequency 60Hz

Case 1:

The clock Frequency is 6Khz

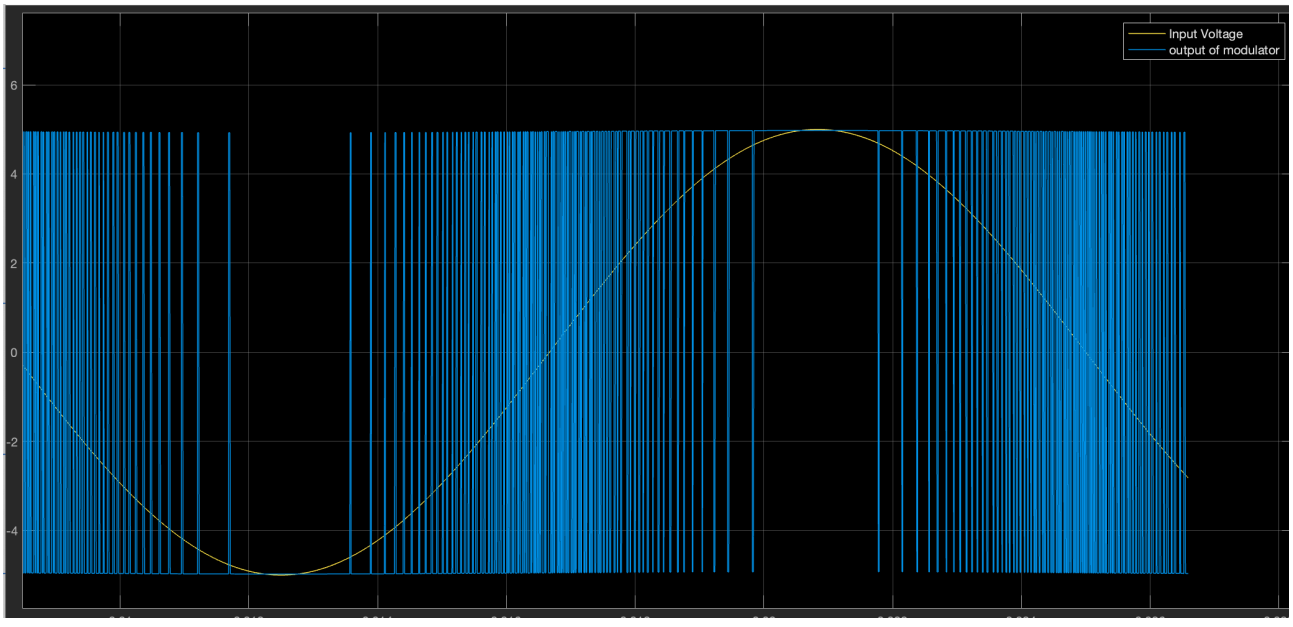
Means OSR is 50



Case 2:

The clock frequency is 60KHz

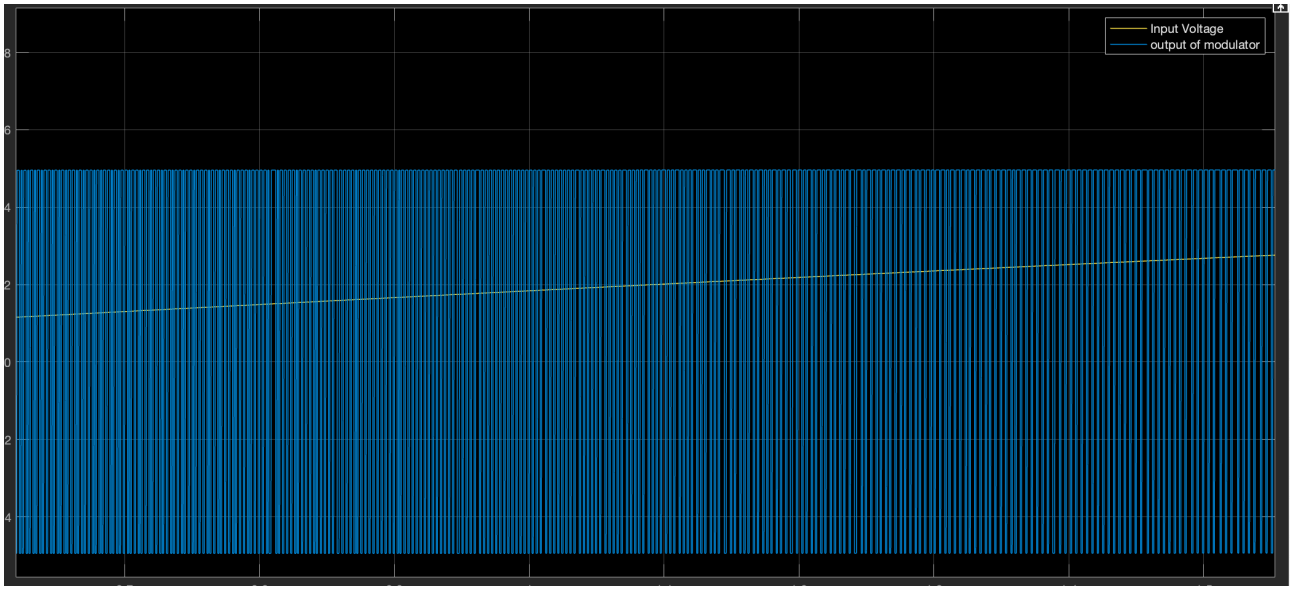
Means OSR is 500



Case 3:

The clock frequency is 100 KHz

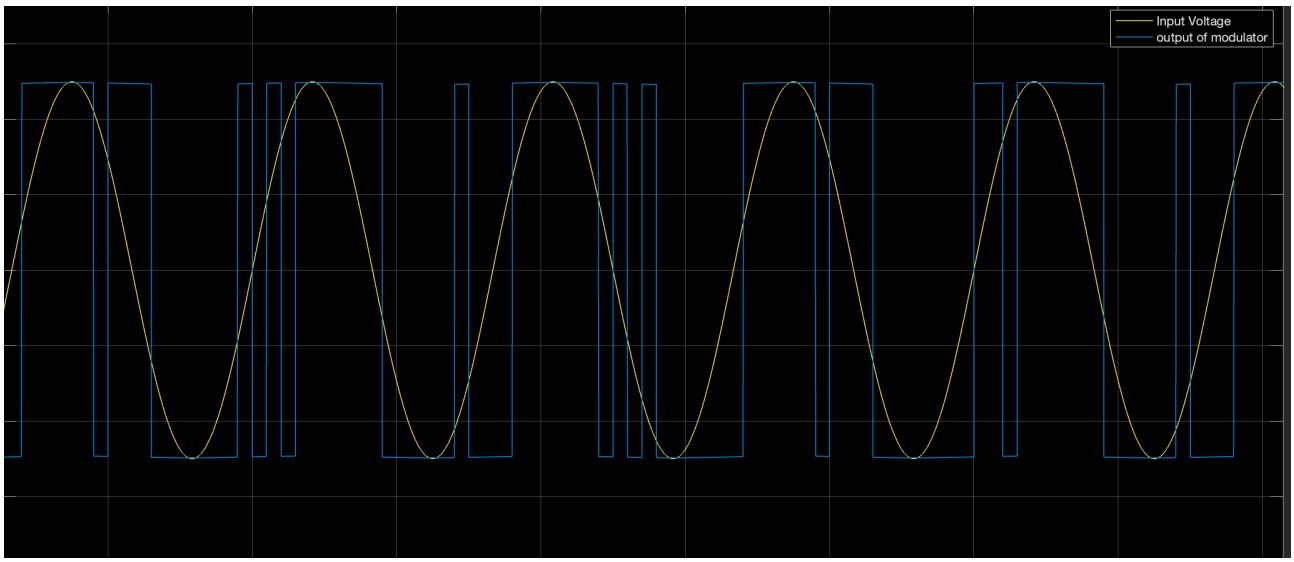
Means OSR is 833.33



Case 4:

The clock frequency 1000Hz

Means OSR is <100



Conclusion From our side:

As you can see from from the results ,anything that is outside the range of 6khz to 60Khz from input frequency of 60Hz will give us trouble.

So choosing the clock frequency in the provided range is good

And I believe the OSR range being 50 to 500 is good for any input frequency, and if the resolution of the bits is higher lets say 16 then we need higher OSR, If less resolution then low OSR is good.

I believe we can have an OSR of 150 - 300, for a eight bit resolution.

Made by :
Siva Dhanush Reddy
Jlspk
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M.L.P.Puneeth