Sparkonics

Home-Plug

ADC

Findings and Initial Research

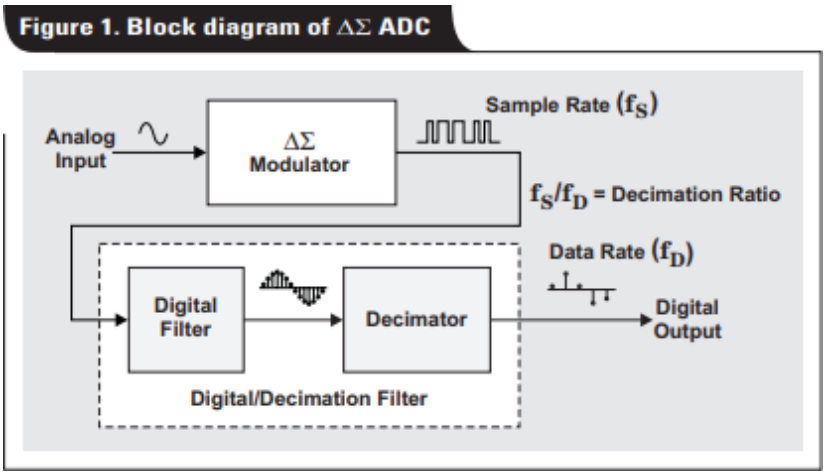
ADC is sigma delta ADC (from page 3 bottom - Embedded Metrology) ΣΔ24 ADC is differential and requires the pins do not exceed +-928mV ΣΔ24 ADC setup:
ΣΔ24 ADC (fM) is fixed at 1.024 MHz.

Now, ΣΔ24 ADC is too costly and beyond us. hence, we are breaking it down

Findings:

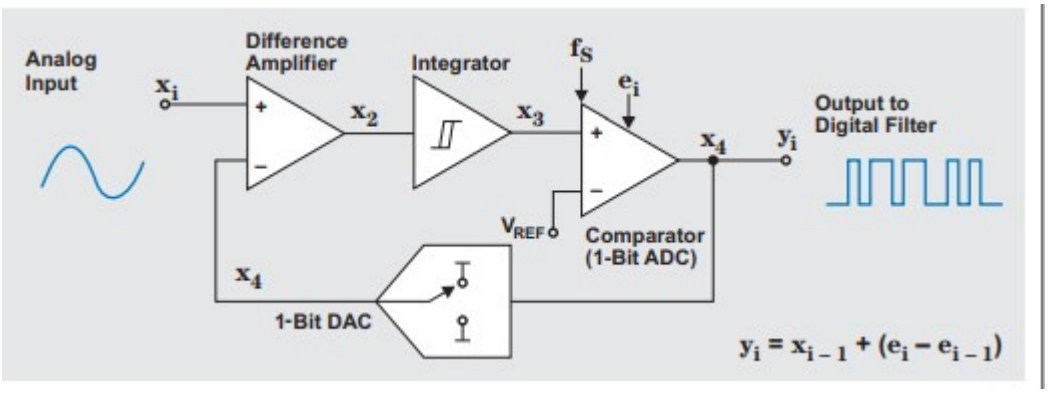
From

1. ΣΔ ADC are industrial standard used ADC, for precise and fast sampling rates



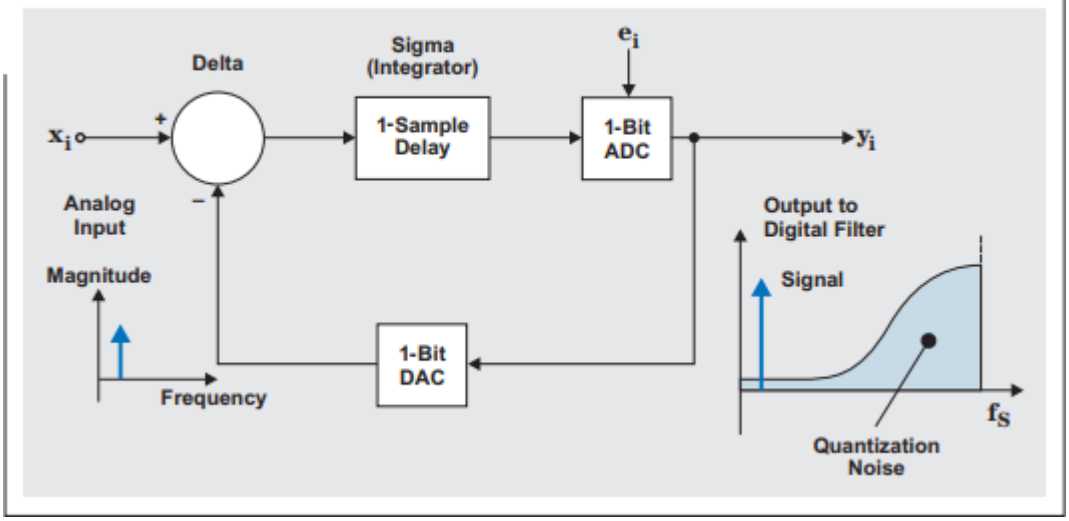
2.
3. ΣΔ ADC have two major components
    a. ΣΔ Modulator, meaning the quantization is being done
        i. This modulator pushes the noise to higher frequency making it out of intereset
        ii. But the
    b. Digital/Decimation Filter
4. ΣΔ modulator gives the digital output as 1-bit sample rate with a simple circuit How delta-sigma ADCs work, Part 1 (Rev. A)

a. First-order modulator filter in time domain



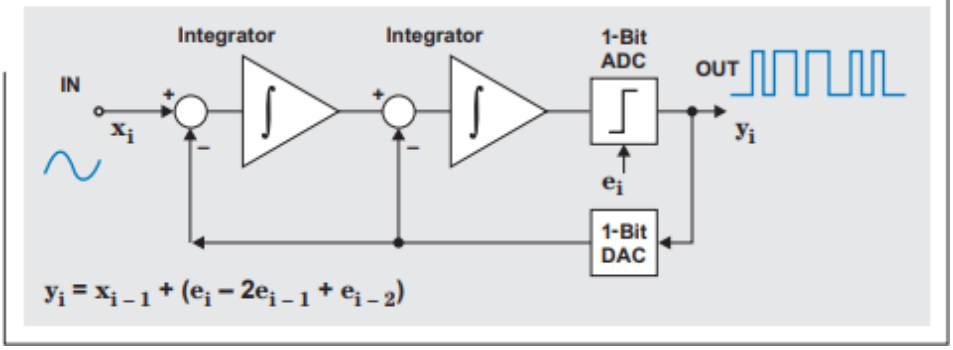
b. First-order modulator filter in frequency domain

Figure 4. First-order ΔΣ modulator in the frequency domain

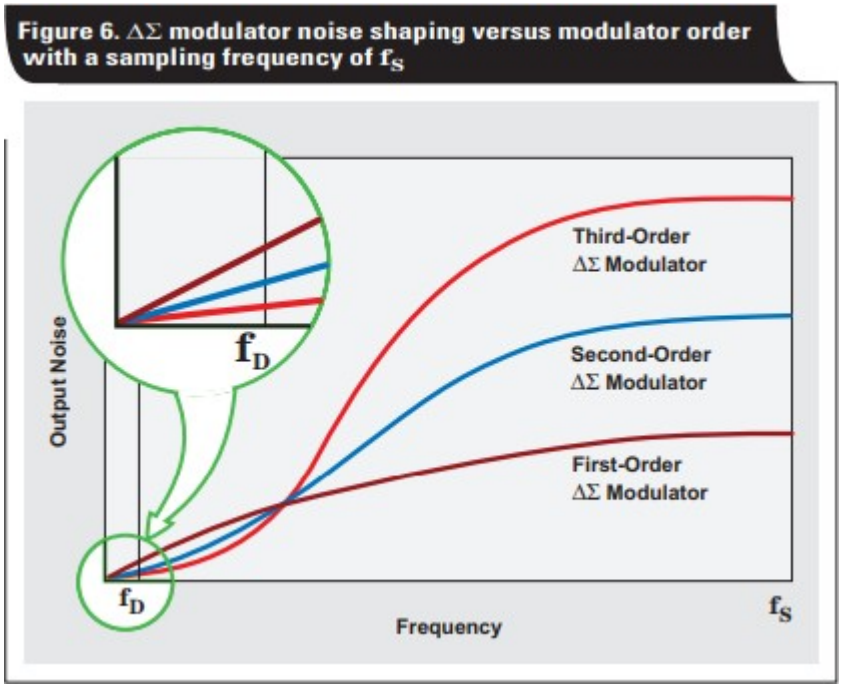


c. Second-order modulator

Figure 5. Block diagram of a second-order ΔΣ modulator



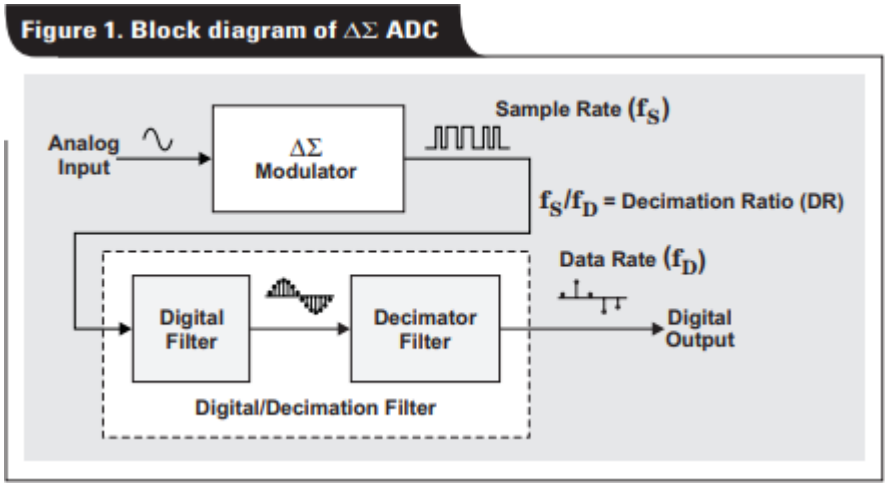
d. First order modulator have high output noise at lower frequency and lower noise at higher frequency, and higher order modulator have low output noise at lower frequency and higher noise at lower frequency



e. Now we were able to reduce noise at lower frequency at this first step now we will reduce the noise at higher frequency with low pass filters

5. Digital/Decimation Filter :-[How delta-sigma ADCs work, Part 2]

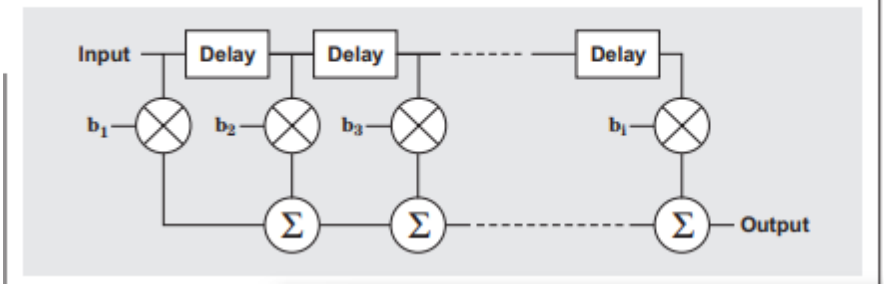
a. The inner Working of the digital/decimation filter



b. Digital filter:-

i. Here we try to reduce the sampling rate, by using a low-pass averaging

Figure 2. First-order, low-pass averaging filter



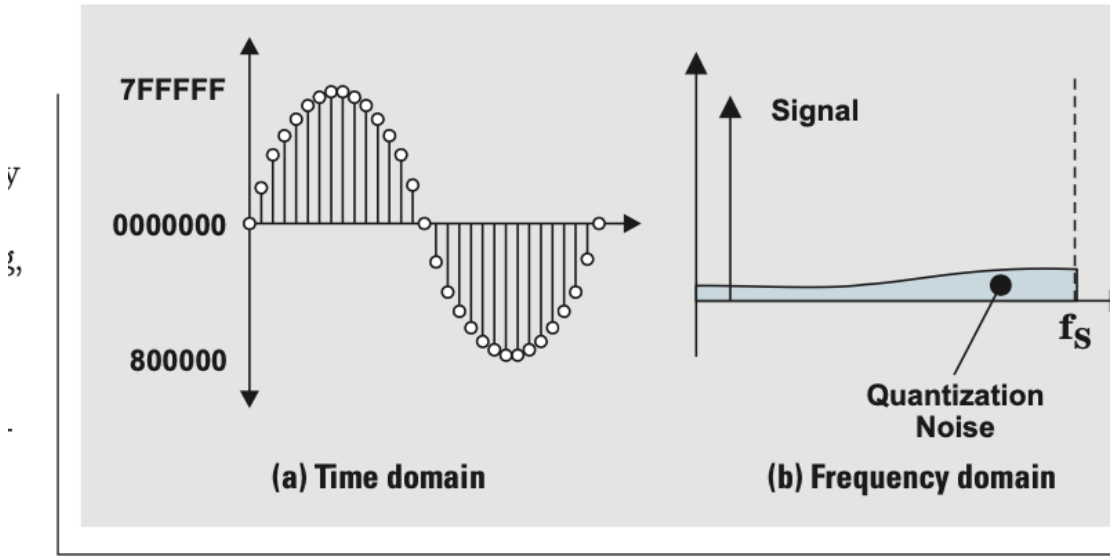
filter this has a weighted sum

ii. They are using sinc filter, these are averaging filter

iii. After the digital filter, the output has the same sampling rate as the modulator output, and this digital filter acts a low-pass filter in frequency

domain, removing much noise.

Figure 3. Outputs of a digital filter



iv. Decimation filter: This brings the sampling rate down, by the required resolution, Here we define data rate, the rate of the decimation filter output.

1. We have to note that the sampling rate(Fs) from the modulator and decimation filter rate called output-data rate (Fd) are important parameters to be determined.
2. The ratio between these two, is called the decimation ratio(DR). Simply means Fs/Fd
3. This decimation ration plays important role in the

quality of the resolution of the data output

4. Now, ENOB(effective number of bits) means the number of useful bits that has useful information without the interference of much noise
5. Now, High DR means the Fd is a much lower frequency means there less noise in the data, where as Low DR means Fd is at

   closer to Fs and has noise

6. There is a trade off, that has to be maintained.

Conclusion:

This sigma-delta ADC, uses a modulator and Digital/Decimation filter. Modulator converts the analog into digital by using 1-bit ADC, Now digital/ decimation filter reduces noise and creates a data-rate based on use
Its highly effective in noise reduction and enough fast (5kHz) tops and high resolution

Figure 5. Increased DR provides a lower-noise, slower output signal