Analog Electronics

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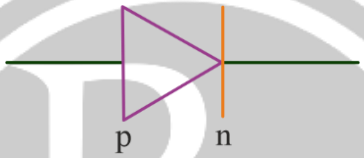
ANALOG ELECTRONICS

INDEX

1 DIODE CIRCUITS & APPLICATIONS

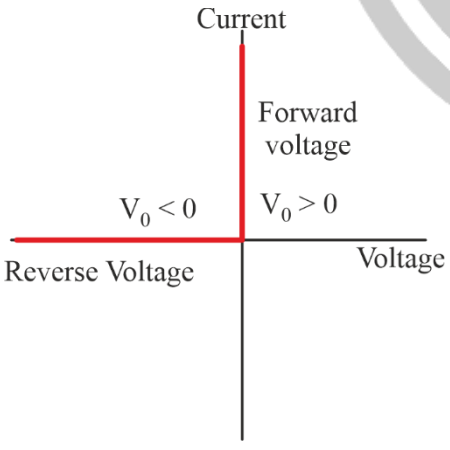
1.1. Diode

- A two terminal semiconductor device with PN junction is called a diode
- A PN junction diode is a two terminal device formed by doping with acceptor and dopant impurities at different regions.

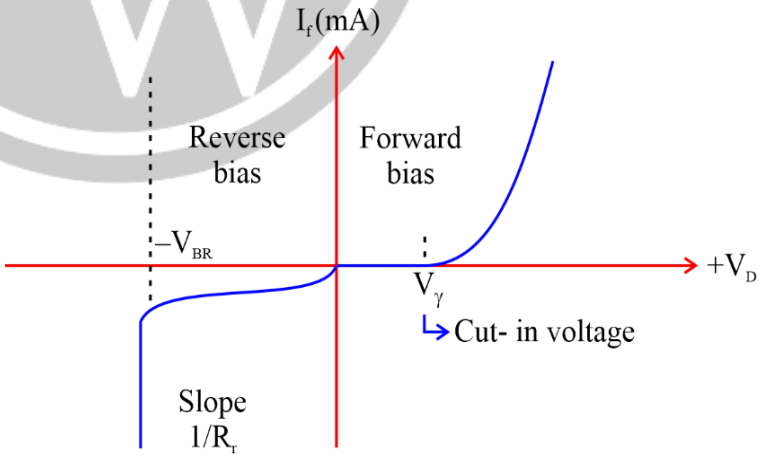


1.2. VI Characteristics

- In ideal condition, a diode works as a short circuit at during forward bias and open circuit during reverse bias, i.e. like an ideal switch
- In practical condition a diode works as low resistance, and high resistance at reverse bias, i.e. like a practical switch.



Ideal Characteristics



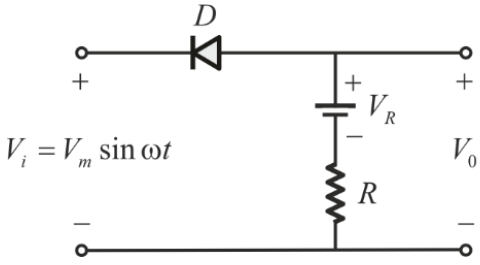
Practical Characteristics

1.2.1. Application of Diode in Clipper circuit

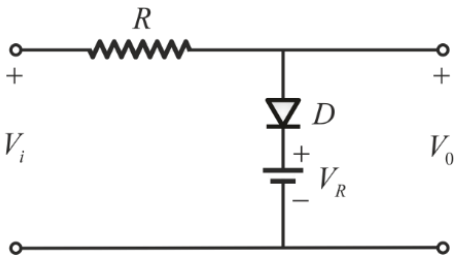
- The Circuit clips a portion of the input signal
- On the basis of which part the circuit clips, the circuit is named as Positive or Negative clipper
- A series or shunt clipper is named according to the placement of diode in the circuit.

Positive Clipper

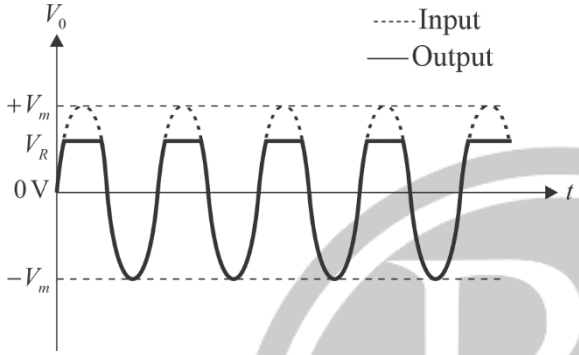
Clips positive portion of the input signal.



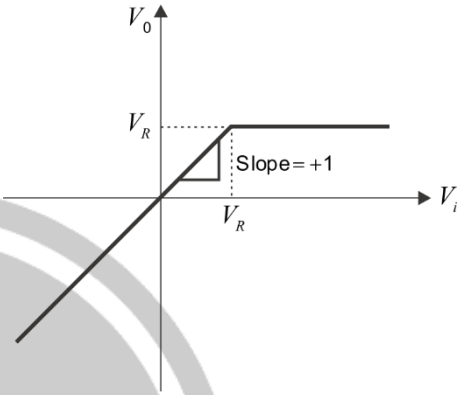
Series Clipper



Shunt Clipper



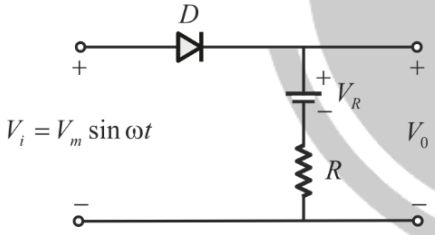
Response



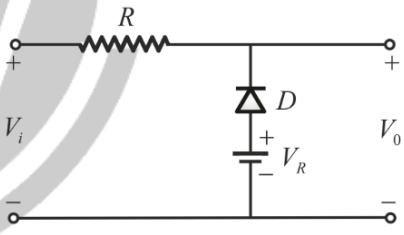
Transfer Characteristics

Negative Clipper

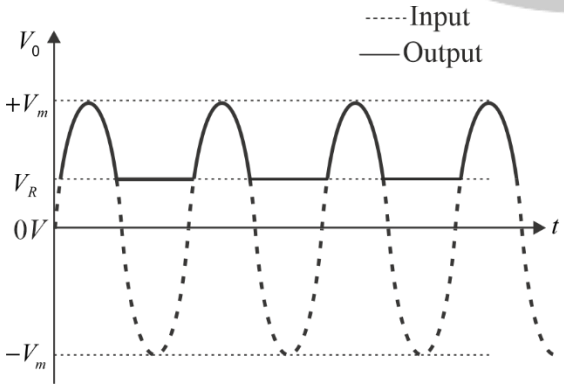
Clips negative portion of the input signal.



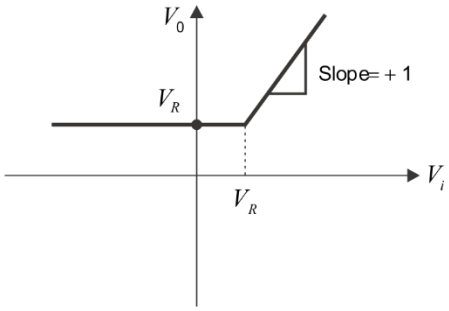
Series Clipper



Shunt Clipper



Response



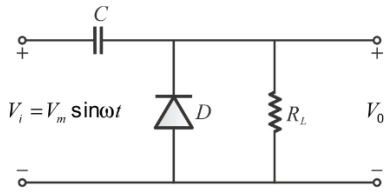
Transfer Characteristics

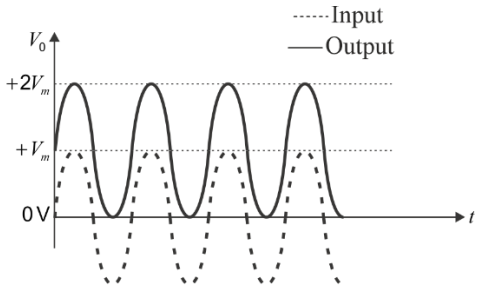
Application of Diode in Clamper Circuit

- A clamper circuit clamps or adds a DC shift to the input signal.
- Based on the polarity of shift, a Positive or Negative clamper is named.

Positive Clamper Circuit

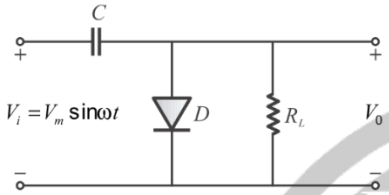
Adds a positive DC shift to the input signal.

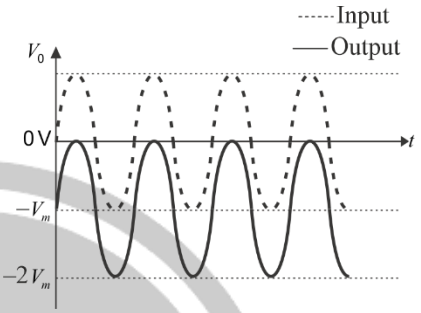




Negative Clamper Circuit

Adds a negative DC shift to the input signal.





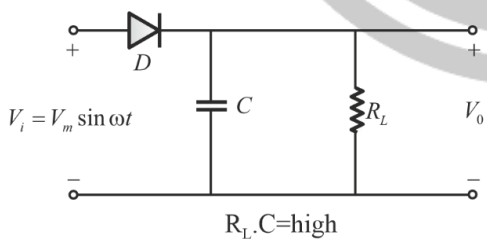
Note: For Proper functioning of clamper circuit, time constant of circuit should be much greater than time period of input signal ($R_LC >> T$)

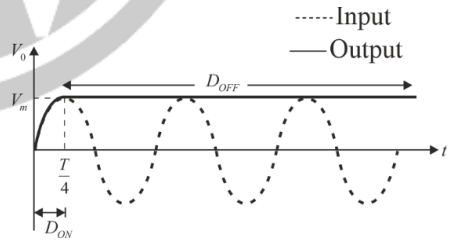
1.3. Application of Diode in Peak Detector

A peak detector detects the peak of the input signal.

Positive Peak Detector

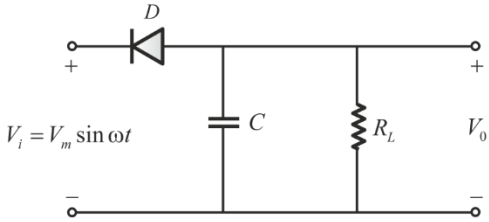
Detects the positive peak of input signal.

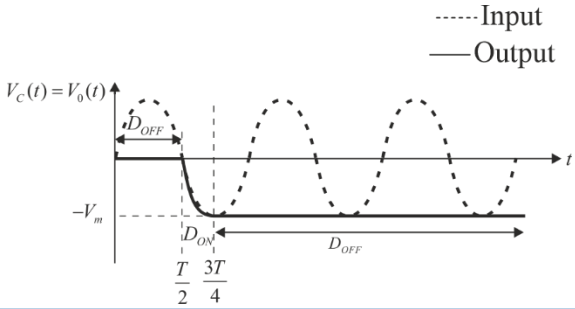




Negative Peak Detector

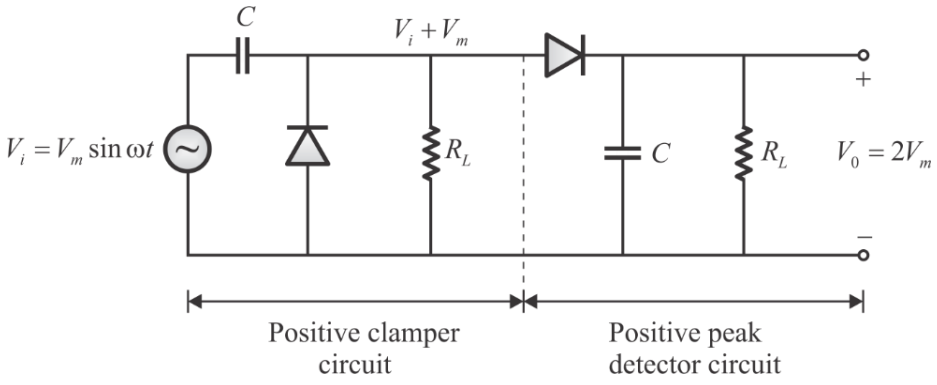
Detects the negative peak of input signal





1.4. Application of Diode in Voltage Doubler

- Voltage doubler gives the output as double of the input signal.
- A level shifter or clamper followed by a peak detector gives a Voltage Doubler



$R_L C >> T$

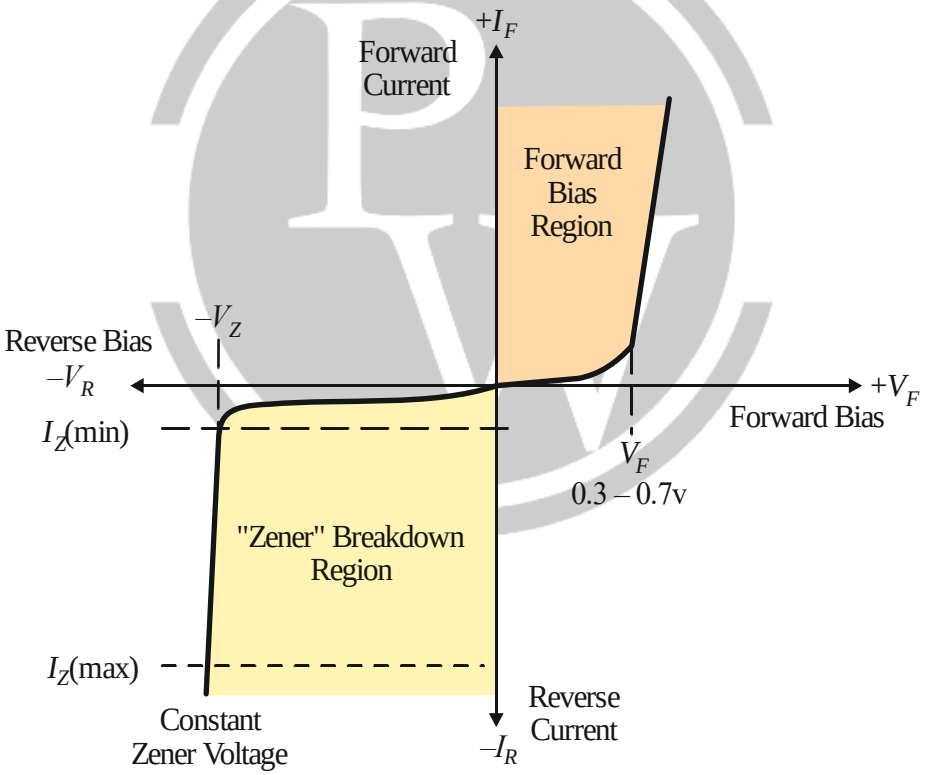
1.5. Application of Diode in Voltage Multiplier

Using multiple stages of a set of a clamper and peak detector gives voltage multiplier, also called as Cockroft-Walton Voltage Multiplier.

2 ZENER DIODES REGULATOR CIRCUIT

2.1. Zener Diode VI Characteristics

- A "reverse biased" diode blocks current in the reverse direction, but will suffer from premature breakdown or damage if the reverse voltage applied across it is too high.
- Zener Diode are basically the same as the standard PN junction diode but are specially designed to have a low predetermined Reverse Breakdown Voltage that takes advantage of this high reverse voltage.



Zener Diode in Forward Bias:

Works same as a normal PN diode i.e short circuit ideally and a low resistance practically.

Zener Diode in Reverse Bias:

1. $V < V_Z$, works as a normal PN diode in reverse bias i.e open circuit ideally and a high resistance practically.
2. $V > V_Z$, works as a voltage regulator i.e becomes a source of constant voltage for the connected load.

Ideal Zener Diode

Zener Diode | Reverse Biased (with Breakdown) | Reverse Biased (without Breakdown) | Forward Biased

Practical Zener Diode

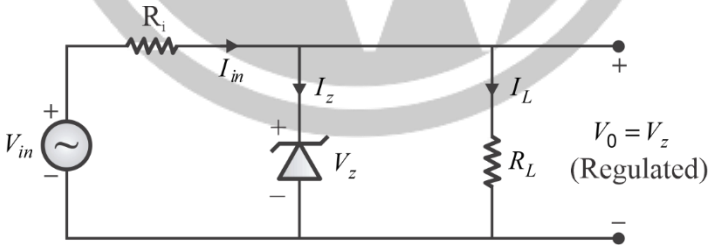
Zener Diode | **Reverse Biased (with Breakdown)** | **Reverse Biased (without Breakdown)** | **Forward Biased**

Operating Conditions for Zener diode to maintain break down characteristics:

1. Current through Zener diode, $I_{Z(\text{knee})} \le I \le I_{Z(\text{max})}$
2. The magnitude of open circuit reverse voltage across the Zener diode should be greater than or equal to V_Z.
   - I_Z (knee) is the minimum current required for the Zener diode to work as a voltage regulator
   - I_Z (max) is the maximum current the Zener diode can operate without damaging the device. It is specified by manufacturer.

Zener Diode as Voltage Regulator

Zener Diodes are used to produce a stabilised voltage output with low ripple under varying load current conditions.



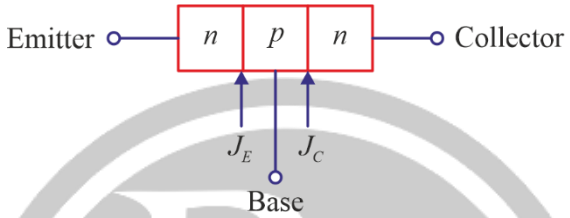
Output voltage : $V_0 = V_z = \text{Zener voltage}$

- Input current : $I_{in} = \dfrac{V_i - V_0}{R}$
- Source resistance : $R = \dfrac{V_i - V_0}{I_Z + I_L}$
- Zener power dissipation : $P_{Z(\text{max})} = I_{Z(\text{max})} V_Z$

Note: Zener diodes can also be connected together in series along with normal silicon diodes to produce a variety of different reference voltage output values

3 BJT BIASING AND REGION OF OPERATION

3.1 Operating Region of BJT



where, J_E = Base-Emitter Junction

J_C = Collector-base Junction

Normal Active Region

In this region, J_E operating in forward bias while J_C operating in reverse bias. It is used as amplifier.

Saturation Region

Both J_E and J_C are operating in forward bias and is used as switch (ON).

Cut-OFF Region

Both J_E and J_C are operating in reverse bias and is used as switch (OFF).

Reverse Active Region

In this region, J_E in reverse bias and J_C in forward bias. It is used as attenuator.

Some Standard values for *npn* transistor.

	Si	Ge
V_{BE} (Active Region)	0.7 V	0.2
V_{BE} (Saturation region)	0.8 V	0.3 V
V_{CE} (Saturation region)	0.2 V	0.1 V
V_{BE} (Cut-off region)	0 V	– 0.1 V

Note : If nothing is mentioned then we will assume transistor is silicon type.

3.2. Different Methods used to Identify Operating Region of BJT

Method-I

Assume transistor in Saturation Region

1. $I_C \neq \beta I_B$
2. $V_{CE} = V_{CE}(\text{sat})$
3. $I_{B(\min)} = \dfrac{I_C(\text{sat})}{\beta_{dC}}$ $\quad (\beta_{dC} = h_{fe})$
4. If $I_B \geq I_B$ (min) then transistor will work in saturation region otherwise in active region.

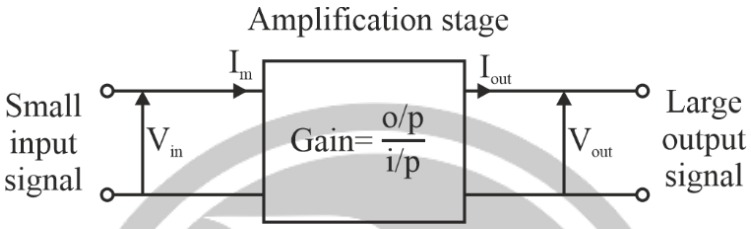
Method-II

Assume transistor in active region.

1. $I_C = \beta_{dc} I_B$
2. $I_E = I_C + I_B = (I + \beta_{dc}) I_B$
3. For active region = $\begin{cases} V_{CB} > 0 & \textit{for npn transistor} \\ V_{CB} < 0 & \textit{for pnp transistor} \end{cases}$

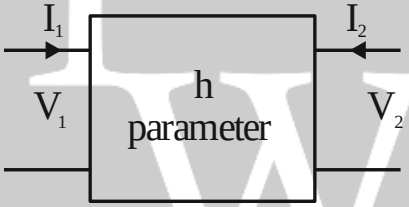
4 LOW FREQUENCY BJT AMPLIFIER

4.1. Amplifiers



4.1. Small Signal Modelling of BJT

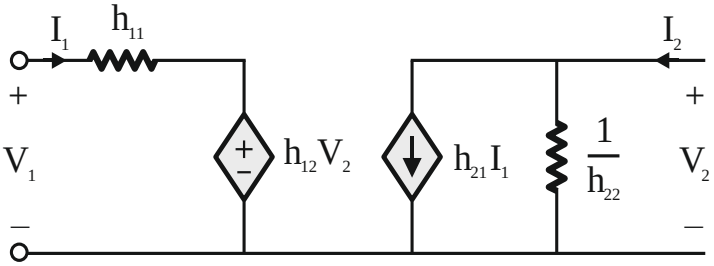
1. *h*-parameter modelling:



$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$V_2 = h_{21}I_1 + h_{22}V_2$$



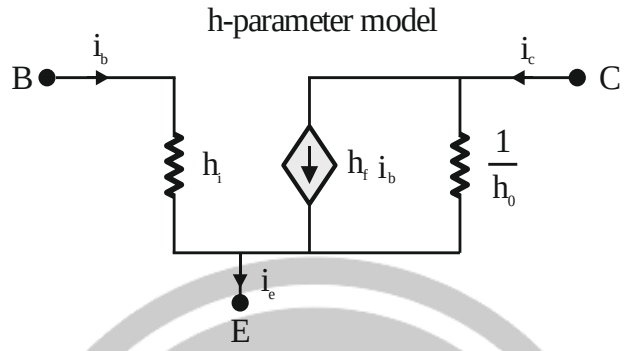
$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = \text{input impedance} = h_i$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \text{reverse voltage gain} = h_r$$

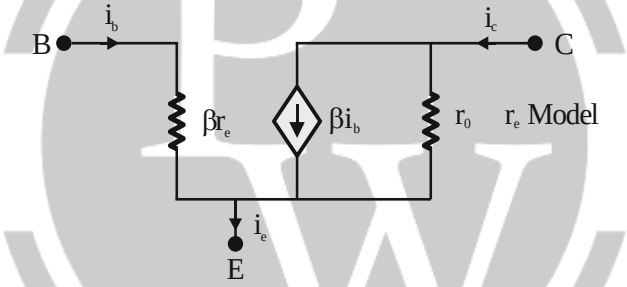
$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} = \text{forward current gain} = h_f$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0} = \text{output admittance} = h_0$$

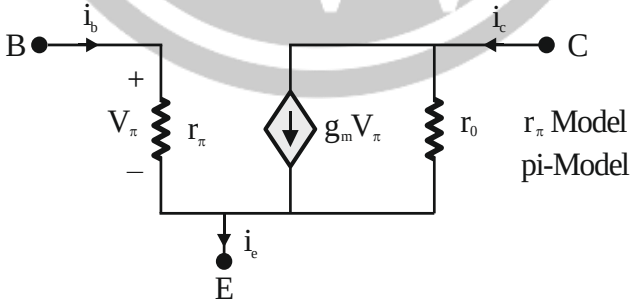
2. Approximated h-model



2. r_e modelling



3. r_π modelling



Relation between small signal modelling parameters

1. $h_i = \beta r_e = r_\pi$
2. $h_f = \beta$
3. $\frac{1}{h_0} = r_0 = V_A / I_{CQ} = \infty$ if no early effect

4. $\beta i_b = g_m V_\pi$

$= g_m r_\pi i_b$

$= g_m \cdot \beta r_e i_b$

$= g_m \cdot \beta r_e i_b$

$\Rightarrow g_m = \frac{1}{r_e}$

r_e = emitter dynamic resistance

$r_e = \frac{\eta V_T}{I_{EQ}}.$

Note: Practically $r_0 = 0$, and $1/h_0 = \infty$, if not mentioned explicitly.

4.2. Procedure of AC analysis

Step 1: Do the mid frequency analysis

(a) $C_{c_1}, C_{c_2}, C_E \rightarrow$ short circuit

$C_T, C_D, C_{sh} \rightarrow$ Open circuit

(b) all DC independent voltage source ⟶ Short circuit

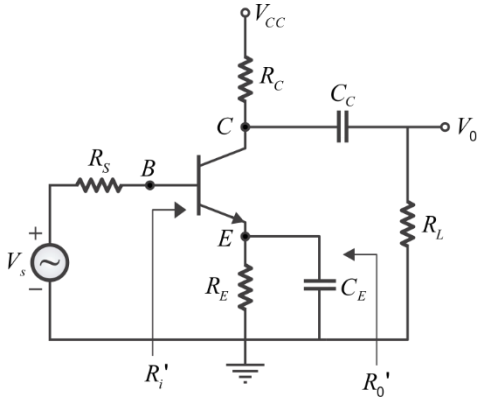
All independent current source = open circuit

Step 2: Replace BJT with small signal equivalent.

Internal Performance Parameter of an Amplifier

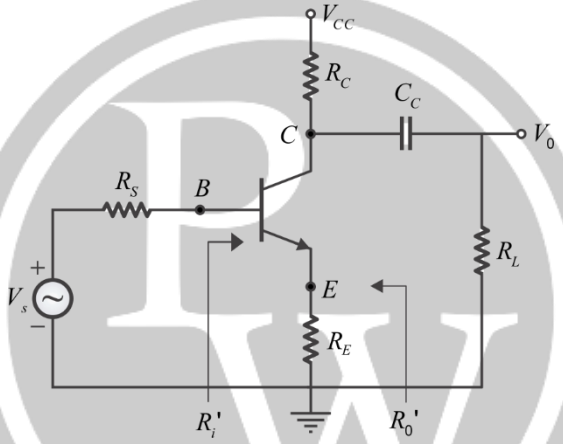
1. Current Gain (A_i) = $-I_2 / I_1$
2. Input Resistance (R_i) = V_1/I_1
3. Voltage Gain (A_v) = V_2/V_1
4. Output Resistance (R_o) = 1/Output Admittance ($1/y_o$) = $I_2/V_2 \mid V_S = 0$

CE Amplifier without R_E



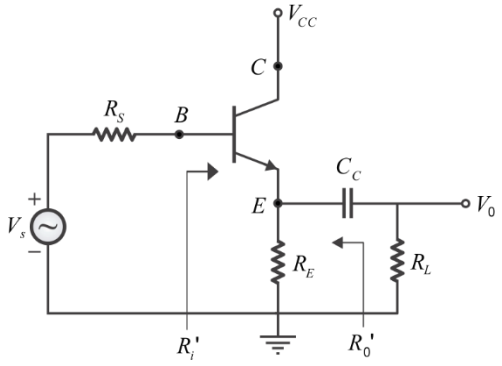
Parameter	Current Gain	Input Resistance	Voltage Gain	Output Resistance
h-model	$A_I' = -h_{fe}$	$R_i' = h_{ie}$	$A_V' = A_I' \times \frac{R_L'}{R_i'}$ $R_L' = R_L \parallel R_C$	$R_0' = \infty$
r_e model	$A_I' = -\beta$	$R_i' = r_\pi = \frac{\beta}{g_m}$	$A_V' = A_I' \times \frac{R_L'}{R_i'} = \frac{-\beta \times R_L'}{r_\pi}$ $A_V' = -g_m R_L' = \frac{-R_L'}{r_e}$ $R_L' = R_L \parallel R_C$	$R_0' = r_0 = \left\lvert\frac{V_A}{I_C}\right\rvert \; [V_A = \infty]$ $R_0' = r_0 = \infty \quad [V_A = \infty]$

CE Amplifier with R_E



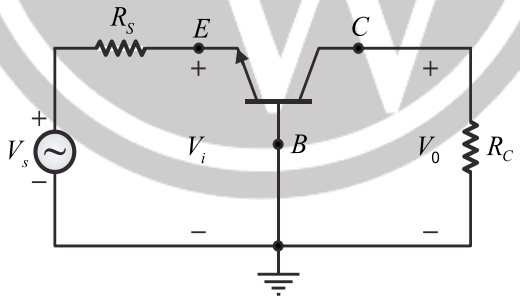
Parameter	Current Gain	Input Resistance	Voltage Gain	Output Resistance
h-model	$A_I' = -h_{fe}$	$R_i' = h_{ie} + (1 + h_{fe}) R_E$	$A_V' = A_I' \times \frac{R_L'}{R_i'}$ $A_V' \approx \frac{-R_L'}{R_E}$ $R_L' = R_C \parallel R_L$	$R_0' = \infty$
r_e model	$A_I' = -\beta$	$R_i' = r_\pi + (1+\beta) R_E$	$A_V' = A_I' \times \frac{R_L'}{R_i'}$ $A_V' = \frac{-\beta R_L'}{r_\pi + (1+\beta) R_E} \approx \frac{-R_L'}{R_E}$ $[(1+\beta) R_E \gg r_\pi]$ $R_L' = R_C \parallel R_L$	$R_0' = \infty \quad [V_A = \infty]$

CC Amplifier



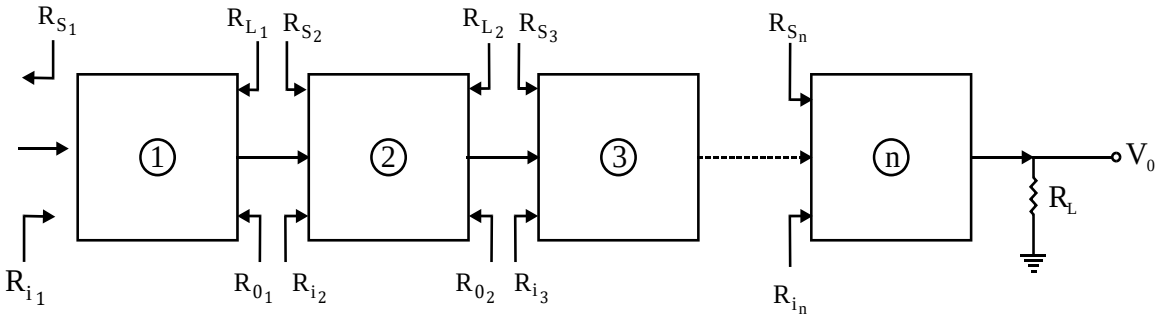
Parameter	Current Gain	Input Resistance	Voltage Gain	Output Resistance
h-model	$A_i' = 1 + h_{fe}$	$R_i' = h_{ie} + (1 + h_{fe})R_L'$	$A_V' = \frac{A_i' R_L'}{R_i'} \approx 1$ $R_L' = R_E \parallel R_L$	$R_0' = \frac{R_S' + h_{ie}}{1 + h_{fe}}$ R_S' = Effective source impedance
r_e model	$A_i' = 1 + \beta$	$R_i' = r_\pi + (1+\beta)R_L'$	$A_V' = \frac{(1+\beta)R_L'}{r_\pi + (1+\beta)R_L'} \approx 1.0$ $R_L' = R_E \parallel R_L$	$R_0' = \frac{R_S' + r_\pi}{1+\beta}$ If $r_\pi > R_S'$ $R_0' = \frac{r_\pi}{1+\beta} \approx \frac{r_\pi}{\beta}$ $R_0' = \frac{r_\pi}{\beta} = \frac{1}{g_m}$

CB Amplifier



Parameter	Current Gain	Input Resistance	Voltage Gain	Output Resistance
h-model	$A_i' = \frac{h_{fe}}{1+h_{fe}} \approx 1$	$R_i' = \frac{h_{ie}}{1+h_{fe}}$	$A_V' = \frac{A_i' R_L'}{R_i'}$ $R_L' = R_C$	$R_0' = \infty$
r_e model	$A_i' = \frac{\beta}{1+\beta} \approx 1$	$R_i' \approx \frac{r_\pi}{1+\beta} \approx \frac{r_\pi}{\beta} = \frac{1}{g_m}$	$A_V' = \frac{1 \times R_L'}{1/g_m} = g_m R_L'$ $R_L' = R_C$	$R_0' = \infty \quad [V_A = \infty]$

Cascade Amplifier (Multistage Effect)



1. $R_{L_1} \neq f\left(R_{01}, R_{sa}\right)$

   $R_{L_1} = f\left(R_{i2}\right)$

2. $R_{s_2} \neq f\left(R_{L1}, R_{i2}\right)$

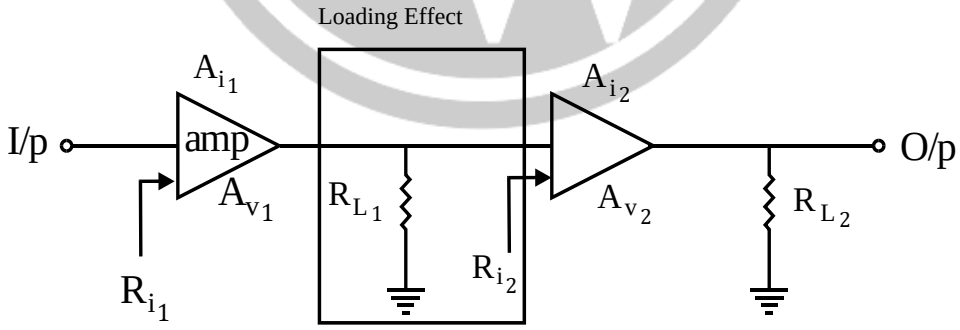
   $R_{s2} = f\left(R_{01}\right)$

3. R_i [cascade] = R_i (1^{st} stage)
4. o/p R_0 (cascade) = R_{0N} (last stage)
5. $A_v = A_{v1} \times A_{v2} \times A_{v3} \times \ldots\ldots A_N$

   (for proper impedance matching)
6. $A_I = A_{i1} \times A_{i2} \times A_{i3} \times \ldots\ldots A_{iN}$

   (for proper impedance matching)

Loading Effect

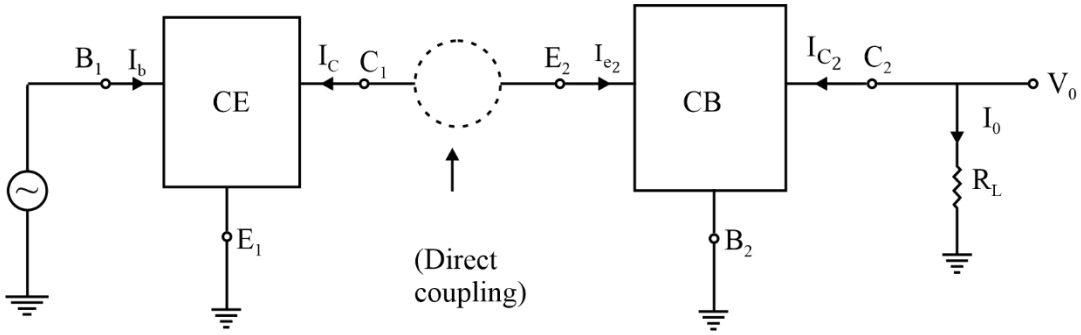


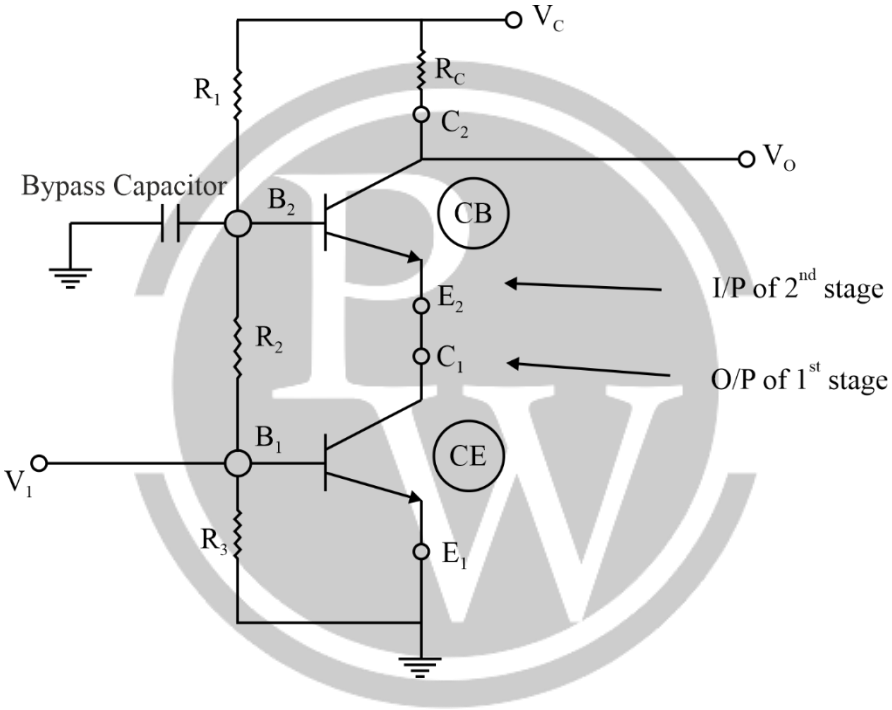
1. The decrease in the gain of first stage due to low value of input impedance of second stage is called Loading effect
2. Loading effect occurs in BJT amplifiers, and not in JFET and MOSFET amplifiers because they have a very high input impedance.

Cascode Amplifier

- A combination of CE followed by CB is referred as Cascode amplifier
- CE acts as input stage and CB acts as output stage.

- Cascode amplifier can amplify both voltage and current
- Also known as direct coupled amplifier because output of CE configuration is directly connected to input of CB configuration.



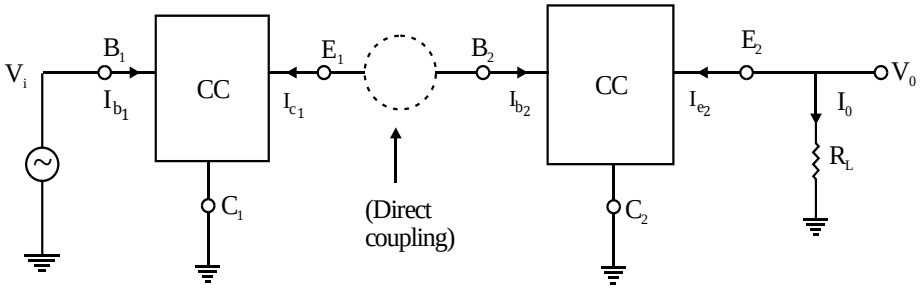


Cascode Amplifier Parameters

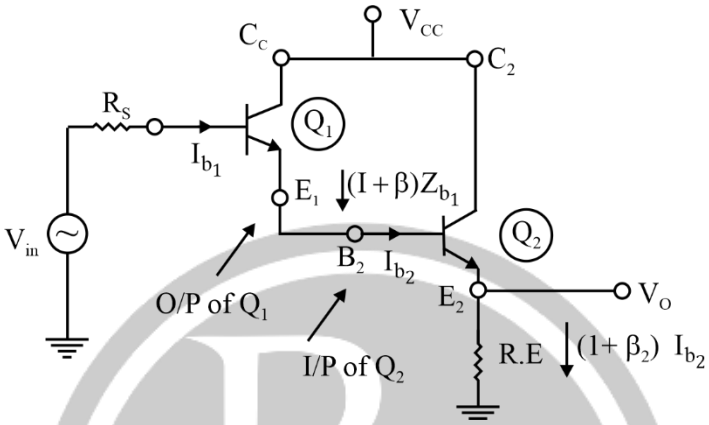
1. Transconductance (g_m) = A_I[CB] × g_m[CE]
2. Input Impedance (R_i) = R_i [CE]
3. Output Impedance (R_O) = R_O [CB]
4. Current Gain (A_I) = A_I [CB] × A_I [CB] > A_I [CE]
5. Voltage Gain (A_V) = A_V [CB] × A_V [CE] > – A_V [CB]

Darlington Pair

- Series combination of two CC configurations.
- Also referred as direct coupled amplifier



4. Circuit diagram of Darlington pair -

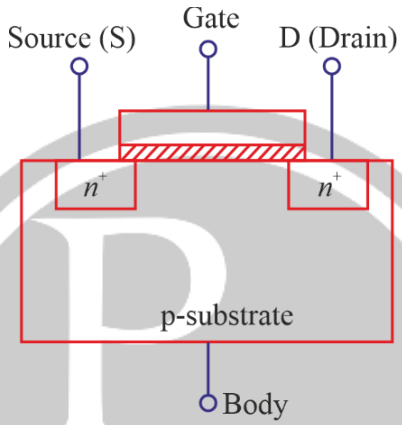


Darlington Amplifier Parameters

1. Transconductance (g_m) = A_i [2nd stage] × g_m[1st stage]
2. Input Impedance (R_i) = R_i [1st stage]
3. Output Impedance (Ro) = R_O [2nd stage]
4. Current Gain (A_i) = A_i [1st stage] × A_i [2nd stage]
5. Voltage Gain (A_v) = 1

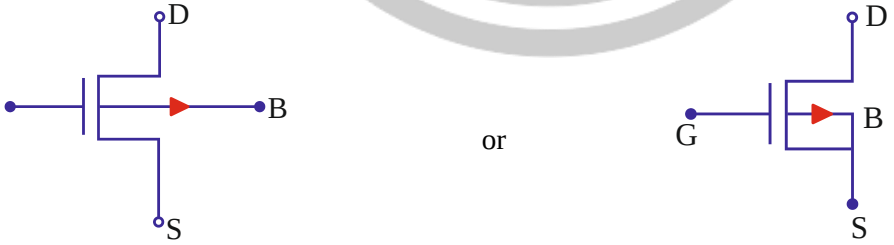
5 MOSFET AMPLIFIER WITH BIASING

5.1. MOSFET

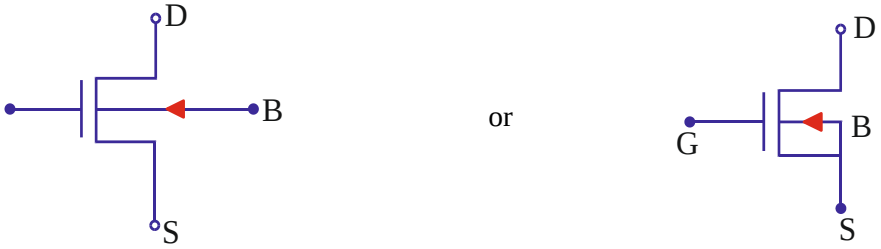


- **Source :** terminal through which majority charge carrier enters into the SC bar.
- **Drain :** terminal through which majority charge carriers leaves the SC bar.
- **Channel:** path between source & drain by which majority carrier travel from source to drain
- **Gate :** Terminal to control the flow of charge carrier from source to drain

Symbol :



- P-channel Enhancement type MOSFET :



- N-channel Enhancement type MOSFET.

Channel Current

The current flowing from source to drain via the channel. It is a function of aspect ratio of MOSFET and applied voltages V_{GS}, and V_{DS}.

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

Trans Conductance :

It is a figure of merit indicates that how well a transistor convert the voltage to the current

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS} = \text{const.}}$$

In cut-off Region:

MOSFET works as an OFF switch.

$V_{GS} < V_T$

$I_D = 0$

In Triode Region:

MOSFET works as a resistor

$V_{GS} > V_T$

$V_{DS} > (V_{GS} - V_T)$

$$I_D = \frac{1}{2}\mu_n Cox\frac{W}{L}\left[(v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$\frac{\partial I_D}{\partial V_{GS}}\bigg|_{(V_{DS} = \text{const.})} = g_m = \mu_n Cox\frac{W}{L}v_{DS}$$

In Saturation region :

MOSFET works as on ON switch

$V_{GS} >> V_T$

$v_{DS} = v_{GS} - v_{TH}$

$$\boxed{I_{D\,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[v_{GS} - v_{TH}]^2}$$

and

$$g_m = \mu_n C_{ox}\frac{W}{L}[v_{GS} - v_{TH}]$$

$$g_m = \frac{2I_{D\,sat}}{v_{GS} - v_{TH}}$$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D}$$

MOSFET Biasing

- Biasing is a process of applying the operating point of device.
- Three operating regions.

  Cut-off $V_{GS} < V_T$

  Linear: $V_{GS} > V_T \,|\, V_{DS} < V_{GS} - V_T$

  Saturation: $V_{GS} > V_T \,|\, V_{DS} < V_{GS} - V_T$

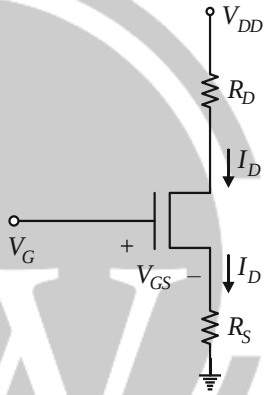
- There are three types of biasing

  (1) Fixed bias

  (2) Drain to base bias

  (3) Potential divider bias

1. Fixed Bias Configuration:



by kVL

$$V_G - V_{GS} - I_D R_S = 0$$

$$\Rightarrow \quad V_{GS} = V_G - I_D R_S$$

Assume operating in saturation mode

Find I_D from standard drain current equation

kVL in output loop

$$V_{DD} - I_D R_D - V_{DS} - I_D R_s = 0$$

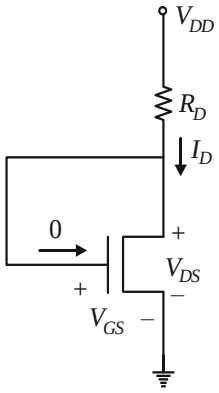
$$\Rightarrow \quad V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Now checks VDS & $V_{GS} - V_T$ condition for saturation.

True $\rightarrow$ assumption correct

False $\rightarrow$ assumption false, assume linear & solve again.

2. Drain to Gate Bias



As $V_{DS} = V_{GS}$

$V_{DS} > V_{GS} - V_T$

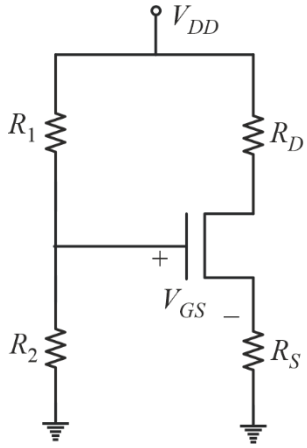
MOS biased in saturation region.

Applying KVL $V_{DD} - I_D R_D - V_{DS} = 0$

$V_{DS} = V_{DD} - I_D R_D$

as saturation, $I_D = k[V_{GS} - V_T]^2$

3. Potential Divider Bias



By voltage division

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$I_S = I_D$$

$$V_{GS} = V_G - I_D R_S$$

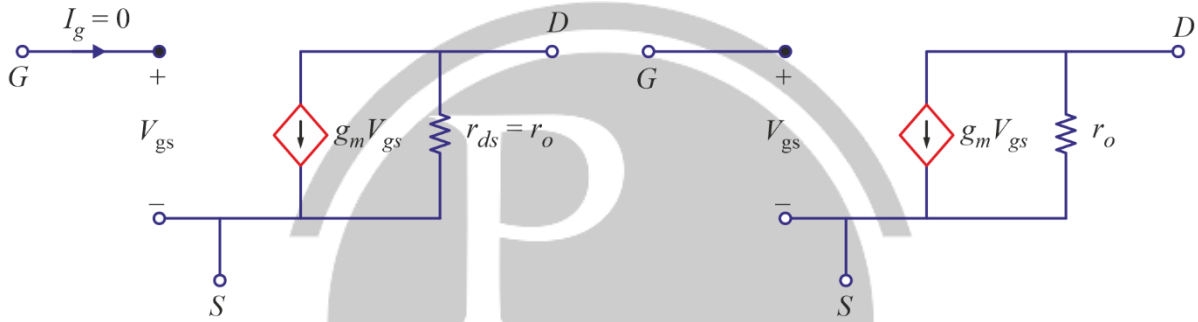
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Assume saturation, $I_D = k\left[V_{GS} - V_T\right]^2$ find I_D, V_{GS}, V_{DS}

$V_{DS} > V_{GS} - V_T$ saturation.
otherwise assume active.

Small Signal (or) AC Analysis

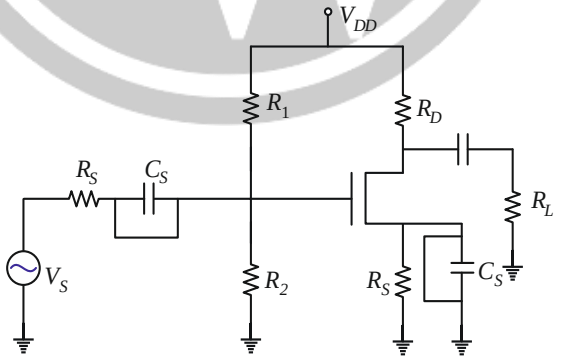
(nMOS) **(pMOS)**

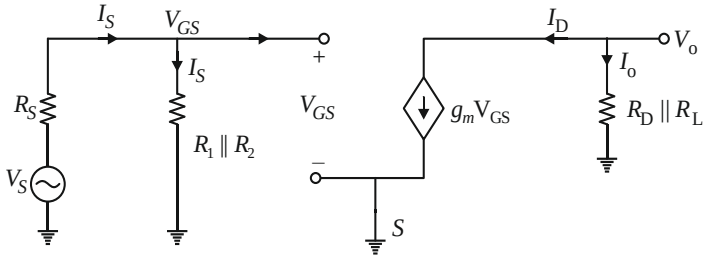


If no channel length modulation (λ = 0).

$$V_A = \frac{1}{\lambda} = \infty; \quad r_{ds} = r_o = \frac{V_A}{I_D} = \infty$$

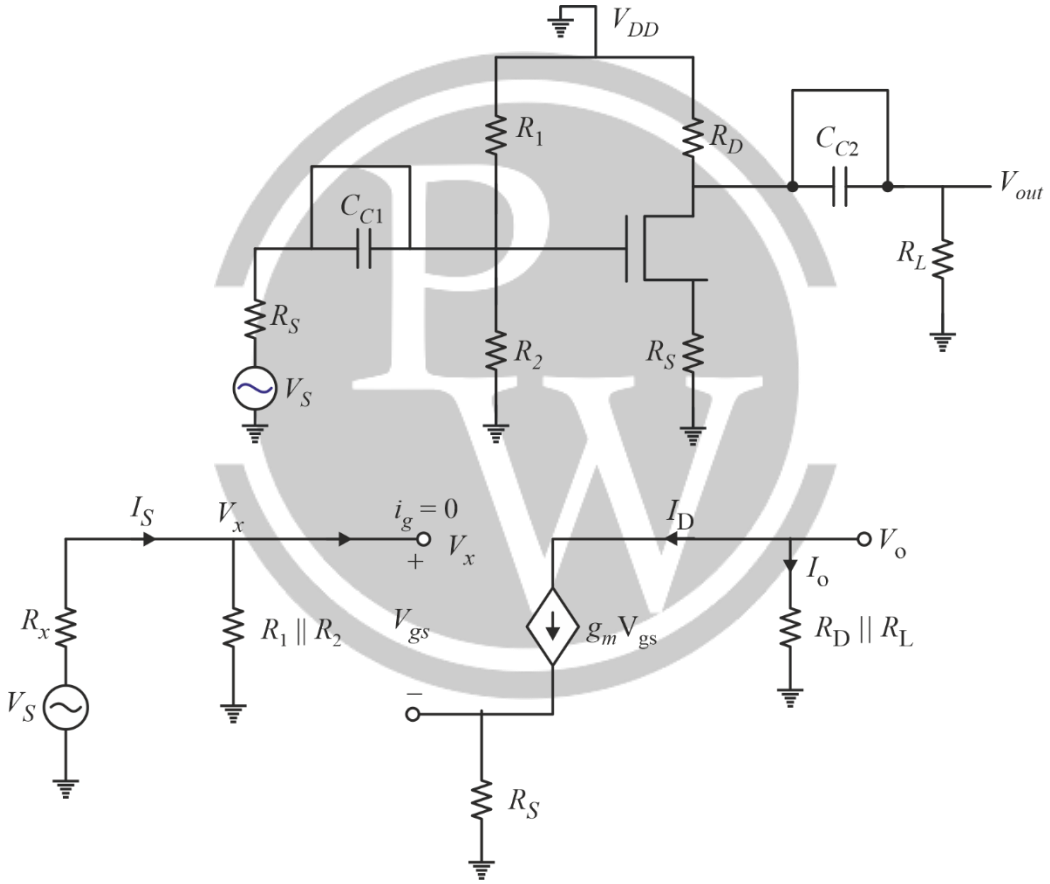
(a) RC Coupled amplifier with Coupling Capacitor





1. $I_S = \dfrac{V_{GS}}{R_1 \| R_2}$
2. $I_0 = -g_m V_{GS}$
3. $A_I = -g_m \left[R_1 \| R_2\right]$
4. $R_{in} = R_s + [R_1 \| R_2]$
5. $V_S = I_S \cdot R_{\text{in}}$
6. $V_0 = -g_m V_{GS}\ (R_D \| R_L)$
7. $A_V = \dfrac{V_0}{V_S} = -\dfrac{g_m (R_D \| R_L)}{R_{\text{in}}} [R_1 \| R_2]$
8. $R_{\text{out}} = R_D (\text{Load open})$

(b) RC coupled amplifier without bypass capacitor:



$$i_o = -g_m v_{gs}$$

$$V_o = -[R_L \| R_D]\, g_m V_{gs}$$

$$R_{\text{in}} = R_x + [R_1 \| R_2]$$

$$Vx = V_{gs} + g_m V_{gs} R_s$$

$$= (1 + g_m R_s) V_{gs}$$

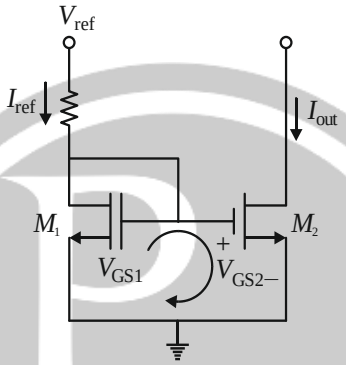
$$V_x = \frac{R_1 \| R_2}{(R_1 \| R_2 + R_2)}$$

$$\Rightarrow \quad Vx = \left[\frac{R_1 \| R_2 + R_x}{R_1 \| R_2}\right](1 + g_m R_s)V_{gs}$$

$$\text{Voltage gain} = \frac{V_o}{V_s}$$

Current Mirror

- It copies the ref current flowing at the input of the system to the output.
- It is also known as practical current source.
- It is designed by using IC technology.



$$V_{GS1} = V_{GS2} = V_{GS}$$

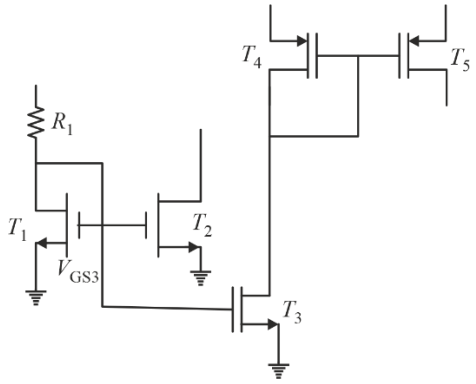
$$I_{ref} = \frac{1}{2}\mu_x C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2 \quad \ldots(1)$$

$$I_{out} = \frac{1}{2}\mu_x C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2 \quad \ldots(2)$$

$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1}$$

as now output current is independent of output resistance, if $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \rightarrow \boxed{I_{out} = I_{ref}}$

MOS Current Steering Circuit:



T_1 and T_2 are in current mirror.

$$\Rightarrow \quad I_{D_2} = I_{\text{ref}}\left[\frac{(W/L)_2}{(W/L)_1}\right]$$

T_1 and T_3 are in current mirror.

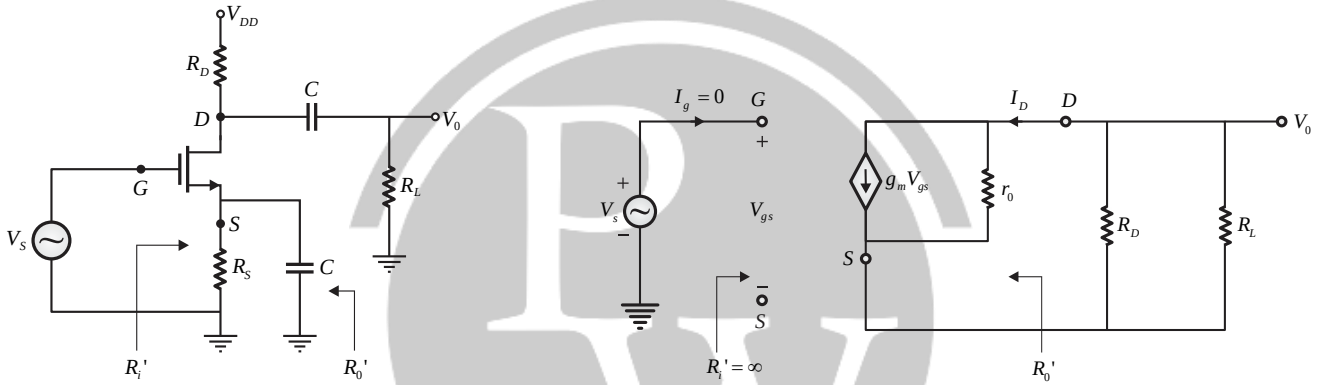
$$I_{D_3} = I_{\text{ref}}\left[\frac{(W/L)_3}{(W/L)_1}\right]$$

T_4 and T_5 are in current mirror $\rightarrow$ pMOS

$$I_{D_5} = I_{D_4}\left[\frac{(W/L)_5}{(W/L)_4}\right] = I_{D_3}\left[\frac{(W/L)_5}{(W/L)_4}\right]$$

5.2. MOSFET Amplifiers

Common Source MOSFET Amplifier without R_S and its AC Equivalent circuit



(a) CS MOSFET amplifier without Rs **(b) AC equivalent of CS MOSFET amplifier without Rs**

Common Source MOSFET Amplifier with R_S and its AC Equivalent circuit

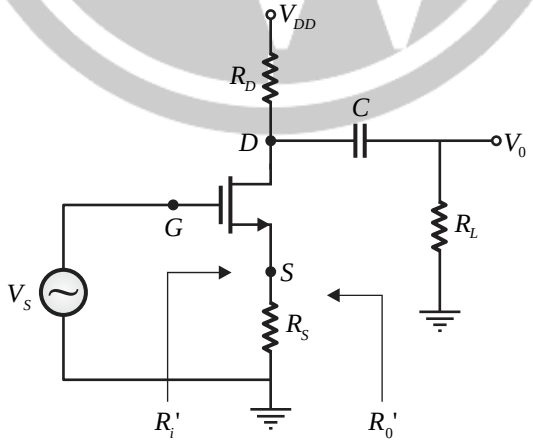


Fig. (a) CS MOSFET amplifier with Rs

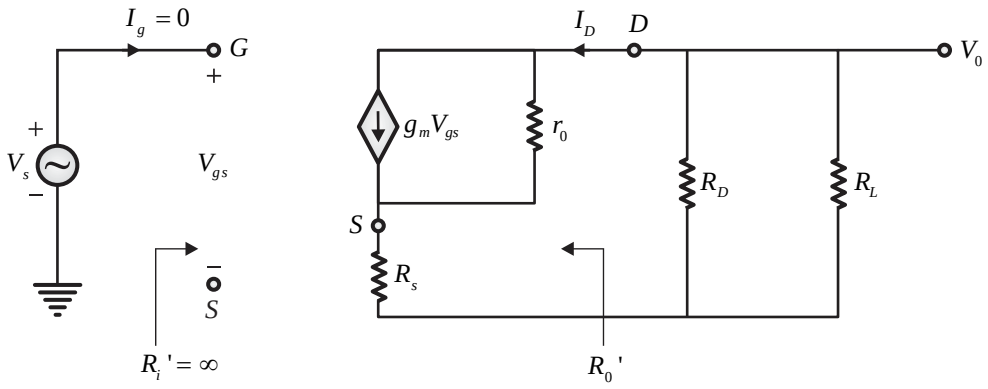
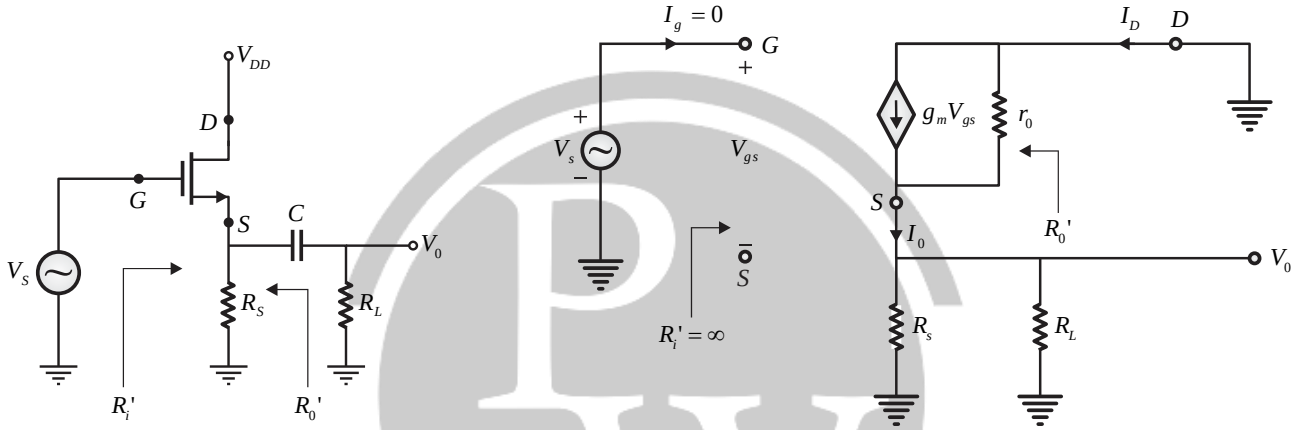


Fig. (b) AC equivalent of CS MOSFET amplifier with R_S

Common Drain MOSFET Amplifier and its AC Equivalent circuit



(a) CD MOSFET amplifier (n-channel enhancement) **(b) AC equivalent of CD MOSFET amplifier**

Common Gate MOSFET Amplifier and its AC Equivalent circuit

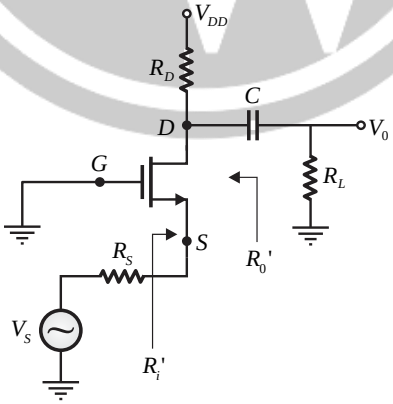


Fig. (a) CG MOSFET amplifier (n channel enhancement)

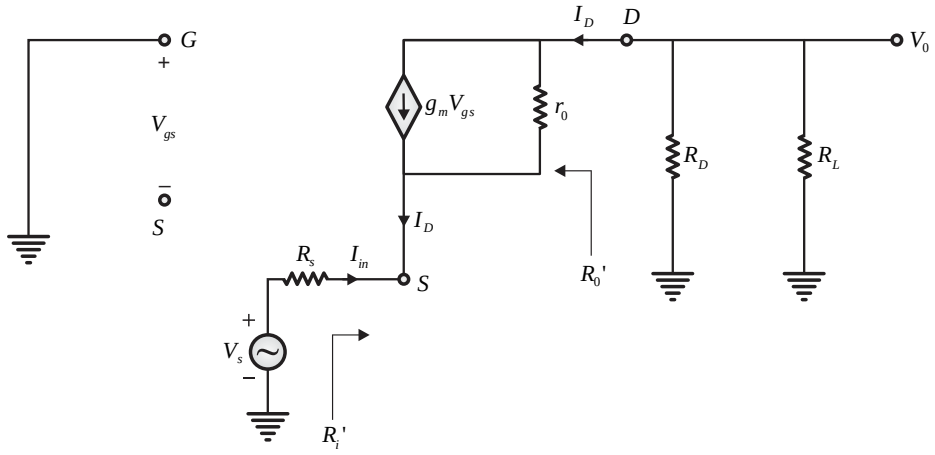


Fig. (b) AC equivalent of CG MOSFET amplifier

MOSFET Amplifiers AC Parameters

AC parameter	CS without R_S	CS with R_S	Common drain	Common Gate
Input resistance	$R_i' = \infty \ [\because I_g = 0]$	$R_i' = \infty \ [\because I_g = 0]$	$R_i' = \infty$	$R_i' \approx \frac{1}{g_m}$
Output resistance	$R_0' = r_0 \ [\lambda \neq 0]$ $R_0' = \infty \ [\lambda = 0] \ \left[r_0 = \frac{1}{\lambda I_D}\right]$	$R_0' = r_0 + (1+\mu)R_S$ $R_0' = \infty \ [\text{if } \lambda = 0 \Rightarrow r_d = \infty]$	$R_0' \approx \frac{1}{g_m}$	$R_0' = r_0 + R_S(1+\mu)$ $R_0' = \infty \ [\text{if } \lambda = 0 \Rightarrow r_0 = \infty]$
Voltage gain	$A_V' = -g_m R_L''$ $(R_L'' = r_0 \parallel R_D \parallel R_L)$	$A_V' = \frac{-\mu R_L'}{R_L' + r_0 + R_S(1+\mu)}$ $(R_L' = R_D \parallel R_L)$	$A_V' = \frac{g_m R_L'}{1 + g_m R_L'}$ $(R_L' = R_s \parallel R_L)$	$A_V' = g_m R_L''$ $(R_L'' = r_0 \parallel R_D \parallel R_L)$
Current gain	Does not exist $[I_g = 0 \text{ A}]$	Does not exist $[I_g = 0 \text{ A}]$	Does not exist $[I_g = 0 \text{ A}]$	$A_I' = 1.0$

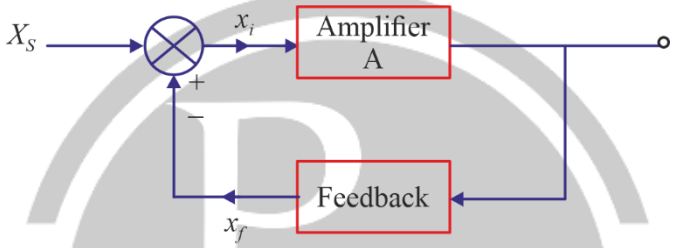
❐❐❐

6 FEEDBACK AMPLIFIERS

6.1. Introduction

6.1. Feedback

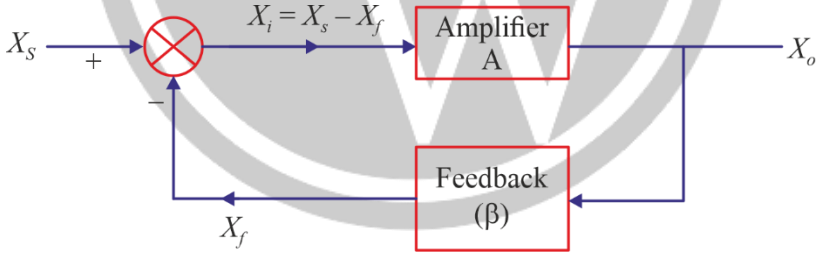
It is a process of taking sample from output and mix with input.



According to type of mixing two types of feedback.

I. Negative Feedback

If sample gets subtracted from supply.



1. Overall Gain:

$$A_F = \frac{A}{1 + A\beta}$$

gain reduced by $(1 + A\beta)$

if $A\beta >> 1 \Rightarrow \boxed{A_f = \frac{1}{\beta}}$

2. Bandwidth:

$$\text{Gain} \times \text{B.W.} = \text{Constant}$$

$$\Rightarrow \quad (\text{B.W.})_f = (\text{BW})(1 + A\beta)$$

so, bandwidth increased by $(1 + A\beta)$

3. Noise and Distortion

without feedback:

$$V_o = AV_i + V_N + V_o$$

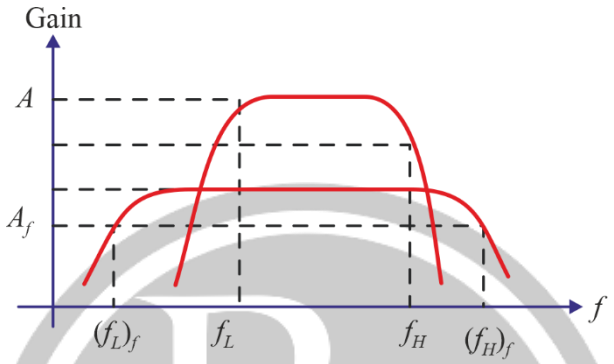
with Feedback

$$V_o = A(V_s - \beta V_o) + V_N + V_D$$

$$\Rightarrow \quad V_o = \frac{AV_s}{1+A\beta} + \frac{V_N}{1+A\beta} + \frac{V_D}{1+A\beta}$$

Hence, noise and distortion reduced by $(1 + A\beta)$

4. Frequency Response:



5. Gain Sensitivity:

$$S_g = \frac{\partial A_f / A_f}{\partial A / A} = \frac{A}{A_f} \times \frac{\partial A_f}{\partial A}$$

$$= \frac{A}{\left(\frac{A}{1+A\beta}\right)} \times \frac{\partial}{\partial A}\left[\frac{A}{1+A\beta}\right]$$

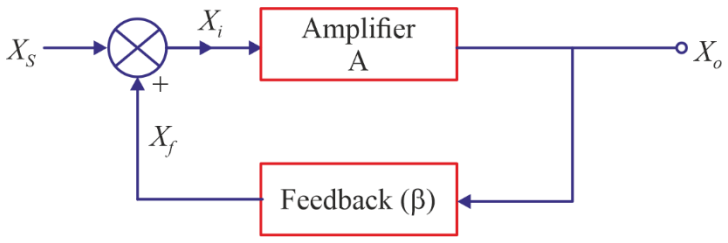
$$= (1+A\beta)\left[\frac{(1+A\beta) - A\beta}{(1+A\beta)^2}\right] = \frac{1}{1+A\beta}$$

6. Desensitivity

$$D = \frac{1}{S_g} = (1+A\beta)$$

II. Positive Feedback

If sampled signal gets added with input then it is called as positive feedback.



(a) Gain:

$$A_f = \frac{X_o}{X_s} = \frac{X_i A}{X_i - X_f} = \frac{X_i A}{X_i - A\beta X_i}$$

$$\Rightarrow \quad X_o = \left[\frac{A}{1 - A\beta}\right] X_S$$

$$\Rightarrow \quad \boxed{A_F = \frac{A}{1 - A\beta}} \text{ practically } |A\beta| < 1.$$

Effects:

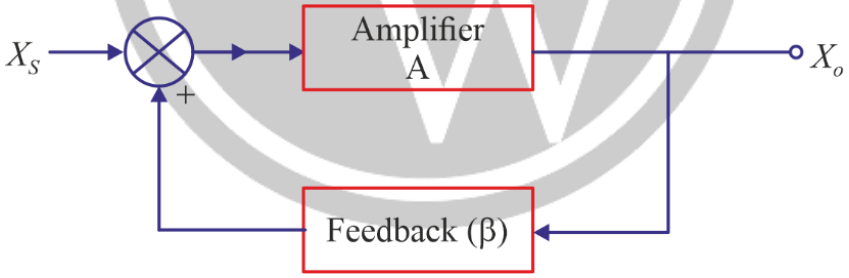
1. Reduces bandwidth of system.
2. Increase noise, as well as distortion of system.

Negative feedback amplifiers classificed into 4-types.

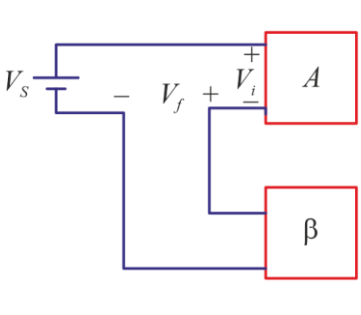
1. Series Series Feedback
2. Series Shunt Feedback
3. Shunt Series Feedback
4. Shunt Shunt Feedback

6.2. Classification of Amplifier

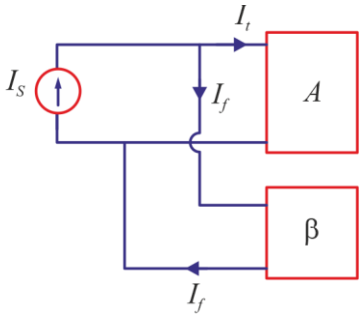
In the feedback amplifier



A Mixter Network

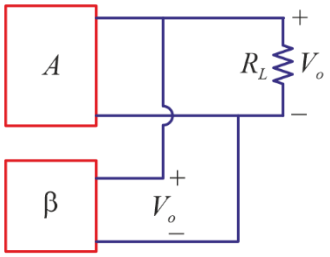


Voltage Mixing
$V_i = V_s - V_f$
R_i increase

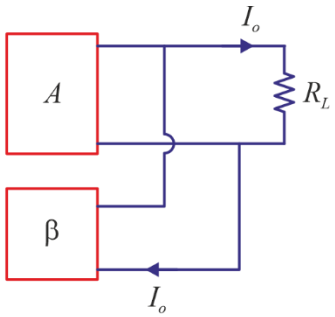


Current Mixing
$I_i = I_s - I_f$
R_{in} decrease

B-Sampling Network

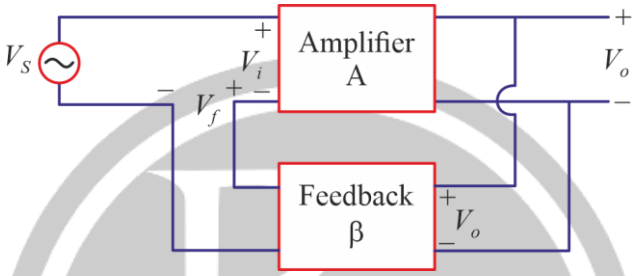


Voltage Sampling
R_o decrease



Current Sampling
R_o increase

(1) Series-Shunt Feedback: (Voltage Amplifiers)



Observations:

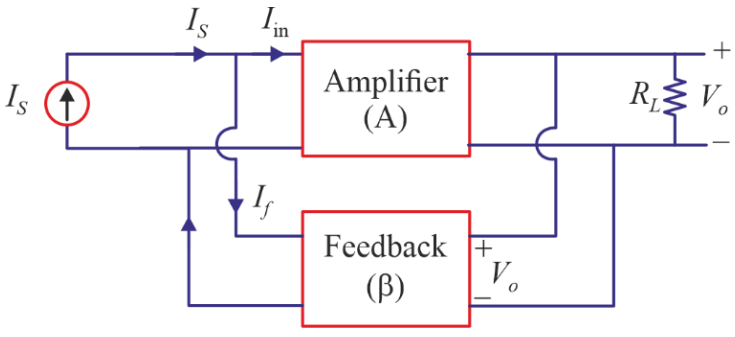
$$\text{Gain} = \frac{A_V}{1+A_V\beta}$$

$$\text{Bandwidth} = BW\left[1+A_V\beta\right]$$

$$(R_{in})f = R_i[1+A_V\,\beta]$$

$$(R_o)f = \frac{R_o}{1+A_V\beta}$$

(2) Shunt-Shunt Feedback : (Trans-resistance Amplifiers)



Gain:

$$I_f = \beta V_o$$

$$I_{in} = \left(I_f - \beta V_o\right)\cdot\frac{R_s}{R_s+R_{in}}$$

$$V_o = R_M I_{in}\left[\frac{R_L}{R_L+R_o}\right] = R_m\left[\frac{R_L}{R_L+R_o}\right]\left[\frac{R_S}{R_S+R_{in}}\right] = (R_m)\,f\,(I_s-\beta V_o)$$

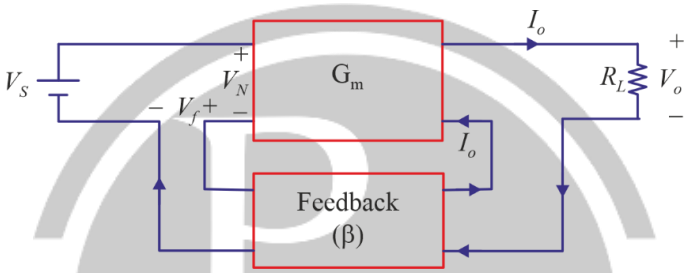
$$V_o[1+\beta(R_m)] = I_S R_{ms}$$

$$\Rightarrow \quad \boxed{\frac{V_o}{I_s}=\frac{R_{ms}}{1+\beta R_{ms}}}$$

Observations:

1. Gain $(R_m)_f = \frac{R_{ms}}{1+R_{ms}\beta}$ decreased.
2. $(R_i)_f = \frac{R_i}{1+R_{ms}\beta}$ decreased
3. $(R_o)_f = \frac{R_o}{1+R_{ms}\beta}$ decreased.

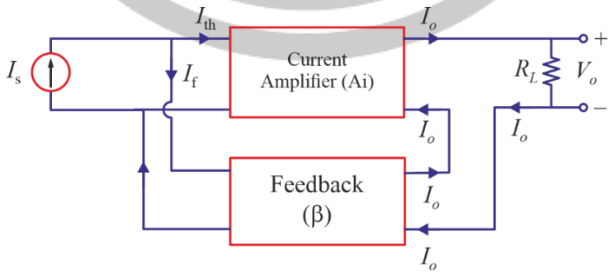
3. Series-Series Feedback Current Series Feedback (Trans-Conductance Amplifier)



Observations:

1. $\frac{I_o}{V_s}=\frac{G_{ms}}{1+G_{ms}\beta}$
2. $(R_{in})_f = R_{in}(1+G_m\beta)$
3. $(R_o)_f = R_o(1+G_m\beta)$

4. Shunt-Series Feedback : (Current Amplifier)



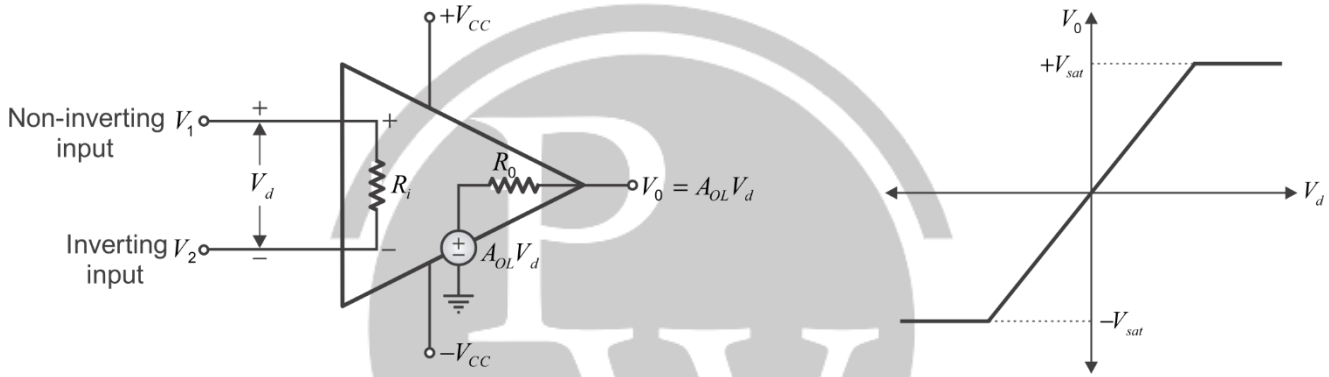
Observations:

1. $\frac{I_o}{I_s}=\frac{A_I}{1+A_I\beta}$
2. $(R_{in})_f = \frac{R_{in}}{1+A_I\beta}$
3. $(R_0)_f = R_0[1+A_I\beta]$

7 OPERATIONAL AMPLIFIERS

7.1. Op-amp

A difference amplifier (amplifies the difference between two inputs)



where, $V_d = V_1 - V_2$

Op-amp Characteristics/Parameters

1. Open Loop Voltage Gain $\left(A = \frac{V_o}{V_i}\right)$**:** The internal gain of op-amp without any feedback.

   Ideally = ∞; Practically = very high

2. Gain Bandwidth Product (GBW)**:** Unity gain bandwidth product i.e. GBW = 1 refers to be behavior that the gain reduces at the same rate as frequency increases.

3. Input Resistance $\left(R_i = \frac{V_i}{I_i}\right)$**:** It is the internal input impedance of the op-amp.

   Ideally = ∞ ; practically = very high

4. Output Resistance $\left(R_o = \frac{V_o}{I_o}\right)$: Ideally = 0 ; practically = very small

5. CMRR (Common Mode Rejection Ratio) : Metric used to quantify the ability of the device to reject common-mode signals.

   Ideally CMRR is infinite, Practically very high.

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right|$$

- $\text{CMRR in dB} = 20\log\left|\frac{A_d}{A_c}\right| = (A_d)_{\text{dB}} - (A_c)_{\text{dB}}$

6. Slew Rate :

   The maximum rate of change in output voltage per unit of time

$$SR = \left|\frac{dV_0}{dt}\right|_{\max} = \left|\frac{dV_0}{dV_i}\right|_{\max} \times \left|\frac{dV_i}{dt}\right|_{\max} = |A_{CL}| \times \left|\frac{dV_i}{dt}\right|_{\max}$$

Non-Idealities in Op-amp

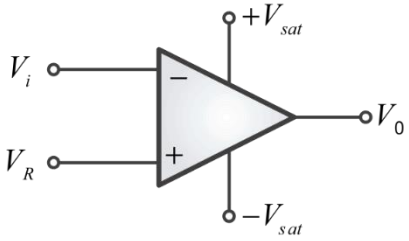
- Offset voltage (V_{OS}): If the two transistors are not perfectly matched, an offset will show up as a non-zero DC offset at the output.
- Bias current (I_{bias}): The transistor inputs actually do draw some current. The bias current is defined to be the average of the currents of the two inputs.
- Offset current (I_{OS}): The difference between the input bias currents.

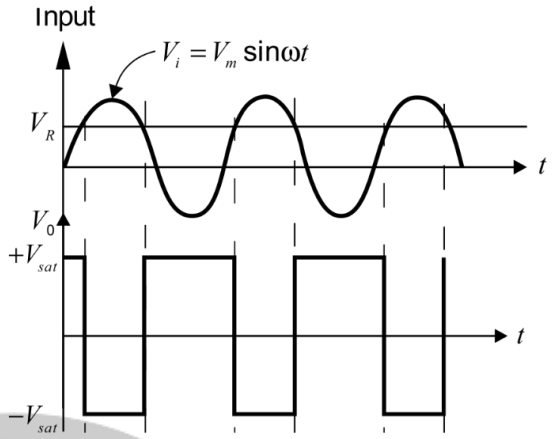
Ideal Op-amp Characteristics

Parameter	Symbol	Ideal
Open loop voltage	A	∞
Unity gain frequency	F_{unity} (GBW)	∞
Input resistance	R_{in}	∞
Output resistance	R_{out}	Zero
Input bias current	I_{bias}	Zero
Input offset current	$I_{\text{in(OS)}}$	Zero
Input offset voltage	$V_{\text{in(OS)}}$	Zero
Slew rate	S_R	∞
Common mode rejection ration	CMRR	∞

7.2. Common Op-amp Circuits

Comparator

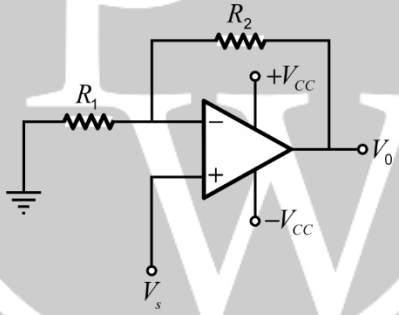




$$V_0 = V_{sat} \;\; ; \;\; V_i > V_R$$

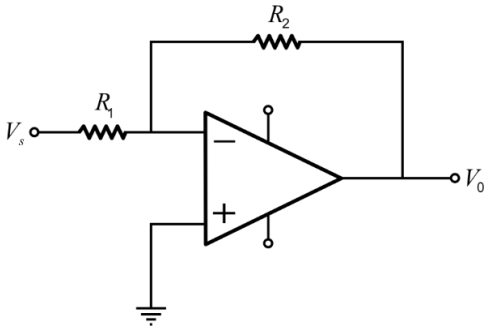
$$V_0 = -V_{sat} \;\; ; \;\; V_i < V_R$$

Non Inverting Op-amp



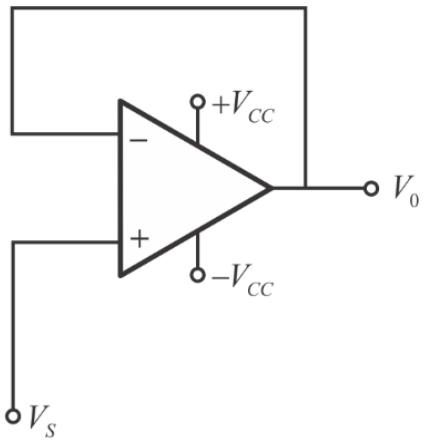
$$\frac{V_0}{V_s} = A_V = \left(1 + \frac{R_2}{R_1}\right)$$

Inverting Op-amp



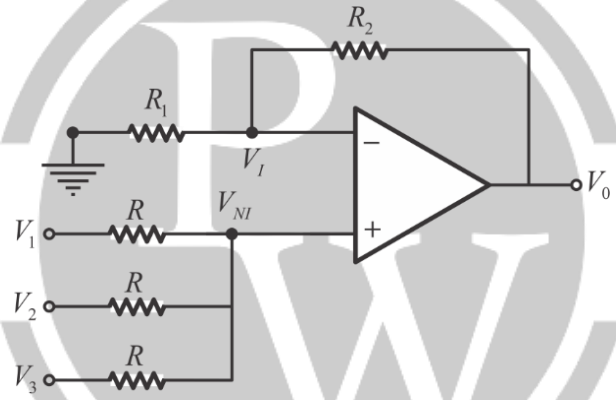
$$\frac{V_0}{V_s} = A_v = \frac{-R_2}{R_1}$$

Voltage Follower



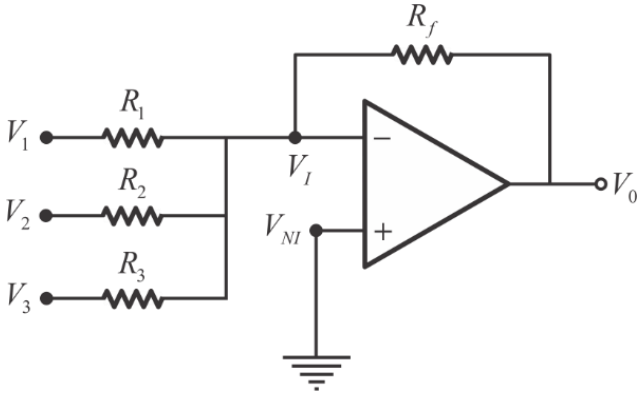
$$V_0 = V_S$$

Non Inverting Summing Amplifier



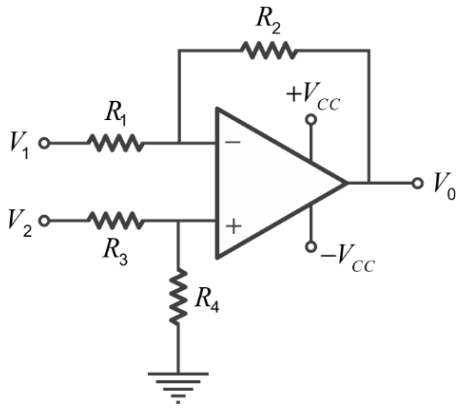
$$V_0 = \frac{1}{3}(V_1 + V_2 + V_3)\left(1 + \frac{R_2}{R_1}\right)$$

Inverting Summer



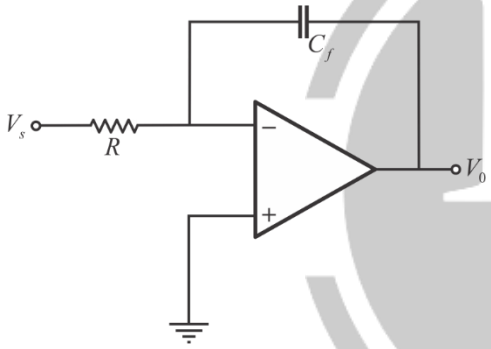
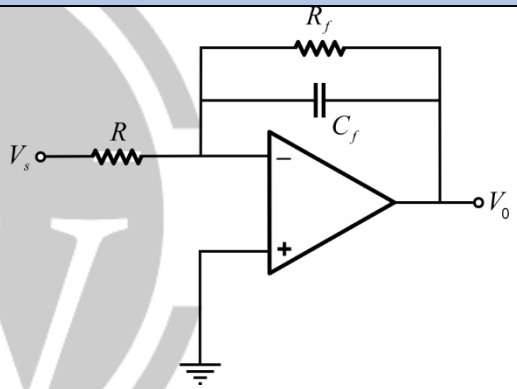
$$V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

Difference/Subtractor

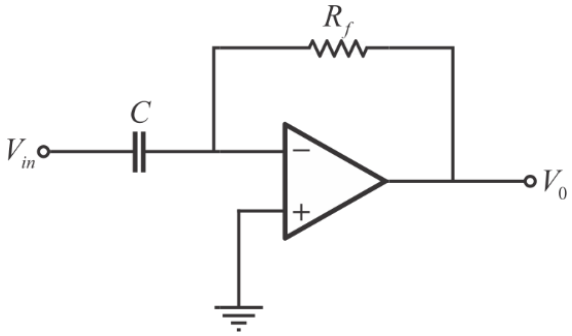
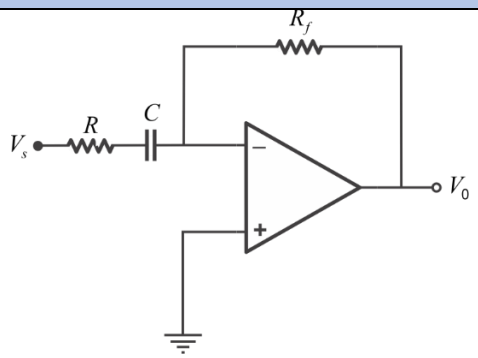


$$V_0 = V_2\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right) - V_1\left(\frac{R_2}{R_1}\right)$$

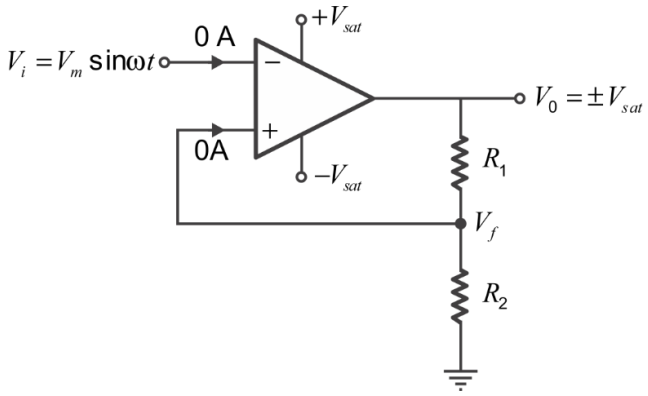
Integrator Circuit

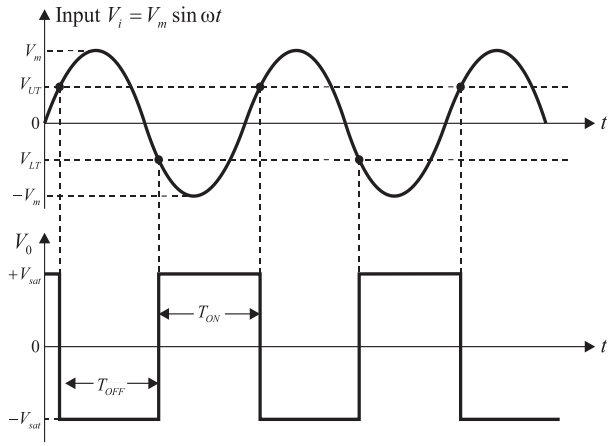
Ideal Integrator	Practical Integrator
	
$V_0 = -\frac{1}{RC_f}\int V_s dt$	$\frac{V_o}{V_S} = \frac{-R_f/R}{sR_fC_f+1}$

Differentiator Circuit

Ideal Differentiator	Practical Differentiator
	
$V_0 = -R_f\, C\frac{d}{dt}V_{in}$	$\frac{V_o}{V_S} = \frac{-sR_fC}{1+sRC}$

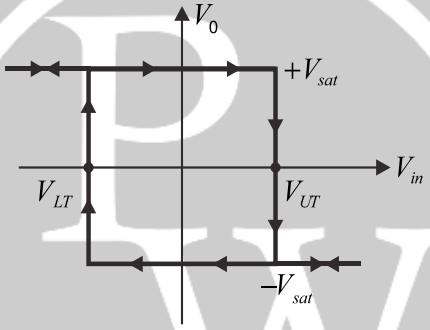
Schmitt Trigger





$$V_{UT} = \frac{V_{sat} R_2}{R_1 + R_2},\ V_{LT} = \frac{-V_{sat} R_2}{R_1 + R_2}$$

Hysteresis Curve:



$$V_H = V_{UT} - V_{LT}$$
$$V_H = \frac{2V_{sat} R_2}{R_1 + R_2}$$

For more questions, kindly visit the library section: Link for web: https://smart.link/sdfez8ejd80if

PW Mobile APP: https://smart.link/7wwosivoicgd4