EEDG 6306 ASIC Design

Introduction

Mini stereo digital audio processor (MSDAP) is fundamentally a programmable finite impulse response (FIR) digital filter for implementing two-channel FIR digital filtering in various audio applications. It is having the lower power consumption, simpler hardware architecture and lower cost compared to a general DSP chip.

Specifications

1. System Settings

- MSDAP performs 2 channel FIR digital filtering based on POT coefficients.
- Two clocks, Data clock and System clock are used to receive inputs and compute outputs respectively.
- Two pins, one for each channel, receive inputs operating at Data clock.
- Inputs (Rj, Coefficients and Inputs) are all received serially at the same pin in order to save the total number of pins used.
- Internal and control signals are provided by the controller based on which MSDAP receives the input and computes the output.
- During the sleeping mode, MSDAP does not compute the output in order to save energy.

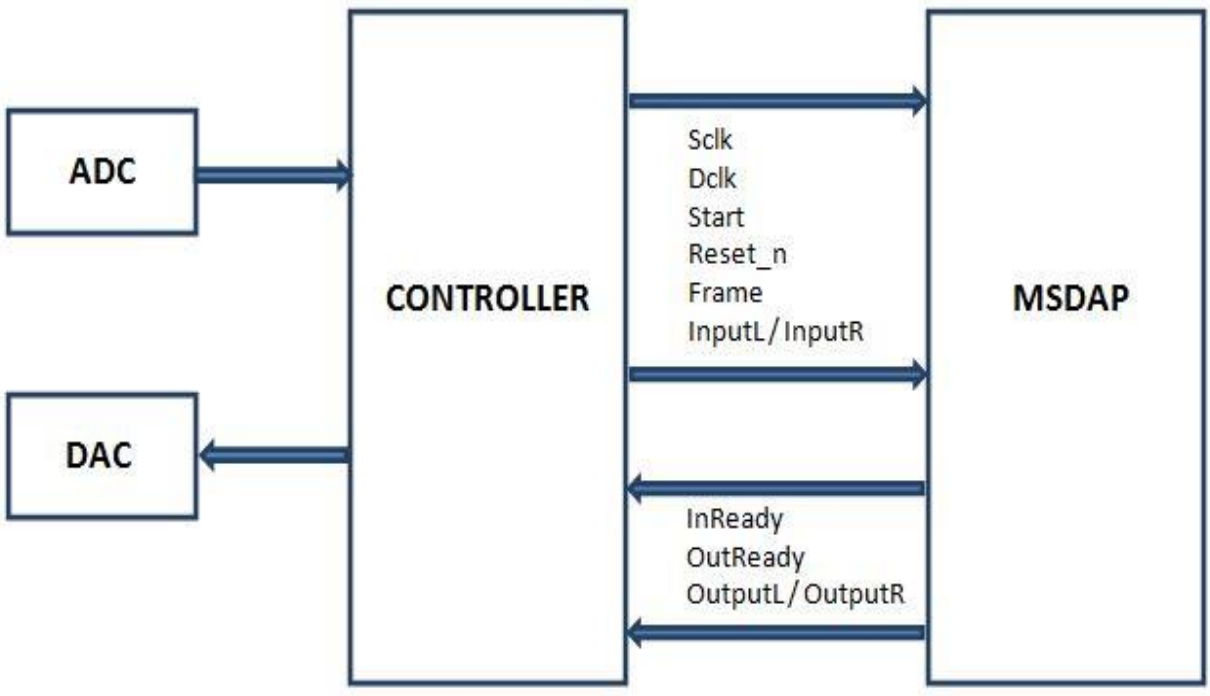


Fig1. Block Diagram of MSDAP

2. Signals

Sclk (Input):

System clock runs at a frequency of 26.88 MHz and provides the timing reference for output, internal and control signals. The output computation is performed at this frequency. The output is updated at falling edge of Sclk.

Dclk (Input):

Data clock runs at a frequency of 768 kHz provides the timing reference for input samples (Rj, Coefficient and InputL/R). The input bits are received at the falling edge of Dclk.

Start (Input):

The chip begins to initialize and memories are cleared when the Start signal is set high. This signal can be asynchronous with Sclk and Dclk. This signal is mandatory because it serves as an "on" button for MSDAP to start.

Reset (Input):

The chip begins to clear the Input samples stored in the memory when Reset signal goes low. When the Reset transitions from low to high, the inputs are received from the beginning. This signal can be asynchronous with Sclk and Dclk. When the chip goes to an indefinite state, reset has to be performed to restart the output computation from the beginning.

Frame (Input):

The beginning of the frame for input samples like Rj, Coefficients and Inputs are denoted by the Frame Signal. This signal is set low for one Dclk when the first bit of input samples/Rj/Coefficients is received and then its set high. Frame is set low only when InReady is set high. Frame signal is the indication that the bit received in the next falling edge of Dclk is the first bit of the next input.

InReady (Output):

InReady is set high when MSDAP is ready to receive the Rj, Coefficients and input samples. Timing reference for this signal is provided by Sclk.

OutReady (Output):

When the chip is ready to send the outputs, OutReady is set low. Once all the 40 bits of the output is transmitted OutReady is set back to high. This signal is aligned to the falling edge of Frame.

InputL (Input):

Inputs Rj, Coefficients and input samples for the left channel are carried by InputL signal. Bit 0 is the sign bit and transmitted first. Bit 15 is the LSB and transmitted last. Inputs are loaded on every falling edge of Dclk.

InputR (Input):

Inputs Rj, Coefficients and input samples for the right channel are carried by InputR signal. Bit 0 is the sign bit and transmitted first. Bit 15 is the LSB and transmitted last. Inputs are loaded on every falling edge of Dclk.

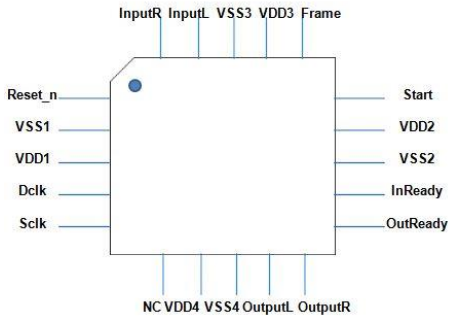
OutputL (Output):

Output samples computed for the left channel are carried by the OutputL signal. Bit 0 is the sign bit and transmitted first. Bit 39 is the LSB and transmitted last. This signal is updated on the falling edge of Sclk and lasts for 40 Sclks. OutputL is aligned with the falling edge of Frame and OutReady. OutputL is set to low when there is no output being sent (OutReady is high)

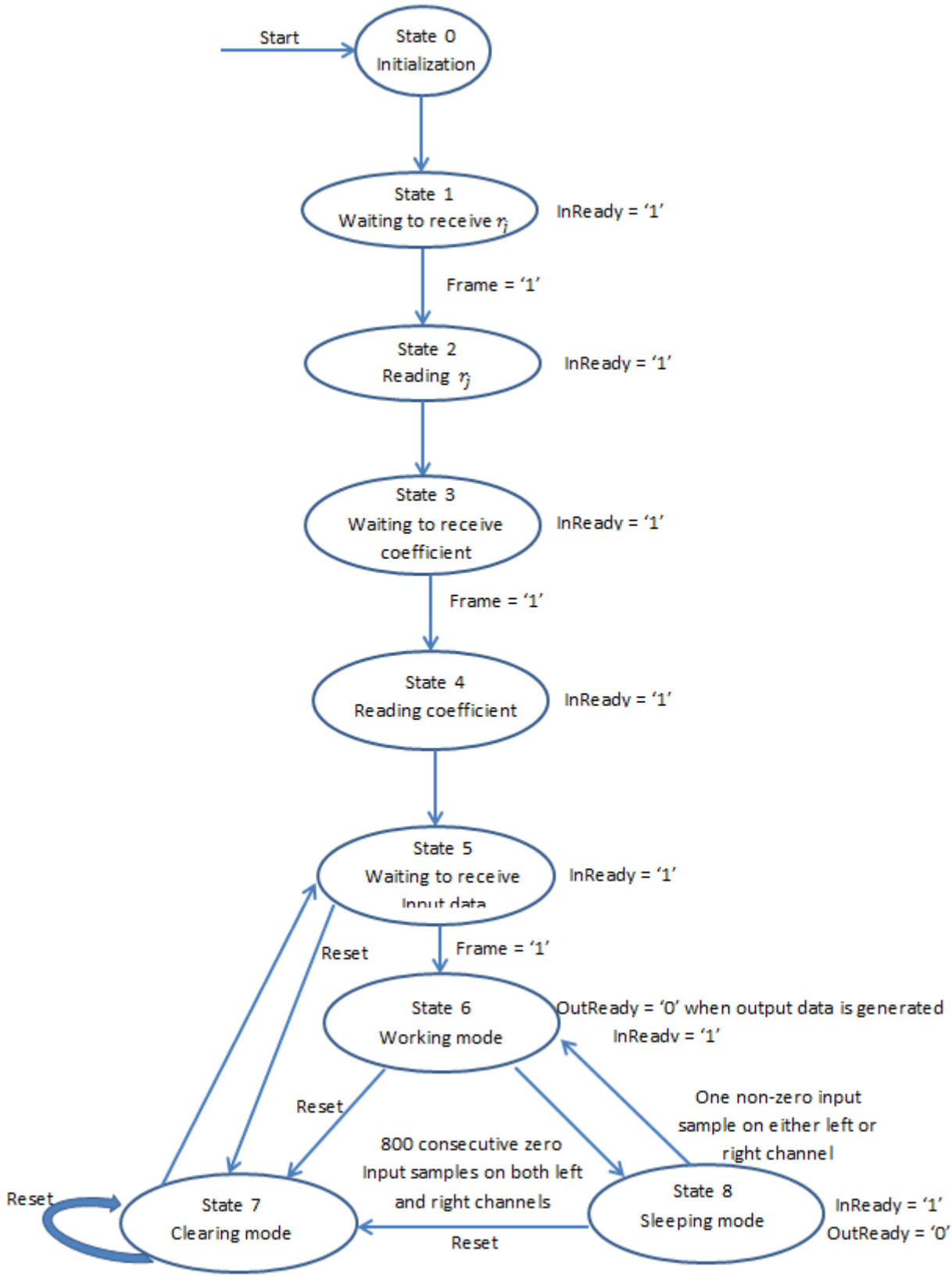
OutputR (Output):

Output samples computed for the right channel are carried by the OutputR signal. Bit 0 is the sign bit and transmitted first. Bit 39 is the LSB and transmitted last. This signal is updated on the falling edge of Sclk and lasts for 40 Sclks. OutputR is aligned with the falling edge of Frame and OutReady. OutputR is set to low when there is no output being sent (OutReady is high)

Pin Diagram



3. Operation Modes



State 0 (Initialization):

The processor waits for Start signal to become high. On Start signal, the initialization process begins which clears all the memories and registers used. Once the initialization is complete, the chip enters State 1.

State 1 (Waiting to receive Rj):

InReady is set to high, indicating that MSDAP is now ready to receive inputs. When Frame is detected to be low, the chip enters State 2.

State 2 (Reading Rj):

In this state, all the 16 bit Rj values are read while InReady remains high. When all the values are loaded, the chip enters State 3.

State 3 (Waiting to receive Coefficients):

InReady is set high, indicating that MSDAP is now ready to receive Coefficients. When Frame is detected to be low, the chip enters State 4.

State 4 (Reading Coefficients):

In this state, all the 16 bit Coefficients are read while InReady remains high. When all the values are loaded, the chip enters State 5.

State 5 (Waiting to receive data):

InReady is set high, indicating that MSDAP is now ready to receive Inputs. When Frame is detected to be low, the chip enters State 6. If Reset is detected low, the chip enters State 7.

State 6 (Working):

Inputs are read continuously on negative edge of Dclk. Convolution computation of input obtained is computed during every Sclk, while next input bits are read during every Dclk. Output computation is completed before the 16 bits of next input are obtained. Outputs are sent when Frame low is detected, on every negative edge of Sclk, for 40 Sclks. OutReady remains low for this period, and then is set to high. InReady remains high as this operation don't affect receiving inputs. If Reset is detected low, the chip enters State 7.If 800 consecutive zero inputs are read in both left and right channels, the chip enters State 8 sending the most recent output calculated.

State 7 (Clearing):

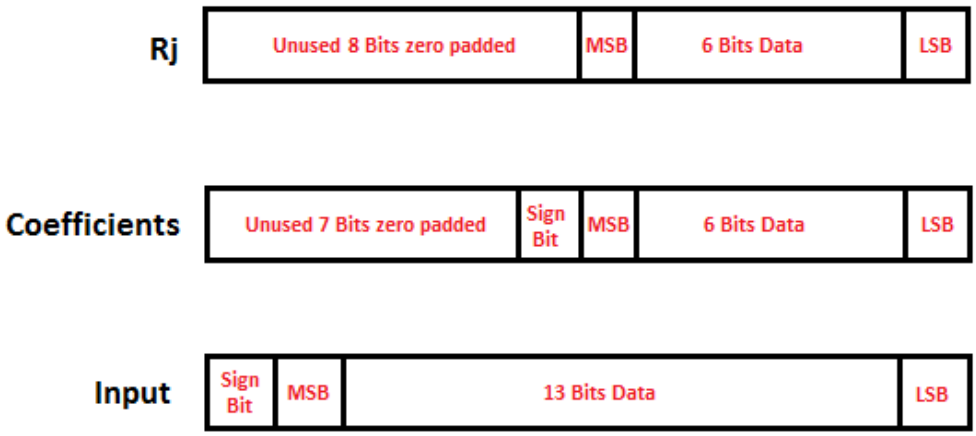
Inready is set low and all the input samples previously loaded except Rj and Coefficents are cleared and the process is repeated untill Reset goes high. When Reset is high, the chip enters State 5.

State 8 (Sleeping):

The Chip enters sleeping mode setting InReady high and remains in the same state until a non zero Input either in the Left or Right channel arrives. Once a non zero value is detected in either of the input channels, the chip enters State 6 and resumes the computation. If Reset is detected low, the chip enters State 7.

4. Data Format

Since only a single pin is used to receive Rj, Coefficients and Input samples, and Input sample has the largest length, all the inputs are converted to 16 Bits. Rj is 8 Bits long and remaining 8 bits are zero padded to the MSB. Coefficients are 9 Bits, remaining 7 bits are zero padded to the MSB. Inputs are 16 bits and occupy the entire frame.



Output is 40 bits long.

5. Steps involved in Output computation:

1. Rj and Coefficients are read and loaded into 16 bit arrays.
2. 16 bit Inputs are stored into 40 bit arrays by left shifting Inputs to 16 bits and sign extended to 8 bits in the MSB.
3. Uj values are accumulated and simultaneously added to the output. For example, when Uj(1) is being accumualted, Uj(0) which was accumulated earlier is added to the output simultaneously.
4. Addition of Uj to output is performed in one Sclk and Shifting of output is performed in the next Sclk in order to avoid data dependency/sequential flow.

5. When the LSB of first Input is received, the computation of first output begins and lasts for 514 Sclks. The computed output is sent when the Frame is low.
6. The first output is sent when the Frame goes low for sending the third Input.

Block Diagram

The architecture of MSDAP is given below. For simplicity only one channel is represented.

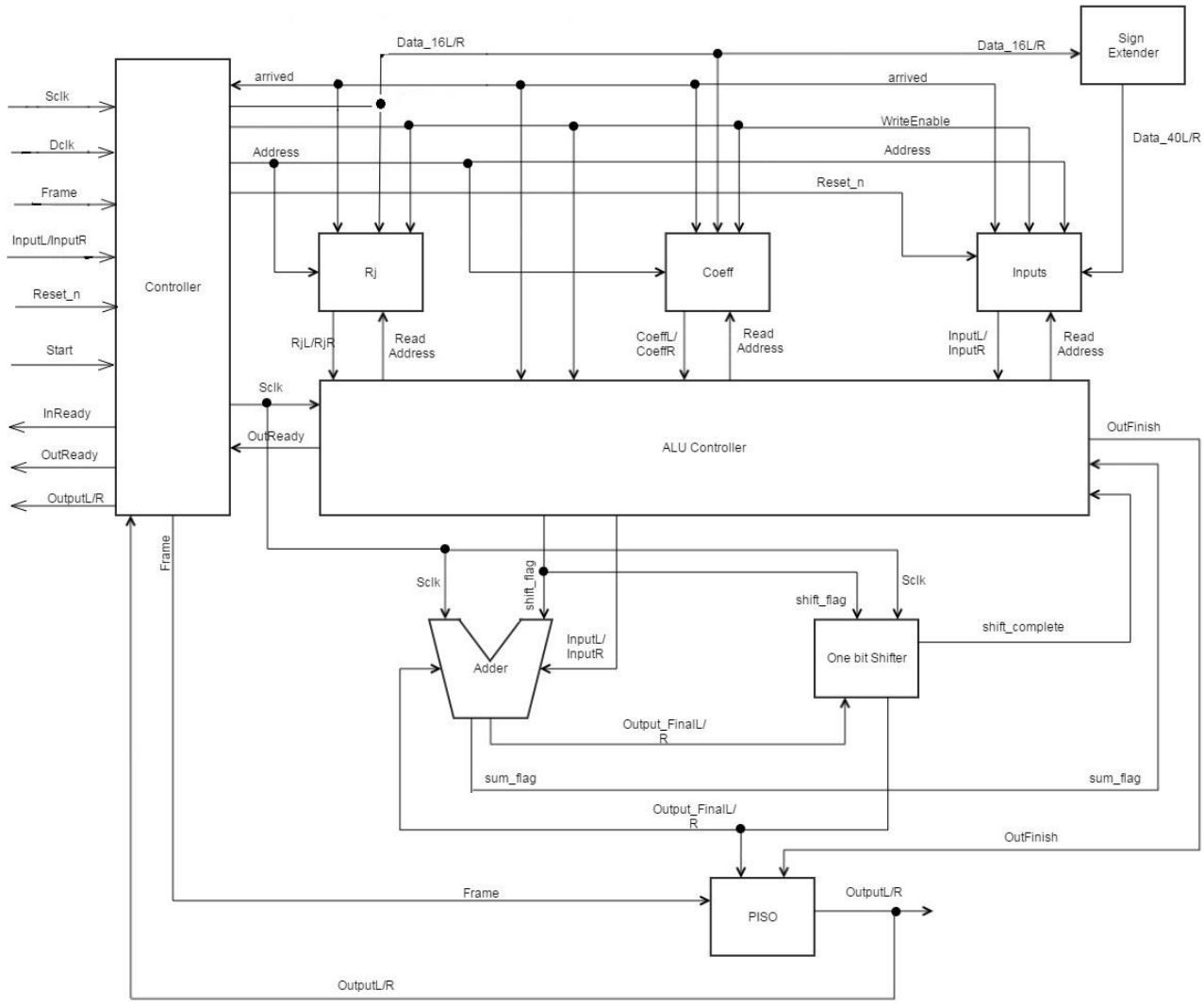


Fig2. MSDAP Architecture

ALU Block

The ALU Block controls the functionality of main blocks which perform the computation. This block operates in Sclk frequency and uses internal counters and logic in order to set certain flags which are used for performing various tasks of the entire convolution. The ALU block is responsible for receiving Rj, Coefficients and 40 bit Inputs from the memory and based on number of values in each Rj, the coefficients are accumulated and output is computed through series of addition and shift.

During the addition, ALU controller passes a memory address to memory blocks to receive the inputs. The computation begins when the first 16-bit input is arrived and involves accumulation where Uj's are either added or subtracted based on the Coefficient value, followed by addition of Uj to the output and shifting the output.

Time Budget and working

The system starts when Start signal is high and this signal is asynchronous with Dclk and Sclk. The computation starts as soon as one 16 bit input is received. The total time available for one output to be computed is 16 Dclks, after which MSDAP has to start computation for the second input.

In our design, Dclk = 768 MHz and Sclk = 26.88 MHz

Total number of Sclks in one Dclk = $\frac{26.88\ \mathrm{MHz}}{768\ \mathrm{KHz}} = 35$

Hence for one computation, total number of Sclks needed = 16 × 35 = 560

For the output computation, an adder is used for addition and accumulation of coefficients and one bit shifter is used to shift the accumulated coefficients by one bit. Loading of Rj, Coefficients and Inputs are done instantaneously at this stage.

Calculation to find out the computation time is as follows:

Total number of coefficients = 512

Time required to compute Uj(0) to Uj(16) = 512

Addition of Uj to Output and shifting is done in a sequential manner. When Uj(0) accumulation is completed, Uj(1) accumulation starts, and at the same cycle accumulated Uj(0) is added to the Output. In the next cycle, Output is shifted by one bit where in Uj(1) accumulation is still happening. Thereby saving the resources and time. All the above operation is with respect to Sclk.

Hence, total time required for computation = 512 + 1 + 1 = 514 Sclks.

The additional two Sclks are to add Uj(15) to output and shift the output by 1. We have performed optimization techniques to reduce the computation clocks. Now that we have saved 46 Sclks, we can reduce the Sclk frequency from 26.88 MHz to 25.344 MHz so that it consumes less power. Another

method is to use 16 adders, which would parallely accumulate all the 16 Uj to increase the computation speed drastically for extra hardware tradeoff.

Functionality of each block and Signals used

Encode & Sign Extender

This block is used for encoding and sign extending the input samples to 40 bits. This is done by assigning bits [15:0] to InputL/R[31:16] and then sign extending by assigning InputL/R[39:32] to 0/1 based on MSB of the received input. The array which stores the input samples are initialized to zero, so zero padding bits InputL/R[15:0] need not require a separate hardware. Input to this block is Data_16L/R and output are encoded and sign extended data of the name Data_40L/R.

Memory Unit for Rj, Coefficients and Inputs

The memory unit stores the input data. It stores up to 16 16-bit words of Rj, 512 16-bit words of coefficients and 40-bit sign extended Inputs. This block is controlled by signals WriteEnable, Address, Data_16L/R, arrived. The main controller sends the required control signals for this block. When WriteEnable is 00, the data Data_16L/R is written to Rj memory. When WriteEnable is 01, Data_16L/R is written to Coefficients memory. When WriteEnable is 10, the Data_16L/R is encoded and sign extended to 40 bit Data_40L/R and then stored in the memory. The address where the inputs are stored are sent by the main controller. When Reset_n goes low, only the 40-bit Input memory is cleared.

ALU Controller

This block provides control signal for blocks like Adder, One bit shifter, PISO and memory and works based on Sclk. The computation starts when WriteEnable is 10 and inputs are received (arrived is 1). The inputs are accessed from the memory using the address. This block is responsible for setting flags shift_flag and OutReady.

Adder

This block adds two operands with respect to Sclk. Accumulation of Uj and addition of Uj's are performed in this block. The output of this block is fed back to the same block for adding all the accumulated Uj's for a single output. A flag sum_flag is set high when addition is complete and this flag is sent to the ALU controller.

One Bit Shifter

This block is controlled by the signal shift_flag. When shift_flag is high, the added output Output_FinalL/R is shifted to right by one bit. A flag shift_complete is set high and sent to the ALU controller indicating that shifting operation is complete, so that ALU can clear the shift_flag to start adding the Uj in the next cycle.

Parallel In Serial Out (PISO)

This block converts the parallel computed output data to serial data. This block is controlled by signals Outfinish and Frame. The computed data Ouput_FinalL/R which is 40 bit long are transmitted bit by bit when Outfinish is set high and Frame is set low.