EEDG 6306 ASIC Design

Specifications

1. System Settings

- MSDAP performs 2 channel (InputL and InputR) FIR digital filtering based on POT (Power of Two) coefficients.
- Two clocks, Data clock and System clock are used to receive inputs and compute outputs respectively.
- Two pins, one for each channel, receive inputs operating at Data clock.
- Inputs (Rj, Coefficients and Inputs) are all received serially at the same pin in order to save the total number of pins used.
- Internal and control signals are provided by the controller based on which MSDAP receives the input and computes the output.
- During the sleeping mode, MSDAP does not compute the output in order to save energy.

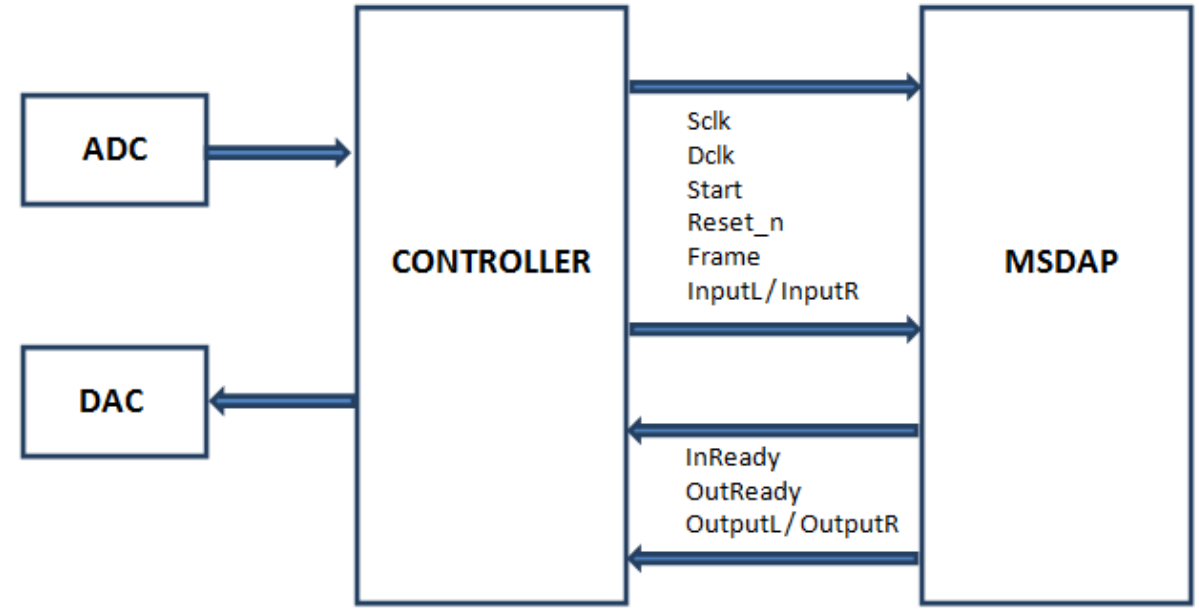

Fig 1. Block Diagram of MSDAP

2. Operation Modes