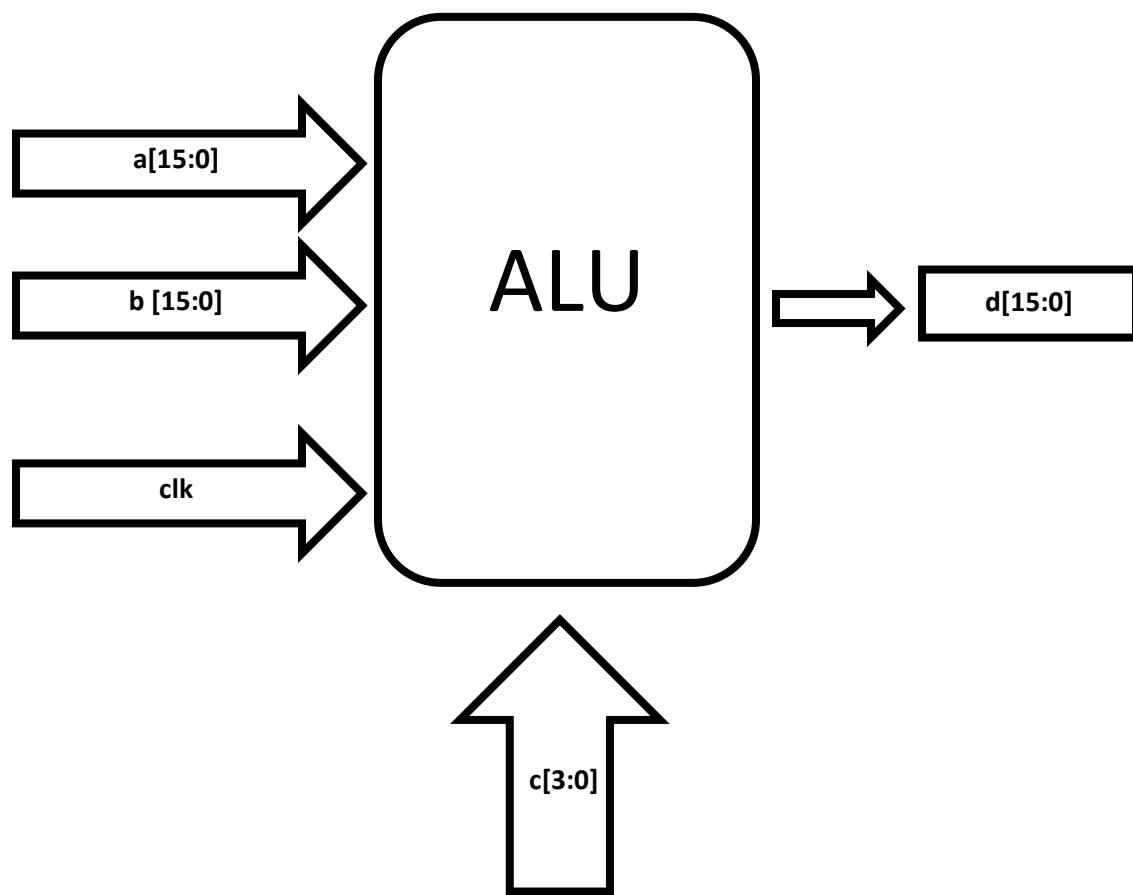


## General Description

Arithmetic and Logical Unit is a critical component of the microprocessor, the core component of central processing unit. ALU comprises the combinational logic that implements logic operations such as AND, OR, NOT, XOR, NAND, NOR, XNOR, and increment, decrement and transfer operations. Even the arithmetic operations such as addition and subtraction are implemented. All the functions are operated on values (16-bit) from the registers.

## Block Diagram



## Parameter Description

a and b : 16 bit input

clk: Clock input

c: Select lines

d: 16 bit output

## Verilog Code

```
Module alu_vr (a,b,c,s,clk,d,e);

input [15:0] a, b, c;
input [3:0]s;
input clk;

output [15:0]d;
output [31:0]e;
reg [15:0]d;
reg [31:0]e;

always@(posedgeclk)

begin

    case(s)

        4'b0000:      d=a&b;           //16-bit and
        4'b0001:      d=a|b;           //16-bit or
        4'b0010:      d=~(a|b);        //16-bit nor
        4'b0011:      d=((~a)&b)|((~b)&a)); //16-bit xor
        4'b0100:      d=~(((~a)&b)|((~b)&a)); //16-bit xnor
        4'b0101:      d=~(a&b);        //16-bit nand
        4'b0110:      d=~a;            //16-bit not
        4'b0111:      d=a+b;           //16-bit add
        4'b1000:      d=a-b;           //16-bit sub
        4'b1001:      d=a+1;           //16-bit increment
        4'b1010:      d=b-1;           //16-bit decrement
        4'b1011:      d=a;             //16-bit input
        4'b1100:      e=(((~(a&b))&c)|((~c)&(a&b)))*c;
        4'b1101:      e=((a&b)*(a|b));
        4'b1110:      e=a*b;
        4'b1111:      e=((~a)&b)*(a&(~b));

    endcase

end
endmodule
```

## INDIVIDUAL GATES DESIGN AND LAYOUT

### Standard cell design and layout:

The inverter layout was drawn in Cadence complying with the IBM 130nm rules. This layout was then extracted and simulated using HSPICE. In general, standard cells dimensions have to be chosen to achieve optimum EDP (Energy delay product). It was observed that with increase in transistor widths, the EDP was found to decrease till it reaches a minimum and increases from there upon.

The energy drawn from the supply is given by

$$E = (C_{load} + C_{self})V_{DD}^2$$

$C_{self}$  is directly proportional to width of the transistor. When width is less,  $C_{load}$  is much greater than  $C_{self}$ . For smaller values of width, Energy is constant. When width increases,  $C_{self}$  increases. When the value of  $C_{self}$  becomes comparable with  $C_{load}$ , Energy increases with width.

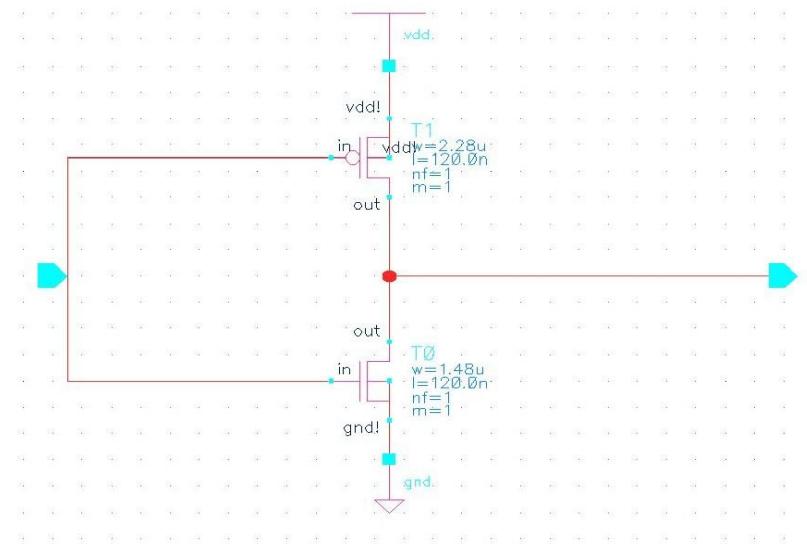
Delay is proportional to time constant. Consider an nMOS with  $R_n$  as its resistance.

$$\tau_n = R_n (C_{load} + C_{self})$$

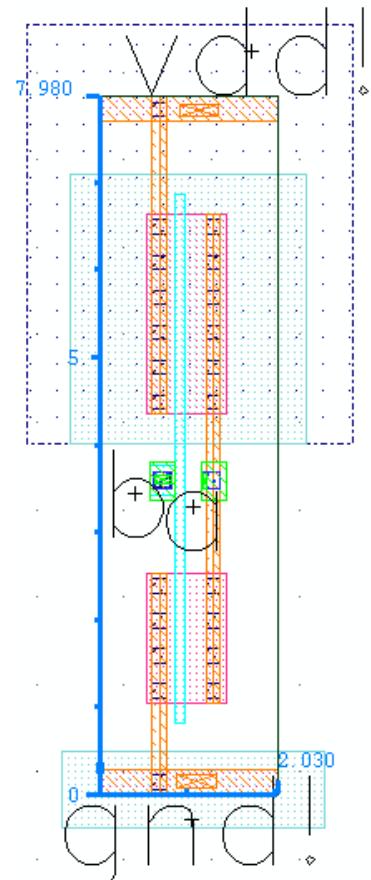
$R_n$  is inversely proportional to width. When width is less,  $C_{load}$  dominates the capacitance. So for smaller values of width, delay decreases with width. For higher values of W, delay attains a constant value.

## INVERTER (Library name: project6, Cell name: inv)

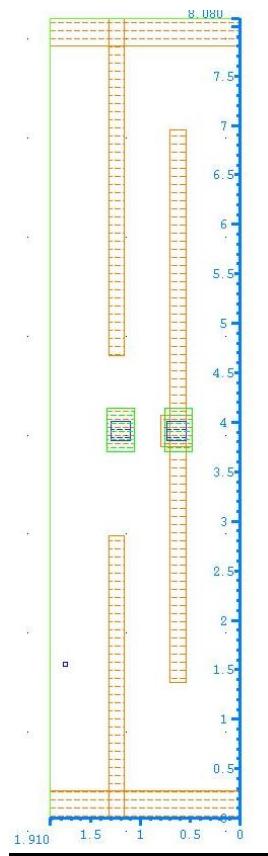
Schematic:



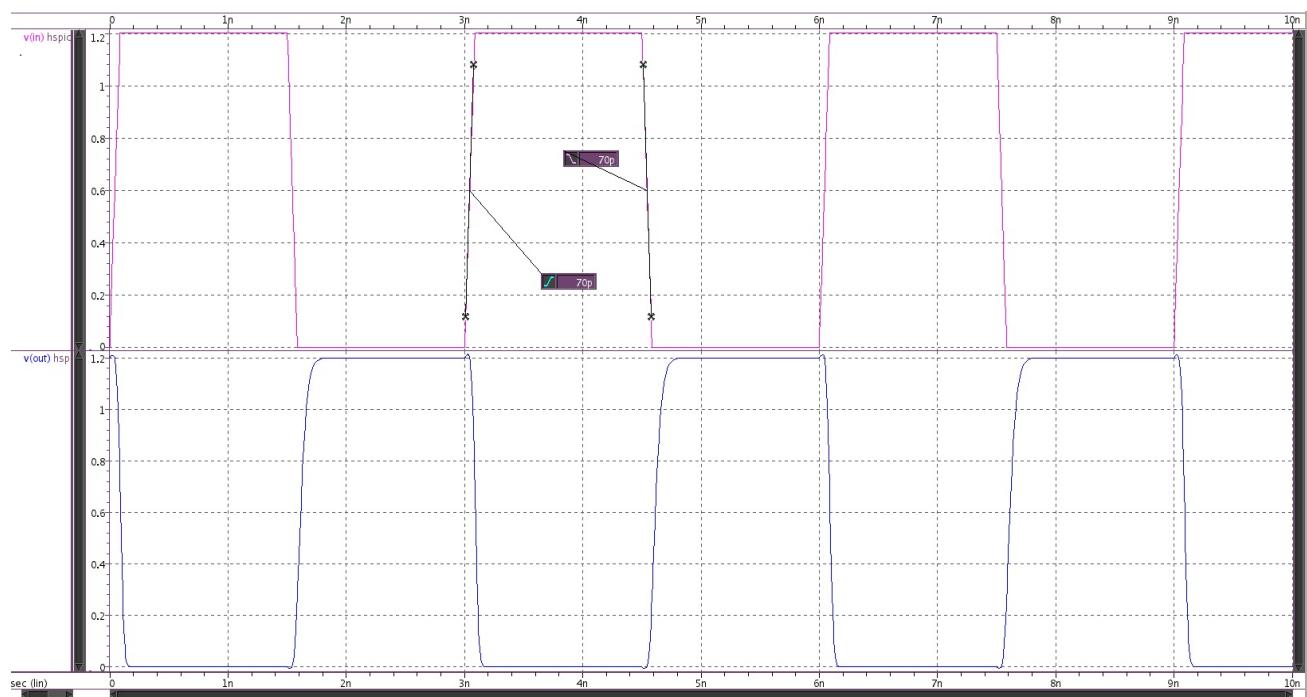
Layout:



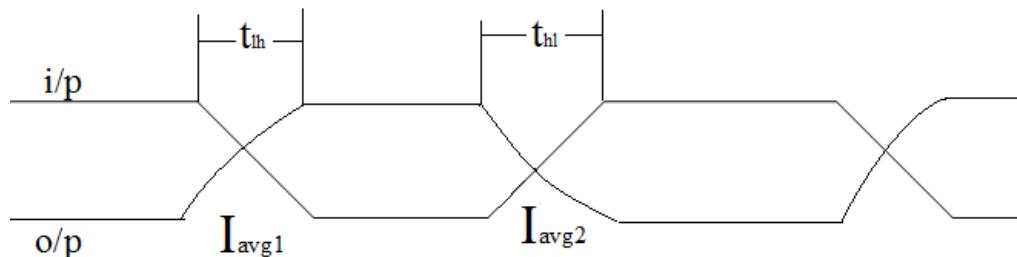
### Abstract View:



### Simulation Waveforms:



## EDP calculation

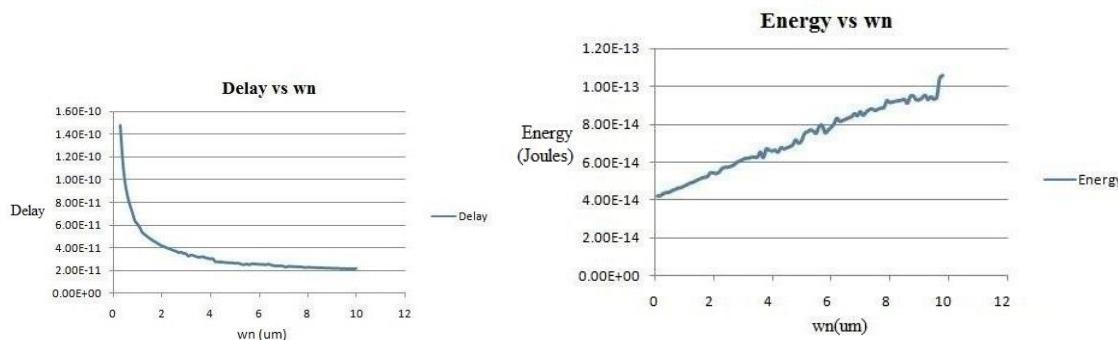


$$EDP = V_{dd} * I_{avg} * (\text{Start Time} - \text{End Time}) * (\text{Delay})$$

$$\text{Delay} = \max \{T_{plh}, T_{phl}\}$$

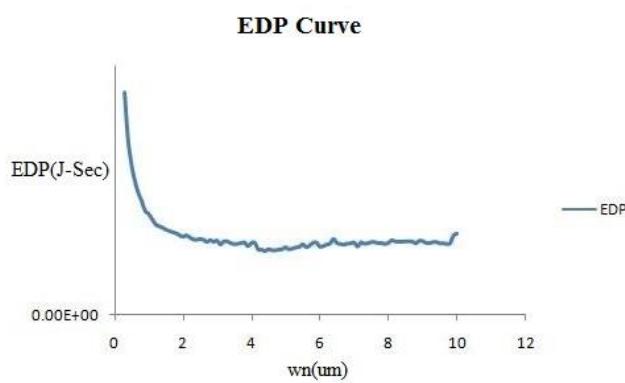
$$I_{avg} = \max \{|I_{avg1}|, |I_{avg2}|\}$$

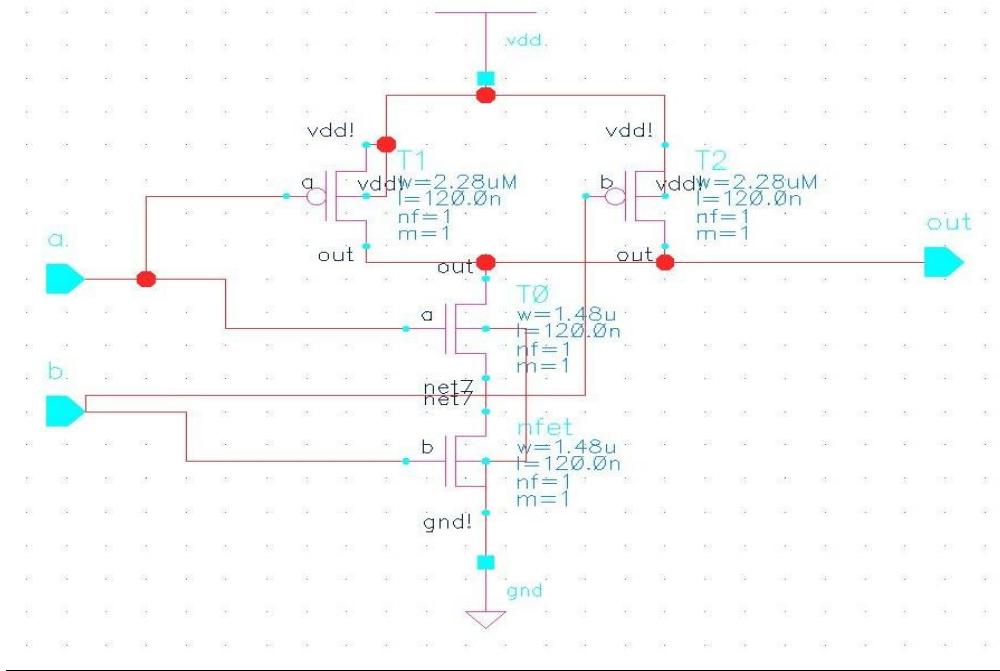
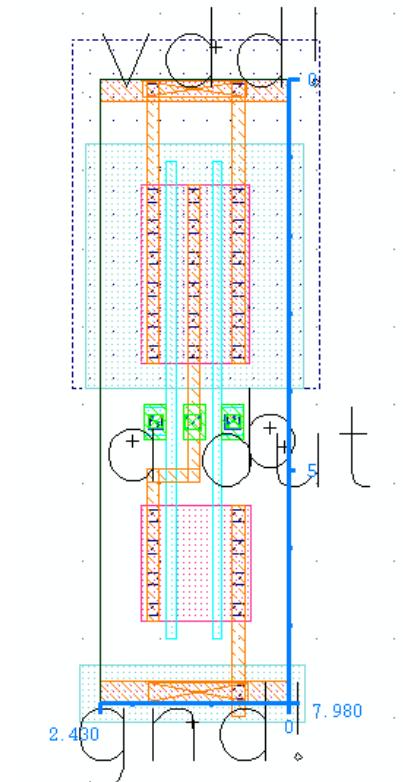
The below plot shows propagation delay versus  $w_n$  trend. Initially delay decreases with increasing value of width. It attains a constant value for higher values of width.



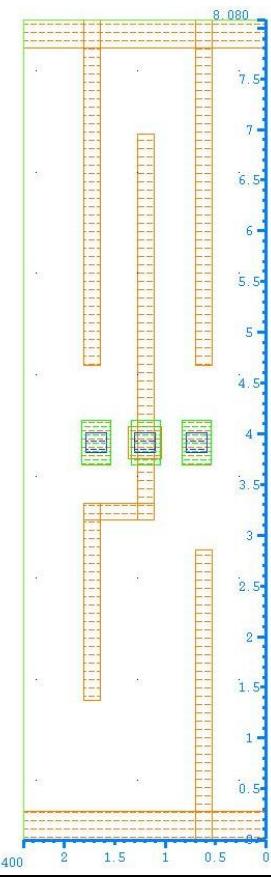
Following plot shows the relation between energy and width of nmostransistor( $w_n$ )

The below graph is plotted between EDP and width of n-mostransistor ( $w_n$ ). For designing an inverter the width of the transistor is chosen in such a way that minimum EDP is achieved. For our inverter design the minimum value of EDP is achieved when  $w_n=4.38\mu m$ .

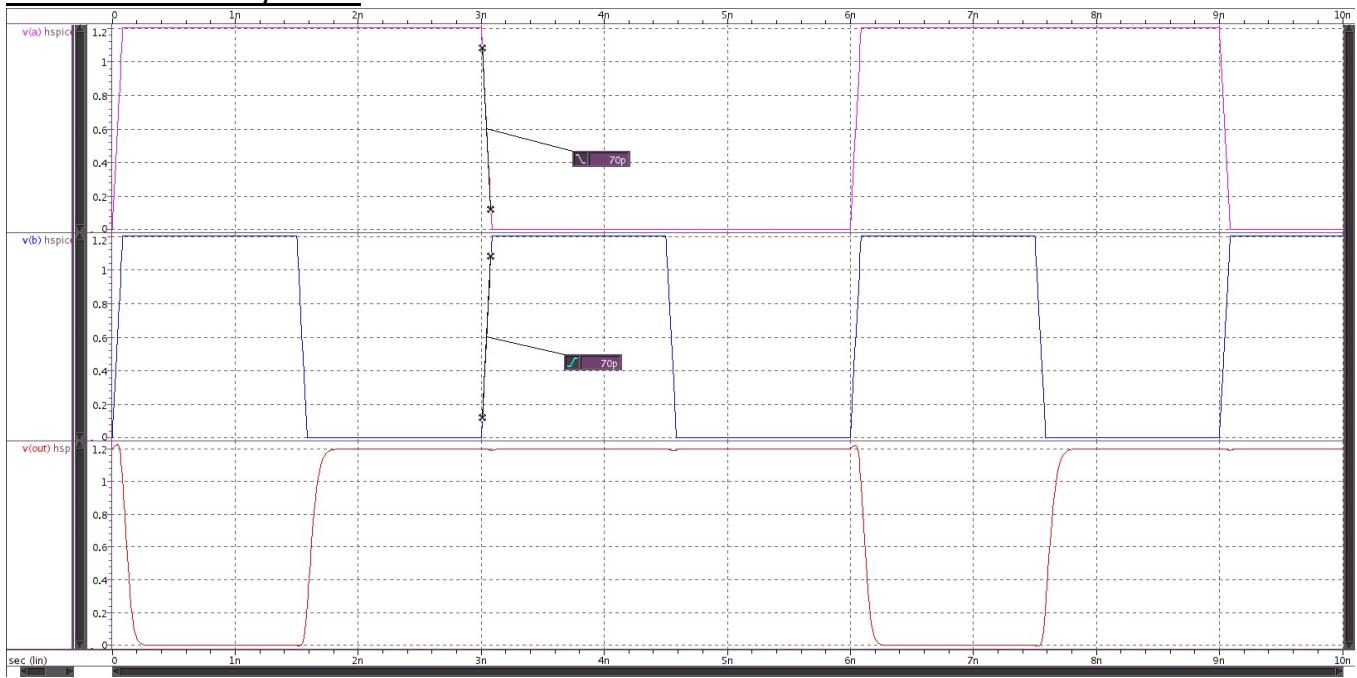


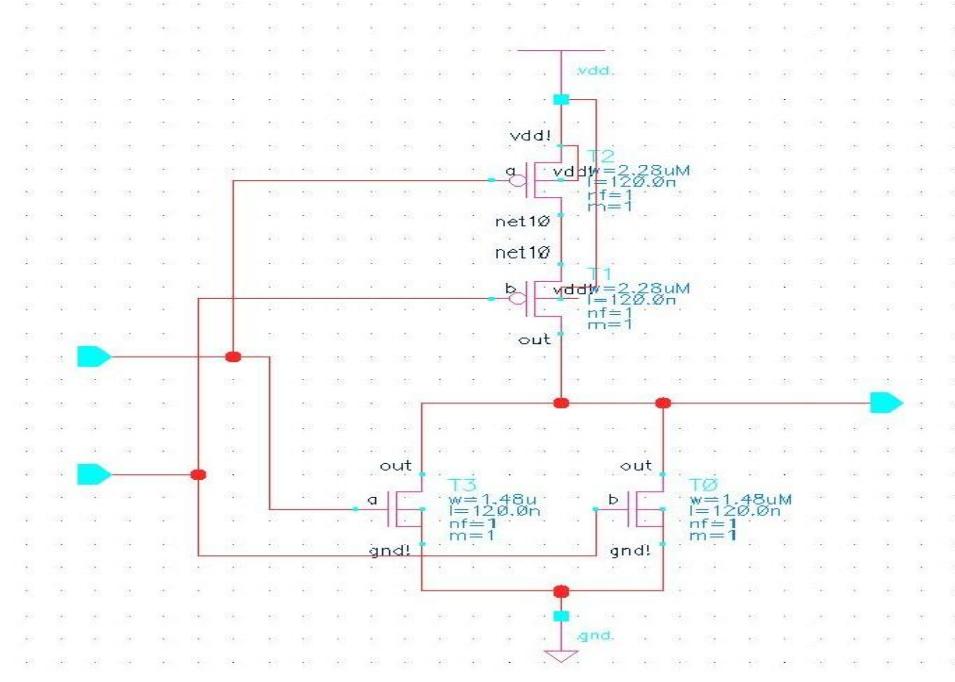
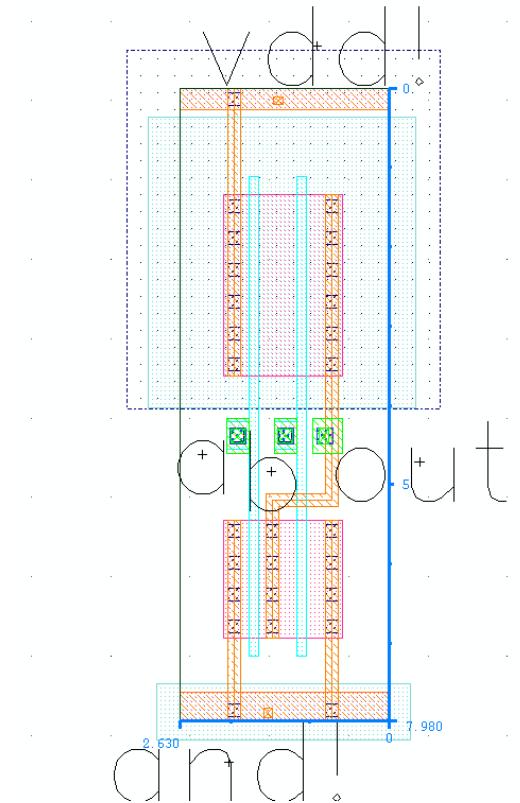
**NAND2 (Library name: project6, Cell name: nand2)**Schematic:Layout:

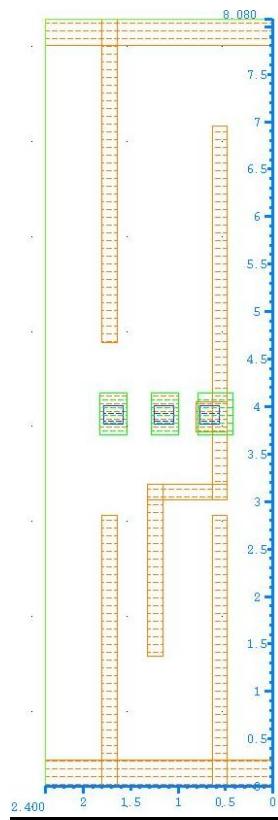
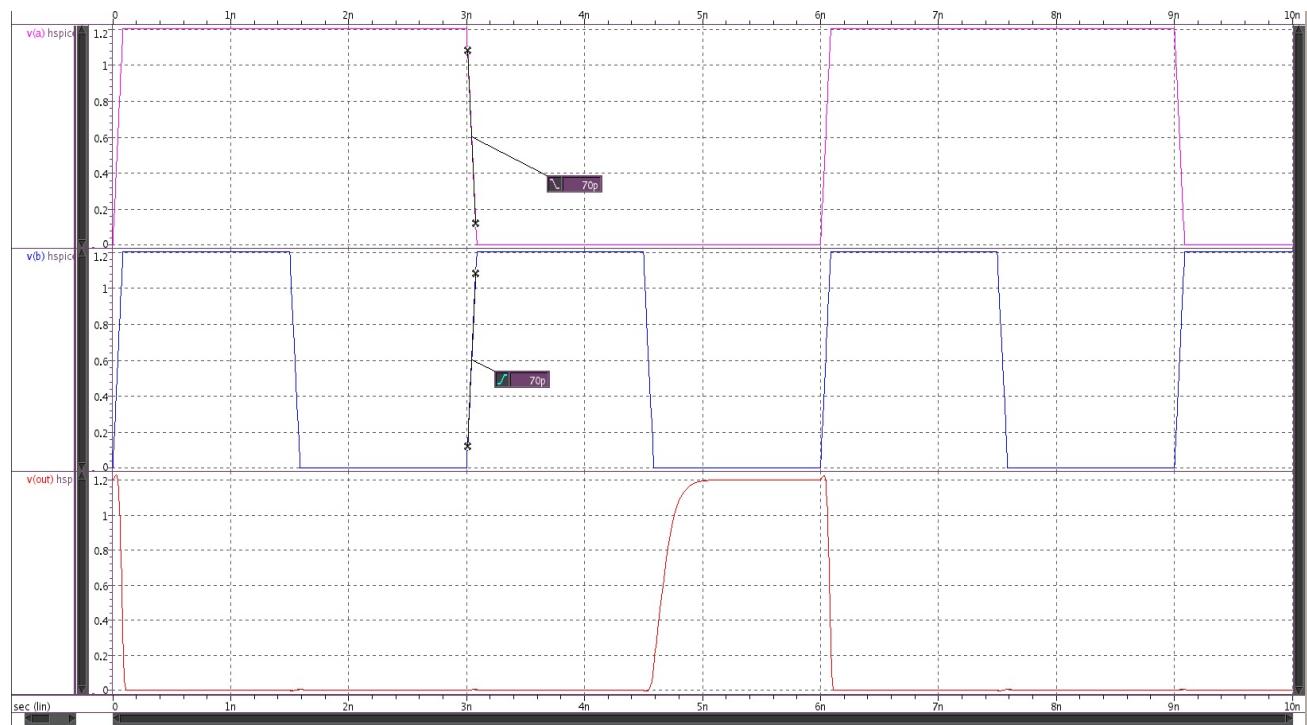
### Abstract View:

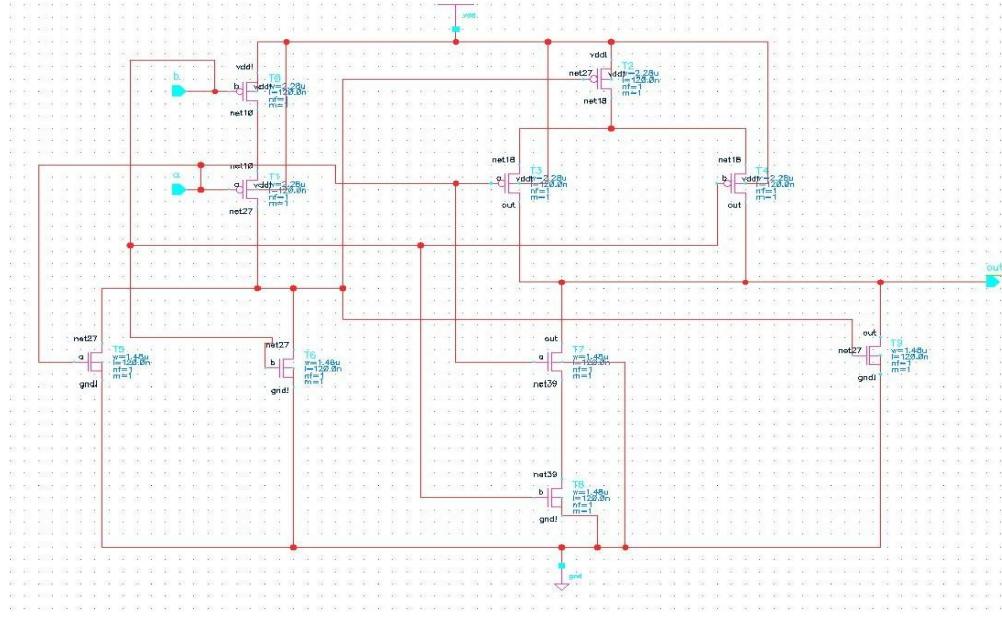
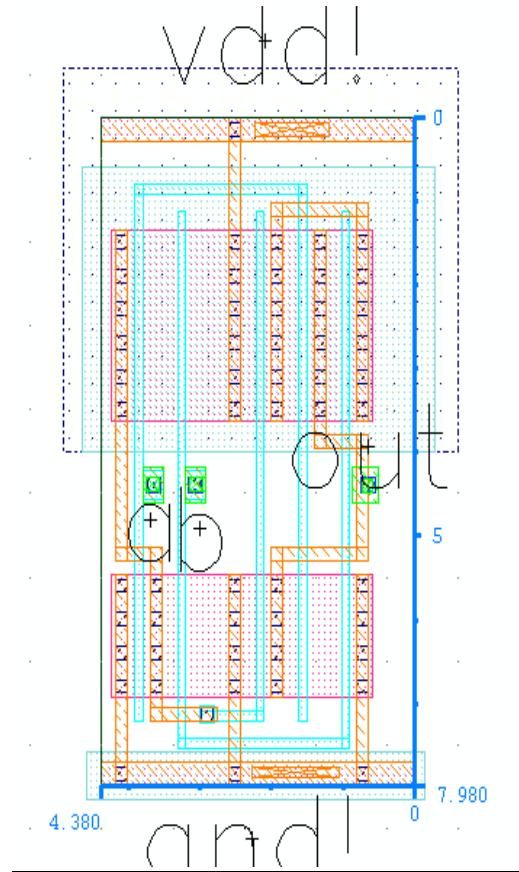


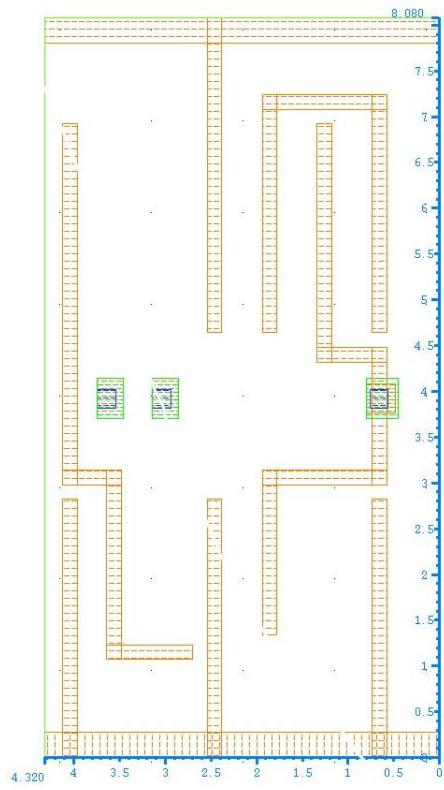
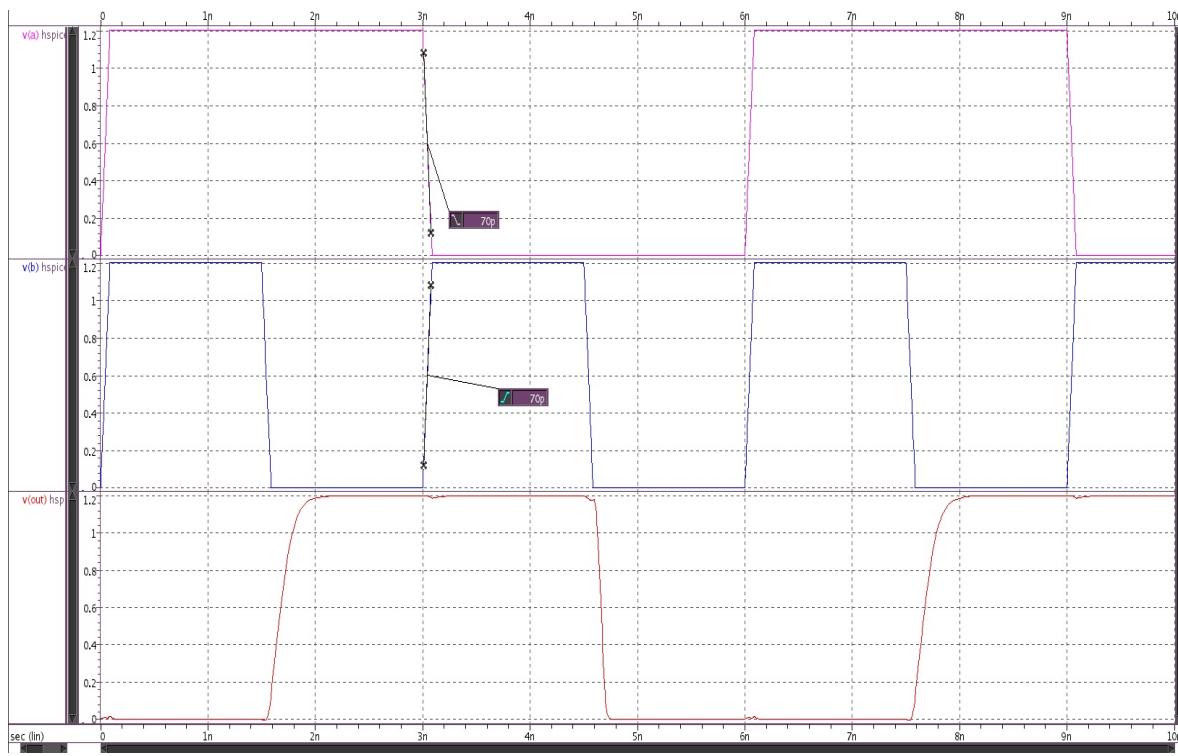
### Simulation Waveforms:



**NOR2 (Library name: project6, Cell name: nor2)**Schematic:Layout:

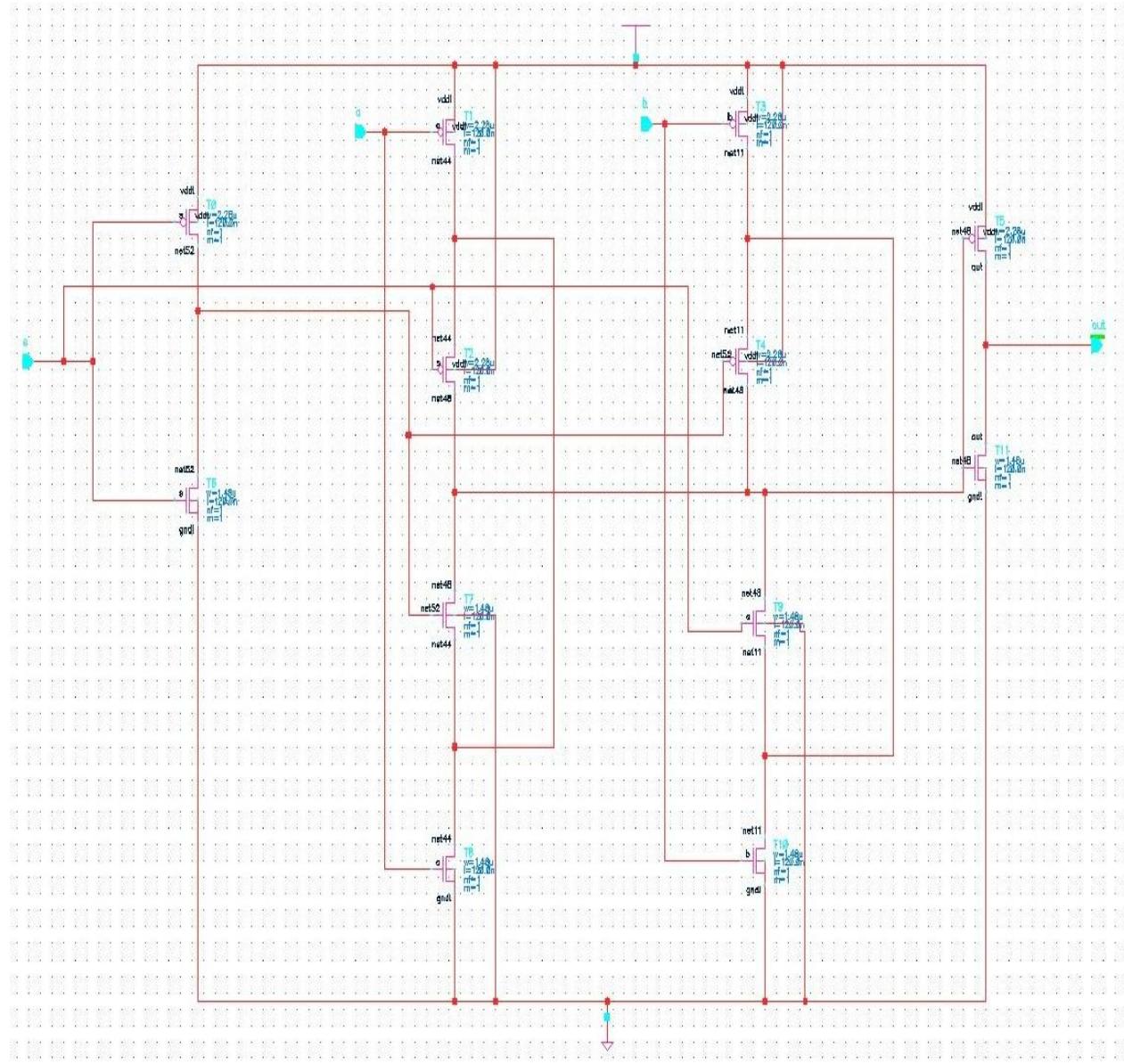
Abstract View:Simulation Waveforms:

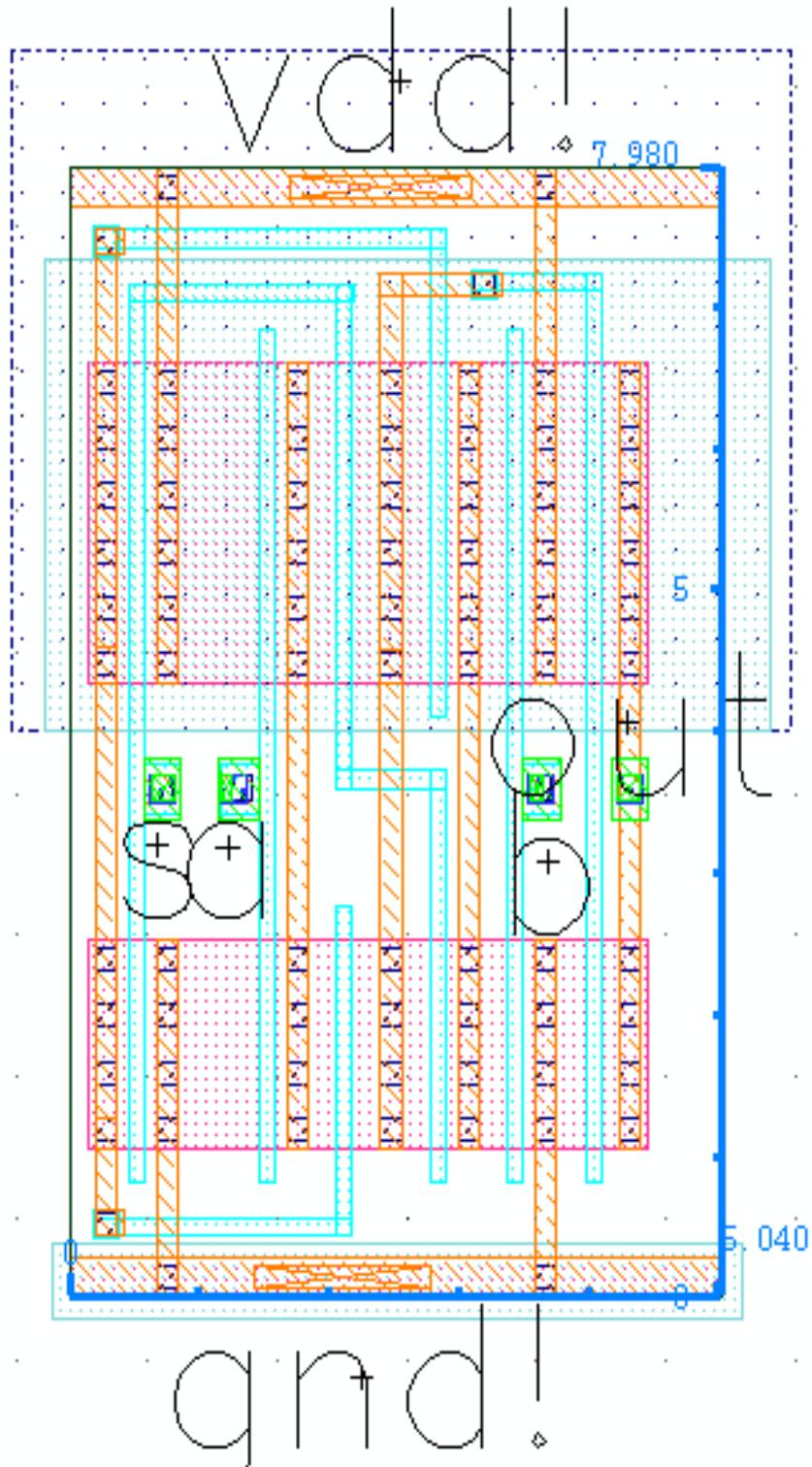
**XOR2 (Library name: project6, Cell name: xor2)**Schematic:Layout:

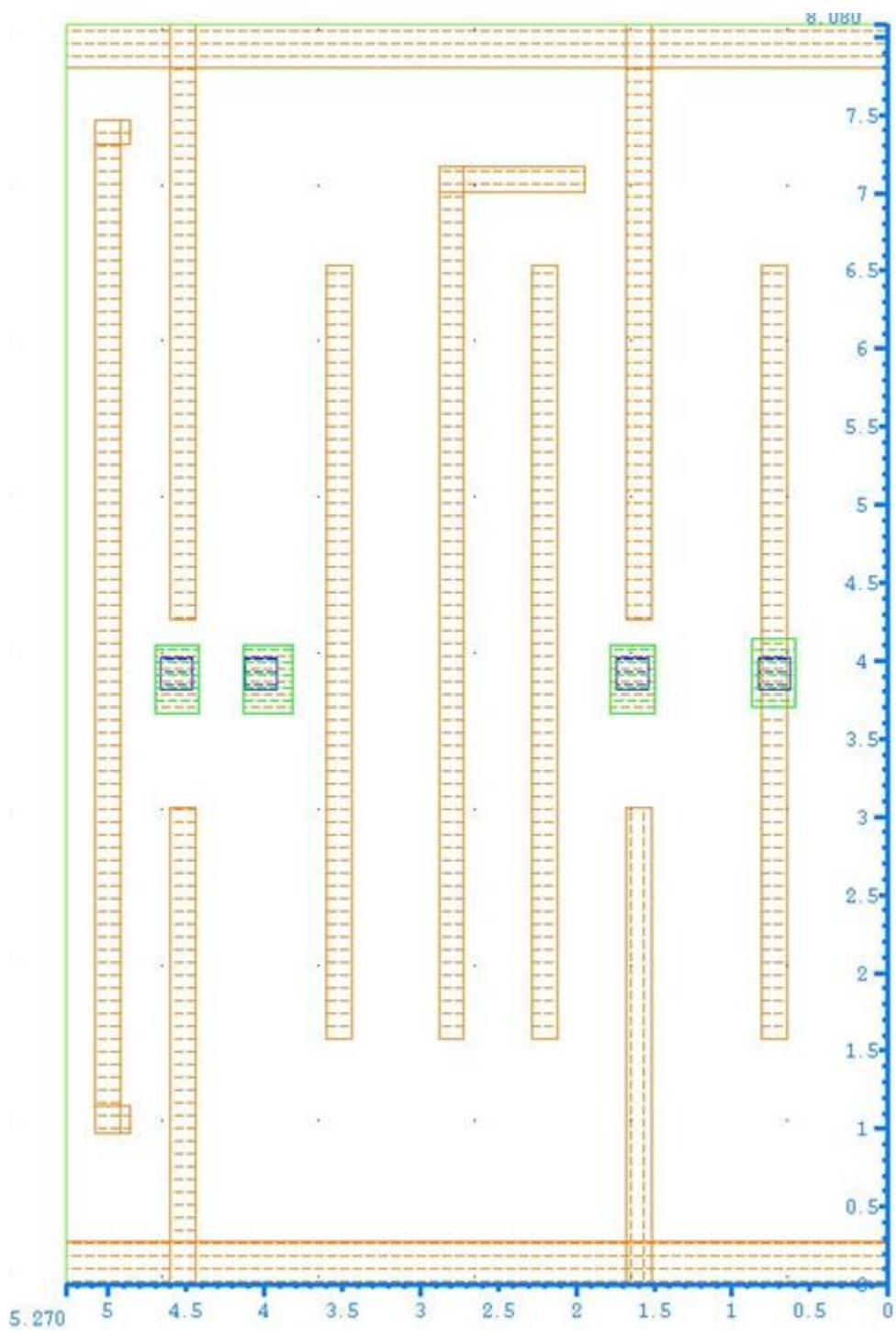
Abstract View:Simulation Waveforms:

## MUX 2:1 (Library name: project6, Cell name: mux21)

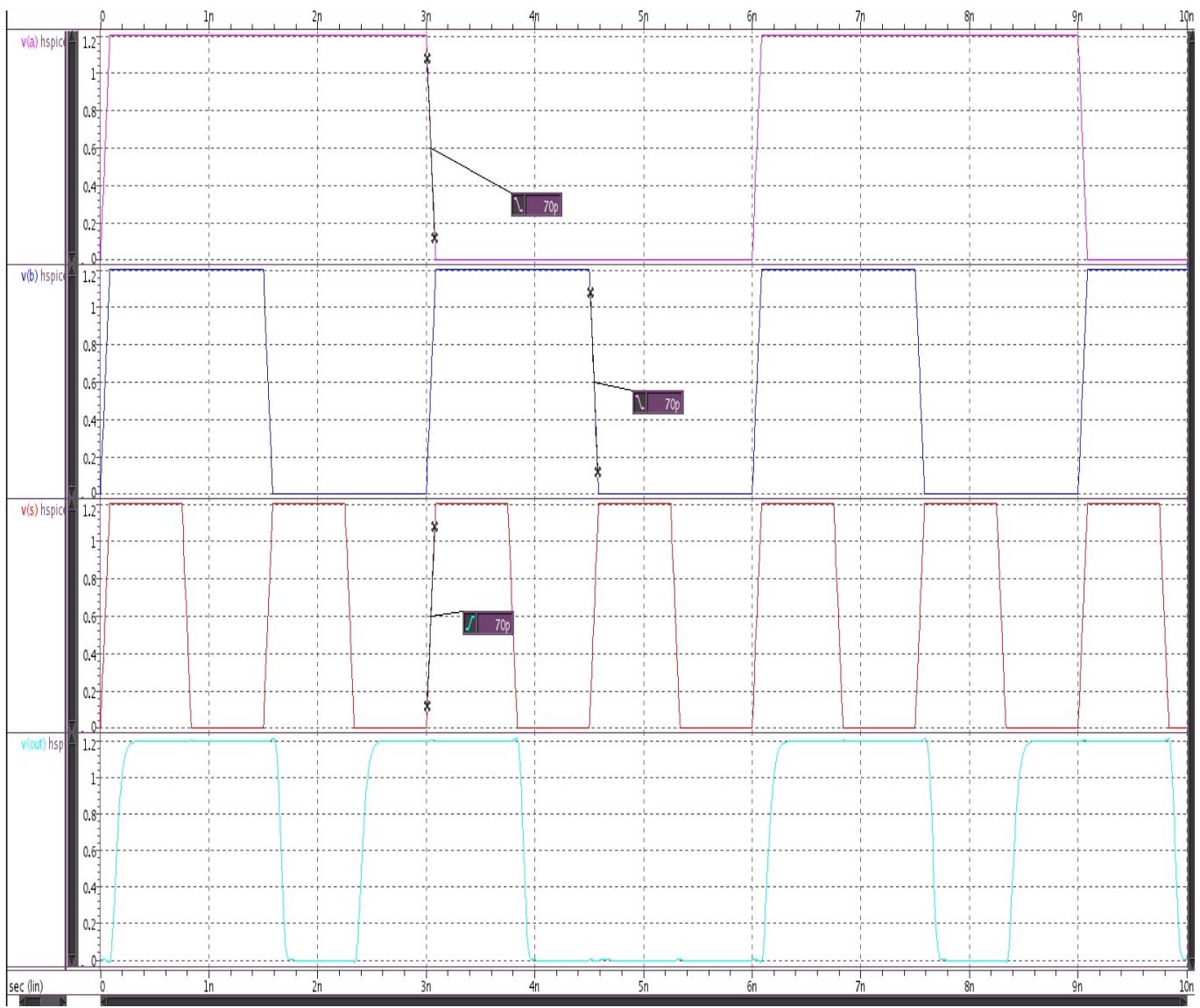
*Schematic:*



Layout:

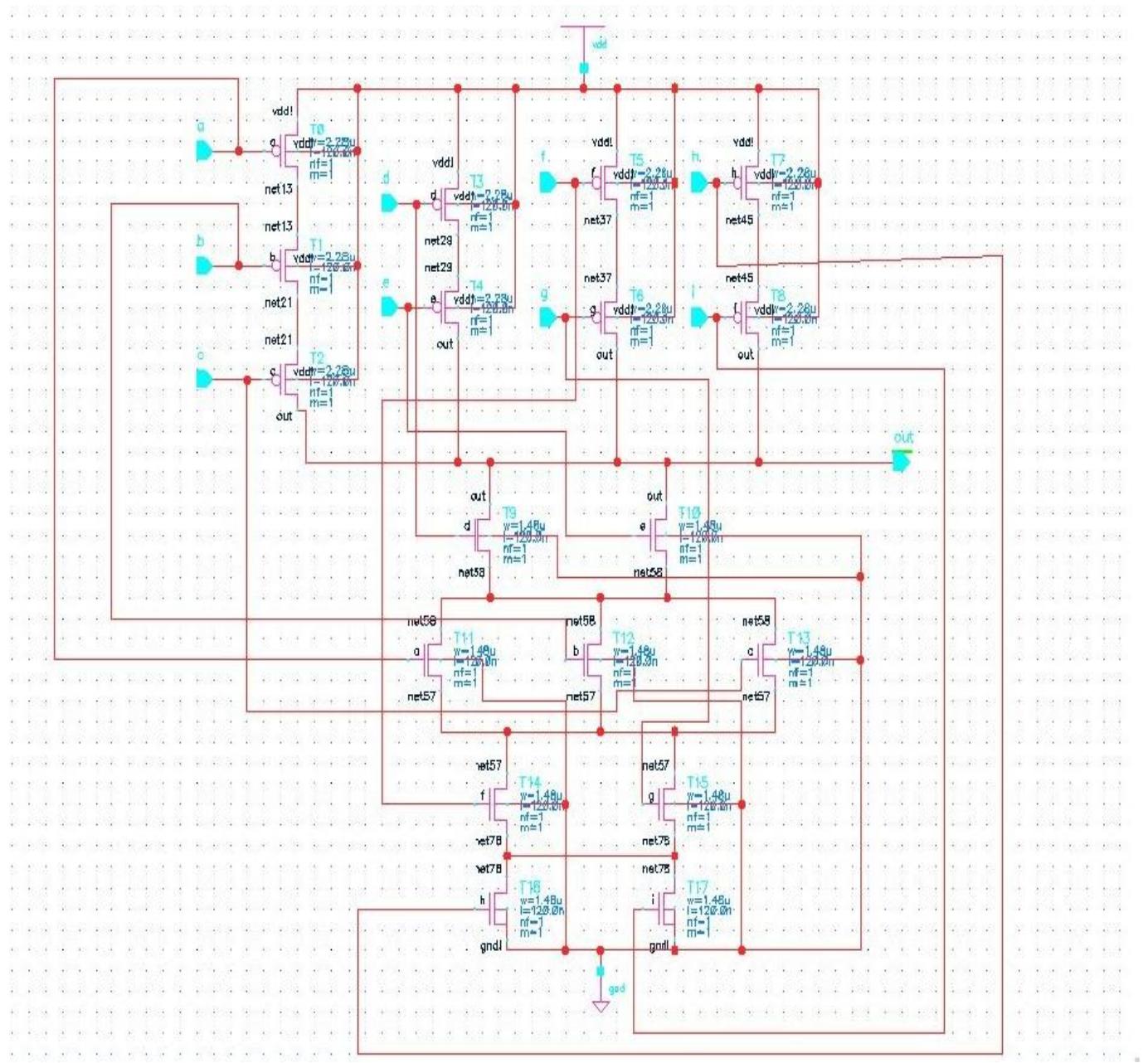
Abstract View:

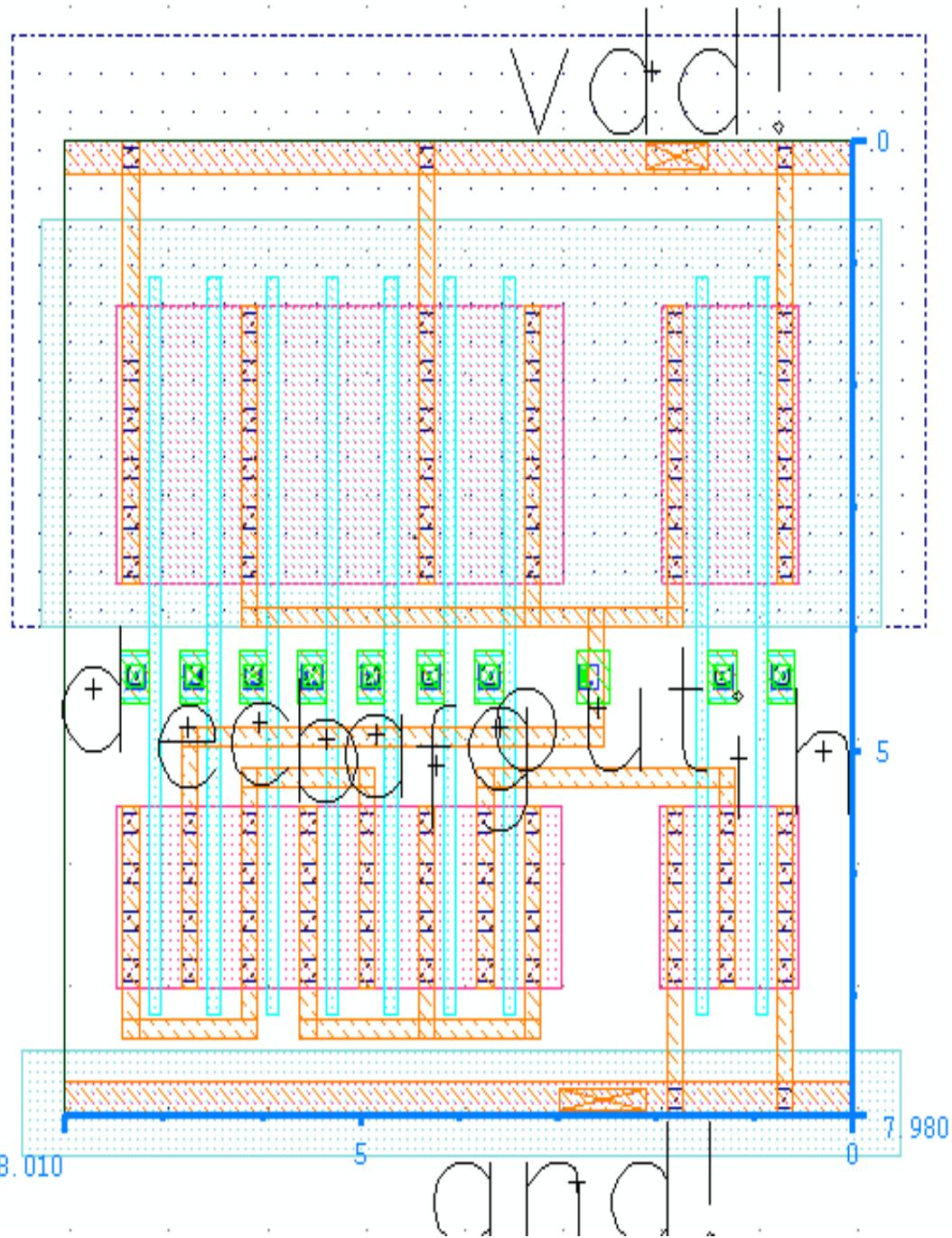
### Simulation Waveforms:

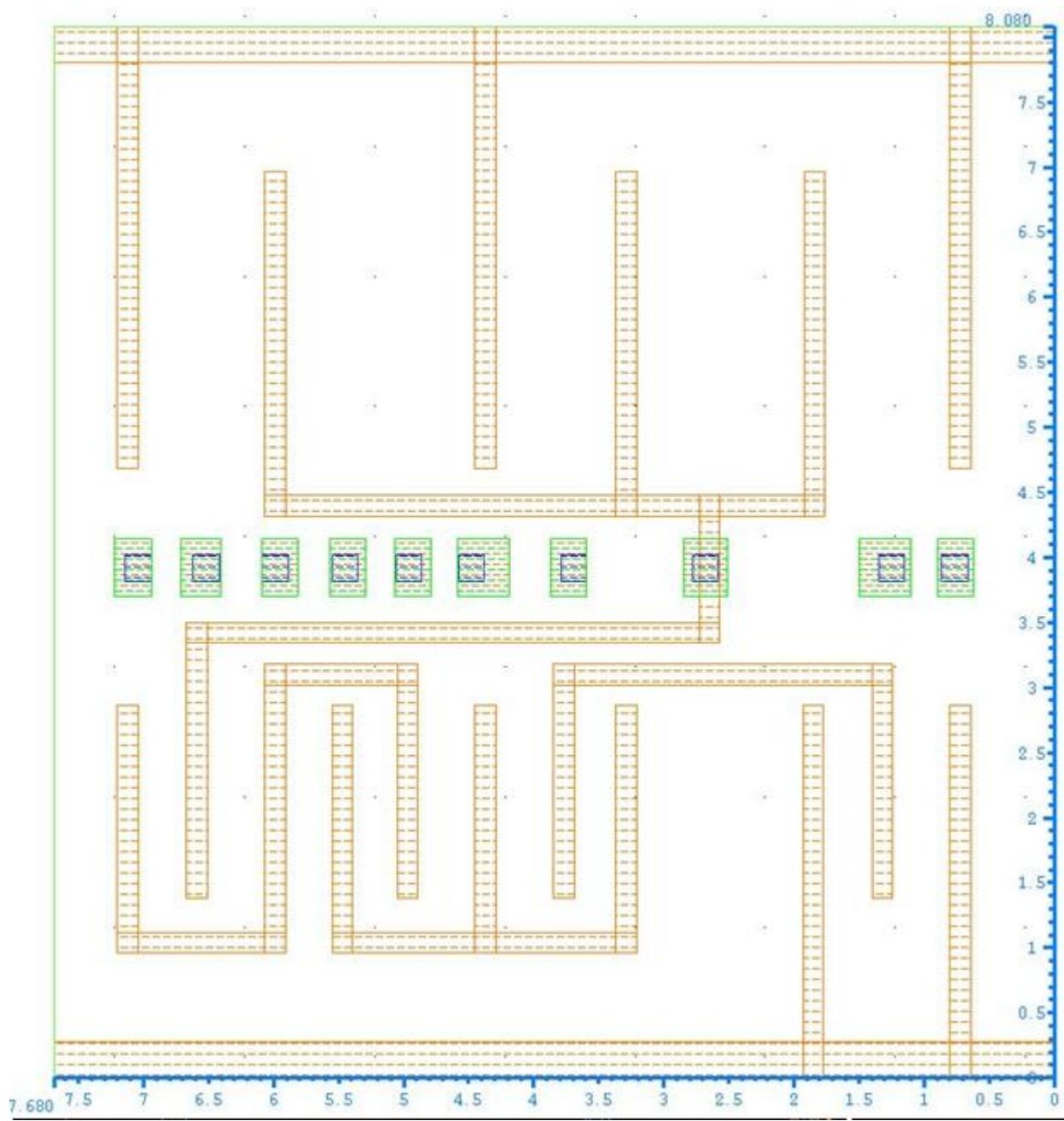


OAI3222 (Library name: project6, Cell name: oai3222)

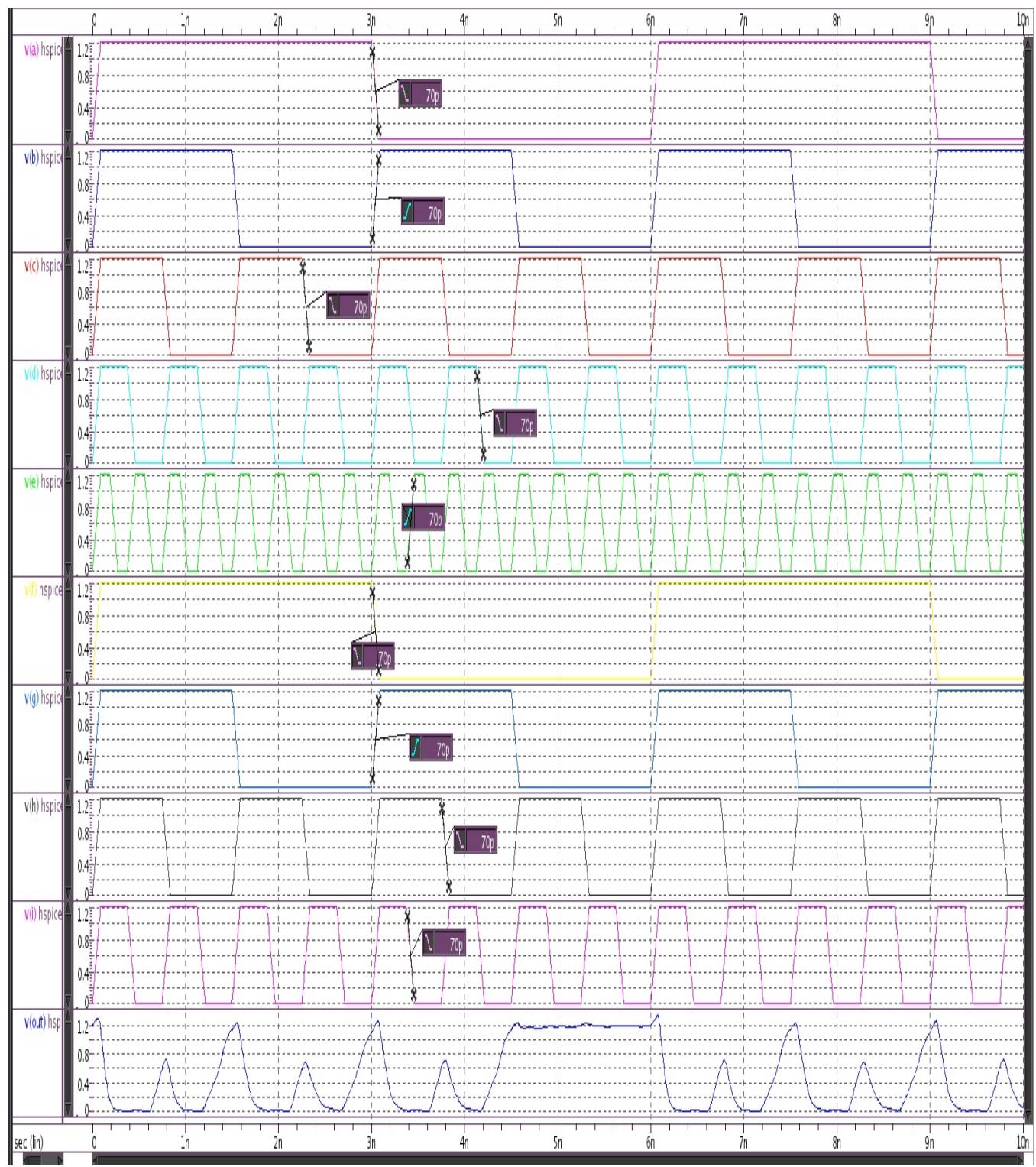
### Schematic:

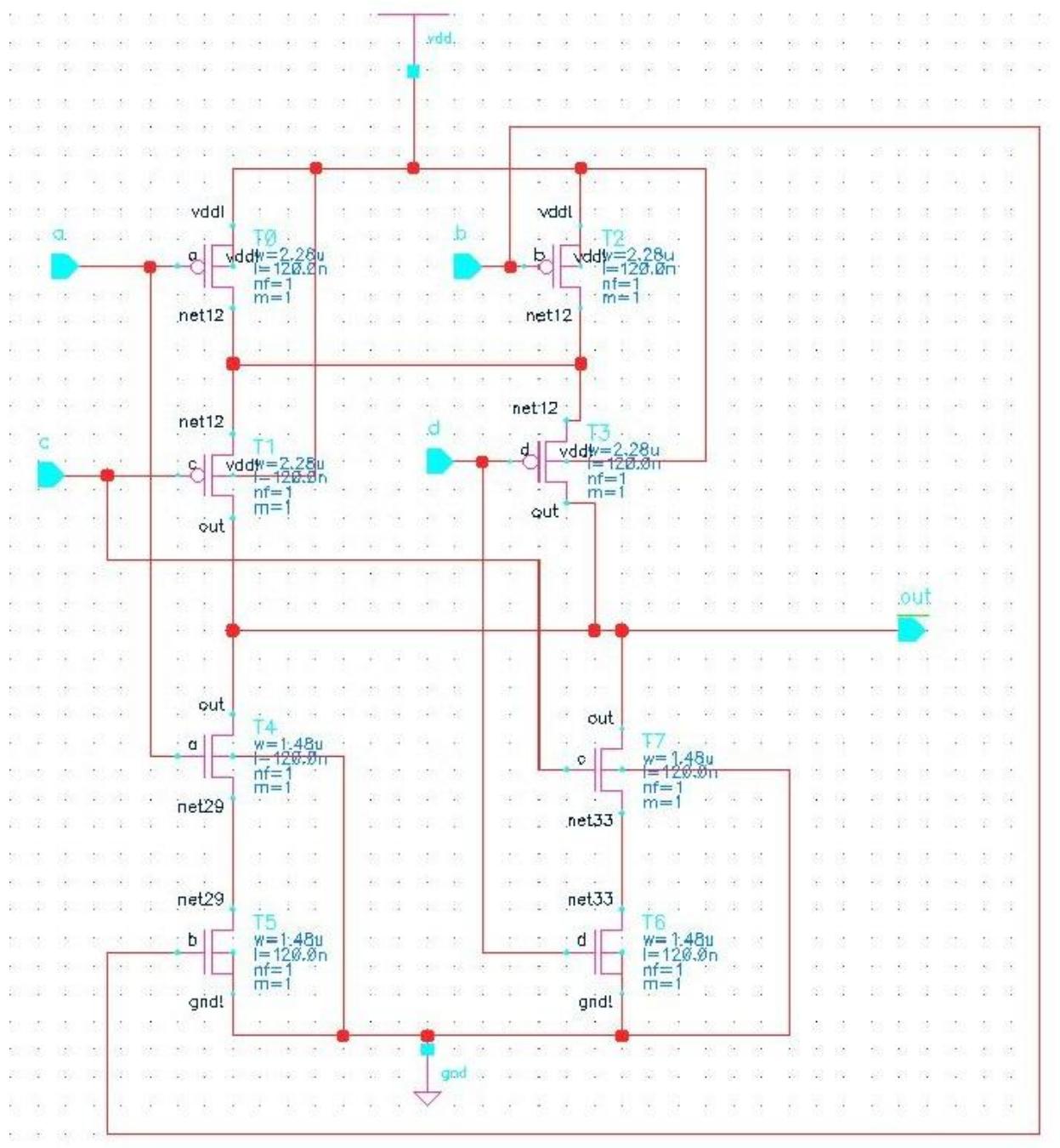


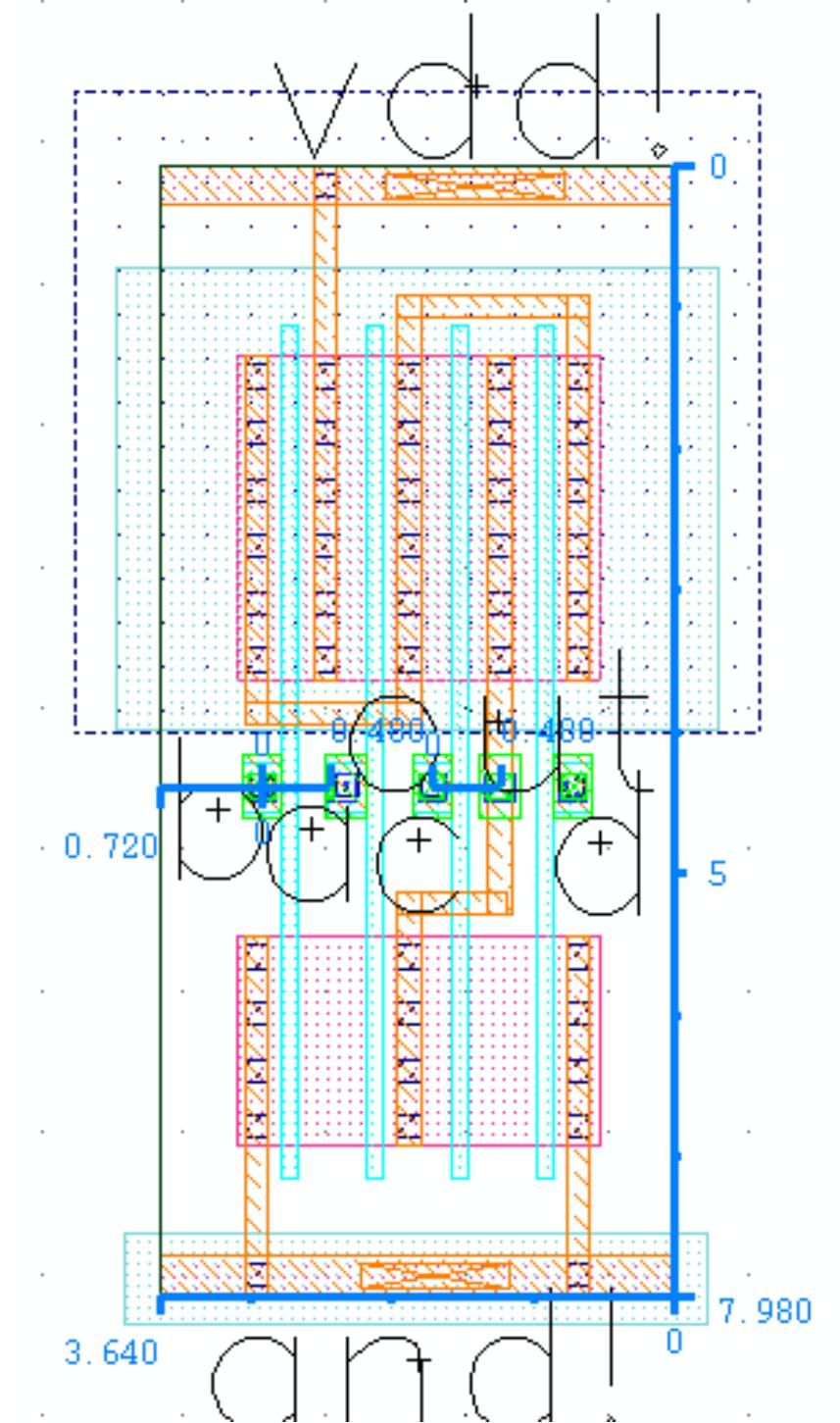
Layout:

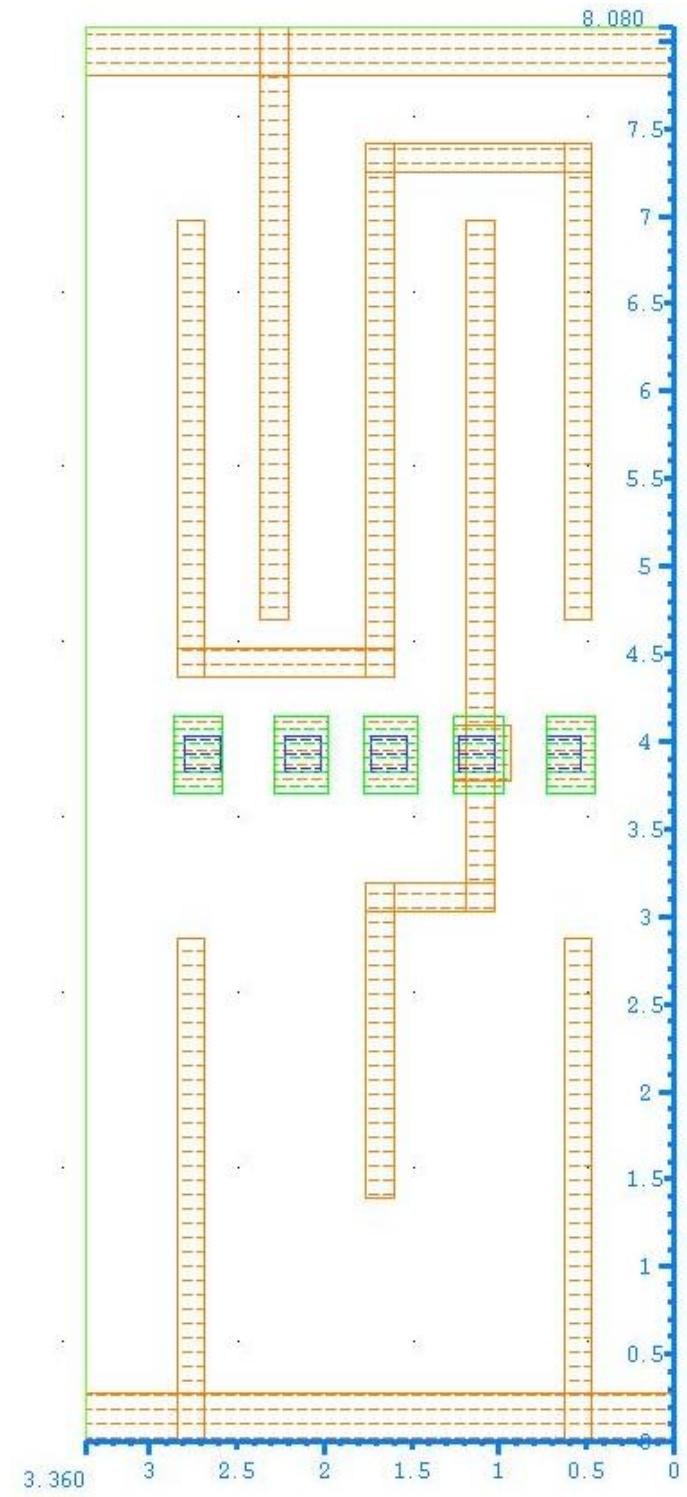
Abstract View:

### Simulation Waveforms:

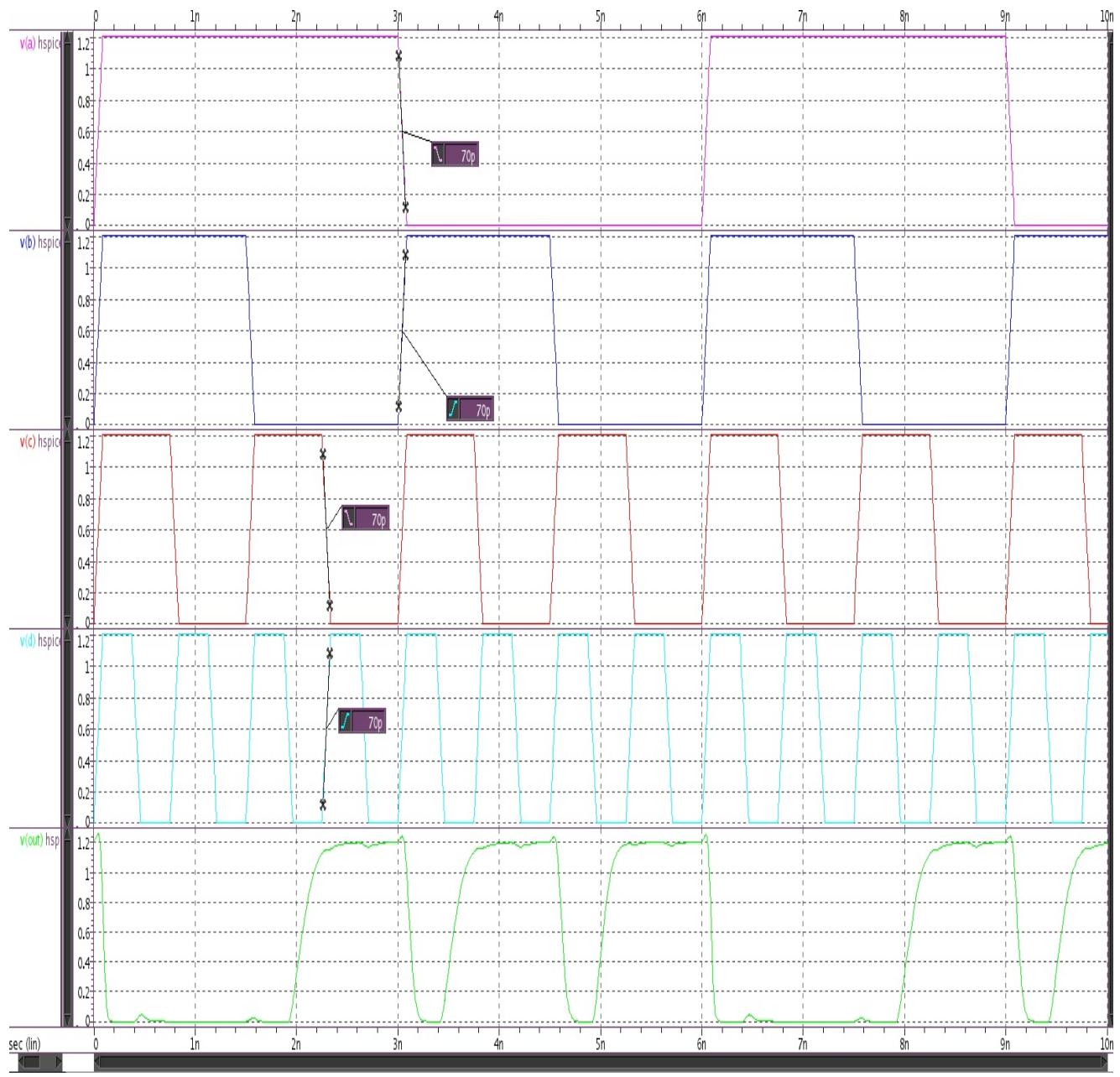


**AOI22 (Library name: project6, Cell name: aoi22)***Schematic:*

Layout:

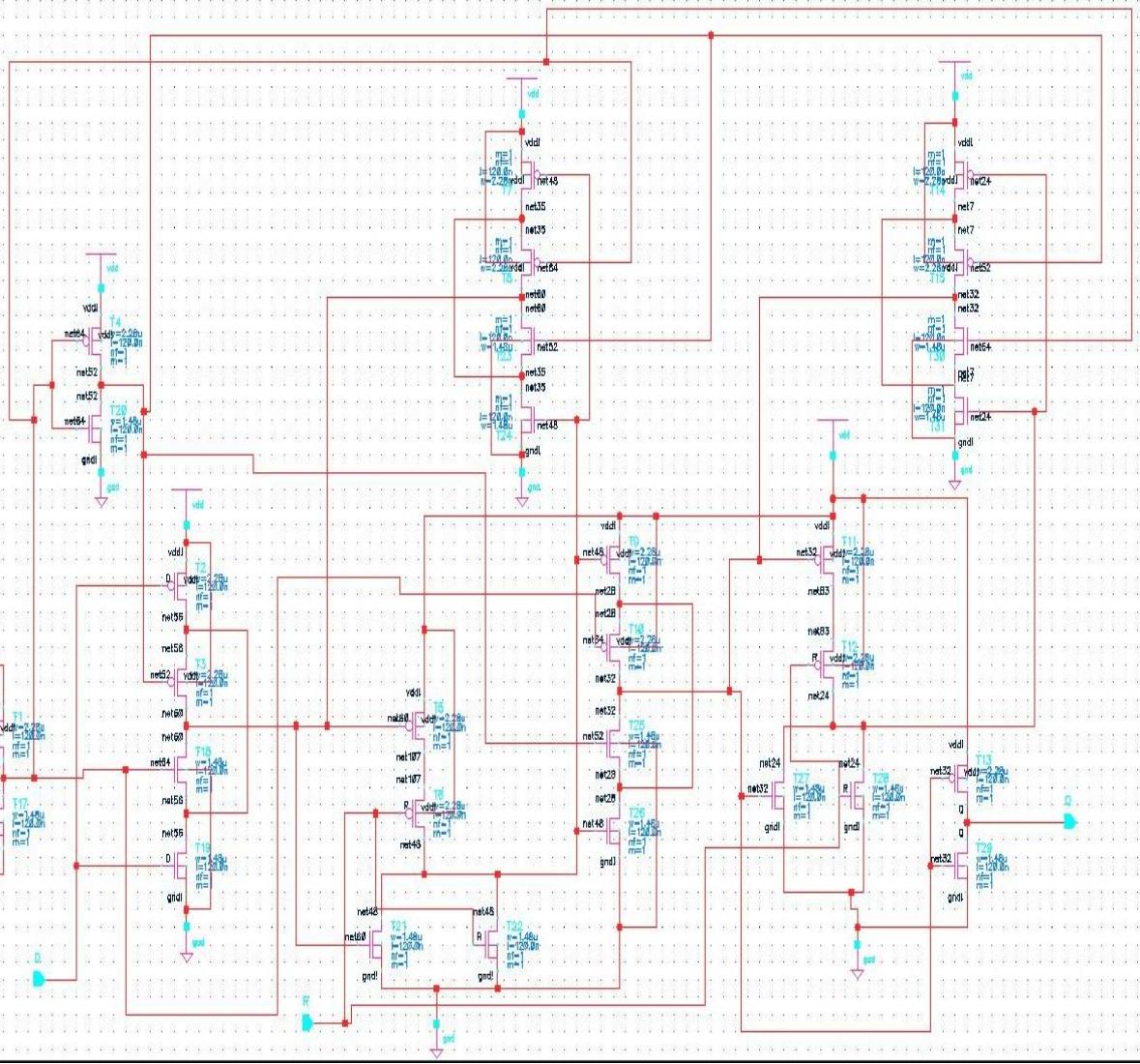
Abstract View:

### Simulation Waveforms:



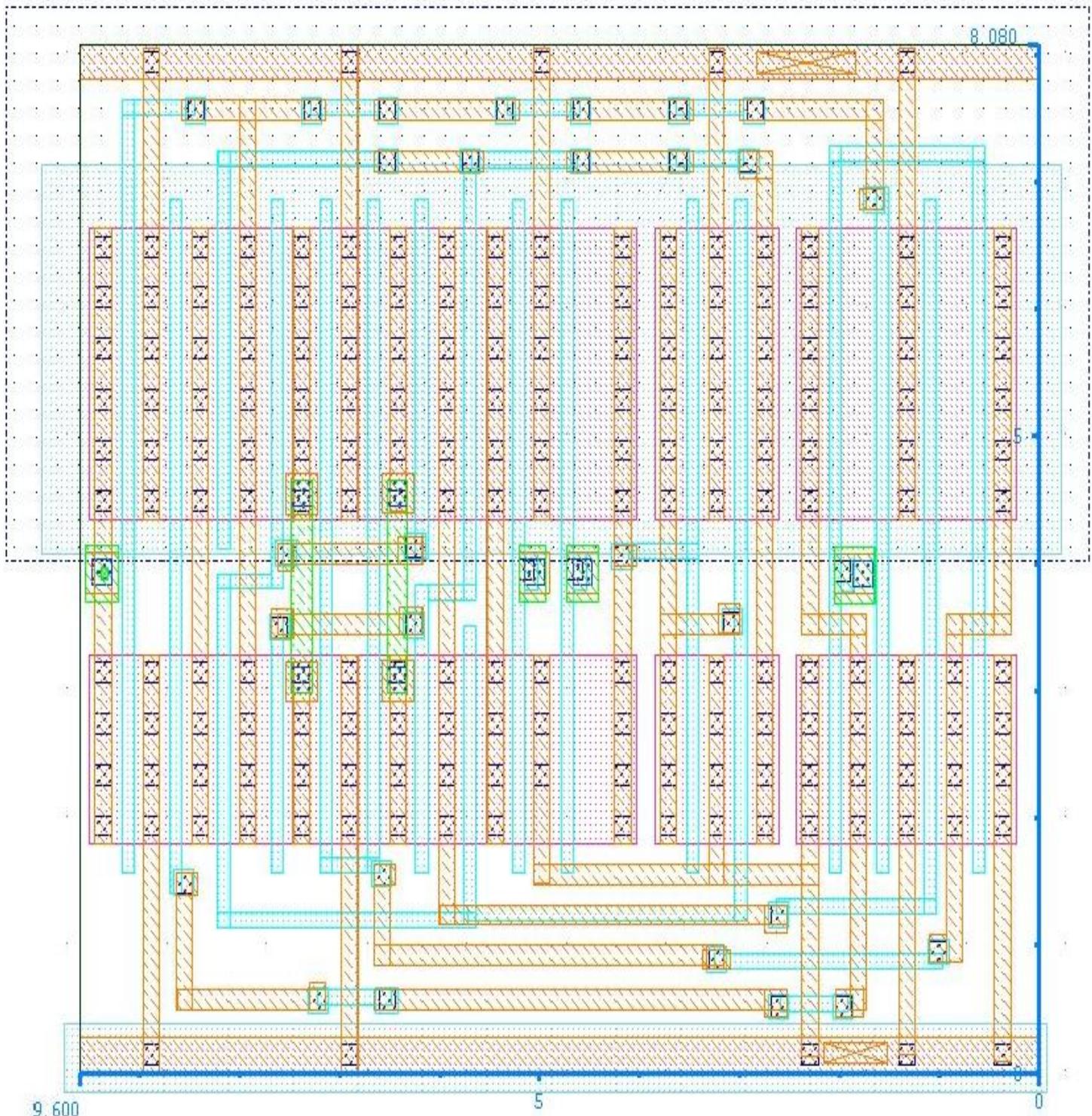
## D Flip Flop (Library name: project6, Cell name: dffreduced)

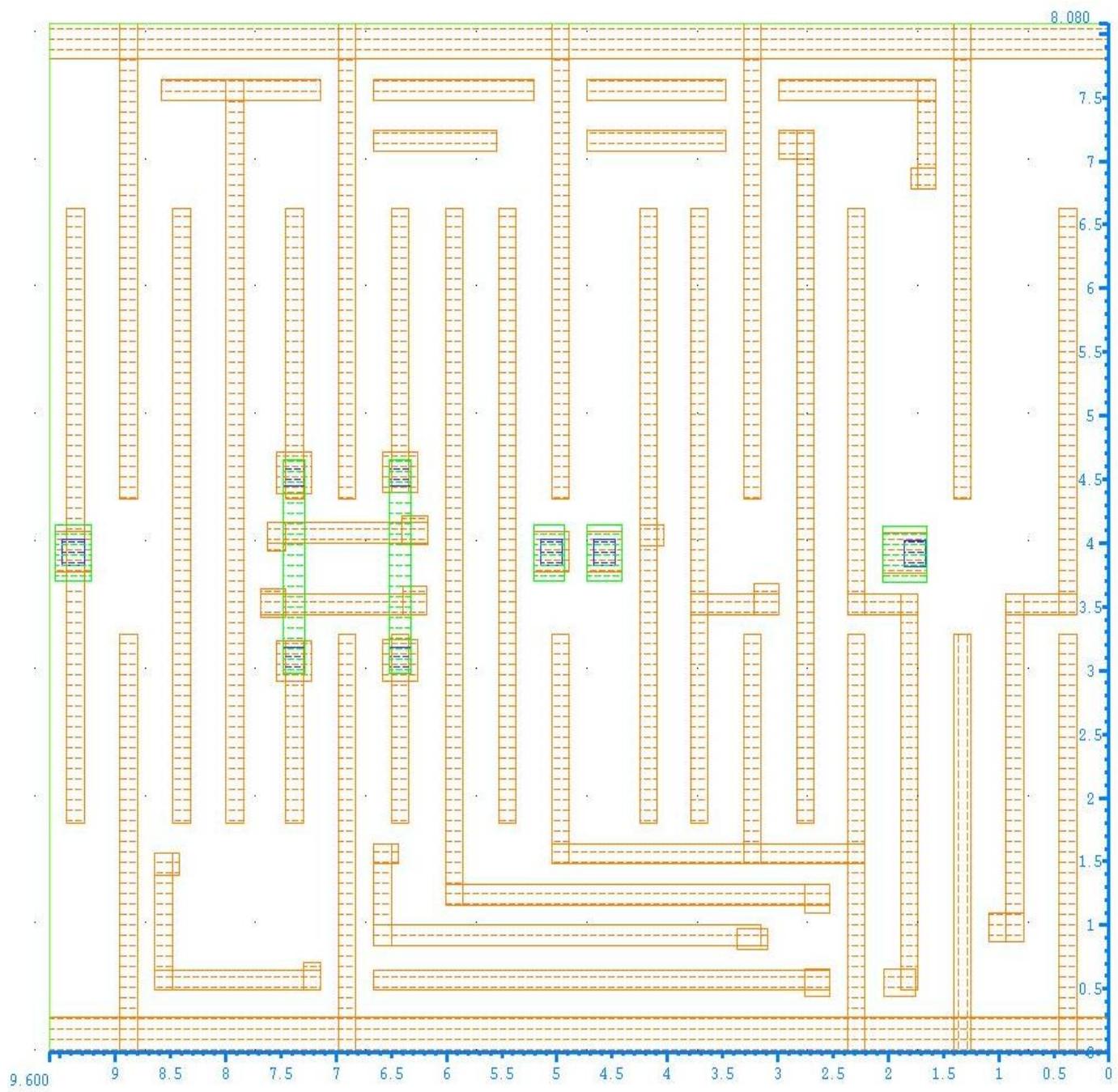
Schematic Representation:



### Layout Representation:

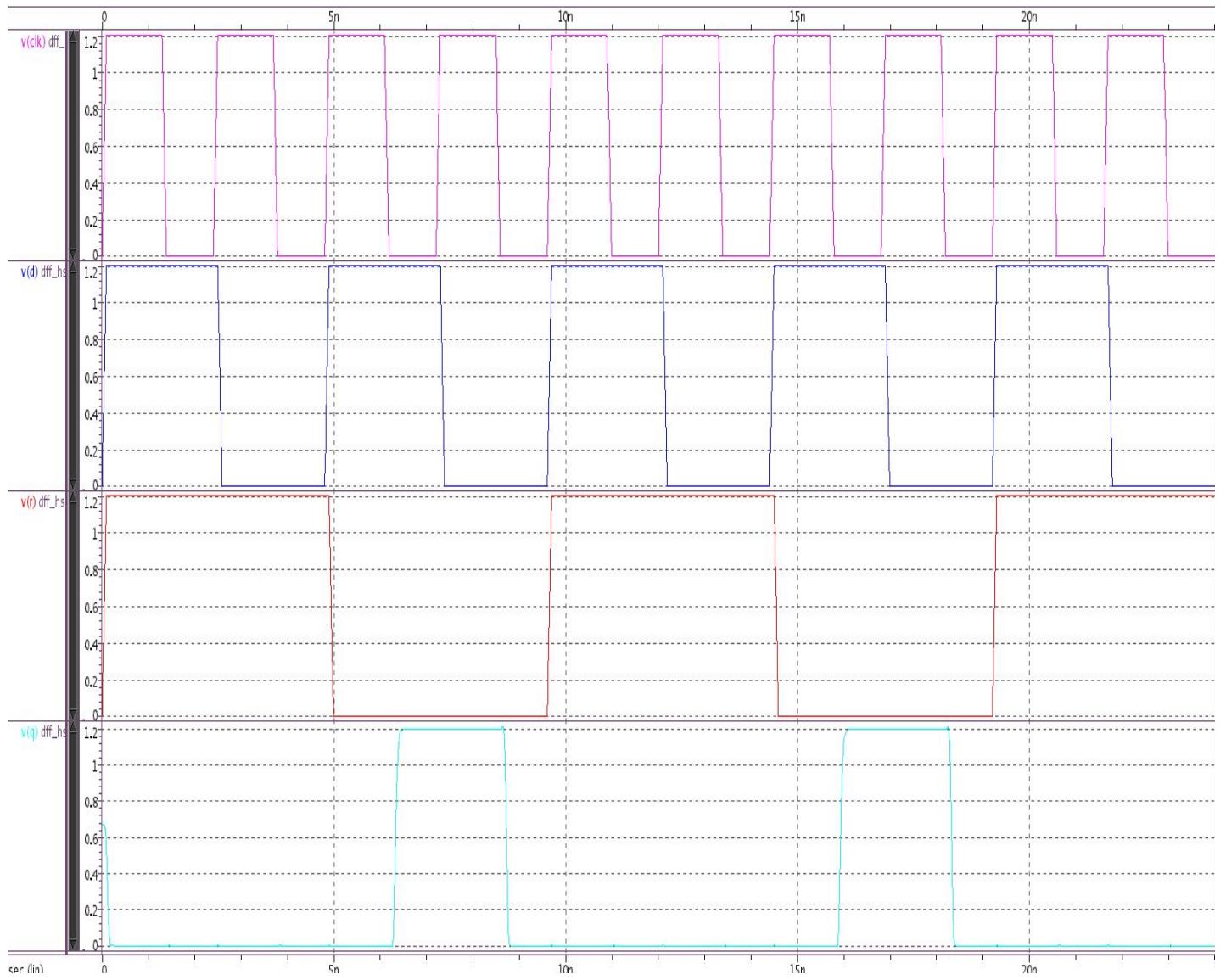
The below diagram shows the layout representation of the schematic shown. This layout is drawn using the above mentioned Euler's trail.



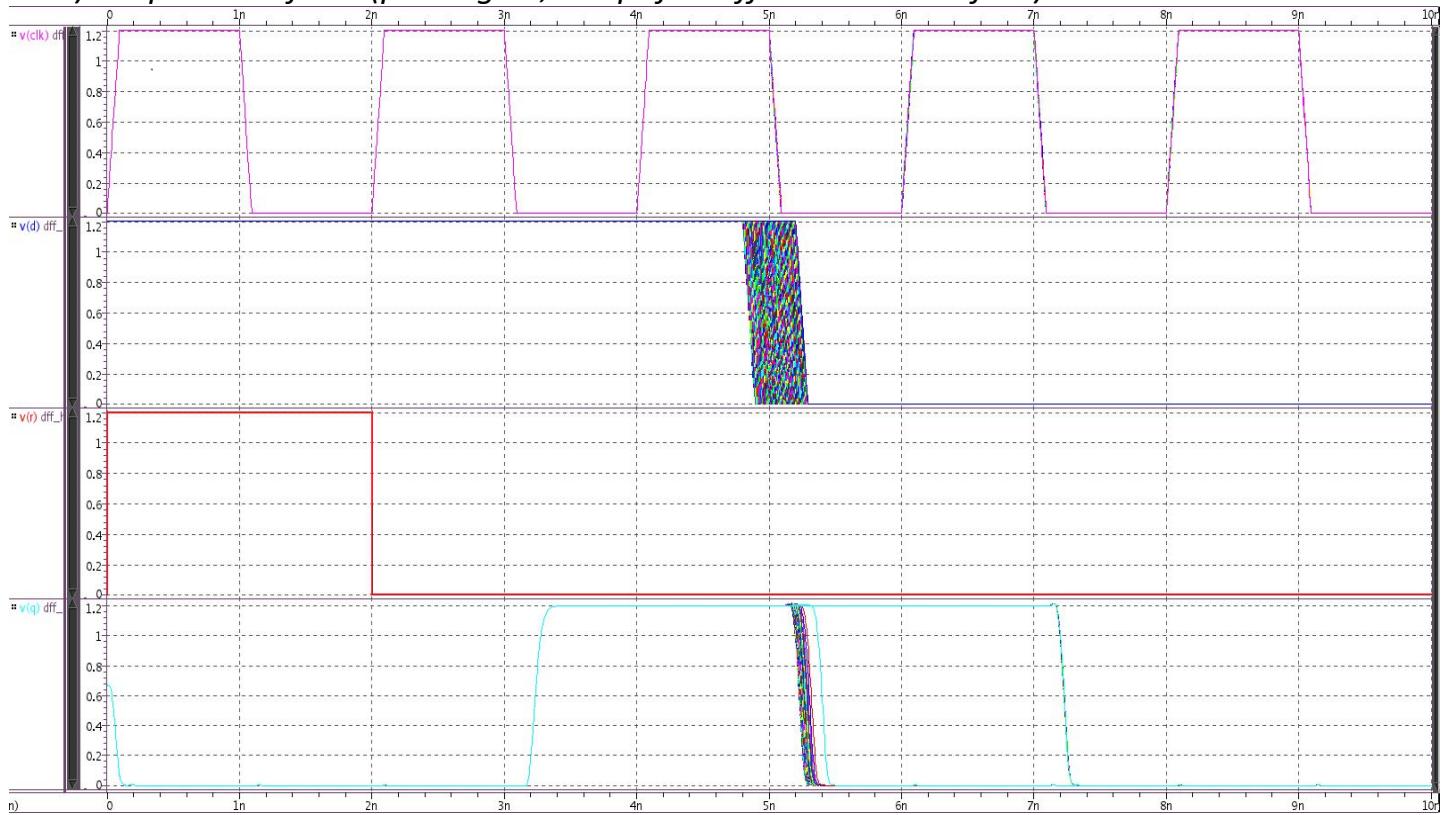
Abstract View:

## Simulation Waveforms:

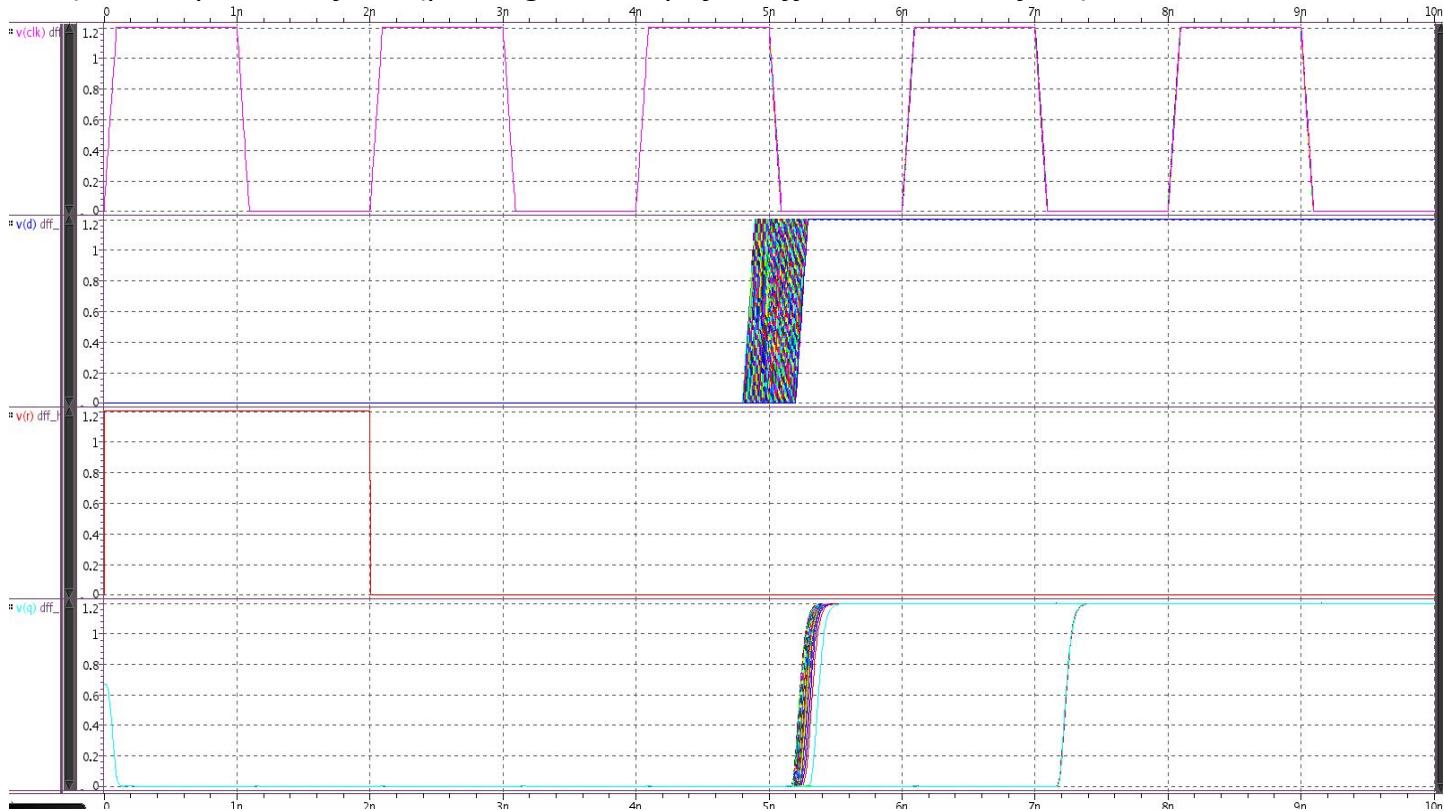
### 1) Output wave showing the functionality of D FLIP-FLOP



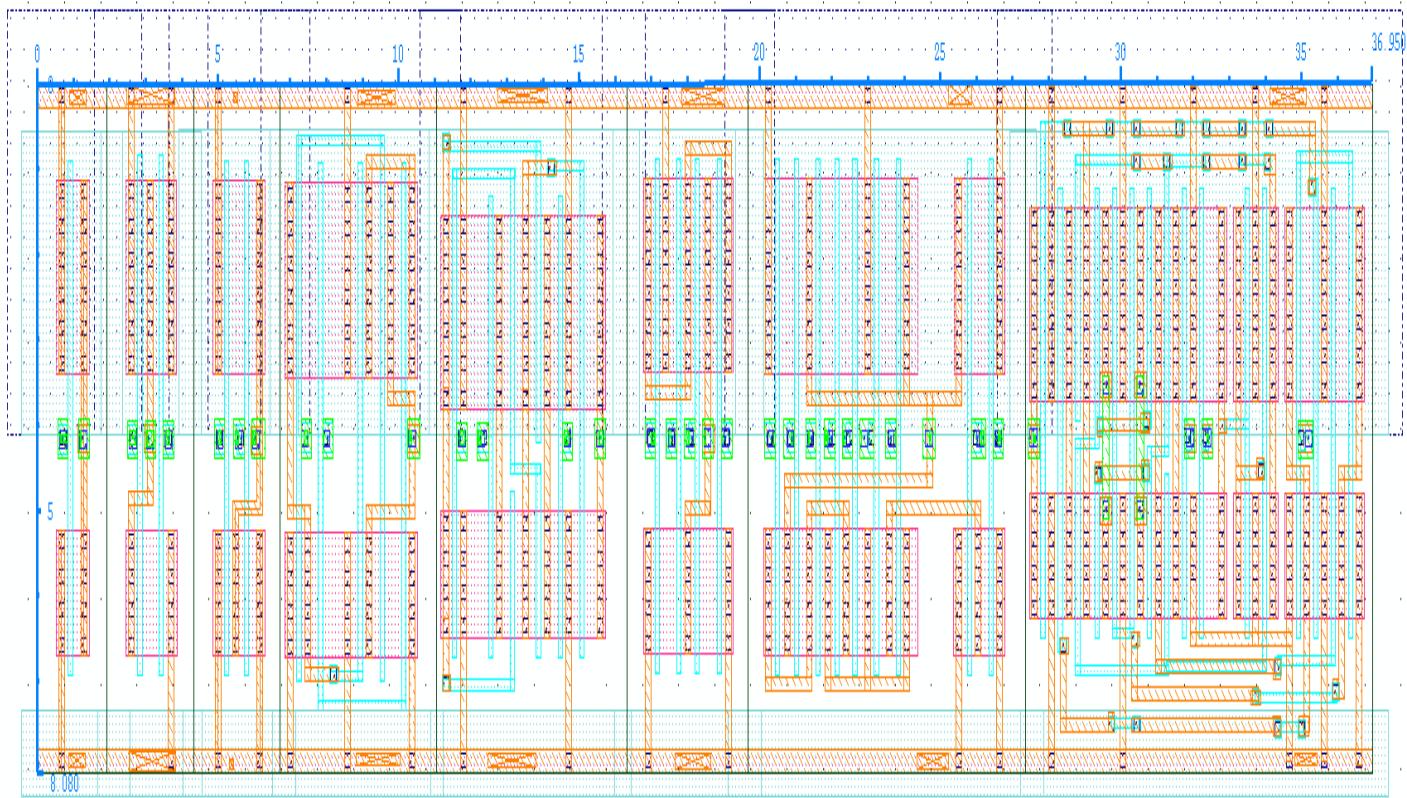
**2) Output waveform (passing '0', swept for different values of 'D')**



**3) Output waveform (passing '1', swept for different values of 'D'):**



### Final Concatenated Layout (Library name: project6, Cell name: aligned)



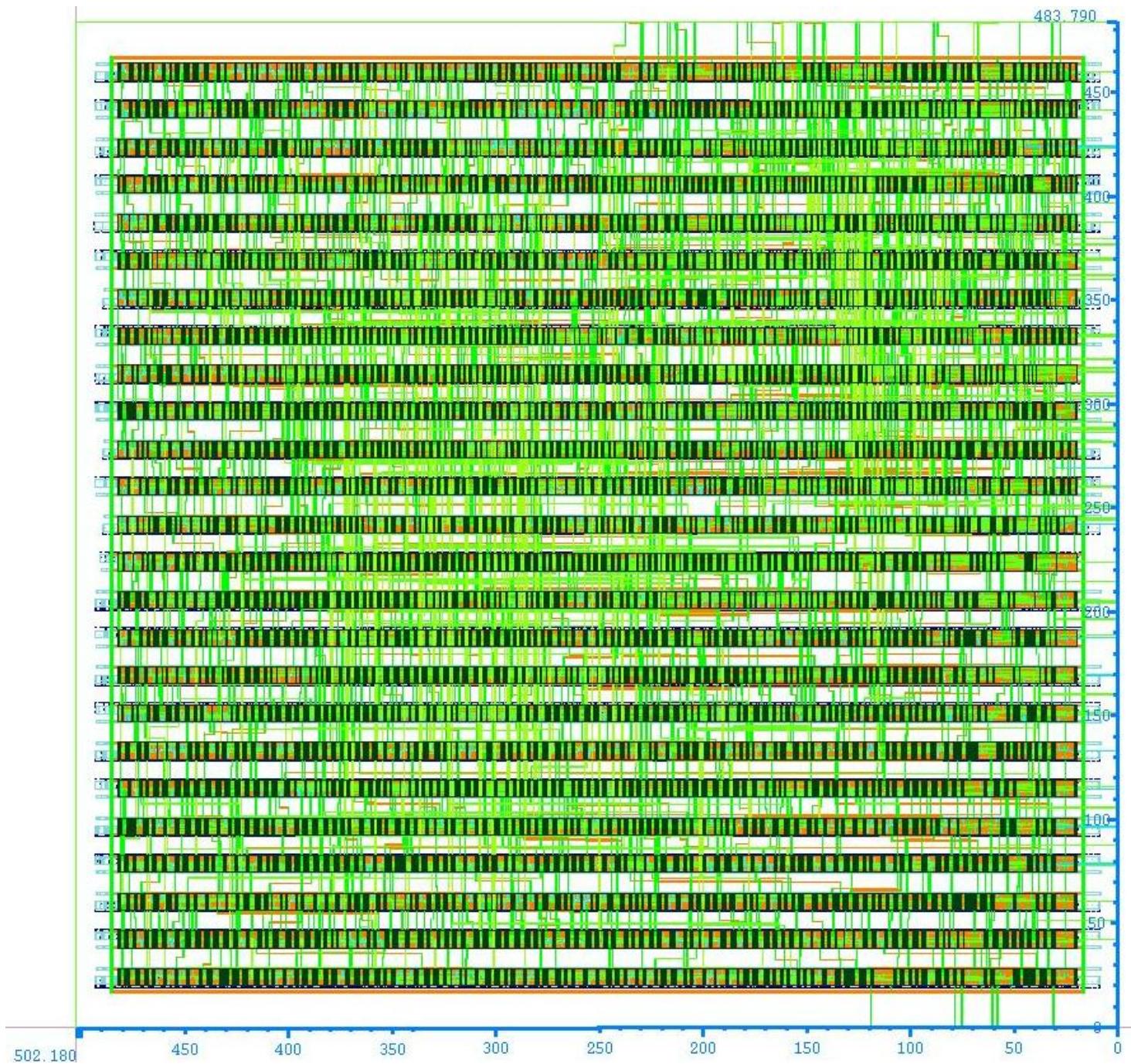
## TRADEOFFS

1. Energy delay product or EDP is used as a quality measure for a logic gate (Lesser the EDP better is the performance). In the process of minimizing the EDP we actually had to increase the total area of the Inverter. Increasing the area further would increase the EDP.
2. The height of the MUX layout has the maximum width because of which all the layout widths had to be increased. Using the extra green wires to increase the MUX speed would increase the MUX area and in turn increase the widths of the other cells to match the MUX width. So we have compromised speed with area by giving area more importance and not using extra green wires.
3. In DFF we have tried to minimize the diffusion breaks to two. Avoiding poly breaks leads to more diffusion breaks. Hence we had to have poly breaks in the layout.

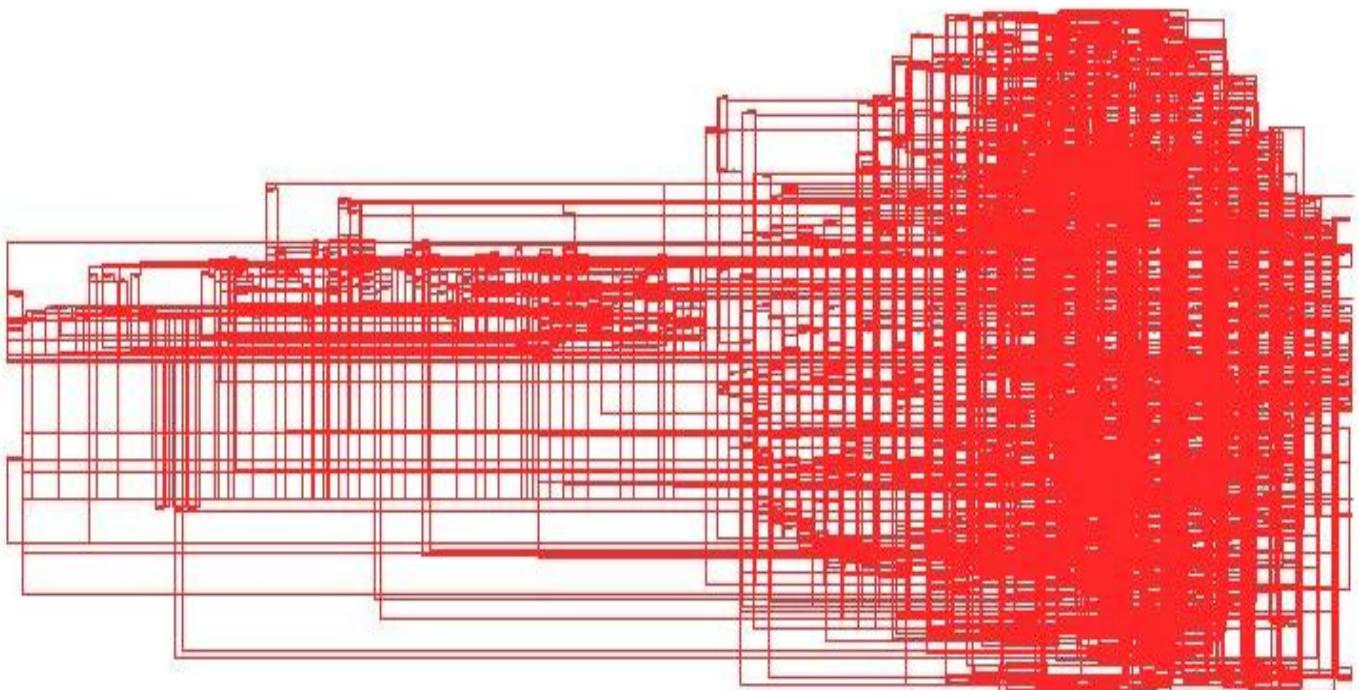
## PLACING AND ROUTING:

Cadence Encounter is used for the automatic placement and routing of synthesized verilognetlist . DRC and LVS are performed to check for errors, error free layout is then extracted using Assura RCX.

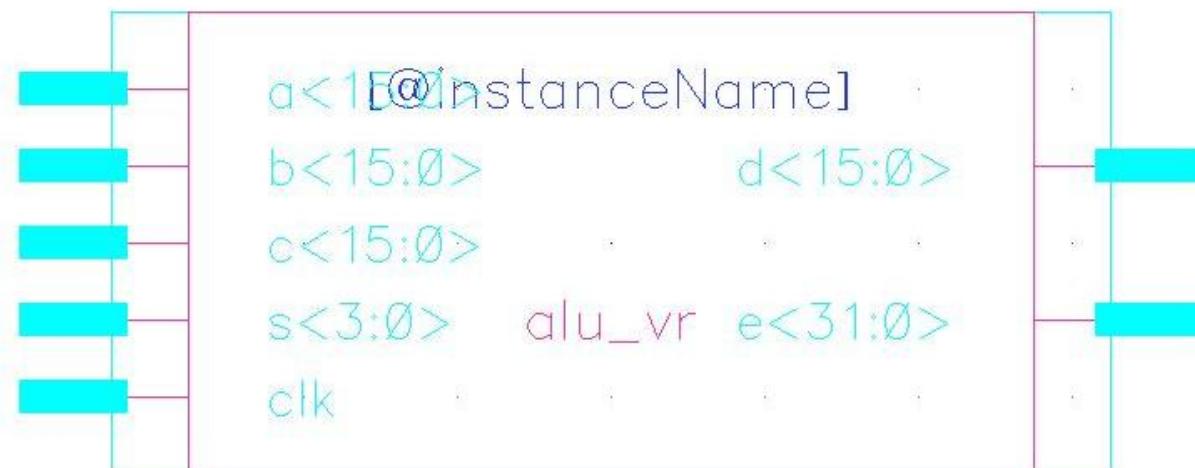
**FINAL ALU LAYOUT (Library name: project6, Cell name: alu\_vr)**



## ALU SCHEMATIC



## ALU SYMBOL



## Netlist

```
`timescale 1ns / 1ps
moduleinv(b, a);
input b;
output a;
assign a = ~b;
endmodule

module nand2(a, b, out);
input a, b;
output out;
assign out = ~(a & b);
endmodule

module nand3(a, b, c, out);
input a, b, c;
output out;
assign out = ~(a & b & c);
endmodule

module nand4(a, b, c, d, out);
input a, b, c, d;
output out;
assign out = ~(a & b & c & d);
endmodule

module nor2(a, b, out);
input a, b;
output out;
assign out = ~(a | b);
endmodule

module nor3(a, b, c, out);
input a, b, c;
output out;
assign out = ~(a | b | c);
endmodule

module xor2(a, b, out);
input a, b;
output out;
assign out = (a ^ b);
endmodule

module aoi12(a, b, c, out);
input a, b, c;
output out;
assign out = ~(a | (b & c));
endmodule

module aoi22(a, b, c, d, out);
input a, b, c, d;
output out;
assign out = ~((a & b) | (c & d));
endmodule

module oai12(a, b, c, out);
```

```

input a, b, c;
output out;
assign out = ~(a & (b | c));
endmodule

module oai22(a, b, c, d, out);
input a, b, c, d;
output out;
assign out = ~((a | b) & (c | d));
endmodule

module mux21(a, b, s, out);
input a, b, s;
output out;
assign out = (((~s) & a) | (s & b));
endmodule

module oai3222(a, b, c, d, e, f, g, h, i, out);
input a, b, c, d, e, f, g, h, i;
output out;
assign out = ~((a | b | c) & (d | e) & (f | g) & (h | i));
endmodule

moduledffreduced( D, clk, R, Q);
input D, clk, R;
output Q;
reg Q;
always @(posedgeclk or negedge R)
if (R == 1'b1)
    Q = 1'b0;
else
    Q = D;
endmodule

modulealu_vr ( a, b, c, s, clk, d, e );
input [15:0] a;
input [15:0] b;
input [15:0] c;
input [3:0] s;
output [15:0] d;
output [31:0] e;
inputclk;
wire n1280, n1281, n1282, n1283, n1284, n1285, n1286, n1287, n1288, n1289,
n1290, n1291, n1292, n1293, n1294, n1295, n1296, n1297, n1298, n1299,
n1300, n1301, n1302, n1303, n1304, n1305, n1306, n1307, n1308, n1309,
.
.
.
n4387, n4388, n4389, n4390, n4391, n4392, n4393, n4394, n4395, n4396,
n4397, n4398, n4399, n4400, n4401, n4402, n4403, n4404, n4405, n4406,
n4407, n4408, n4409, n4410, n4411, n4412;

dffreduced \e_reg[31] ( .D(n1296), .clk(n1407), .R(1'b0), .Q(e[31]) );
dffreduced \e_reg[30] ( .D(n1297), .clk(n1407), .R(1'b0), .Q(e[30]) );

```

```
dffreduced \e_reg[29] ( .D(n1298), .clk(n1407), .R(1'b0), .Q(e[29]) );
dffreduced \e_reg[28] ( .D(n1299), .clk(n1407), .R(1'b0), .Q(e[28]) );
dffreduced \e_reg[27] ( .D(n1300), .clk(n1407), .R(1'b0), .Q(e[27]) );
dffreduced \e_reg[26] ( .D(n1301), .clk(n1407), .R(1'b0), .Q(e[26]) );

.
.

inv U1502 ( .b(n2095), .a(n2098) );
inv U1503 ( .b(n2095), .a(n2099) );
inv U1504 ( .b(n4106), .a(n2100) );
inv U1505 ( .b(n2100), .a(n2101) );
inv U1506 ( .b(n2100), .a(n2102) );
inv U1507 ( .b(n2100), .a(n2103) );
inv U1508 ( .b(n2100), .a(n2104) );
inv U1522 ( .b(n4075), .a(n2118) );
inv U1523 ( .b(n2118), .a(n2119) );
inv U1524 ( .b(n2118), .a(n2120) );
inv U1525 ( .b(n2118), .a(n2121) );
inv U1526 ( .b(n2118), .a(n2122) );
inv U1527 ( .b(clk), .a(n1407) );
inv U1528 ( .b(n2123), .a(n1327) );

.
.

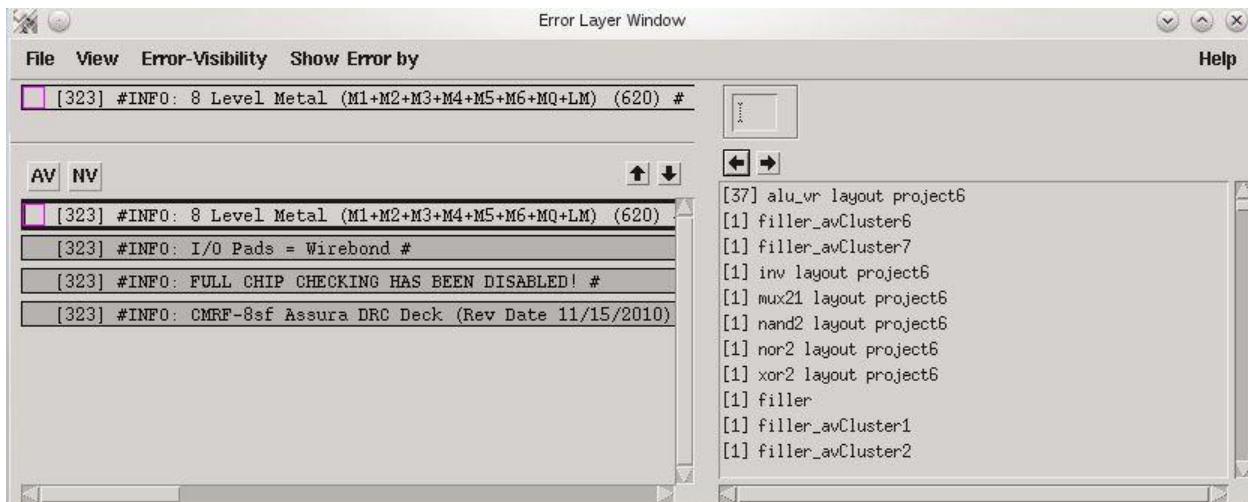
nor2 U3554 ( .a(n4157), .b(n4158), .out(n4156) );
inv U3555 ( .b(n4159), .a(n4158) );
aoi22 U3556 ( .a(d[5]), .b(n2051), .c(n2098), .d(b[5]), .out(n4159) );
xor2 U3557 ( .a(n4160), .b(n4161), .out(n4157) );
xor2 U3558 ( .a(n4162), .b(n4163), .out(n4161) );
nor2 U3559 ( .a(n4164), .b(n4165), .out(n4155) );
mux21 U3560 ( .a(n2067), .b(n2093), .s(n3997), .out(n4165) );
nand2 U3561 ( .a(b[5]), .b(a[5]), .out(n3997) );
mux21 U3562 ( .a(n4166), .b(n4167), .s(a[5]), .out(n4164) );
nand2 U3563 ( .a(n2104), .b(n4168), .out(n4167) );
nand2 U3564 ( .a(n2076), .b(n1824), .out(n4168) );

.
.

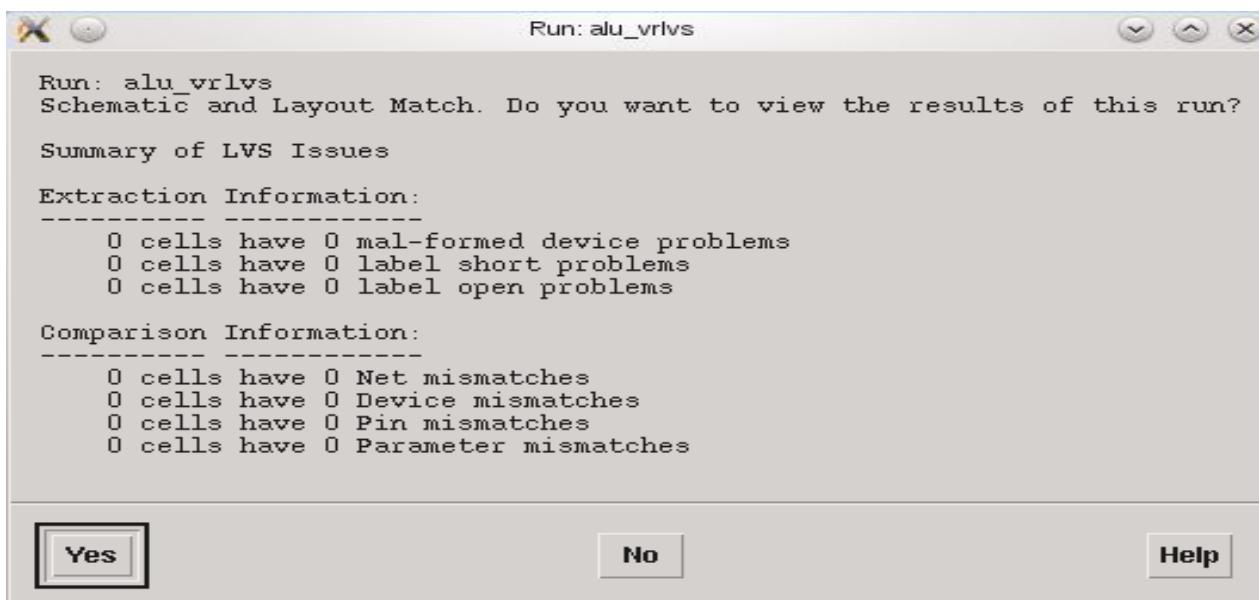
nand2 U3827 ( .a(n4316), .b(n4394), .out(n4087) );
nand2 U3828 ( .a(n4393), .b(n4056), .out(n4394) );

inv U3844 ( .b(n4074), .a(n4106) );
nand2 U3845 ( .a(n4408), .b(n4310), .out(n4074) );
nand2 U3846 ( .a(n4409), .b(n4393), .out(n4310) );
nand2 U3847 ( .a(n4399), .b(n4064), .out(n4408) );
nor2 U3848 ( .a(n4400), .b(n4398), .out(n4064) );
inv U3849 ( .b(s[3]), .a(n4400) );
nand2 U3850 ( .a(n4410), .b(n2041), .out(n4405) );
nand2 U3851 ( .a(n4411), .b(n4397), .out(n4077) );
nor2 U3860 ( .a(s[3]), .b(s[0]), .out(n4412) );
nand2 U3861 ( .a(n4409), .b(n4399), .out(n4075) );
nor2 U3862 ( .a(n2034), .b(s[2]), .out(n4399) );
inv U3863 ( .b(s[1]), .a(n4060) );
nor2 U3864 ( .a(s[3]), .b(n4398), .out(n4409) );
inv U3865 ( .b(s[0]), .a(n4398) );
endmodule
```

## DRC REPORT



## LVS REPORT



## PRIMETIME REPORT

PrimeTime (R)

PrimeTime (R) SI

PrimeTime (R) PX

Version D-2010.06-SP1 for suse64 -- Jul 15, 2010

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```
#####
# Define search path verilog file and library and variables
#####
setsearch_path "/home/eng/g/gxa130630/cad/primetime/test"
/home/eng/g/gxa130630/cad/primetime/test
source variables1
reset
#####
# link library
#####
setlink_library $library_file
library.db
settget_library $library_file
library.db
#set link_library [list $library_file ".db"]
#set target_library [list $library_file "ff.db"]
#####
# link design
#####
remove_design -all
Error: Nothing matched for designs: there are none loaded (SEL-005)
0
read_verilog $verilog_file
Loading verilog file '/home/eng/g/gxa130630/cad/primetime/test/alu_vr_syn.v'
1
#####
# Define IO parameters
#####
```

```
set_driving_cell -lib_cell $driving_cell -input_transition_rise $input_transition -input_transition_fall  
$input_transition [all_inputs]  
Loading db file '/home/eng/g/gxa130630/cad/primetime/test/library.db'  
Linking design alu_vr...  
Information: Issuing set_operating_conditions for setting analysis mode on_chip_variation. (PTE-037)  
set_operating_conditions -analysis_typeon_chip_variation -library [get_libs {library.db:lib_all}]  
1  
set_load $load [all_outputs]  
1  
#####  
#####  
#define the clock - for comb circuit we may not need to use any clock  
#####  
#####  
create_clock -name clk -period $clock_period [get_ports $clock_pin_name]  
1  
set_clock_transition -rise -max $input_transition [get_clocksclk]  
1  
set_clock_transition -fall -max $input_transition [get_clocksclk]  
1  
#####  
# set condition  
#####  
settiming_slew_propagation_modeworst_slew  
worst_slew  
settiming_report_unconstrained_paths true  
true  
setpower_enable_analysis true  
true  
set_disable_timing [get_ports $reset_pin_name]  
Warning: No port objects matched 'reset' (SEL-004)  
Error: Nothing matched for ports (SEL-005)  
Error: Nothing matched for object_list (SEL-005)  
0  
#####  
# analyze delay and power  
#####  
check_timing  
Warning: Some timing arcs have been disabled for breaking timing loops  
or because of constant propagation. Use the 'report_disable_timing'  
command to get the list of these disabled timing arcs. (PTE-003)  
Information: Checking 'no_input_delay'.  
Warning: There are 52 ports with no clock-relative input delay specified.
```

Since the variable 'timing\_input\_port\_default\_clock' is 'true',  
a default input port clock will be assumed for these ports.

Information: Checking 'no\_driving\_cell'.

Information: Checking 'unconstrained\_endpoints'.

Warning: There are 48 endpoints which are not constrained for maximum delay.

Information: Checking 'unexpandable\_clocks'.

Information: Checking 'latch\_fanout'.

Information: Checking 'no\_clock'.

Information: Checking 'partial\_input\_delay'.

Information: Checking 'generic'.

Information: Checking 'loops'.

Information: Checking 'generated\_clocks'.

Information: Checking 'pulse\_clock\_non\_pulse\_clock\_merge'.

Information: Checking 'pll\_configuration'.

0

update\_timing

1

report\_timing -transition\_time -delay min\_max -capacitance -input\_pins

\*\*\*\*\*

Report : timing

-path\_type full  
-delay\_typemin\_max  
-input\_pins  
-max\_paths 1  
-transition\_time  
-capacitance

Design :alu\_vr

Version: D-2010.06-SP1

Date : Mon Dec 16 15:25:44 2013

\*\*\*\*\*

Startpoint: a[1] (input port)

Endpoint: d\_reg[1] (falling edge-triggered flip-flop clocked by clk')

Path Group: clk

Path Type: min

Point	Cap	Trans	Incr	Path
clock (input port clock) (rise edge)		0.00	0.00	

clock network delay (ideal)		0.00	0.00
input external delay		0.00	0.00 f
a[1] (in)	35.95	35.55	30.84 30.84 f
U3506/s (mux21)		35.55	0.00 30.84 f
U3506/out (mux21)		5.53	20.61 81.52 112.35 r
U3503/a (nor2)		20.61	0.00 112.35 r
U3503/out (nor2)		5.35	12.34 23.52 135.88 f
U3497/a (nand2)		12.34	0.00 135.88 f
U3497/out (nand2)		6.05	20.41 27.05 162.93 r
d_reg[1]/D (dffreduced)		20.41	0.00 162.93 r
data arrival time			162.93
clockclk' (fall edge)		20.00	0.00 0.00
clock network delay (ideal)			0.00 0.00
d_reg[1]/clk (dffreduced)			0.00 f
library hold time		-10.64	-10.64
data required time			-10.64
data required time			-10.64
data arrival time			-162.93
slack (MET)			173.57

Startpoint: s[0] (input port)

Endpoint: e\_reg[30] (falling edge-triggered flip-flop clocked by clk')

Path Group: clk

Path Type: max

Point	Cap	Trans	Incr	Path
clock (input port clock) (rise edge)		0.00	0.00	
input external delay		0.00	0.00 r	
s[0] (in)	28.12	54.27	39.78	39.78 r
U3865/b (inv)		54.27	0.00	39.78 r
U3865/a (inv)	19.40	30.33	44.80	84.58 f
U3848/b (nor2)		30.33	0.00	84.58 f
U3848/out (nor2)		22.50	93.79	98.76 183.34 r
U3477/a (nand2)		93.79	0.00	183.34 r
U3477/out (nand2)	5.37	33.25	43.72	227.06 f
U3476/a (nor2)		33.25	0.00	227.06 f

U3476/out (nor2)	16.97	75.81	91.89	318.95	r
U1434/b (inv)		75.81	0.00	318.95	r
U1434/a (inv)	16.14	32.87	45.32	364.27	f
U1436/b (inv)		32.87	0.00	364.27	f
U1436/a (inv)	22.37	45.90	58.45	422.72	r
U1253/b (inv)		45.90	0.00	422.72	r
U1253/a (inv)	16.14	26.13	38.74	461.45	f
U1256/b (inv)		26.13	0.00	461.45	f
U1256/a (inv)	22.63	45.51	55.19	516.65	r
U1248/b (inv)		45.51	0.00	516.65	r
U1248/a (inv)	16.14	26.01	38.60	555.24	f
U1251/b (inv)		26.01	0.00	555.24	f
U1251/a (inv)	22.38	45.08	54.79	610.03	r
U3424/b (nand2)		45.08	0.00	610.03	r
U3424/out (nand2)	5.27	29.35	36.14	646.17	f
U3423/a (mux21)		29.35	0.00	646.17	f
U3423/out (mux21)	5.35	19.54	83.00	729.17	f
U3418/a (nand2)		19.54	0.00	729.17	f
U3418/out (nand2)	5.78	23.64	30.40	759.57	r
U1280/b (inv)		23.64	0.00	759.57	r
U1280/a (inv)	21.52	23.67	35.17	794.73	f
U1281/b (inv)		23.67	0.00	794.73	f
U1281/a (inv)	22.50	45.05	53.72	848.45	r
U2774/b (nand2)		45.05	0.00	848.45	r
U2774/out (nand2)	10.56	30.24	44.34	892.79	f
U2772/a (nor2)		30.24	0.00	892.79	f
U2772/out (nor2)	5.78	40.30	59.16	951.94	r
U2771/b (inv)		40.30	0.00	951.94	r
U2771/a (inv)	20.31	27.26	40.95	992.89	f
U2692/a (nand2)		27.26	0.00	992.89	f
U2692/out (nand2)	20.71	47.83	55.48	1048.37	r
U2690/a (nor2)		47.83	0.00	1048.37	r
U2690/out (nor2)	5.38	20.75	31.64	1080.01	f
U2689/b (inv)		20.75	0.00	1080.01	f
U2689/a (inv)	5.34	18.30	27.98	1107.99	r
U2684/a (aoi22)		18.30	0.00	1107.99	r
U2684/out (aoi22)	20.38	52.13	62.33	1170.32	f
U2575/b (xor2)		52.13	0.00	1170.32	f
U2575/out (xor2)	8.85	33.30	103.51	1273.83	f
U2574/a (xor2)		33.30	0.00	1273.83	f
U2574/out (xor2)	14.95	41.31	94.82	1368.65	f
U2548/a (aoi22)		41.31	0.00	1368.65	f

U2548/out (aoi22)	21.03	81.18	104.53	1473.19 r
U2463/b (xor2)		81.18	0.00	1473.19 r
U2463/out (xor2)	9.13	65.92	109.47	1582.66 r
U2462/a (xor2)		65.92	0.00	1582.66 r
U2462/out (xor2)	15.05	82.69	122.95	1705.61 r
U2422/a (aoi22)		82.69	0.00	1705.61 r
U2422/out (aoi22)	20.38	59.89	89.03	1794.64 f
U2358/b (xor2)		59.89	0.00	1794.64 f
U2358/out (xor2)	8.85	33.30	105.63	1900.27 f
U2357/a (xor2)		33.30	0.00	1900.27 f
U2357/out (xor2)	14.95	41.43	94.82	1995.10 f
U2307/a (aoi22)		41.43	0.00	1995.10 f
U2307/out (aoi22)	21.03	81.18	104.59	2099.69 r
U2269/b (xor2)		81.18	0.00	2099.69 r
U2269/out (xor2)	9.13	65.92	109.47	2209.16 r
U2268/a (xor2)		65.92	0.00	2209.16 r
U2268/out (xor2)	15.05	82.69	122.95	2332.11 r
U2200/a (aoi22)		82.69	0.00	2332.11 r
U2200/out (aoi22)	10.73	47.85	73.41	2405.52 f
U2196/b (inv)		47.85	0.00	2405.52 f
U2196/a (inv)	15.18	38.17	55.97	2461.50 r
U2077/b (xor2)		38.17	0.00	2461.50 r
U2077/out (xor2)	9.13	63.61	99.49	2560.99 r
U2076/a (xor2)		63.61	0.00	2560.99 r
U2076/out (xor2)	21.15	102.44	139.60	2700.59 r
U2075/b (nand2)		102.44	0.00	2700.59 r
U2075/out (nand2)	5.31	30.85	44.48	2745.07 f
U2071/a (aoi22)		30.85	0.00	2745.07 f
U2071/out (aoi22)	21.03	81.19	99.85	2844.92 r
U1949/b (xor2)		81.19	0.00	2844.92 r
U1949/out (xor2)	9.13	64.38	109.47	2954.39 r
U1948/a (xor2)		64.38	0.00	2954.39 r
U1948/out (xor2)	10.46	38.84	51.67	3006.06 f
U1947/b (inv)		38.84	0.00	3006.06 f
U1947/a (inv)	15.37	36.52	51.57	3057.64 r
U1946/b (nand2)		36.52	0.00	3057.64 r
U1946/out (nand2)	5.31	30.85	34.15	3091.78 f
U1943/a (aoi22)		30.85	0.00	3091.78 f
U1943/out (aoi22)	21.15	81.51	100.13	3191.91 r
U1826/b (xor2)		81.51	0.00	3191.91 r
U1826/out (xor2)	9.13	64.33	109.53	3301.44 r
U1825/a (xor2)		64.33	0.00	3301.44 r

U1825/out (xor2)	20.88	101.68	138.95	3440.39 r
U1824/b (nand2)		101.68	0.00	3440.39 r
U1824/out (nand2)	19.58	49.07	71.56	3511.95 f
U1711/a (nand2)		49.07	0.00	3511.95 f
U1711/out (nand2)	5.51	28.54	42.23	3554.18 r
U1710/b (nor2)		28.54	0.00	3554.18 r
U1710/out (nor2)	10.73	22.37	28.92	3583.09 f
U1709/a (nand2)		22.37	0.00	3583.09 f
U1709/out (nand2)	5.53	31.18	31.50	3614.59 r
U1706/a (nand2)		31.18	0.00	3614.59 r
U1706/out (nand2)	4.74	19.69	30.52	3645.12 f
U1705/b (nor2)		19.69	0.00	3645.12 f
U1705/out (nor2)	5.51	38.53	45.92	3691.04 r
U1704/b (nor2)		38.53	0.00	3691.04 r
U1704/out (nor2)	5.37	16.50	25.49	3716.53 f
U1701/a (nor2)		16.50	0.00	3716.53 f
U1701/out (nor2)	5.51	38.54	53.17	3769.70 r
U1700/b (nor2)		38.54	0.00	3769.70 r
U1700/out (nor2)	5.08	25.67	25.13	3794.84 f
U1699/c (aoi22)		25.67	0.00	3794.84 f
U1699/out (aoi22)	11.04	56.89	54.59	3849.42 r
U1698/b (nor2)		56.89	0.00	3849.42 r
U1698/out (nor2)	5.37	20.30	28.63	3878.05 f
U1695/a (nor2)		20.30	0.00	3878.05 f
U1695/out (nor2)	11.31	57.40	71.17	3949.22 r
U1693/a (nand2)		57.40	0.00	3949.22 r
U1693/out (nand2)	15.64	38.75	55.89	4005.11 f
U1692/b (nand2)		38.75	0.00	4005.11 f
U1692/out (nand2)	5.66	27.70	43.37	4048.48 r
U1691/b (nand2)		27.70	0.00	4048.48 r
U1691/out (nand2)	5.31	18.47	32.03	4080.51 f
U1683/a (aoi22)		18.47	0.00	4080.51 f
U1683/out (aoi22)	11.04	57.03	72.27	4152.78 r
U1682/b (nor2)		57.03	0.00	4152.78 r
U1682/out (nor2)	5.37	20.32	28.65	4181.42 f
U1679/a (nor2)		20.32	0.00	4181.42 f
U1679/out (nor2)	11.31	57.40	71.18	4252.60 r
U1677/a (nand2)		57.40	0.00	4252.60 r
U1677/out (nand2)	15.64	38.75	55.89	4308.49 f
U1676/b (nand2)		38.75	0.00	4308.49 f
U1676/out (nand2)	5.66	27.70	43.37	4351.86 r
U1675/b (nand2)		27.70	0.00	4351.86 r

U1675/out (nand2)	5.31	18.47	32.03	4383.89 f
U1671/a (aoi22)		18.47	0.00	4383.89 f
U1671/out (aoi22)	10.92	56.33	72.00	4455.89 r
U1667/a (nand2)		56.33	0.00	4455.89 r
U1667/out (nand2)	8.85	30.87	44.42	4500.30 f
U1666/a (xor2)		30.87	0.00	4500.30 f
U1666/out (xor2)	5.19	30.74	83.54	4583.85 f
U1665/b (nand2)		30.74	0.00	4583.85 f
U1665/out (nand2)	6.05	26.12	40.22	4624.06 r
e_reg[30]/D (dffreduced)		26.12	0.00	4624.06 r
data arrival time				4624.06
 -----				
clockclk' (fall edge)	0.00	5000.00	5000.00	
clock network delay (ideal)		0.00	5000.00	
e_reg[30]/clk (dffreduced)			5000.00 f	
library setup time	-43.95	4956.05		
data required time		4956.05		
 -----				
data required time		4956.05		
data arrival time	-4624.06			
 -----				
slack (MET)		331.99		

1

update\_power

Information: Checked out license 'PrimeTime-PX' (PT-019)

Warning: Neither event file or switching activity data present for power estimation. The command will propagate switching activity values for power calculation. (PWR-246)

Information: Running averaged power analysis... (PWR-601)

1

report\_power

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Report : Averaged Power

Design :alu\_vr

Version: D-2010.06-SP1

Date : Mon Dec 16 15:25:45 2013

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Attributes

-----  
i - Including register clock pin internal power

u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
<hr/>					
io_pad	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	
clock_network	6.999e-04	8.030e-05	8.268e-10	7.802e-04 (52.69%)	i
register	3.344e-05	4.722e-06	4.594e-07	3.862e-05 ( 2.61%)	
combinational	3.175e-04	3.415e-04	2.910e-06	6.620e-04 (44.70%)	
sequential	0.0000	0.0000	0.0000	0.0000 ( 0.00%)	

Net Switching Power = 4.265e-04 (28.81%)

Cell Internal Power = 1.051e-03 (70.97%)

Cell Leakage Power = 3.370e-06 ( 0.23%)

-----  
Total Power = 1.481e-03 (100.00%)

1

Information: Defining new variable 'driving\_cell'. (CMD-041)

Information: Defining new variable 'library\_file'. (CMD-041)

Information: Defining new variable 'verilog\_file'. (CMD-041)

Information: Defining new variable 'input\_transition'. (CMD-041)

Information: Defining new variable 'clock\_period'. (CMD-041)

Information: Defining new variable 'load'. (CMD-041)

Information: Defining new variable 'reset\_pin\_name'. (CMD-041)

Information: Defining new variable 'clock\_pin\_name'. (CMD-041)

## TESTING

The Xilinx waveforms of the alu Verilog code and the simulation from the generated alu\_syn.v of the designed alu are compared and found to match.

The test bench is shown below:

```
module alu_vrtf;

// Inputs
reg [15:0] a;
reg [15:0] b;
reg [15:0] c;
reg [3:0] s;
reg clk;

// Outputs
wire [15:0] d;
wire [31:0] e;

// Instantiate the Unit Under Test (UUT)
alu_vruut (
    .a(a),
    .b(b),
    .c(c),
    .s(s),
    .clk(clk),
    .d(d),
    .e(e)
);
initial begin
    clk = 0;
    a=0;
    b=0;
    c=0;
    s=0;
end

always
#5 clk = ~clk;

initial
begin
```

```
// Add stimulus here
a = 16'b00010100101001000 ; #10;
b = 16'b0101011000101001      ; #10;
c = 16'b0111011000101101 ; #10;
s= 4'b0000; #10;

s= 4'b0001; #10;

s= 4'b0010; #10;

s= 4'b0011; #10;

s= 4'b0100; #10;

s= 4'b0101; #10;

s= 4'b0110; #10;

s= 4'b0111; #10;

s= 4'b1000; #10;

s= 4'b1001; #10;

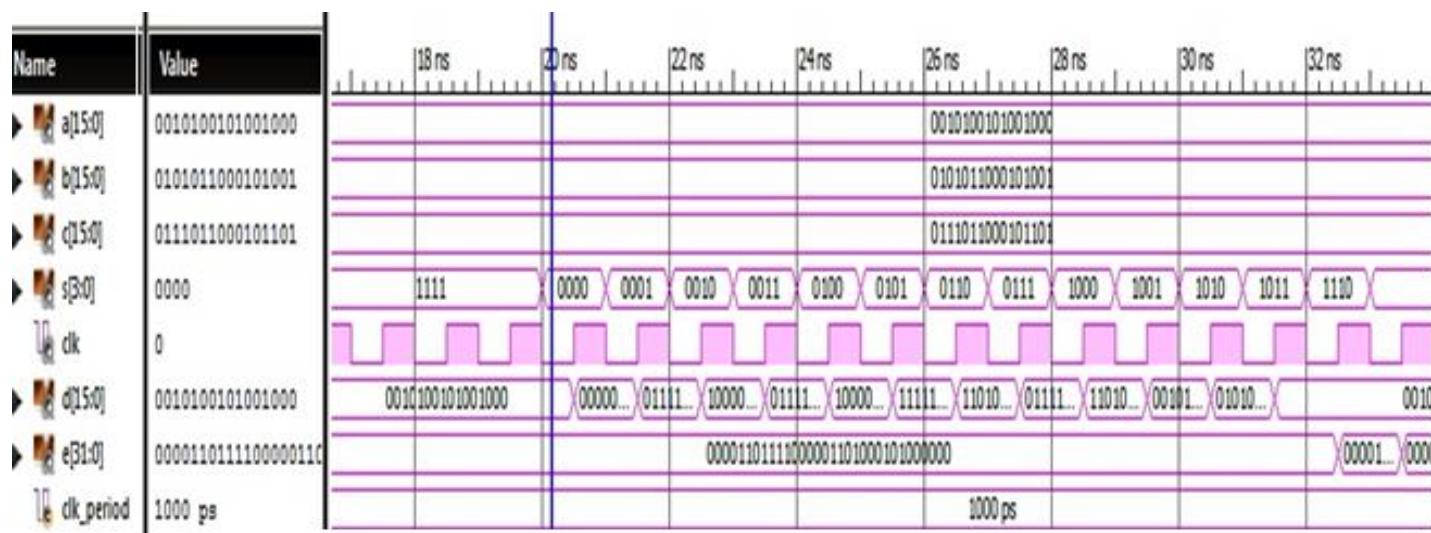
s= 4'b1010; #10;

s= 4'b1011; #10;

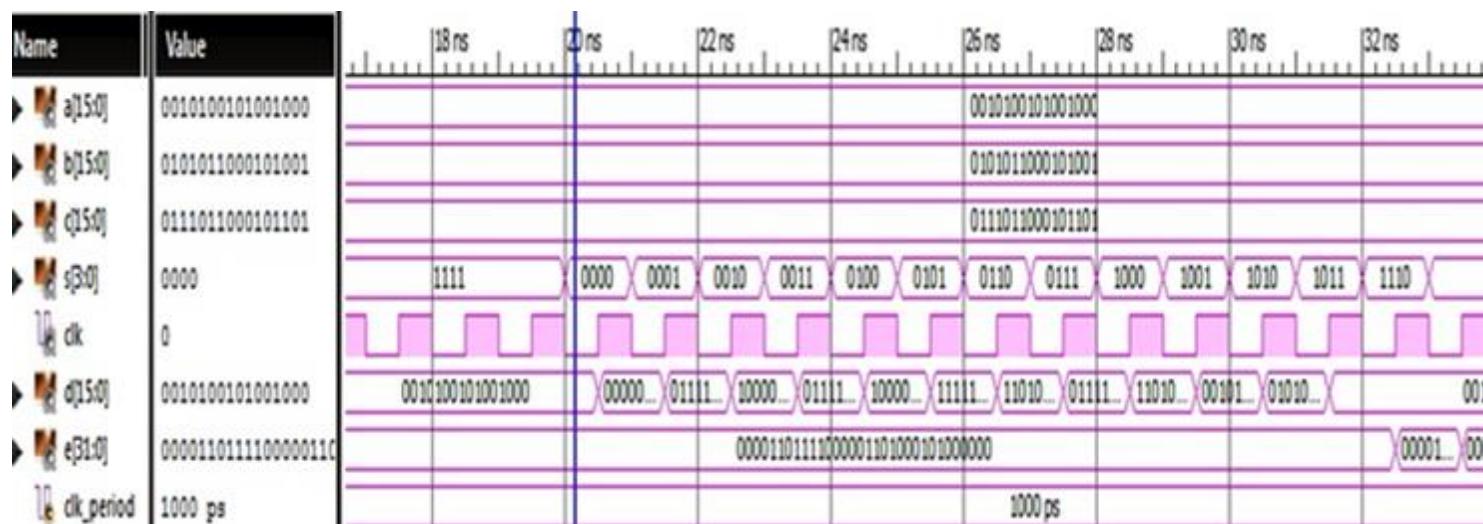
s= 4'b1110; #10;

s= 4'b1111; #10;
end
endmodule
```

### Simulation from Mapped VHDL Code



### Simulation from Behavioral VHDL Code



### CONCLUSION:

The design specification has been met and the ALU has been designed. The output waveforms mapped from Verilog netlist are same as the expected waveforms, verifying the functionality.