Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
2. Program and Data stored in Separate Memory
3. Program and Data stored in same Memory
4. Program and data stored in Cache Memory
5. All of Above
6. Which of the following is the working cycle of CPU
7. Decode, Execute, Fetch
8. Fetch, Decode, Execute
9. Fetch, Execute , Decode
10. All of Above
11. Any condition that causes a processor to stall is called as \_\_\_\_\_\_\_\_\_
12. Hazard
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. Control signals
    4. Timing signals
17. What do processors of all computers must have?
    1. Control unit
    2. ALU
    3. Primary Storage
    4. All of these
18. Which is the fastest memory in the computer?
19. Cache
20. Ram
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_ we reduce the memory access time:
    1. SDRAM
    2. Cache
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. Super-scalar
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. Pipe-lining
    3. Parallel Computation
    4. None of the mentioned
26. A 24 bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. 16,777,216
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

Answer:

Name = 40 characters (40 bytes)

No. of countries= 3100

States = 2 bytes

Population =

= 4 bytes

Space the whole database will take for each country.

= 40+ 2 + 8

= 50 bytes

Space the whole database will take for 3100 countries.

= 50 \* 3100

= 155000 bytes

In kb =

=151.36 kb

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

Answer:

|  |
| --- |
| Let the width of the data bus be X  16GB = 232 \* x  16 \* 230 bytes = 232 \* X  24 \* 230 = 232 \* X  234 = 232 \* X  X = 22 bytes  X = 4 |

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

Answer:

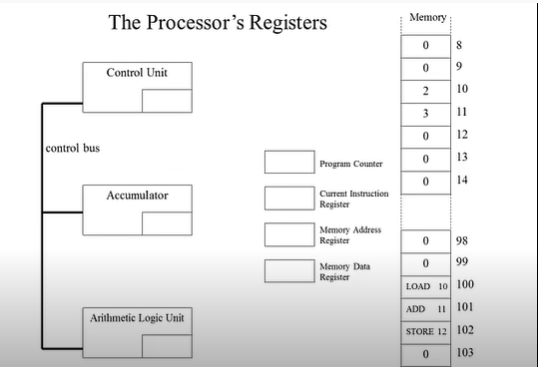
|  |
| --- |
| Let the width of the data bus be X.  16GB = 233 \* x  16 \* 230 bytes = 233 \* X  24 \* 230 = 233 \* X  234 = 233 \* X  X = 21  X = 2 |

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add : [11]

Store: [12]



The steps that a processor follows to execute a program is called the Instruction Cycle of a processor. The instruction cycle is the basic operation of the CPU which consists of three steps which are Fetch, Decode, Execute cycle. The CPU repetitively performs these three steps to execute one program instruction.

In the example given above, the instruction cycle works on the basis of three instruction as load, add and store.

The first step is Fetch. In this step, the processor fetches the instruction from memory.

The second step is Decode. In this step, the processor decodes the instruction to determine what the instruction is.

The third step is Execute. In this step, the processor executes the information by loading memory address into its register.

In the given example, the instruction cycle runs in the following way.

First, the processor fetches the instruction load: [10]. The decoder loads the value from memory to register. The processor now executes the information by loading memory address 2(two) into its register.

Now, the processor fetches another instruction which is Add:[11]. Then the decoder adds the value from memory to register. The processor executes the information by adding memory address 3 into its register.

And finally, the processor fetches the instruction Store:[12]. The decoder stores the value from memory to register. The processor executes the information by storing 5 (2+3=5) to memory address 12.

In this way, the instruction cycle runs through different steps.

1. Write short notes on the following topic:
2. Von Neumann and Harvard Architecture

The Von Neumann Architecture is a classic type of computer architecture that follows the concept of a stored-program computer.

It uses one single physical address for accessing and storing both data and instructions. It consists of a CPU and a Program instruction and data memory (combined) which is used to access and store data with one single physical memory. Meaning that the data and program instructions are stored in same memory.

Harvard architecture is a type of computer architecture that separates its memory into two parts, so data and instructions are store separately. The architecture also has separate buses of different sizes for data transfers and fetching instruction. This allows the CPU to fetch data and instructions at the same time. This architecture allows for faster operation.

1. RISC vs SISC architecture

RISC is a Reduced Instruction Set Computer. It is built to minimize the instruction execution time by optimizing and limiting the number of instructions. It means each instruction cycle requires only one clock cycle, and each cycle contains three parameters: fetch, decode and execute. It uses LOAD and STORE instruction to access the memory location. RISC processor is simpler than a CISC processor because of its simple and quick design, and it can complete its work in one clock cycle. RISC optimises cycles per instruction.

The CISC Stands for Complex Instruction Set Computer. It is built to make programming easier, either for assembly programmer or compiler programmer. CISC optimises instructions per program. It has a large collection of complex instructions that range from simple to very complex and specialized in the assembly language level, which takes a long time to execute the instructions. So, CISC approaches reducing the number of instructions on each program and ignoring the number of cycles per instruction. The length of the code is shorts, so it requires very little RAM. It requires a single register set to store the instruction.