**Instruction:**

Complete all questions in **1 hour.**

1. What is flip flop? Describe the working mechanism RS flip flop.

**Answer:** flip-flops is a circuit that have two stable states that can store state information.

The working mechanism of RS flip flop: RS flip flop consists of two inputs as R and S which stands for Reset and Set. It gives two outputs as Q and . When the inputs in Reset and Set are zero (0), the output cannot be determined because the input in input one and input two is also not determined, which can be seen in the figure given below.

|  |  |
| --- | --- |
|  | A picture containing text, electronics, keyboard  Description automatically generated |
|  |  |

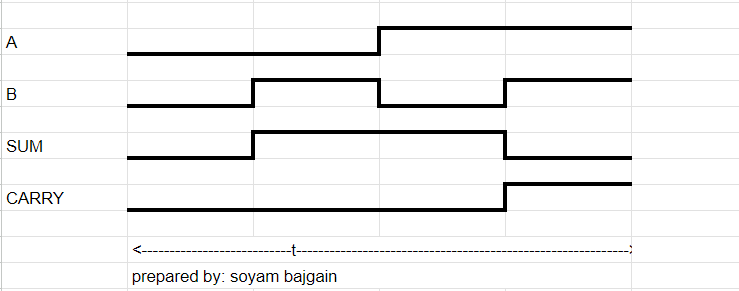
First the inputs are 1 and 0, in S and R respectively, in the IP1 (input one) the input is one which means the output will be zero (in N-OR gate if one input is high the output will be high). And the OP2 (output two) is connected to IP1, which has low input i.e. 0, OP1 (the output one) will be high (1). So, Q will be 1 and will be 0. Now, when the S is set to 0 and R is set to 1, the OP1 will be 0 due to the property of N-OR gate. The OP1 is connected to IP1 which has 0 as an input. So, the OP2 will be zero. When both inputs are 1, the outputs will be invalid.

1. Construct the timing diagram for half adder and half subtractor, full adder.

**Answer:**

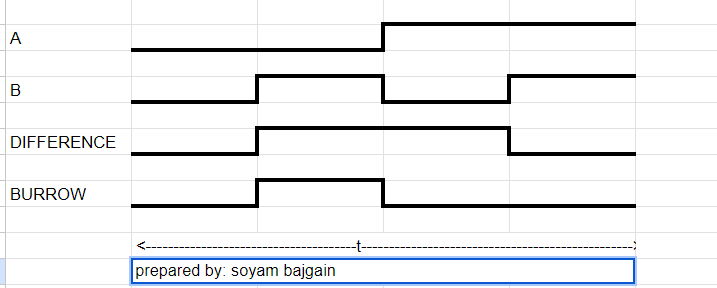
Half adder

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



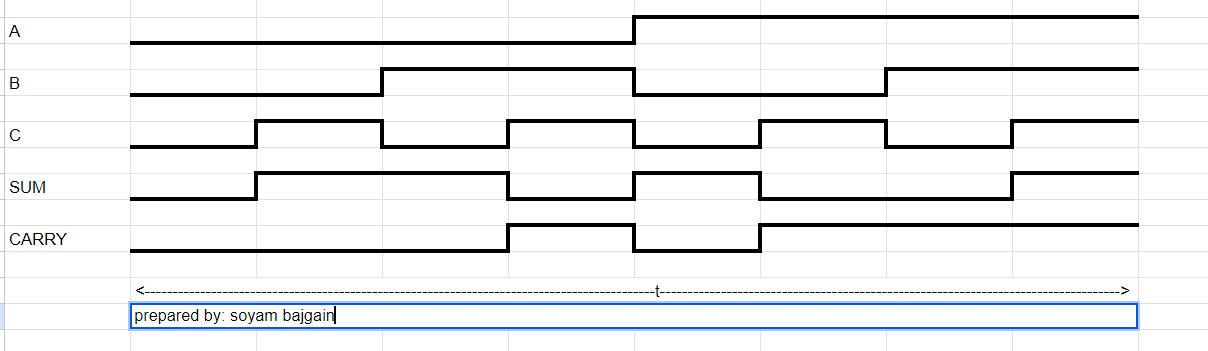
Half subtractor:

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | DIFFERENCE | BURROW |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

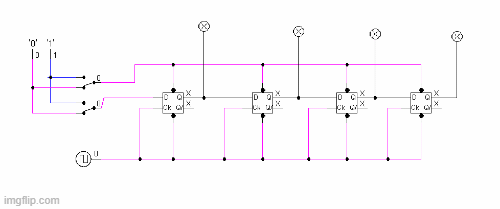


Full Adder:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



1. Describe the working mechanism of 4-bit register by constructing the circuit using D flip flop.



Here, the given circuit is a 4-bit shift register using D-type flip-flop. The working mechanism of the given circuit is given below.

In this type of circuit, the clock input of all the D-type is connected in a common line (due to which they receive clock inputs simultaneously), which can be seen in the figure above. Since we are using D-type flip-flop, the input at D transfers to output Q on the rising edge of every clock pulse and they all do this operation together on the rising edge. This type of shift register is also known as serial in parallel out register.

1. Differentiate between:
2. Flip flop and Latch

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| --- | --- |
| **Flip-flop** | **Latch** |
| Flip-flop is a basic digital memory circuit, which stores one bit of information | Latch is an electronic device, which changes its output immediately based on the applied input. |
| It checks the inputs but changes the output only at times defined by the clock signal or any other control signal. | It checks the inputs continuously and responds to the changes in inputs immediately. |
| Flip-flop always have a clock signal | Latches doesn’t have a clock signal |
| It is an edge triggered device. | It is a level triggered device. |

1. Combinational circuit and Sequential circuit

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| --- | --- |
| **Combinational Circuit** | **Sequential Circuit** |
| Combinational circuits are defined as the time independent circuits which do not depends upon previous inputs to generate any output are termed as combinational circuits. | Sequential circuits are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output. |
| In this circuit, output depends only upon present input. | In this circuit, output depends upon present as well as past input. |
| Combinational circuits don’t have capability to store any state. | Sequential circuits have capability to store any state or to retain earlier state. |
| This is time independent. | This is time dependent. |

1. SIPO and PISO shift register

|  |  |
| --- | --- |
| **SIPO shift register** | **PISO shift register** |
| It stands for Serial In Parallel Out register. | It stands for Parallel In Serial Out register. |
| The shift registers which take data in by series by one bit and gives output in parallel is called SIPO Shift Register. | The shift registers which take data in by parallel by one bit and gives output in series is called PISO Shift Register. |
| For 'n' bit serial input data which need to be stored, the number of clock pulse required are equal to 'n'. | To store 'n' bit; number of clock pulse required is equal to 1. |