

Non ideal I-V Effects

In an ideal I-V model of eqs.

$$I_{ds} = \beta [V_{gs} - V_t - \frac{V_{ds}}{2}] V_{ds}, V_{ds} < V_{dsat}$$

linear

$$\text{and } I_{ds} = \frac{\beta}{2} [V_{gs} - V_t]^2, V_{ds} > V_{dsat}$$

saturation

neglects many effects that are important to modern devices.

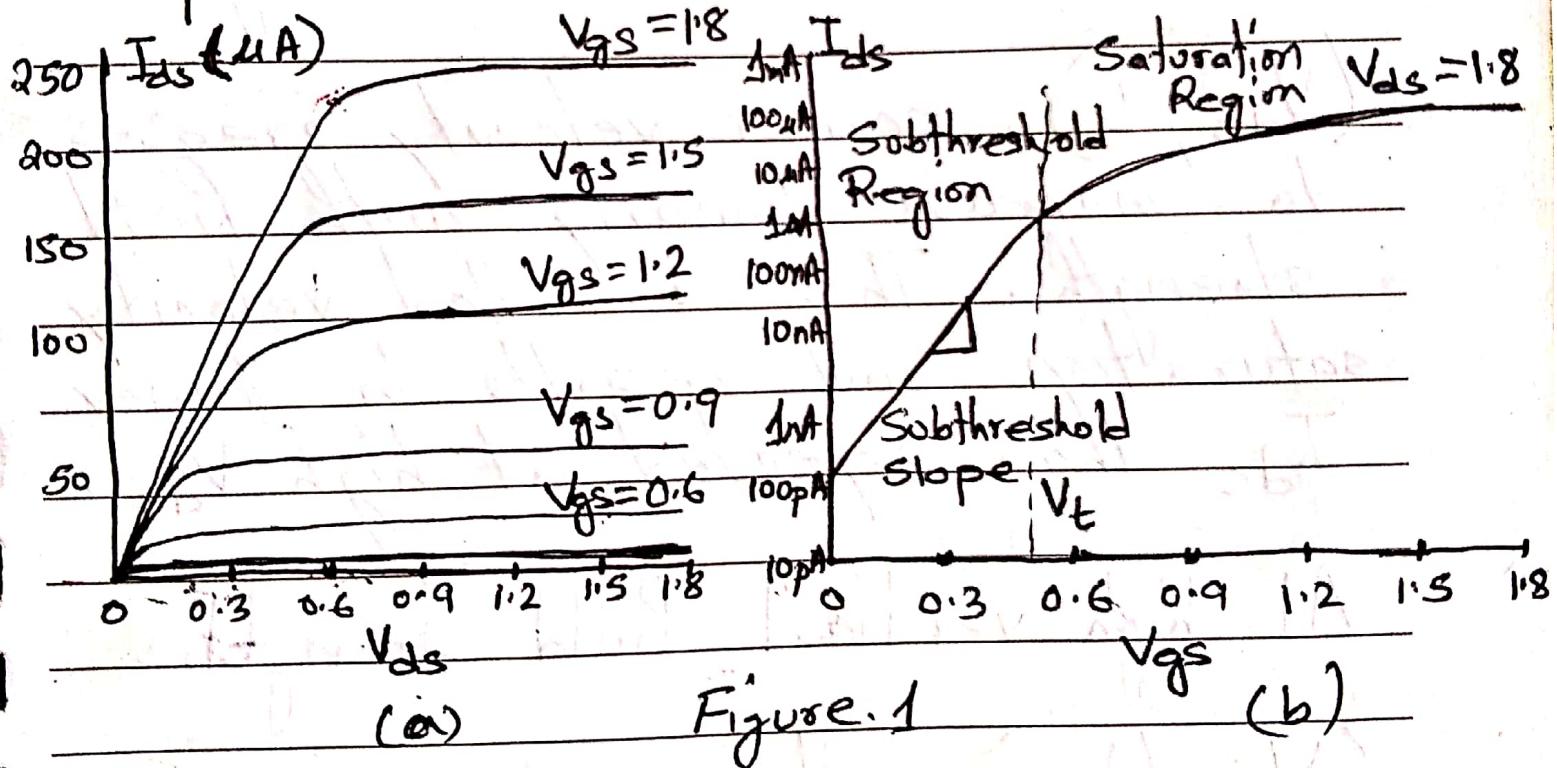


Figure 1 shows the simulated I-V characteristics of a unit nMOS transistor in a 180 nm process.

Now compare the characteristics in linear and saturation regions in fig 1a

to those in ideal device, the saturation current increases less than quadratically with increasing V_{gs} .

This is caused by two effects:
velocity saturation and mobility degradation.

At high lateral field strengths

(V_{ds}/l), carrier velocity creases to increase linearly with field strength. This is called velocity saturation and results in lower I_{ds} than expected at high V_{ds} .

At high vertical field strengths

(V_{gs}/t_{ox}), the carriers scatter more often. This mobility degradation effect also leads to less current than expected at high V_{gs} . The saturation current of the nonideal transistor increases slightly with V_{ds} .

This is caused by channel length modulation, in which higher V_{ds} increases the size of the depletion region around the drain and thus effectively shortens the channel.

There are several sources of leakage resulting in current flow in nominally OFF transistors.

Now observe in Fig 1b. that $V_{gs} < V_t$, the current drops off exponentially rather than abruptly becoming zero. This is called subthreshold condition.

The threshold voltage itself is influenced by the voltage difference between the source and drain body, this is called the body effect.

The source and drain diffusions are reversed-biased diodes and also experiences junction leakage into the substrate or well.

The current into the gate I_g is ideally 0. However, as the thickness of gate oxides reduces to only a small number of atomic layers, electrons tunnel through the gate, causing some gate current.

Both mobility and threshold voltage decrease with rising temperature. The mobility effect is most important for ON transistors, resulting in lower I_{ds} at high temperature.

The threshold effect is most important for OFF transistors, resulting in higher leakage current at high temperature.

Clearly, MOS Characteristics degrade with temperature.

Learn all the effects underlined with yellow colour.

This is for Non-Ideal I-V Characteristics.

Type your text

Channel length Modulation

Describe Channel Length Modulation Effect.

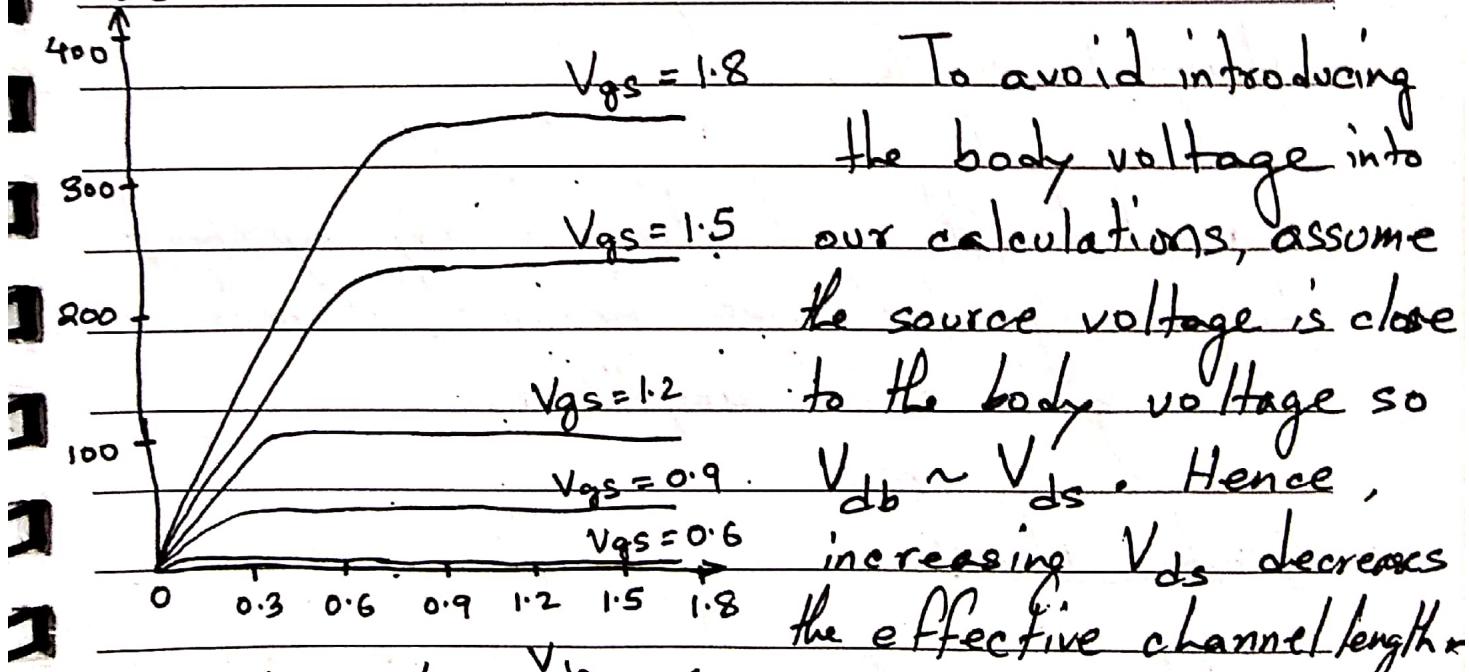
Ideally I_{ds} is independent of V_{ds} for a transistor in saturation, making the transistor a perfect current source.

The reverse-biased p-n junction between the drain and body forms a depletion region with a width L_d that increases with V_{db} .

The depletion region effectively shortens the channel length to

$$L_{eff} = L - L_d$$

I_{ds} (mA)



Shorter channel length results in higher current, thus I_{ds} increases with V_{ds} in saturation as shown in fig. This can be crudely modeled by multiplying the ideal current eq. by a factor of

$(1 + \lambda V_{ds})$. In the saturation region, we find

$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2} (1 + \lambda V_{ds})$$

The parameter λ is an empirical channel length modulation factor that should be confused with the same symbol used in layout design rules.

As channel length gets shorter, the effect of the channel length modulation becomes relatively more important. Hence λ is inversely dependent on channel length.

Channel length modulation is very important to analog designers because it reduces the gain of amplifiers.

Body effect **Describe Body Effect.**

Until now, we have considered a transistor to be a three-terminal device with gate, source and drain. However, the body is an implicit fourth terminal. The

potential difference between the source and body V_{sb} affects the threshold voltage. The threshold voltage can be modeled as,

$$V_t = V_{t_0} + \gamma (\sqrt{\phi_s} + V_{sb} - \sqrt{\phi_s})$$

where, V_{t_0} is the threshold voltage when the source is at the body potential,

ϕ_s is the surface potential at threshold,

γ is the body effect coefficient, typically in the range 0.4 to $1 V^{1/2}$.

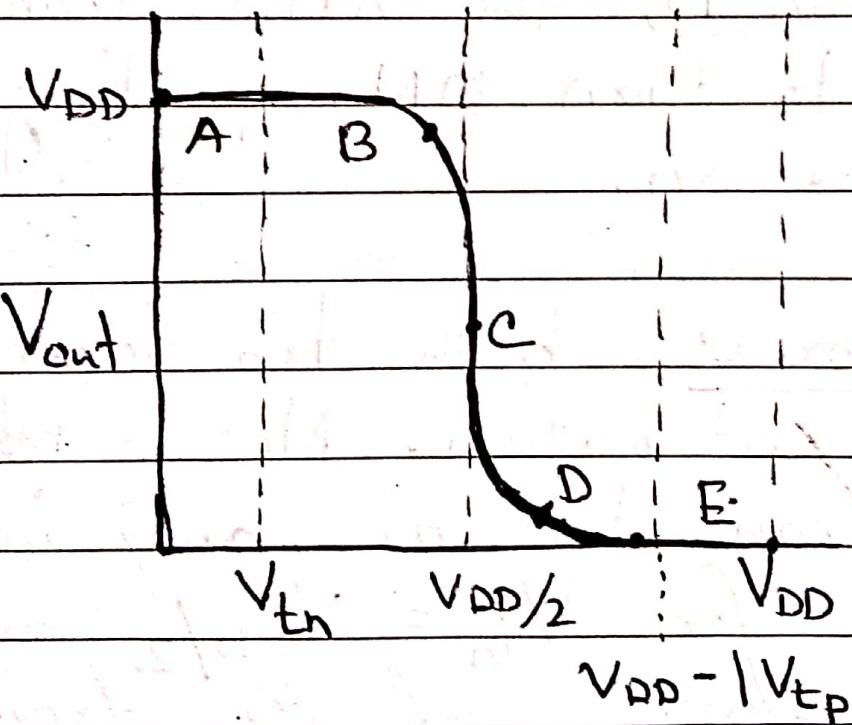
A body bias can intentionally be applied to alter the threshold voltage, permitting trade off between performance and subthreshold leakage current.

$$\phi_s = 2 V_T \ln \frac{N_A}{n_i}$$

$$\gamma = \frac{t_{ox}}{C_{ox}} \sqrt{2q_e E_s N_A} = \frac{\sqrt{2q_e E_s N_A}}{C_{ox}}$$

solve a problem.

Describe all the operating points or regions for PMOS and NMOS in CMOS Inverter.



The possible operating points of the inverter, marked with dots are the values of V_{out} where $I_{dsn} = |I_{dsp}|$ for a given value of V_{in} .

The operation of the CMOS inverter can be divided into five regions.

In region A, the nMOS transistor is OFF so the pMOS transistor pulls the output to V_{DD} .

In region B, the nMOS transistor starts to turn ON, pulling the output down.

In region C, both transistors are in saturation. Notice that ideal transistors are only in region C for $V_{in} = V_{DD}/2$ and that the slope of the transfer curve is negative (-ve) corresponding to infinite gain.

Real transistors have finite output resistances on account of channel length modulation and thus have finite slope over a broader region C.

In region D, the pMOS transistor is partially ON and in region E, it is completely OFF, leaving the nMOS transistor to pull the output down to ground.

Also notice that the inverter's current consumption is zero when the input is within a threshold voltage of the V_{DD} or GND rails. This feature is important for low-power operation.

Explain how Noise Margin is determined for a CMOS Inverter.

Noise Margin

Noise margin is closely related to DC voltage characteristics. It allows to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted.

Low noise margin $\rightarrow NM_L$

High noise margin $\rightarrow NM_H$

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Where,

V_{IH} = minimum High input voltage

V_{IL} = maximum Low input voltage

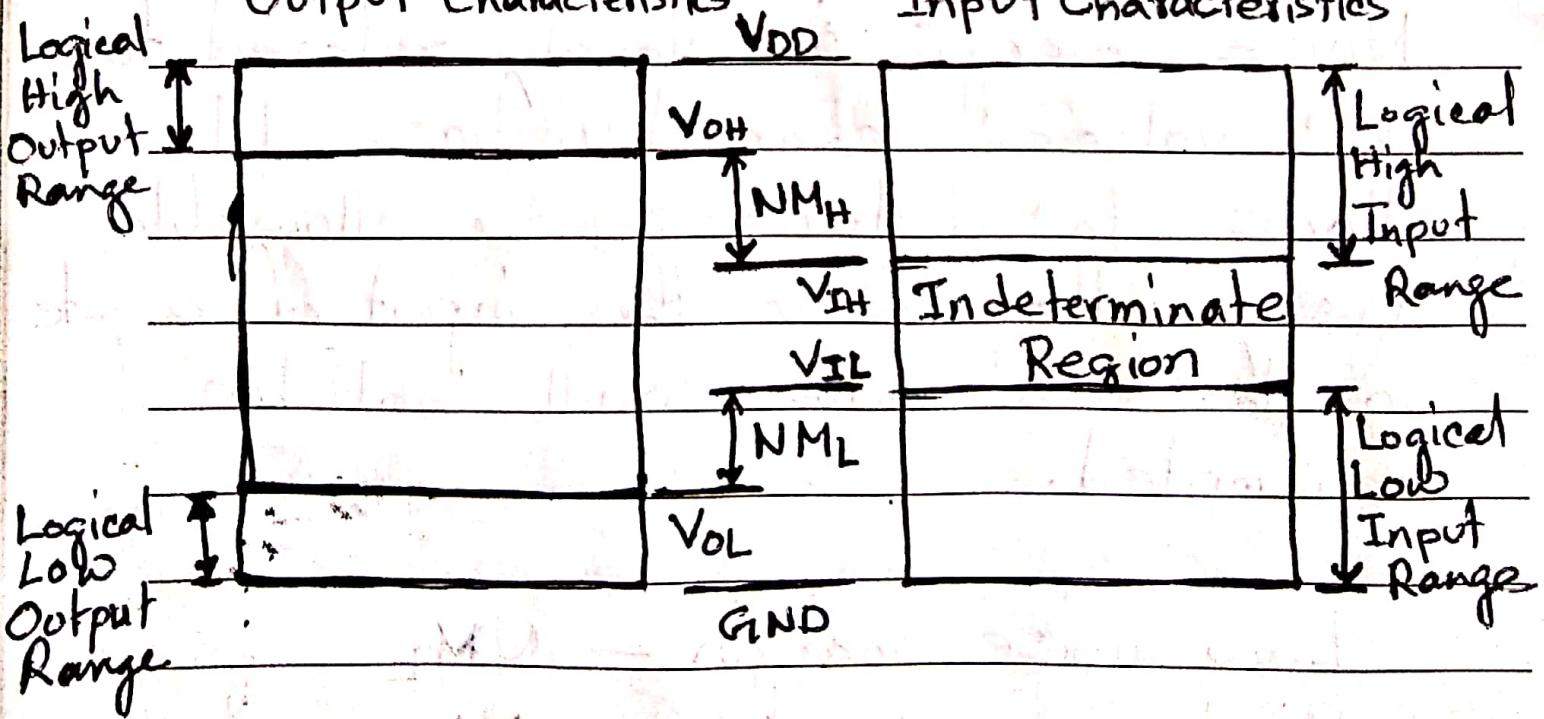
V_{OH} = minimum High output voltage

V_{OL} = maximum Low output voltage.



Output Characteristics

Input Characteristics



Inputs between V_{IL} and V_{IH} are said to be in the indeterminate region or forbidden zone and do not represent legal digital logic levels.

Therefore, it is generally desirable to have V_{IH} as close as possible to V_{IL} and for this value to be midway in the "Logic swing", V_{OL} to V_{OH} .

This implies that the transfer characteristics should switch abruptly, that is, there should be high gain in the transition region.

For the purpose of calculating noise margins, the transfer characteristic of the inverter and the definition of voltage levels V_{IL} , V_{OL} , V_{IH} , V_{OH} are shown in Figure.

Logic levels are defined at the unity gain point where the slope is -1.

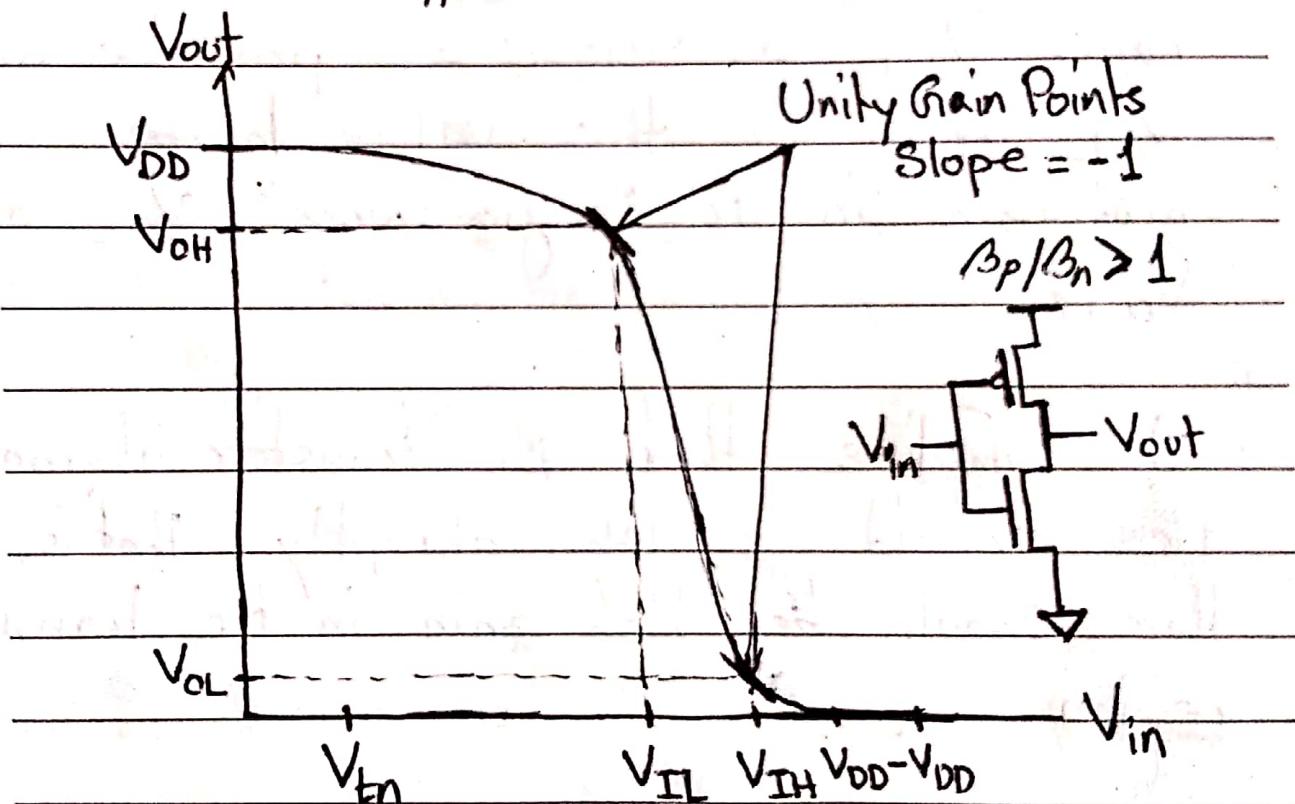
This gives a conservative bound on the

worst-case static noise margin.

For H inverter,

NM_L is $0.46 V_{DD}$ while

NM_H is $0.34 V_{DD}$



Note that output is slightly degraded when the input is at its worst legal value, this is called noise feedthrough or propagated noise.

Note that if $|V_{tp}| = V_{tn}$, then ~~NM_H and NM_L~~ increase as threshold voltages are increased. If either

NM_L or NM_H for a gate are too small (e.g. below about $0.1 V_{DD}$), then gate may be disturbed by noise that occurs on the inputs.

Explain how Beta Ratio Effects is used to change the switching threshold voltage.

Beta Ratio Effects

We have seen that for $\beta_p = \beta_n$, the inverter threshold voltage V_{inv} is $V_{DD}/2$. This may be possible desirable because it maximizes noise margins and allows a capacitive load to charge and discharge in equal times by providing equal current

source and sink capabilities.

Inverters with different beta ratio B_p/B_n are called skewed inverters.

If $B_p/B_n > 1$, the inverter is HI-skewed.

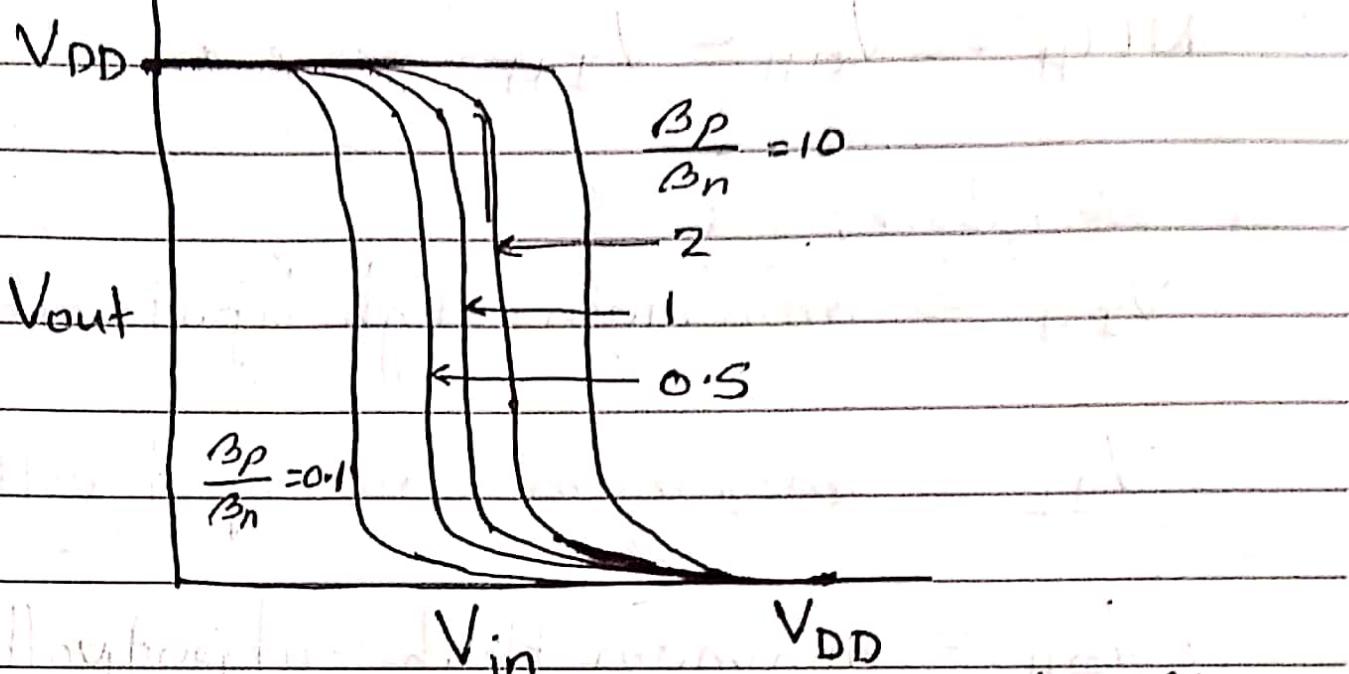
If $B_p/B_n < 1$, the inverter is LO-skewed.

If $B_p/B_n = 1$, the inverter has normal skew or is unskewed.

A HI-skew inverter has a stronger pMOS transistor.

∴ If input is $V_{DD}/2$, then we obtain output higher than $V_{DD}/2$.

Similarly, LO-skew inverter has a weaker pMOS transistor and thus a lower switching threshold.



As beta ratio is changed the switching threshold moves, but the output voltage remains sharp.