PRIMEASIA UNIVERSITY

Lab Assignment

CSE -403

VLSI Design

Submitted To

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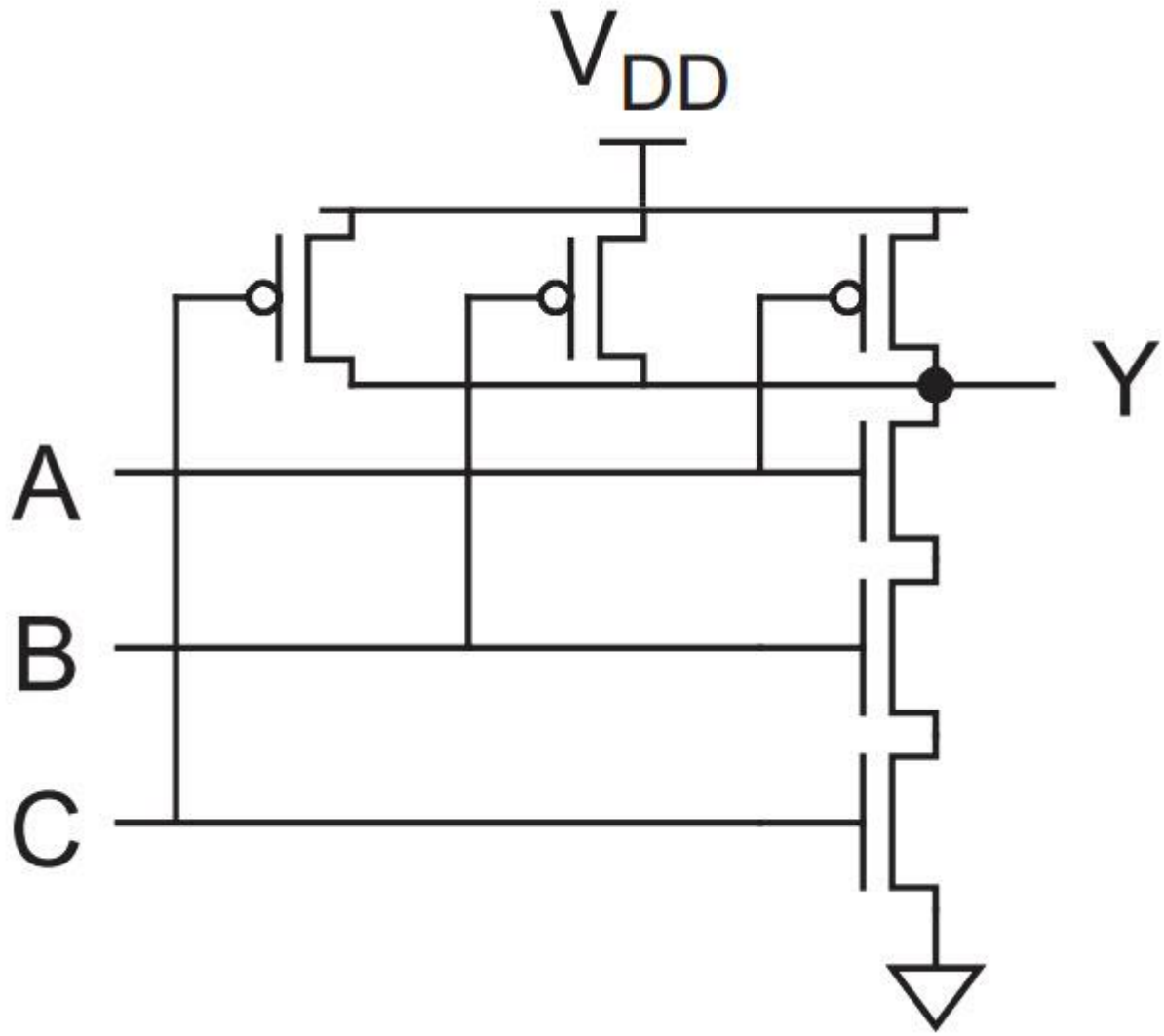
Experiment Name: Design a 3 input CMOS NAND Gate

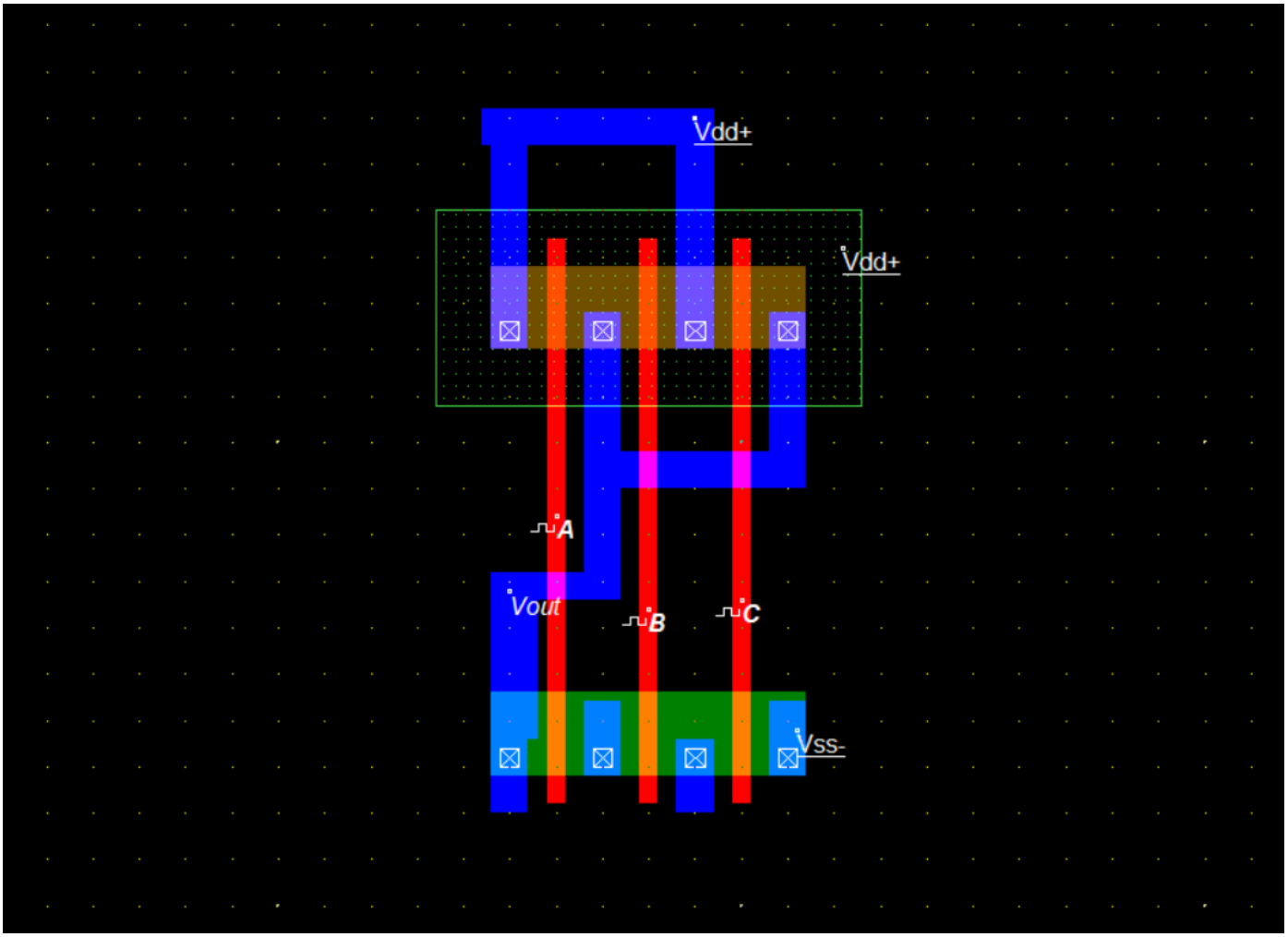
Truth Table:

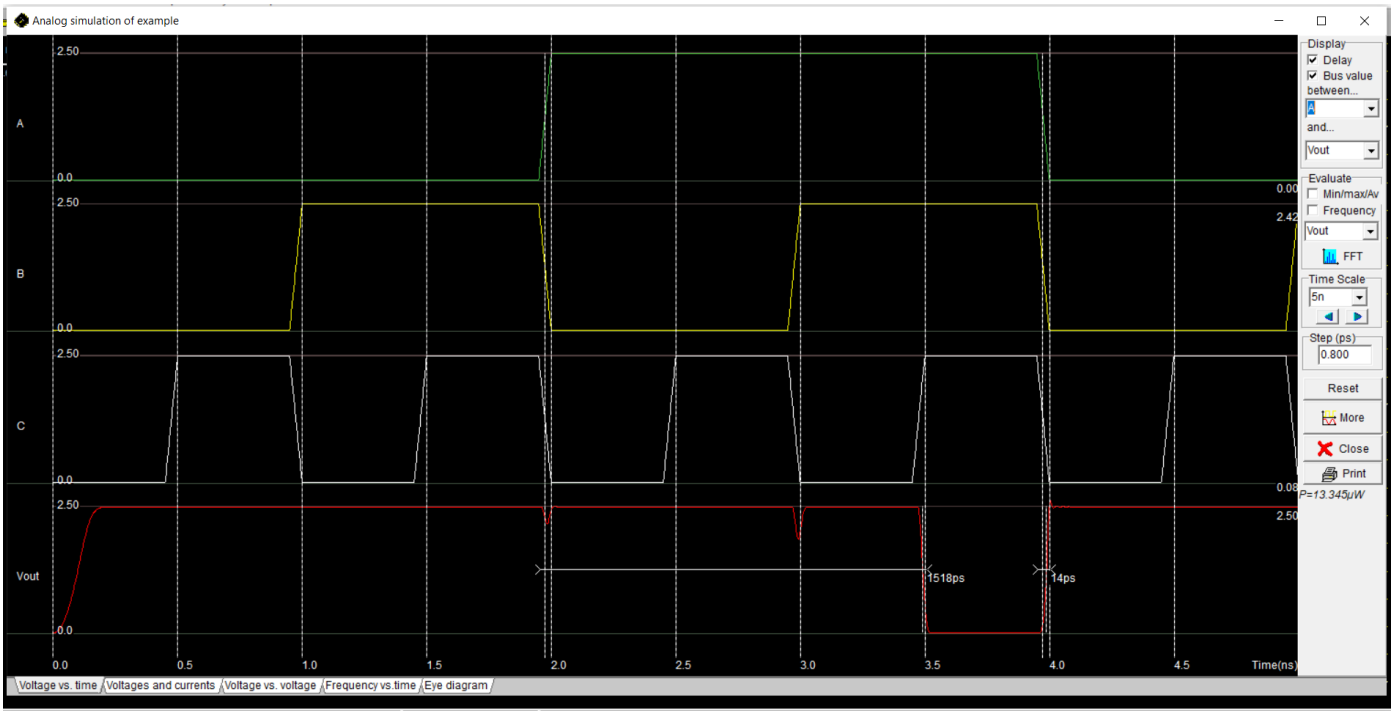
input			Output
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Diagram:



MICROWIND:


Vdd+
Vdd+
A
Vout
B
C
Vss-


Analog simulation of example
A
B
C
Vout
2.50
0.0
1518ps
14ps
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)
Display
Delay
Bus value between...
and...
Vout
Evaluate
Min/max/Av
Frequency
FFT
Time Scale
5n
Step (ps)
0.800
Reset
More
Close
Print
P=13.345µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram