I2C Real Time Clock /Calendar Chip

Features

ÿCan time seconds, minutes, hours based on 32.768kHz crystal,
Week, day, month and year

ÿWith century logo

ÿWide operating voltage range: 1.2ÿ5.5V **ÿI2C**
bus slave address: read, 0A3H; write, 0A2H **ÿProgrammable**
clock output frequency: 32.768kHz ,
1024Hz, 32Hz, 1Hz

ÿ Alarm and timer ÿ
Brownout detector ÿ
Internal integrated oscillator
capacitor ÿ Open drain interrupt
pin ÿ SOP and MSOP packages

application

ÿ Portable media players ÿ
Mobile phones ÿ
Multi-rate electricity meters, IC card water meters, IC card gas meters

ÿ Fax machine
ÿ Security electronics

Overview

LK8563 is a low power CMOS real-time clock/calendar chip, which provides a programmable clock output, an interrupt output and a power-off detector, all addresses and data are transmitted serially through the IIC bus interface. The maximum bus speed is 400Kbits/s, and the embedded word address register will automatically increment after each read and write data.

Typical application circuit application

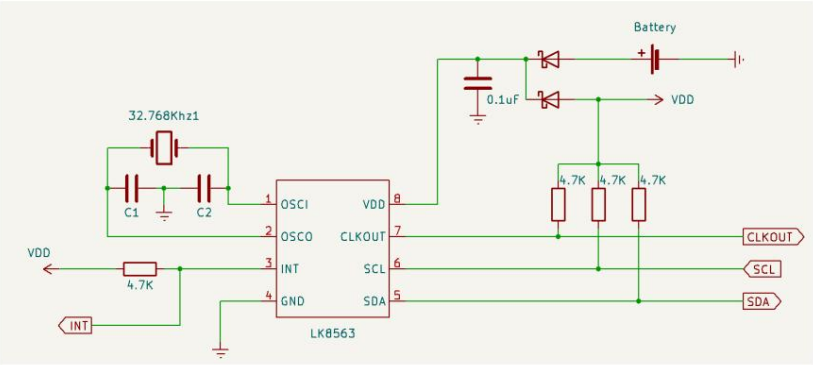


Figure 1 Typical application circuit diagram

Note: In the typical application circuit, the crystal oscillator load capacitors C1 and C2 can be selected to be around 20pF. The actual value of the capacitor can be fine-tuned to obtain the best clock accuracy.

Block Diagram and Pin Functions

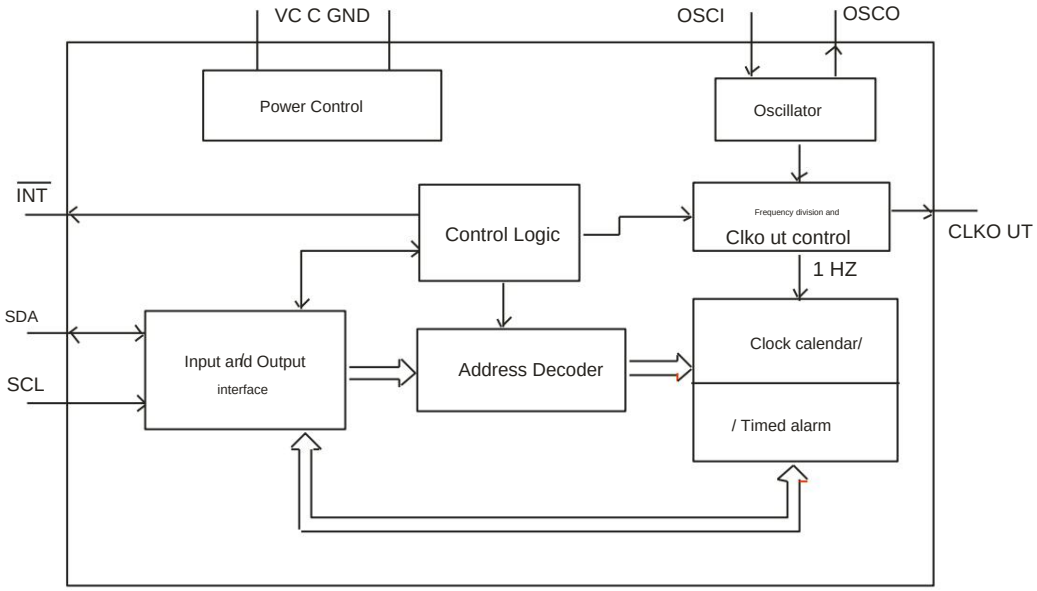


Figure 2. Block diagram

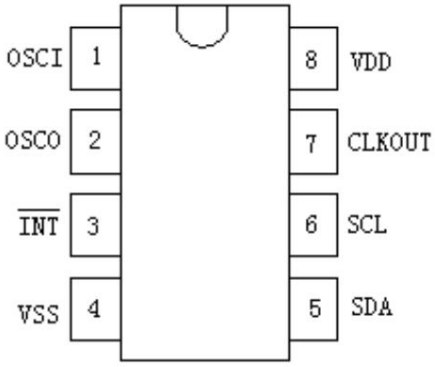


Figure 3. Pin diagram

Pin Description

Pin number	symbol	Functional Description	Pin number	symbol	Functional Description
1	OSCI	Oscillator Input	5	SDA	Serial Data I/O
2	OSCO	Oscillator Output	6	SCL	serial clock input
3	/INT	Interrupt output (open drain)	7	CLKOUT	Clock output (open drain)
4	VSS	Ground	8	VDD	positive power supply

Maximum Ratings

.

parameter	symbol	Minimum	Maximum	unit
Supply voltage	VDD	-0.5	+6.5	V
Supply Current	IDD	-50	+50	mA
SCL and SDA pin input voltage	VI	-0.5	+6.5	V
OSCI pin input voltage		-0.5	VDDÿ0.5	V
CLKOUT and INT pin output voltage	VO	-0.5	+6.5	V
DC input current of all input ports	II	-10	+10	mA
DC output current of all output ports	IO	-10	+10	mA
Total power loss	P	—	300	mW
Operating temperature	TA	-40	+85	ÿ
Storage temperature	TS	-65	+150	ÿ

Electrical characteristics parameters

DC characteristics (unless otherwise specified, VDD=1.2ÿ5.5V, VSS=0V; TA=-40ÿ+85ÿ; fosc=32.768kHz;

Quartz crystal Rs = 40kÿ, CL = 12.5pF)

parameter	symbol	Test conditions	Min	Typ	Max	Unit
power supply						
Operating voltage	VDD	I^2C bus valid, f=400kHz[1]	1.8	-	5.5	V
Provides reliable clock/calendar data The working voltage at		TA=25ÿ	1.2	-	5.5	V
Working current 1 CLKOUT is valid (FE=1)	IDD1	fSCL=400kHz	-	-	800	µA
		fSCL=100kHz	-	-	200	µA
Working current 2 CLKOUT Disable	IDD2	fSCL=0Hz,TA= 25ÿ[2]				
		VDD=3.0V	-	2	6	µA
Working current 3 CLKOUT=32.768kHz	IDD3	fSCL=0Hz,TA= 25ÿ[2]				
		VDD=3.0V	-	2.5	6	µA
Input						
Low level input voltage	VIL		VSS	-	0.3VDD	V
High level input voltage	VIH		0.7VDD	-	VDD	V
Input leakage current	ILI	VI = VDD or VSS	-1	0	+1	µA
Input Capacitance	CI	[3]	-	-	7	pF
Output						
SDA low level output current	IOLS	VOL=0.4VÿVDD=5.0V	-3	-	-	mA
$\overline{INT}$ Low level output current	IOLI	VOL=0.4VÿVDD=5.0V	-1	-	-	mA
CLKOUT low level output current	IOLC	VOL=0.4VÿVDD=5.0V	-1	-	-	mA
CLKOUT high level output current	IOHC	VOL=4.6V, VDD=5.0V	1	-	-	mA
Output leakage	ILO	VO = VDD or VSS	-1	0	+1	µA
current voltage						
detector brownout detection voltage	VLOW	TA = 25ÿ	-	1.0	-	V

1. The oscillator starts reliably when power is applied: VDD (minimum value, when power is applied) = VDD (minimum value) + 0.3V

2. Timer source clock = 1/60Hz; SCL and SDA are both VDD

3. Test on sample basis

AC characteristics (if not otherwise specified, VDD = 1.2 ~ 5.5V, VSS = 0V; TA = -40 ~ + 85 ÿ; fosc = 32.768kHz; quartz Crystal Rs = 40kÿ, CL = 12.5pF)

parameter	symbol	Test conditions	Min	Typ	Max	Unit
Oscillator						
Precision load capacitance	CINT		15	25	35	pF
Oscillator Stability	ÿ fOSC/fOSC	ÿ VDD=200mV,TA=25ÿ	-	2×10-7	-	-
Quartz crystal parameters (f=32.768kHz)						
Series resistance	RS		-	-	40	kÿ
Parallel load capacitance	CL		-	12.5	-	pF
CLKOUT Output						
CLKOUT duty cycle	ÿ CLKOUT	[1]	-	50	-	%
I2C bus timing characteristics[2] [3]						
SCL clock period	f	[4]	-	-	400	kHz
Starting condition holding time	tDSTA		0.6	-	-	µs
Repeated start condition build-up time	SUSTA		0.6	-	-	µs
SCL low time	tLOW		1.3	-	-	µs
SCL high time	tHIGH		0.6	-	-	µs
SCL and SDA rising edge time	tr		-	-	0.3	µs
Falling edge time of SCL and SDA	tf		-	-	0.3	µs
Bus load	Cb		-	-	400	pF
capacitance Data	tSUDAT		100	-	-	ns
setup time Data hold time	tHDDAT		0	-	-	ns
Stop condition setup time	tSUSTO		0.6	-	-	µs
Acceptable bus spike width	tW		-	-	50	ns

1. No special instructions fCLKOUT = 32.768kHz

2. All timing values are valid within the operating voltage range (under TA conditions), and the change between the reference input voltage VSS and VDD is the value of VIL and VIH

3. The access time of the I2C bus under two start and one stop conditions must be less than 1s

I2C bus timing waveform

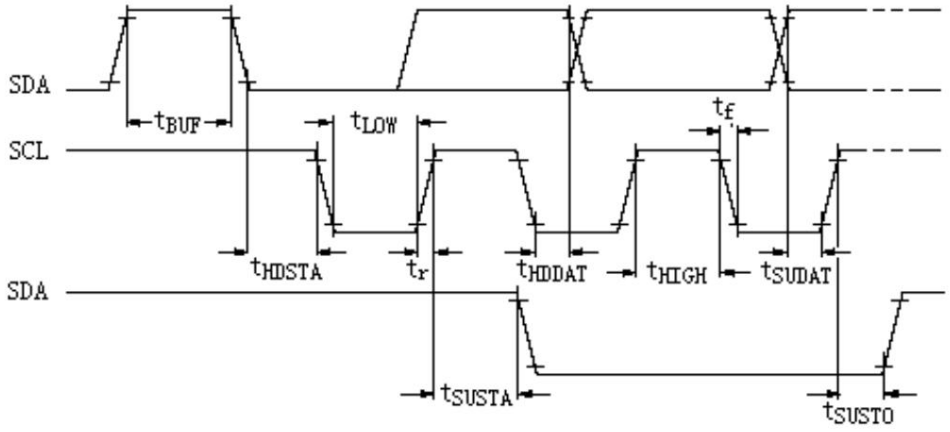
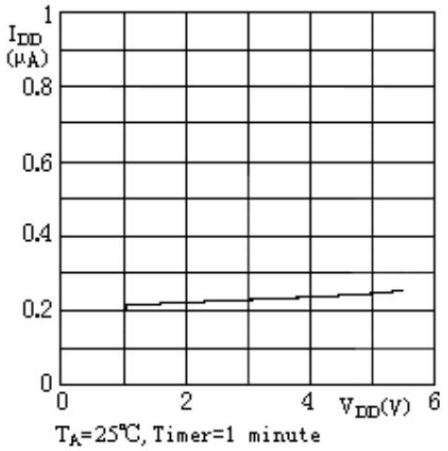
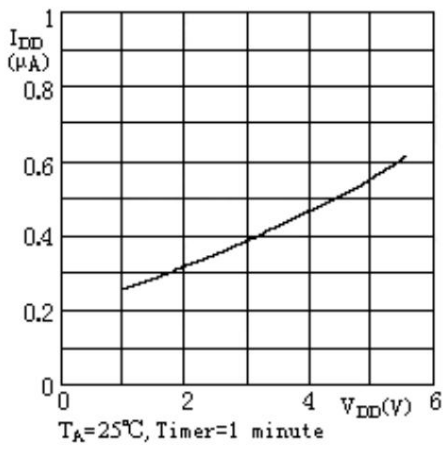


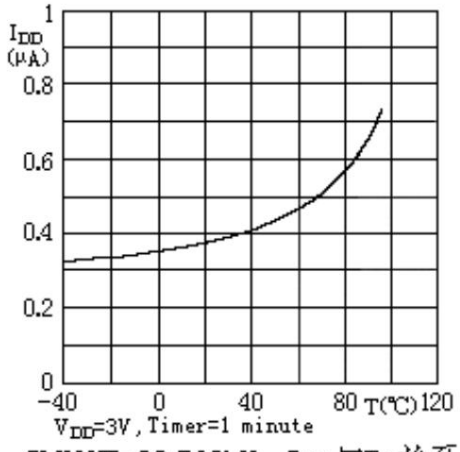
Figure 4 I2C bus timing waveform



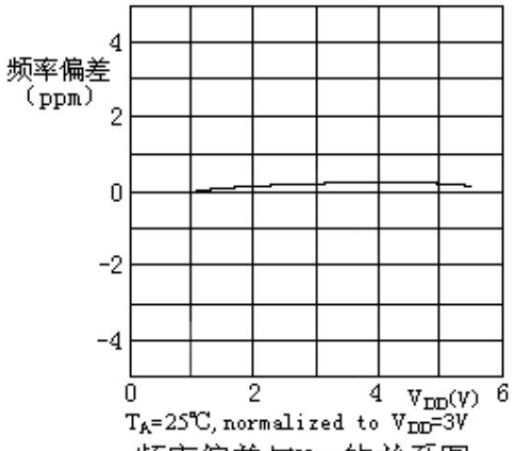
CLKOUT禁止时,IDD与VDD的关系图-



CLKOUT=32.768kHz,IDD与VDD的关系图



CLKOUT=32.768kHz,IDD与TA关系图



频率偏差与VDD的关系图

Functional Description

The LK8563 has 16 8-bit registers, an auto-increment address register, a built-in 32.768kHz oscillator (with

an internal integrated capacitor), a frequency divider (used to provide the clock source for the real-time clock RTC), a programmable clock output, a fixed

The device has a timer, an alarm, a brownout detector and a 400kHz I2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers, but not all bits are used. The first two registers (internal address

00H, 01H) are used as control registers and status registers, addresses 02H to 08H are used for clock counters (second to year counters), addresses 09H to

0CH is used for the alarm register (to define the alarm condition), address 0DH is used to control the output frequency of the CLKOUT pin, and addresses 0EH and 0FH

Used as timer control register and timer register respectively. Seconds, minutes, hours, day, month, year, minute alarm, hour alarm, daily report

The coding format of the alarm register is BCD code, and the week and week alarm registers are not coded in BCD format.

Alarm function mode

When one or more alarm register MSBs (AE = Alarm Enable bit) are cleared to 0, the corresponding alarm conditions are valid.

An alarm will be generated once every minute to once every week. Set the alarm flag bit AF (bit 3 of control/status register 2) to generate an alarm.

An interrupt occurs and AF can only be cleared by software.

Timer

The 8-bit down counter (address 0FH) is controlled by the timer control register (address 0EH, see Table 22).

Used to set the frequency of the timer (4096Hz, 64Hz, 1Hz or 1/60Hz), and to set the timer to be valid or invalid.

The 8-bit binary number set by the device counts down. At the end of each countdown, the timer sets the flag bit TF (see Table 4). TF is used to generate a

Interrupt ($\overline{INT}$). Each countdown cycle generates a pulse as an interrupt signal, and the timer flag TF can only be cleared by software.

See Table 4) to control the conditions for interrupt generation. When the timer is read, the current countdown value is returned.

CLKOUT Output

The CLKOUT pin can output a programmable square wave. The CLKOUT frequency register (address 0DH, see Table 20) determines the output square wave.

The frequency can output 32.768kHz (default), 1024Hz, 32Hz and 1Hz square waves. CLKOUT is an open-drain output transistor.

Pin, valid when powered on, high impedance when invalid.

Reset

LK8563 has a built-in reset circuit. When the oscillator stops working, the reset circuit starts working. In the reset state, the I2C bus is initialized .

Initialization, all registers (including address pointer) will be initialized except TF, VL, TD1, TD0, TESTC, AE bits are set to logic 1.

Cleared.

Brownout detection and clock monitoring

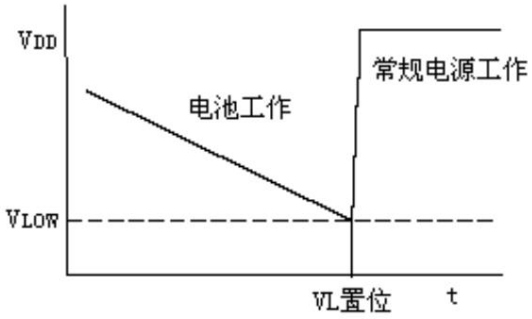


图8. 掉电检测

LK8563 has a built-in power-off detection circuit. When VDD is lower than VLOW, bit VL (Voltage Low, bit 7 of the seconds register) is set.

=1 indicates that inaccurate clock/calendar information may be generated. The VL flag can only be cleared by software .

battery power) to VLOW , VL will be asserted, indicating that an interrupt may occur at this time.

Register structure

Table 1. Register Overview

address	Register Name	Bit7	Bit6	Bit5		Bit4	Bit3	Bit2	Bit1	Bit0	
00H	Control/Status Register 1	TEST	0	STOP		0	TESTC	0	0	0	
01H	Control/Status Register 2	0	0	0		TI/TP	AF	TF	AIE	TIE	
0D	CLKOUT Frequency Register	FE	—	—	—			—FD1		FD0	
0EH	Timer control register	TE	—	—	—	—		— TD1		TD0	
0FH	Timer countdown register	Timer countdown value									

Bits marked with “—” are invalid, and bits marked with “0” should be set to logic 0.

Table 2. BCD format register overview

address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2		Bit1	Bit0	
02H	Second	V L	00ÿ59BCD code format number								
03H	minute	—	00ÿ59BCD code format number								
04H	Hour	--		00ÿ23BCD code format number							
05H	day	--		01ÿ31BCD code format number							
06H	Week	-----						0ÿ6			
07H	Month/Century	C	—	—		01ÿ12BCD code format number					
08H	Year	00ÿ99BCD code format number									
09H	Minute alarm	AE	00ÿ59BCD code format number								
0AH	Hour alarm	AE	—		00ÿ23BCD code format number						
0BH	Daily alarm	AE	—		01ÿ31BCD code format number						
0CH	Weekly alarm	AE	—	—	—			0ÿ6			

The position marked with "—" is invalid.

Control/Status Register **1**

Table 3. Control/Status Register 1 (Address 00H) Bit Description

Tag symbol		describe
7	TEST1	TEST1=0: Normal mode TEST1=1: EXT_CLK test mode
5	STOP	STOP=0: RTC clock is running; STOP=1: All RTC dividers are asynchronously set to logic 0, and the RTC clock stops running (CLKOUT is still available at 32.768kHz)
3	TESTC	TESTC=0: Power reset function disabled (set to logic 0 in normal mode) TESTC=1: Power reset function is valid
6,4,2ÿ0		The default value is logic 0.

Control/Status Register **2**

Bits TF and AF: When an alarm occurs, AF is set to logic 1. Similarly, at the end of the timer countdown, TF is set to logic 1.

The value of these two bits can only be modified by software. If both the timer and alarm interrupt are required in the application, you can read these two bits.

Two bytes are used to determine the interrupt source. To prevent rewriting of the flag bit when clearing the bit during a write cycle, a logical AND operation is performed.

Bits TIE and AIE: These two bits are used to activate the generation of interrupts. When AIE and TIE are set, the interrupt is the logical OR of these two bits.

Table 4. Bit description of control/status register 2 (address 01H)

Tag symbol		describe
7,6,5		The default value is logic 0.
4	TI/TP	TI/TP=0: When TF is valid, INT is valid (depending on the state of TIE) TI/TP=1: INT, pulse valid, see Table 5 (depends on the state of TIE) Note: If AF and AIE are both valid, INT is always valid.
3	AF	AF=0: During read operation, the alarm flag is invalid; during write operation, the alarm flag is cleared AF=1: During read operation, the alarm flag is valid; during write operation, the alarm flag remains unchanged
2	TF	TF=0: When reading, the timer flag is invalid; when writing, the timer flag is cleared TF=1: When reading, the timer flag is valid; when writing, the timer flag remains unchanged
1	AIE	AIE=0: Alarm interrupt is disabled AIE=1: Alarm interrupt is enabled
0	TIE	TIE=0: Timer interrupt is disabled TIE=1: Timer interrupt is enabled

Table 5. $\overline{INT}$ Operation (bit TI/TP = 1)

Clock source (Hz)	~INT cycle [1]	
	n=1[2]	n >1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1], TF and simultaneously $\overline{INT}$ effective

[2] n is the value of the countdown timer. When n=0, the timer stops working.

Seconds, minutes, and hours registers

Table 6. Seconds/VL register (address 02H) bit description

Tag symbol		describe
6ÿ0		(seconds) represents the current second value in BCD format, ranging from 00 to 99, for example: 1011001 represents 59 seconds
7	V L	VL=0: Ensure accurate clock/calendar data VL=1: Accurate clock/calendar data is not guaranteed

Table 7. Minute register (address 03H) bit description

Position No.		describe
7	Symbol —	Invalid
6ÿ0		(Minutes) Represents the current minute value in BCD format, ranging from 00 to 59

Table 8. Hour register (address 04H) bit description

Position No.	symbol	describe
7,6	—	Invalid
5ÿ0		(Hour) Represents the current hour value in BCD format, ranging from 00 to 23

Day, weekday, month/century, and year registers

Table 9. Day register (address 05H) bit description

Position No.	symbol	describe
7,6	—	Invalid
5ÿ0	(day)	Represents the current day value in BCD format, ranging from 01 to 31. If the current year counter value is a leap year, TS8563 Automatically add a value to February to make it 29 days

Table 10. Week register (address 06H) bit description

Tag Symbol - Invalid		describe
7ÿ3		
2ÿ0		(Week) Represents the current week value, ranging from 0 to 6. See Table 11. These bits can also be reallocated by the user.

Table 11. Weekly distribution table

day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 12. Month/Century Register (Address 07H) Bit Description

Position No.	Symbol	Description
7	C	Century digit: C=0 specifies the century as 20XX; C=1 specifies the century as 19XX, "XX" is the year register The value in the device is shown in Table 14. When the year changes from 99 to 00, the century will change.
6,5	—	Invalid
4ÿ0		(Month) represents the current month value in BCD format, ranging from 01 to 12, see Table 13

Table 13. Monthly distribution table

month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 14. Year register (address 08H) bit description

Position No.		describe
7ÿ0	Symbol (year)	represents the current year value in BCD format, ranging from 00 to 99

Alarm Control Register

When one or more alarm registers are written with legal minute, hour, day or week values and their corresponding AE (Alarm Enable)

If the bit is logic 0 and these values are equal to the current minute, hour, day or week value, the flag AF (Alarm Flag) is set.

AF saves the setting value until it is cleared by software. After AF is cleared, it can be set again only when the time increment matches the alarm condition again.

Alarm registers are ignored when their corresponding bit AE is set to logic 1.

Table 15. Minute alarm register (address 09H) bit description

Position No.	symbol	describe
7	AE	AE=0, minute alarm is valid; AE=1, minute alarm is invalid
6ÿ0	Minute alarm	represents the minute alarm value in BCD format, the value is 00ÿ59

Table 16. Hour alarm register (address 0AH) bit description

Position No.	symbol	describe
7	AE	AE=0, hour alarm is valid; AE=1, hour alarm is invalid
5ÿ0	hour alarm	represents the hour alarm value in BCD format, the value is 00ÿ23

Table 17. Daily alarm register (address 0BH) bit description

Position No.	symbol	describe
7	AE	AE=0, daily alarm is valid; AE=1, daily alarm is invalid
5ÿ0	Daily alarm	represents the daily alarm value in BCD format, the value is 01 to 31

Table 18. Week alarm register (address 0CH) bit description

Position No.	symbol	describe
7	AE	AE=0, the day of the week alarm is valid; AE=1, the day of the week alarm is invalid
2ÿ0	Week alarm	represents the week alarm value in BCD format, the value is 0ÿ6

CLKOUT Frequency Register

Table 19. CLKOUT frequency register (address 0DH) bit description

Position No.	symbol	describe
7	FE	FE=0: CLKOUT output is disabled and set to high impedance FE=1: CLKOUT output is valid
6ÿ2	— Invalid	
1	FD1 is used to control the frequency output pin of CLKOUT (fCLKOUT), see Table 20	
0	FD0 is used to control the frequency output pin of CLKOUT (fCLKOUT), see Table 20	

Table 20. CLKOUT frequency selection table

FD1	FD0	fCLKOUT
0	0	32.768kHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

Countdown Timer Register

The timer register is an 8-bit countdown timer. It is enabled or disabled by the bit TE in the timer controller.

The clock of the timer can also be selected by the timer controller. Other timer functions, such as interrupt generation, are controlled by the control/status register 2.

To read back the countdown value accurately, the frequency of the I2C bus clock SCL should be at least twice the selected timer clock frequency.

Table 21. Timer control register (address 0EH) bit description

Position No.	symbol	describe
7	TE	TE=0: timer is invalid; TE=1: timer is valid
6ÿ2	—	Useless
1	TD1	Timer clock frequency selection bit, determines the clock frequency of the countdown timer, see Table 22, TD1 is not used
0		and TD0 should be set to "11" (1/60Hz) to reduce power consumption

Table 22. Timer clock frequency selection

TD1	TD0	Timer clock frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	1/60

Table 23. Timer countdown value register (address 0FH) bit description

Position No.	symbol	describe
7ÿ0	Timer countdown value	countdown value "n", countdown period = n/clock frequency

EXT_CLK Test Mode

The test mode is used for online testing, establishing test mode and controlling the operation of the RTC.

The test mode is set by bit TEST1 in the control/status register 1. The CLKOUT pin then becomes an input pin.

In this case, the frequency signal input through the CLKOUT pin replaces the 64Hz frequency signal inside the chip, and every 64 rising edges will generate a 1 second time increment.

quantity.

Note: When entering EXT_CLK test mode, the clock is not synchronized with the internal 64Hz clock, and the pre-scaling status cannot be determined.

Operation examples

1. Enter EXT_CLK test mode and set bit 7 of control/status register 1 (TEST=1).

2. Set bit 5 of control/status register 1 (STOP = 1).

3. Clear bit 5 of control/status register 1 (STOP = 0).

4. Set the time registers (seconds, minutes, hours, day, weekday, month/century, and year) to the desired values.

5. Provide 32 clock pulses to CLKOUT.

6. Read the time register to observe the first change.

7. Provide 64 clock pulses to CLKOUT.

8. Read the time register to observe the second change. Repeat steps 7 and 8 when additional increments of the time register are required.

Power-On-Reset (POR) Failure Mode

The duration of the POR is directly related to the oscillator start-up time. A built-in long start-up circuit can disable the POR, so

This mode setting requires the signal waveforms of the I2C bus pins SDA and SCL to be as shown in Figure 9.

The time value is the minimum required.

When entering the failure mode, the chip immediately stops resetting and enters the EXT_CLK test mode through the I2C bus.

Logic 0 can eliminate the failure mode. To enter the failure mode again, set TESTC to logic 1.

A logic 0 has no meaning unless one wants to prevent entry into POR Failure Mode.

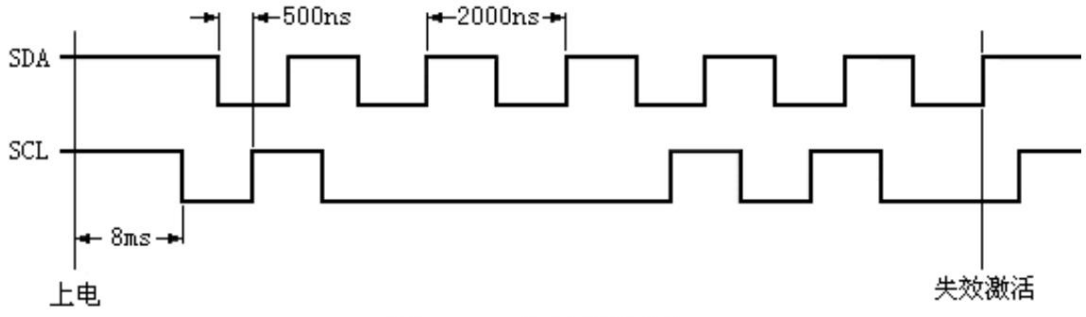


图9. POR失效时序图

Serial Interface

LK8563 uses the serial I2C bus interface.

IIC bus characteristics

The I2C bus transmits information between different chips and modules through two lines, SDA and SCL. SDA is the serial data line and SCL is the serial

Clock line, both lines must be connected to the positive power supply with a pull-up resistor. Data can only be transmitted when the bus is not busy.

See Figure 10 for the system configuration. The device that generates information is the transmitter, the device that receives information is the receiver, and the device that controls information is the master.

The device being controlled is the slave device.

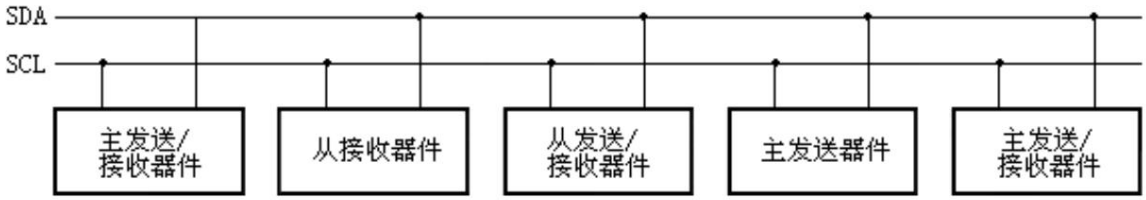


图10. I2C总线系统配置图

Start (START) and stop (STOP) conditions

When the bus is not busy, the data line and the clock line remain at a high level. When the data line is at a falling edge and the clock line is at a high level, it is the start condition (S).

When the data line is at the rising edge and the clock line is at a high level, it is the stop condition (P) (see Figure 11).

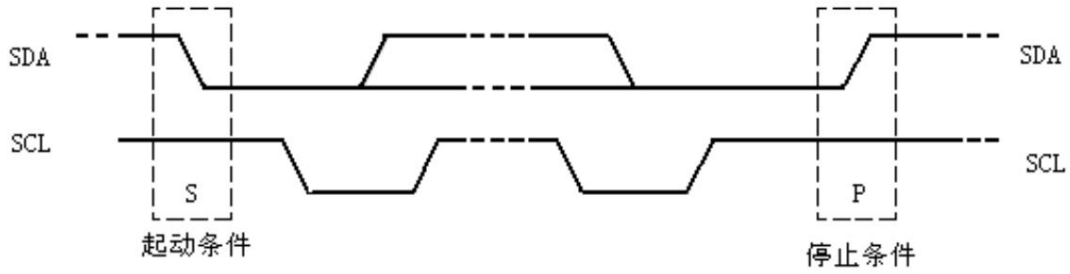


图11：I2C总线的起动（START）和停止（STOP）条件定义

Bit transfer

Each clock pulse transmits one data bit. The data on the SDA line should remain stable when the clock pulse is high. Otherwise, the data on the SDA line

The data will become the control signal mentioned above, see Figure 12.

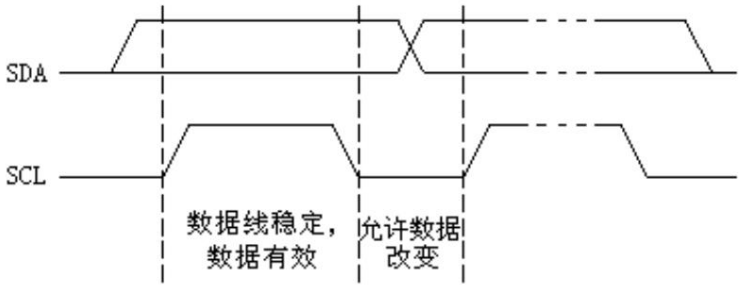


图12. I2C总线上的位传送

Acknowledge bit

There is no limit to the amount of data that the transmitter can send to the receiver between the start and stop conditions. Each 8-bit byte is followed by an acknowledge flag.

The master device generates an additional acknowledgement clock pulse. The slave receiver must generate an acknowledgement after each byte is received.

The master receiver must also generate an acknowledge flag after receiving each byte sent by the slave transmitter.

At this time, the SDA line should be held low (the startup and hold times should be considered). The transmitter should release SDA after receiving the last byte from the slave.

This causes the receiver to generate an acknowledge flag, at which point the master device can generate a stop condition.

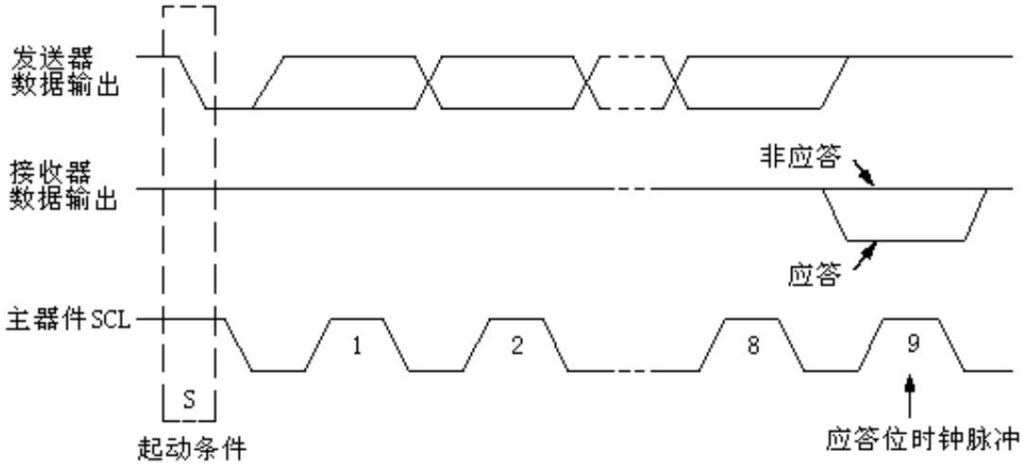


图13. I2C总线的应答位

I2C Bus Protocol

Note: Before using the I2C bus to transfer data, the receiving device should first indicate the address. After the I2C bus is started, this address is the same as the first transmission address.

Bytes are transmitted together. LK8563 can be used as a slave receiver or a slave transmitter. At this time, the clock signal line SCL can only be an input signal.

Line, data signal line SDA is a bidirectional signal line.

See Figure 14 for the slave address of LK8563.

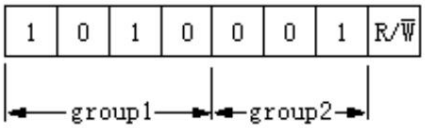


图14. 从地址

Clock/calendar read/write cycles

The LK8563 serial I2C bus read/write cycle has three configurations, see Figures 15, 16, and 17. The word address in the figure is a 4-bit number.

Used to indicate the next register to be accessed. The upper four bits of the word address are useless.

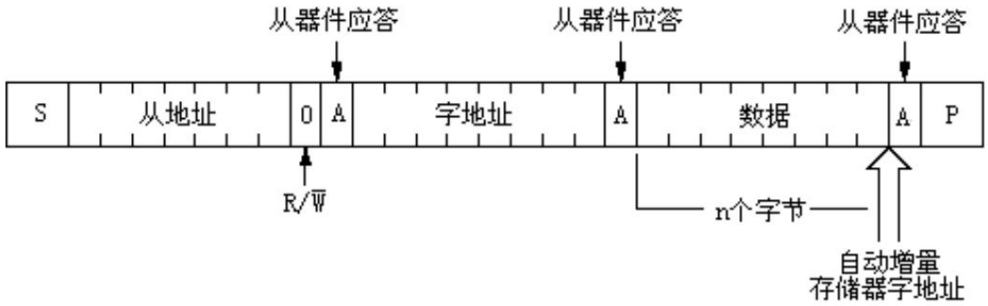


图15. 主发送器到从接收器（写模式）

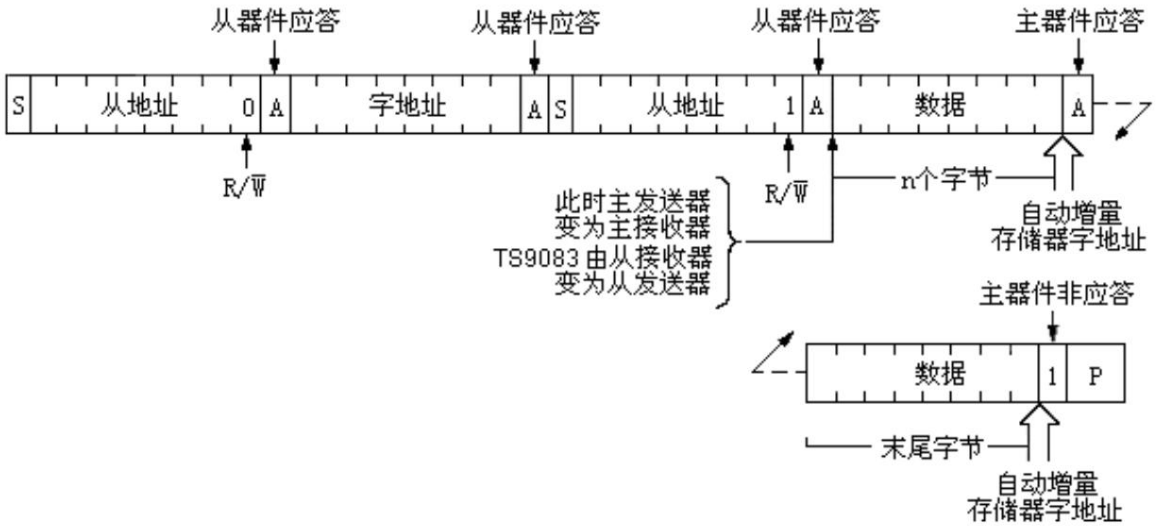


图16. 设置字地址后主器件读数据（写地址，读数据）

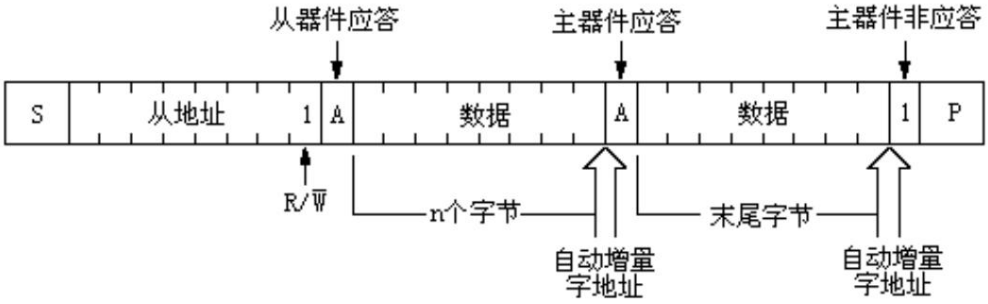


图17. 主器件读从器件第一个字节数据后的数据（读模式）

Quartz crystal frequency adjustment

Method 1: Fixed value OSCI capacitor - Calculate the average value of the required capacitance, use this value of fixed value capacitor, and connect it to the CLKOUT pin after power-on. The measured frequency should be 32.768kHz. The measured frequency value deviation depends on the quartz crystal, capacitance deviation and device deviation (average is ±5×10-6). The average deviation can be controlled within ±5 minutes/year.

Method 2: OSCI trimming capacitor - The oscillator frequency can be adjusted to a precise value by adjusting the trimming capacitor of the OSCI pin. The frequency value on the CLKOUT pin is 32.768kHz.

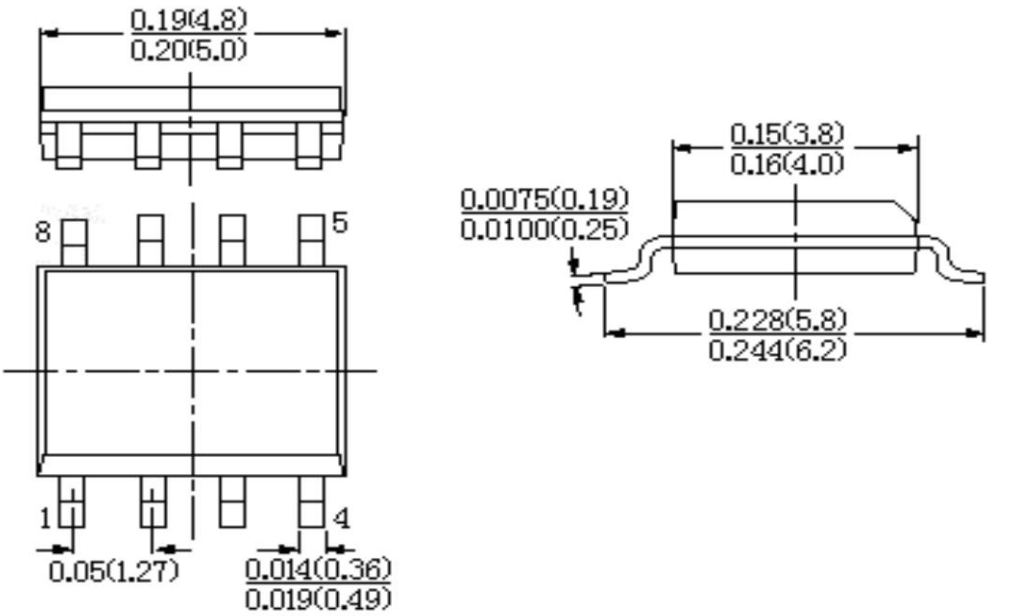
Method 3: OSCO Output - Measure the output of OSCO directly (taking into account the capacitance of the test probe).

Ordering Information

model	Temperature range	Package	MARK
LK8563S	-40ÿ+85ÿ	MSOP8	LK8563S
LK8563T		SOP8	LK8563T

Package size

SOP8 单位：inches（mm）



MSOP8 单位：inches（mm）