EGR226
Operating Systems & Networking

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Today's Objectives

- Syllabus
- Textbook
- Overview of a Computer System

Required Resources

- **Textbook:** Operating System Concepts, Silberschatz, Galvin and Gagne.

Hardware Top-Level View

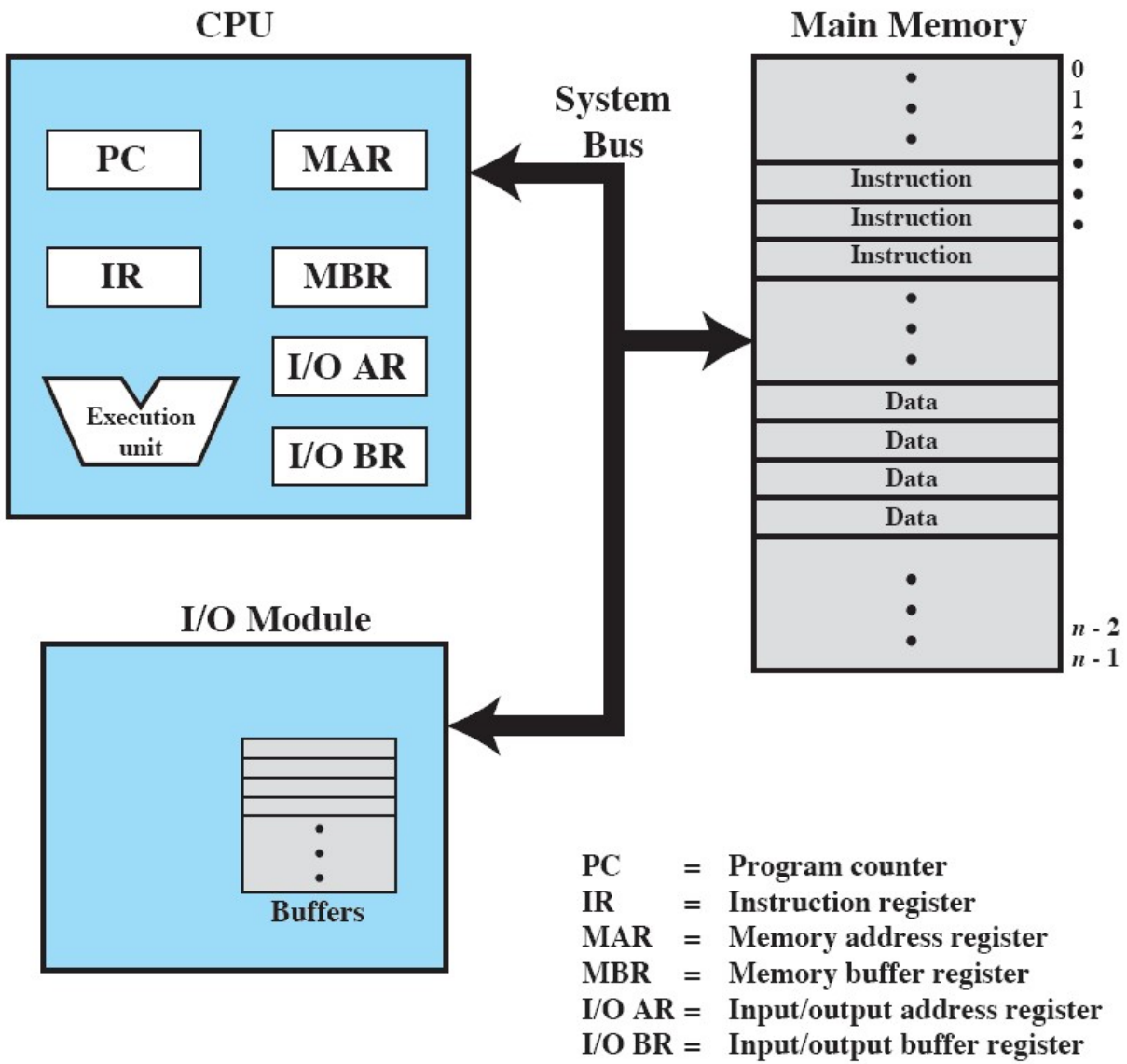
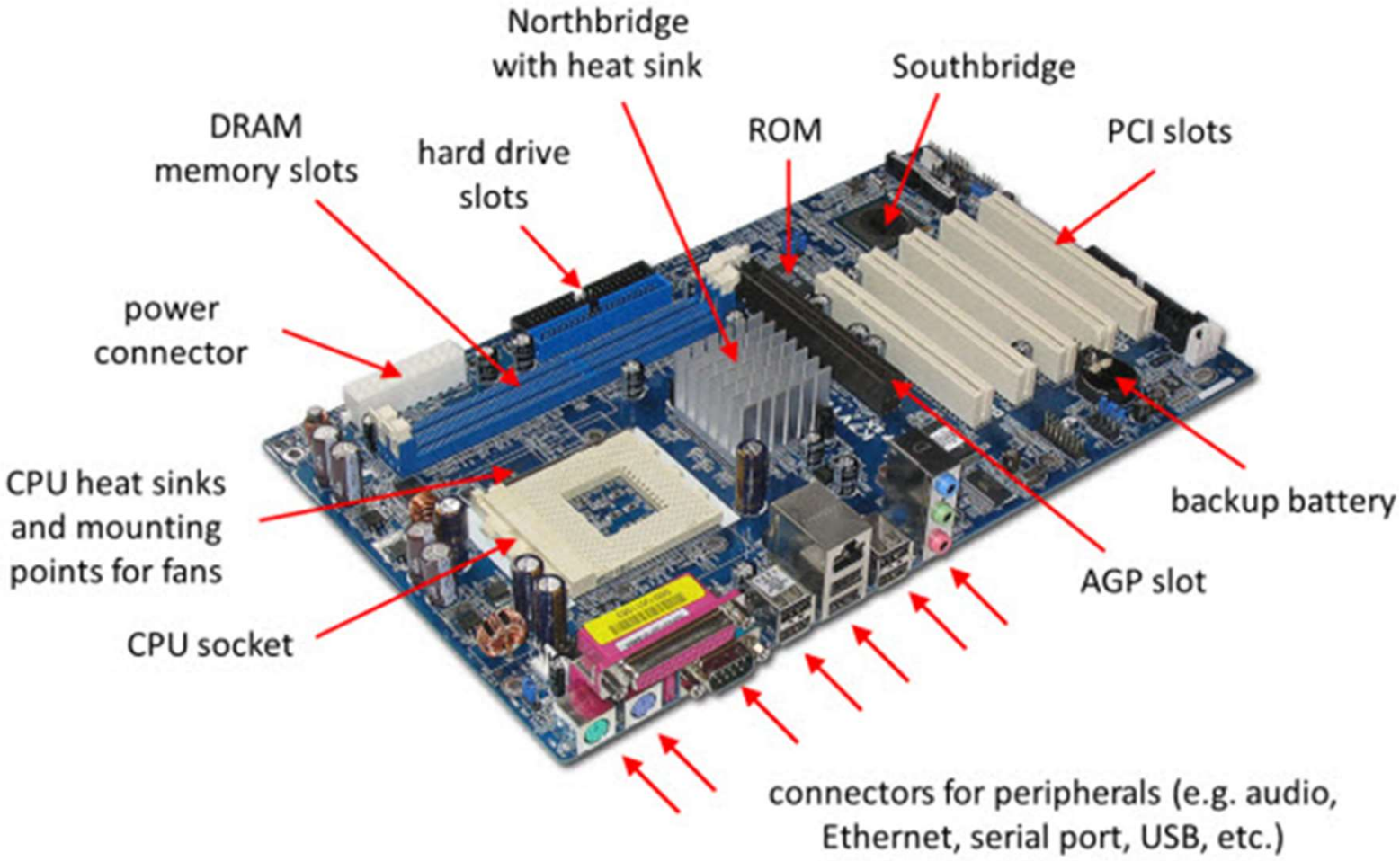


Figure 1.1 Computer Components: Top-Level View

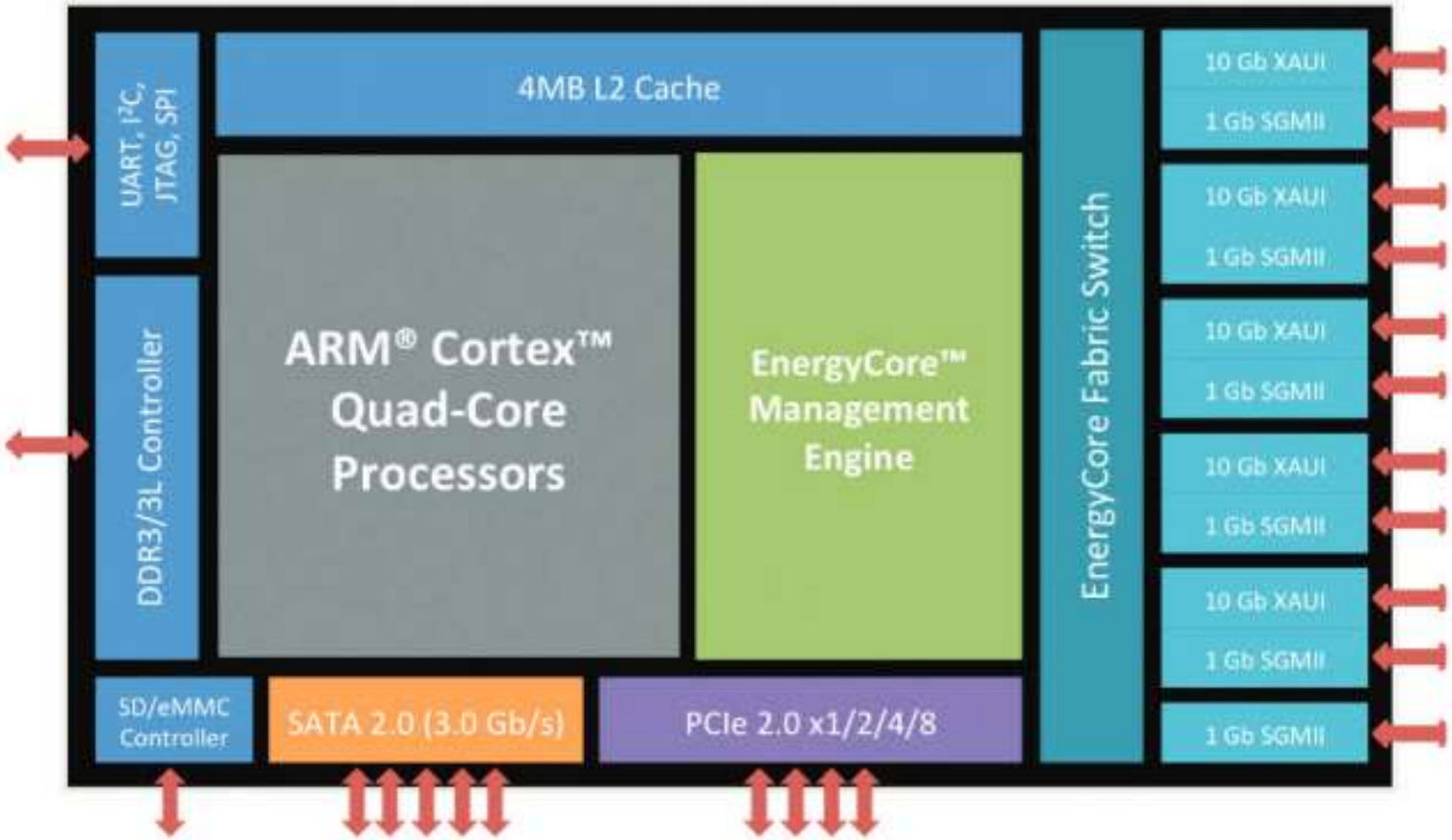
A Motherboard



The Microprocessor is the invention that brought about desktop and handheld computing

Graphical Processing Units (GPU's) provide efficient computation on arrays of data

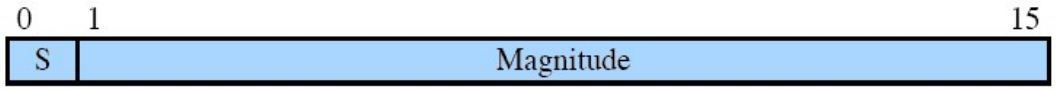
For some applications, the microprocessor is giving way to the System on a Chip (SoC)



Characteristics of a Hypothetical Machine

These are absurdly small word lengths in modern terms, but the principles hold.

(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

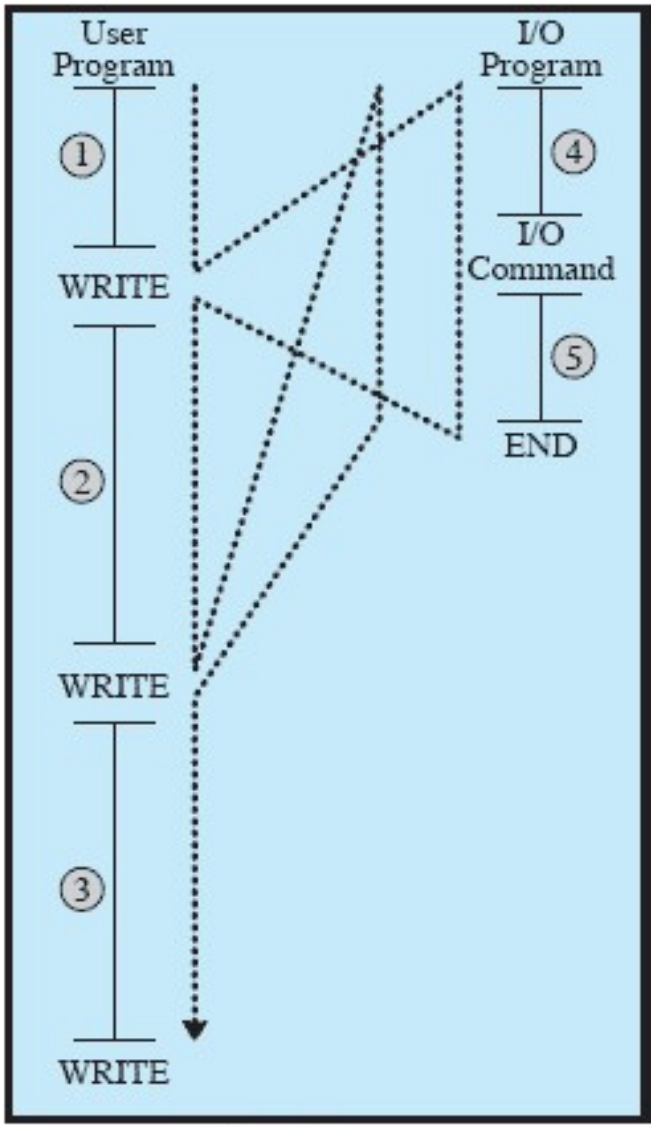
(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

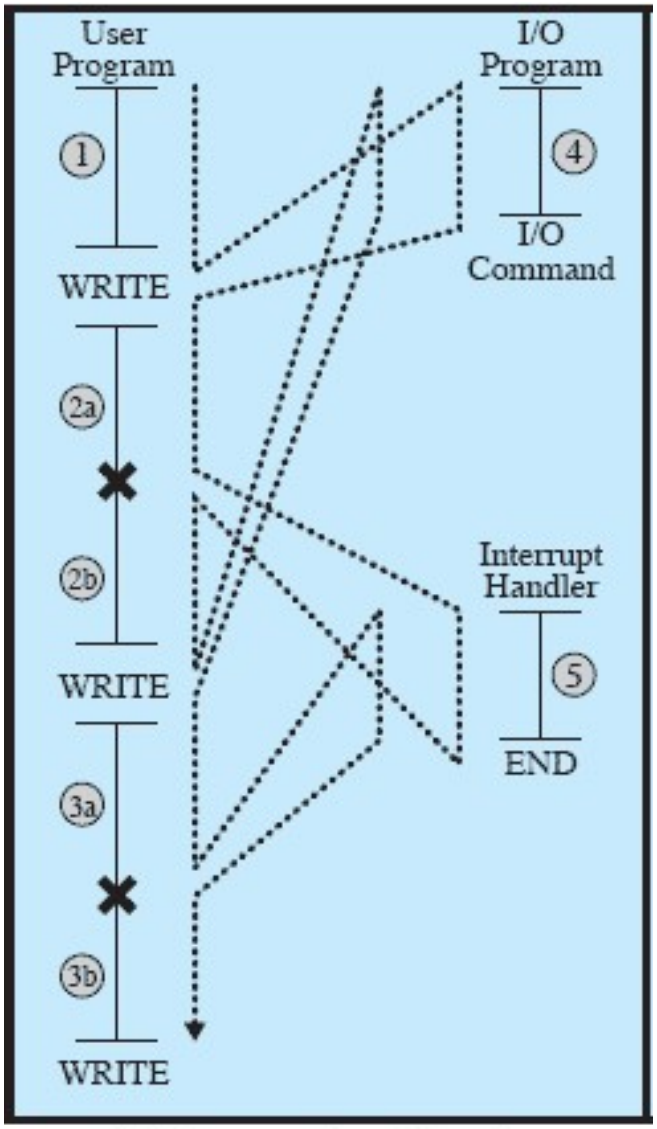
Figure 1.3 Characteristics of a Hypothetical Machine

Flow of Control Without Interrupts



(a) No interrupts

Interrupts: Short I/O Wait



(b) Interrupts; short I/O wait

Transfer of Control via Interrupts

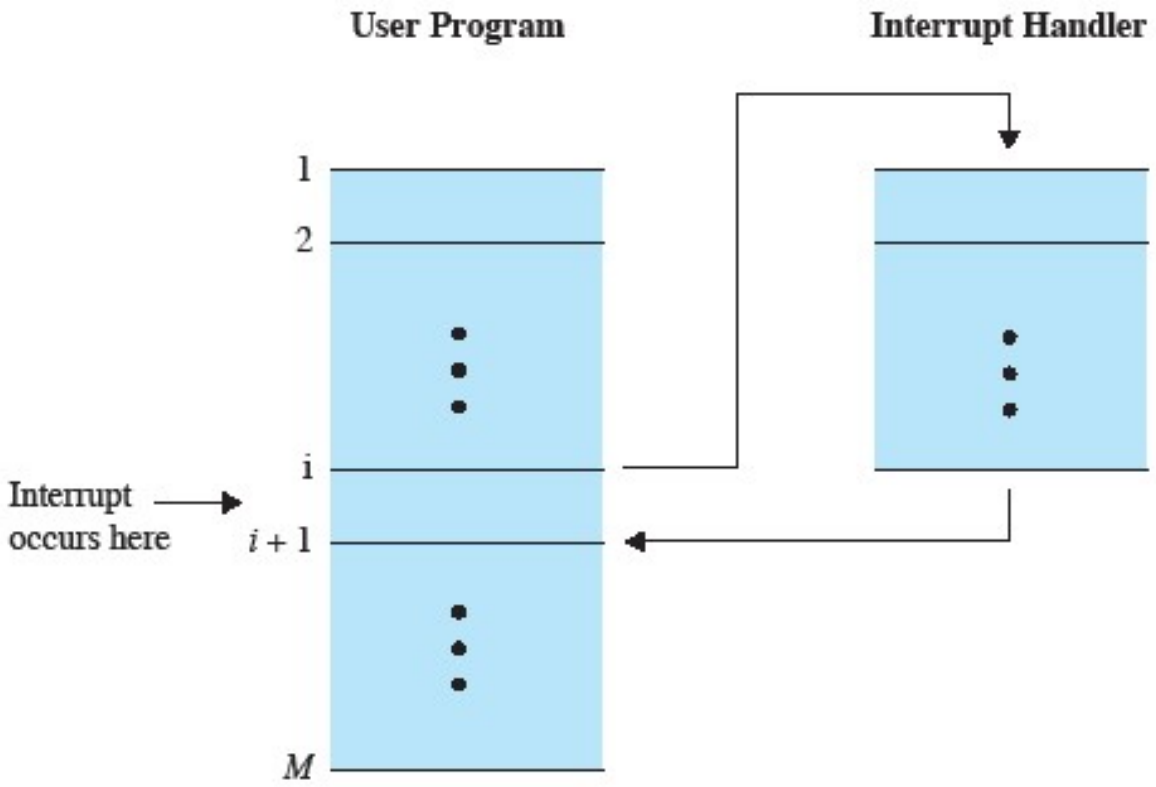


Figure 1.6 Transfer of Control via Interrupts

Instruction Cycle With Interrupts

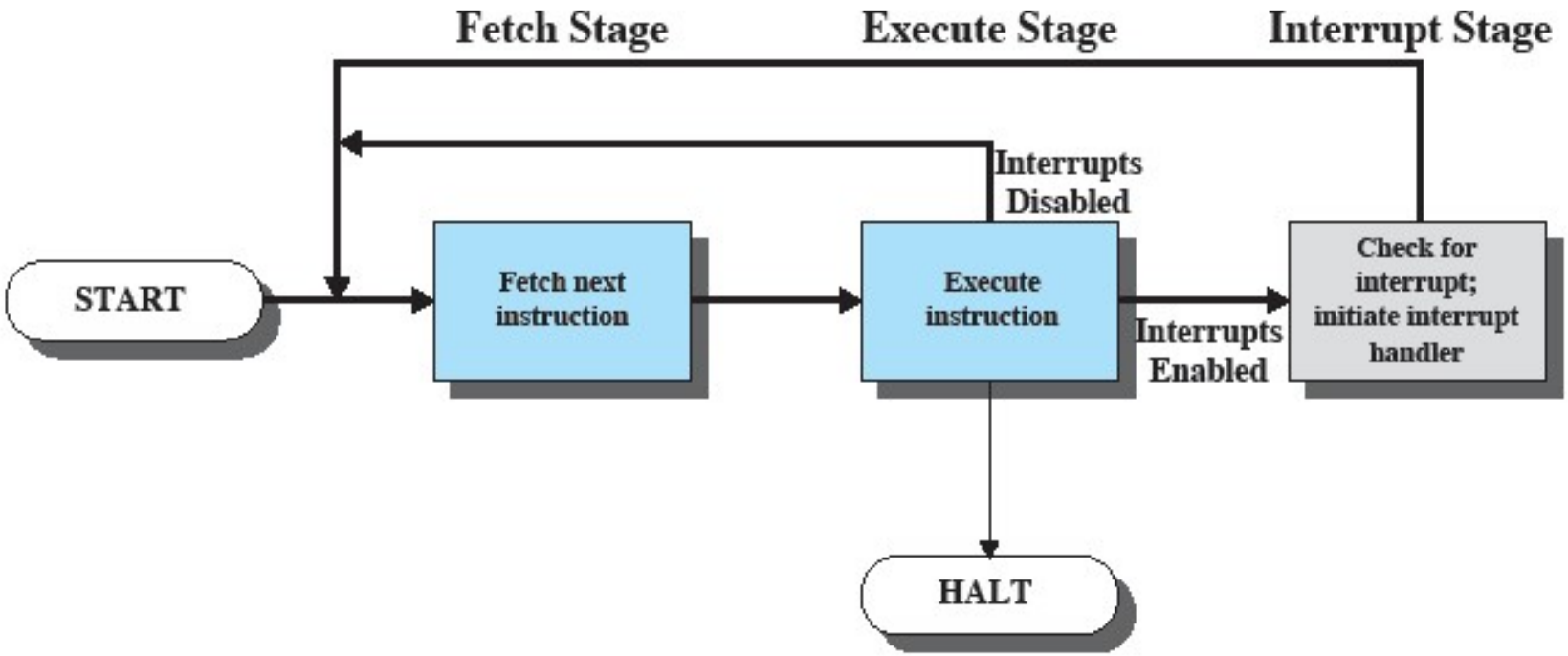
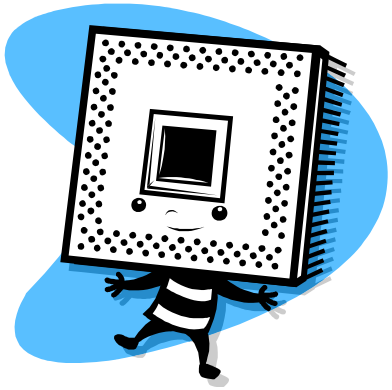


Figure 1.7 Instruction Cycle with Interrupts

Simple Interrupt Processing

Note the requirements on system software



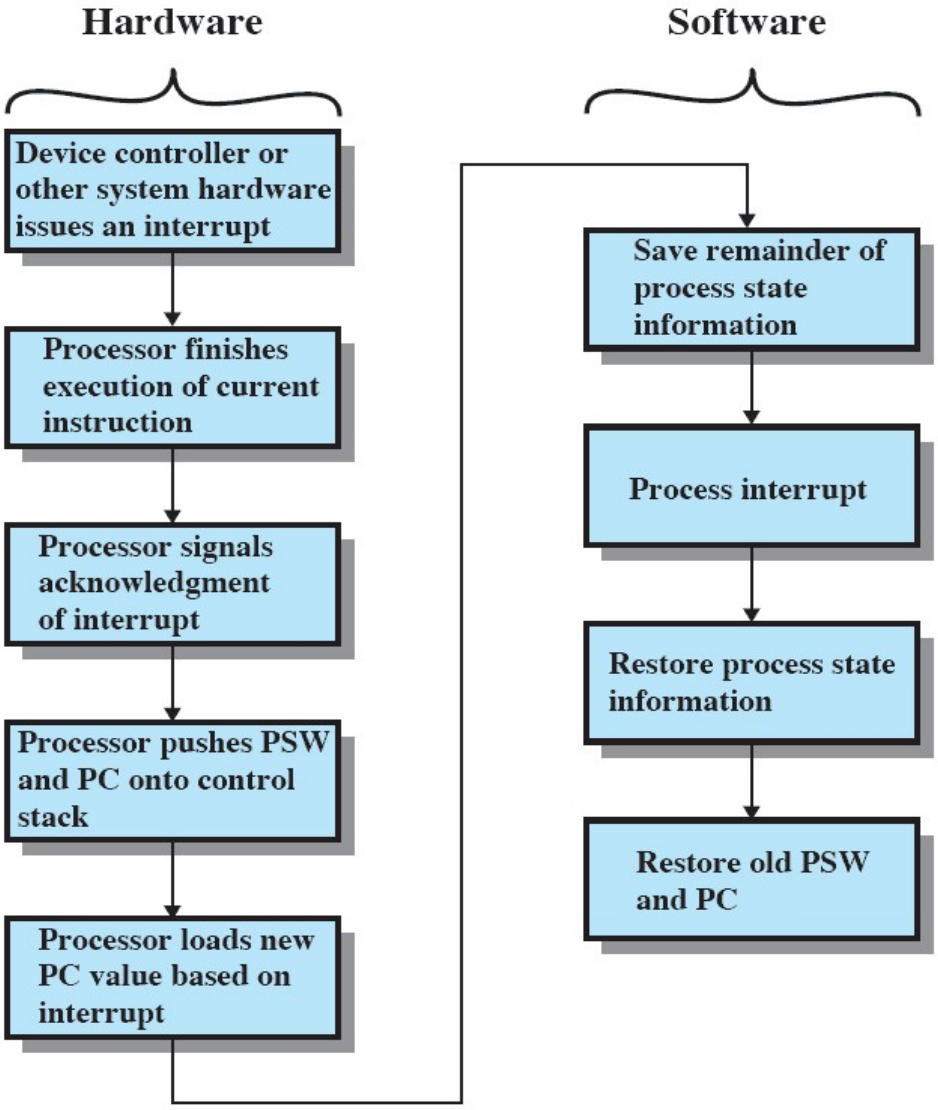
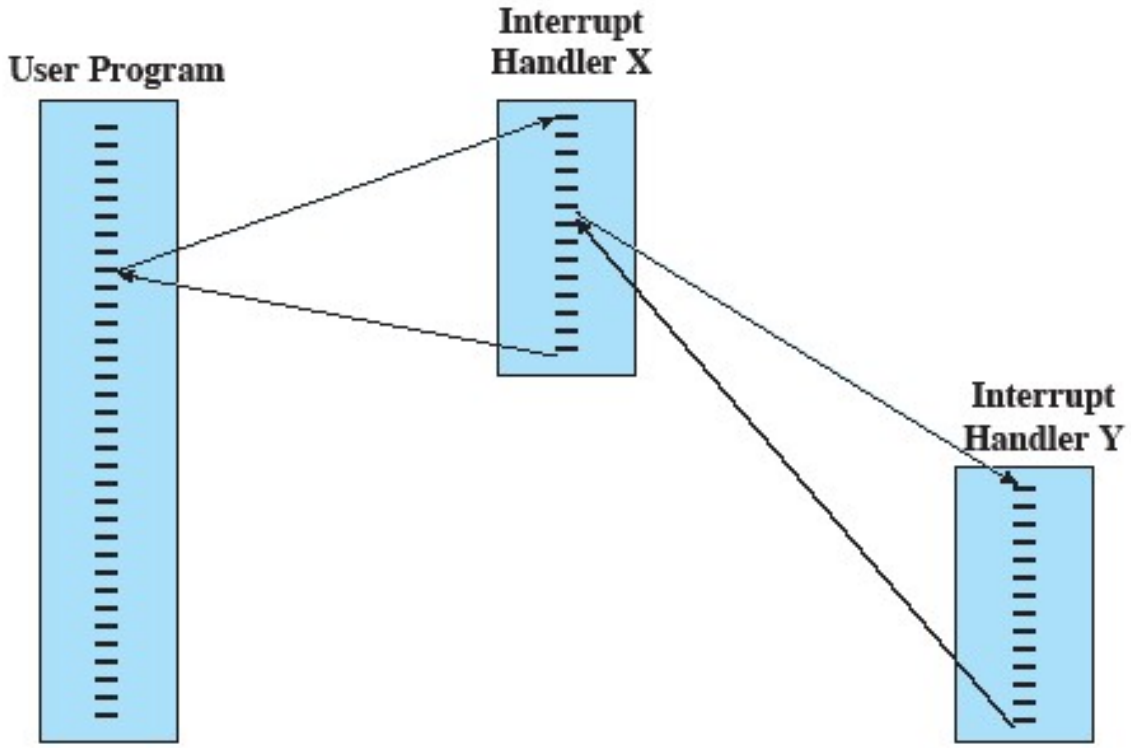


Figure 1.10 Simple Interrupt Processing

Transfer of Control With Multiple Interrupts:



(b) Nested interrupt processing

Nested

Example Time Sequence of Multiple Interrupts

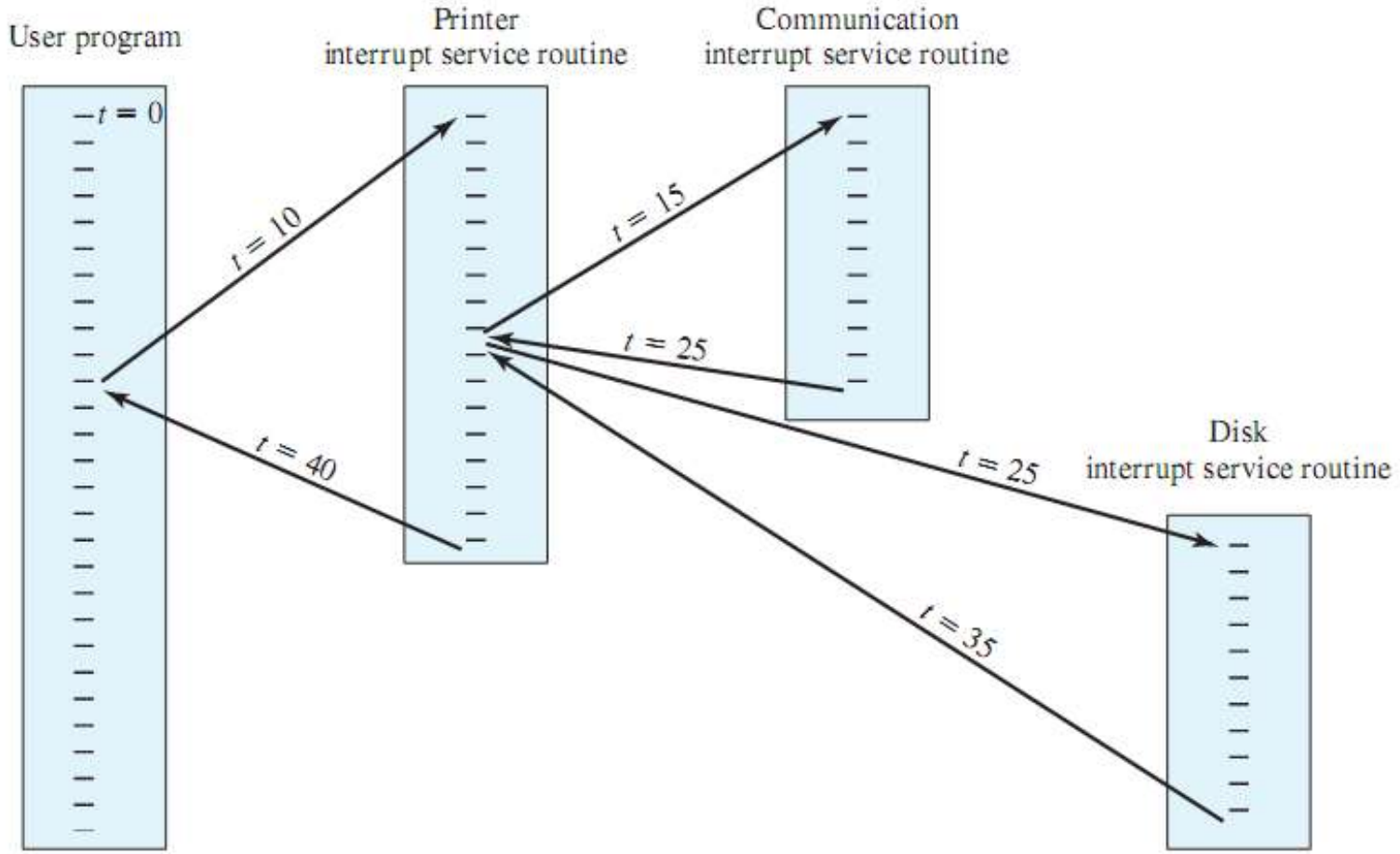


Figure 1.13 Example Time Sequence of Multiple Interrupts

The Memory Hierarchy

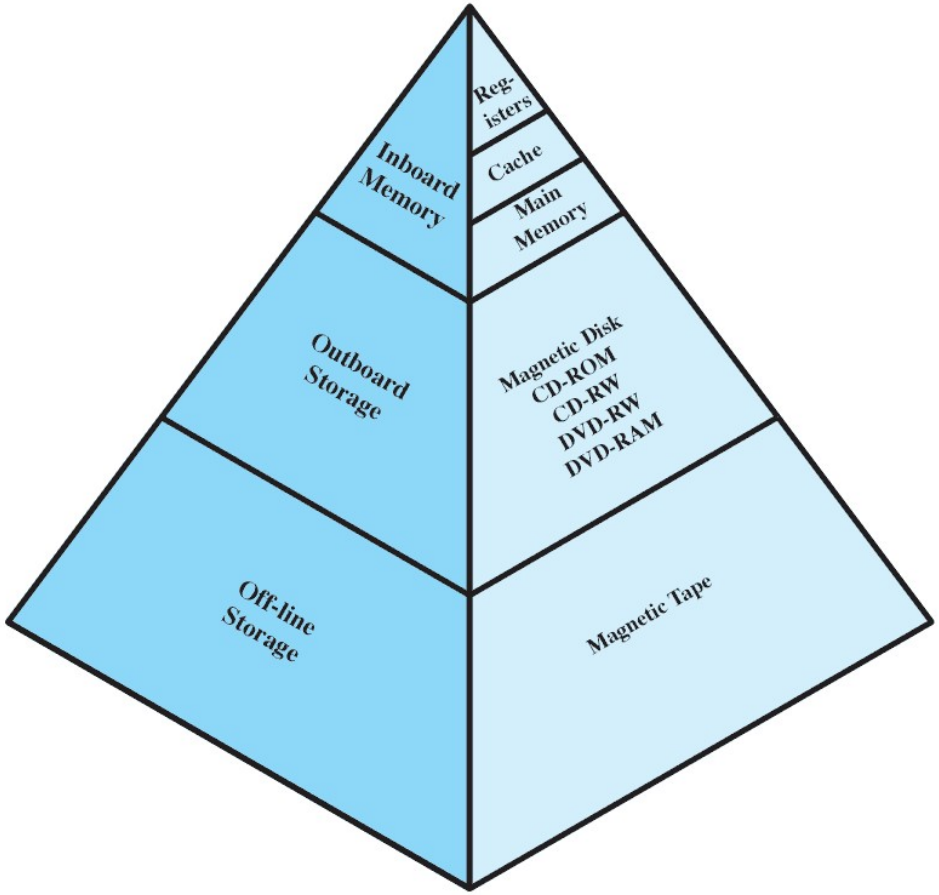
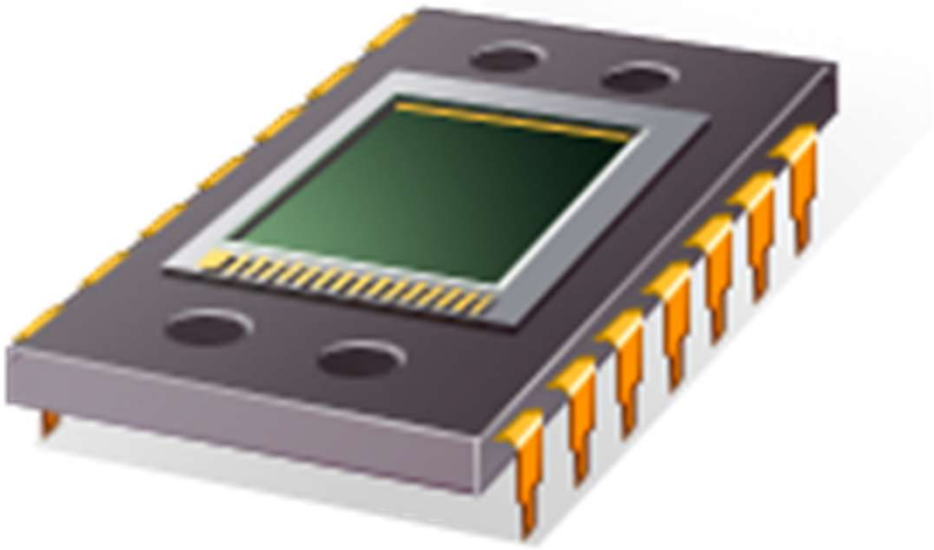
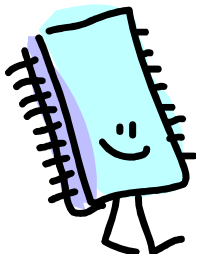


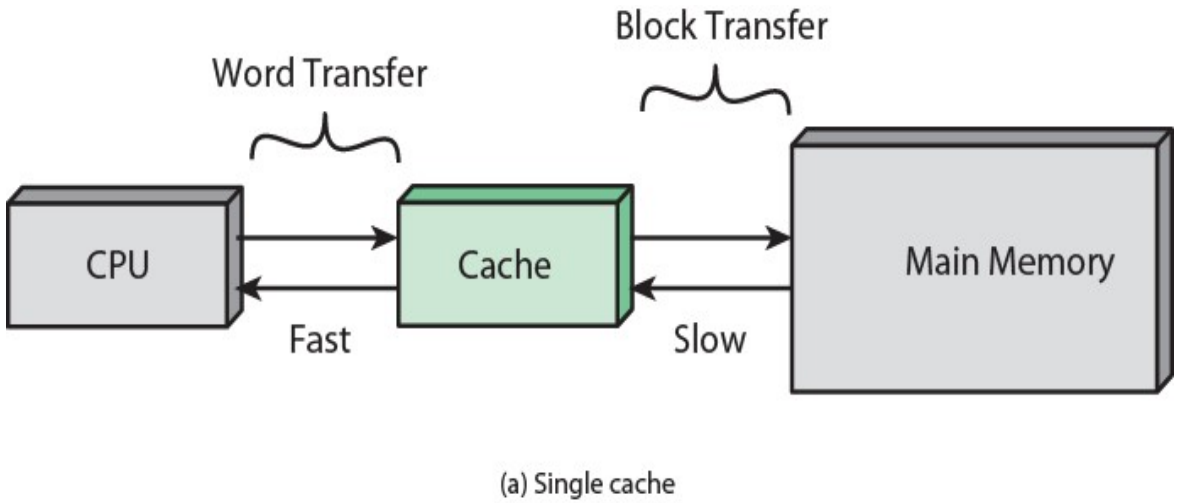
Figure 1.14 The Memory Hierarchy

Cache Memory

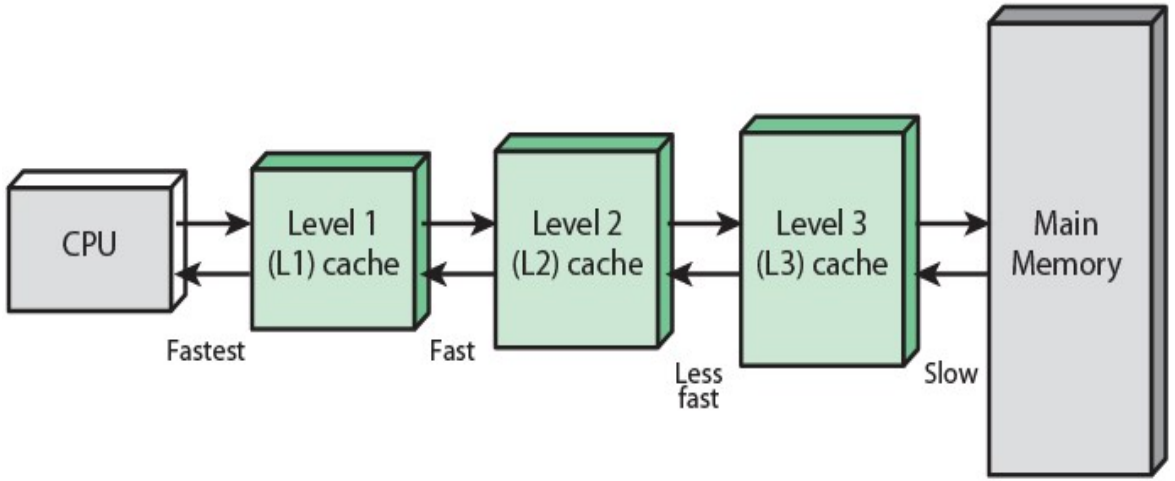


Cache and Main Memory



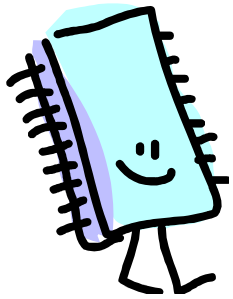


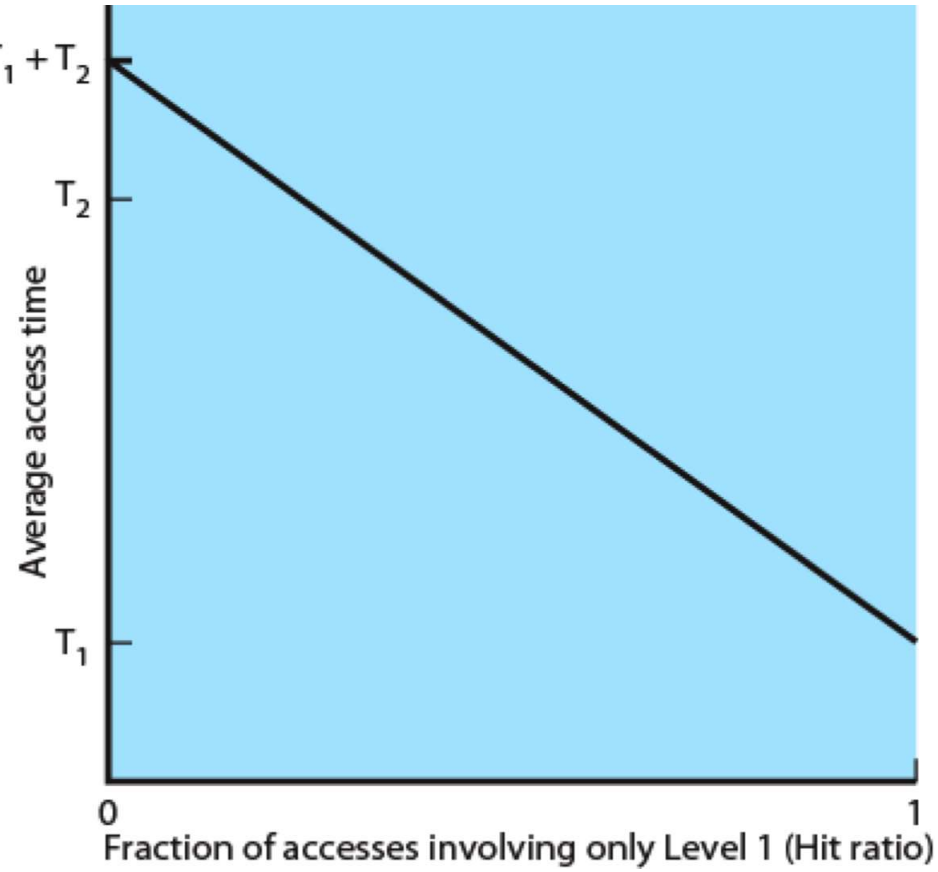
(a) Single cache



(b) Three-level cache organization

Performance of a Simple Two-Level Memory





Cache/Main-Memory Structure

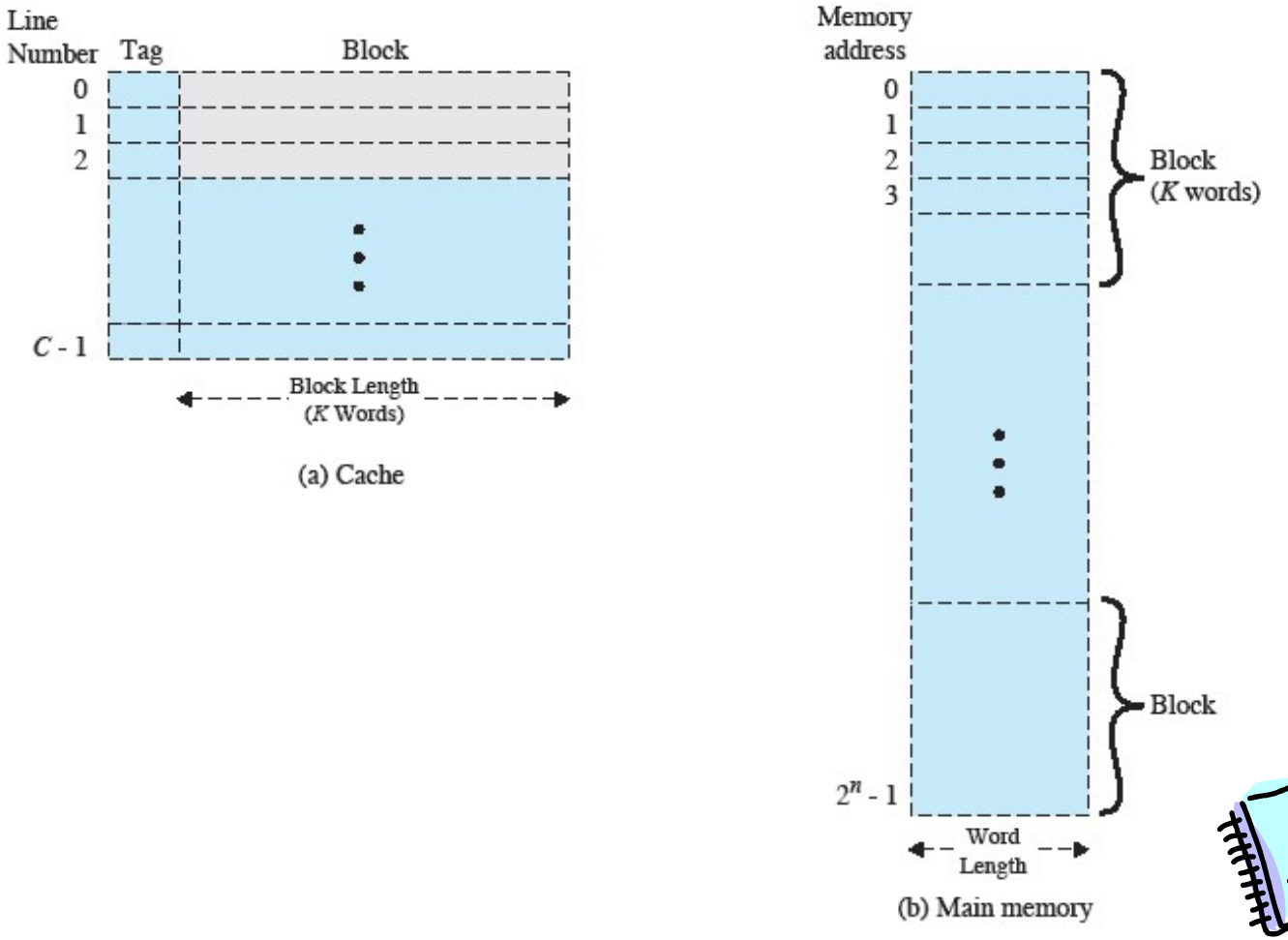
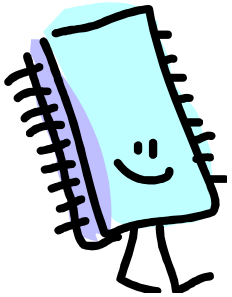


Figure 1.17 Cache/Main-Memory Structure

Cache Read Operation



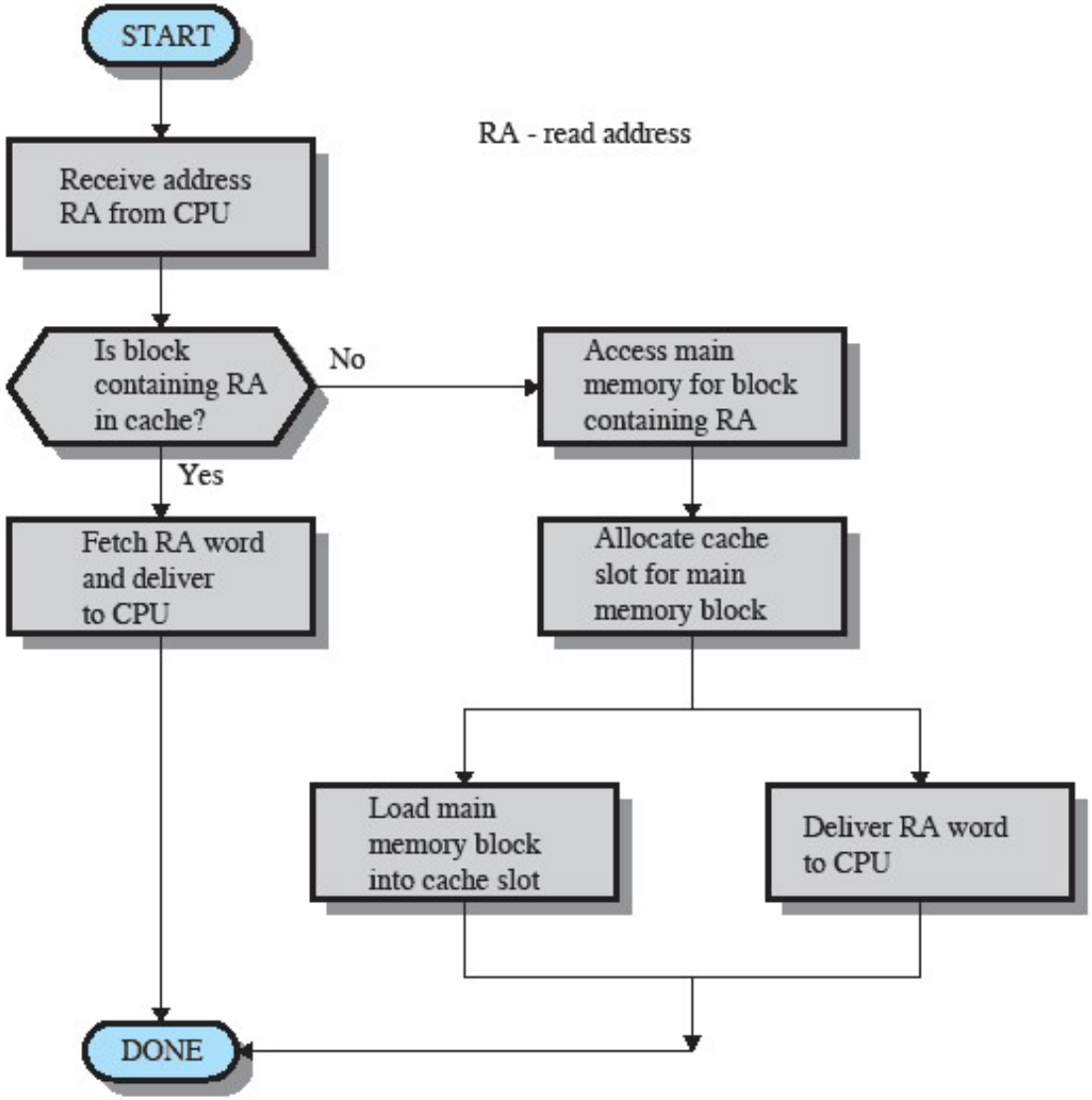
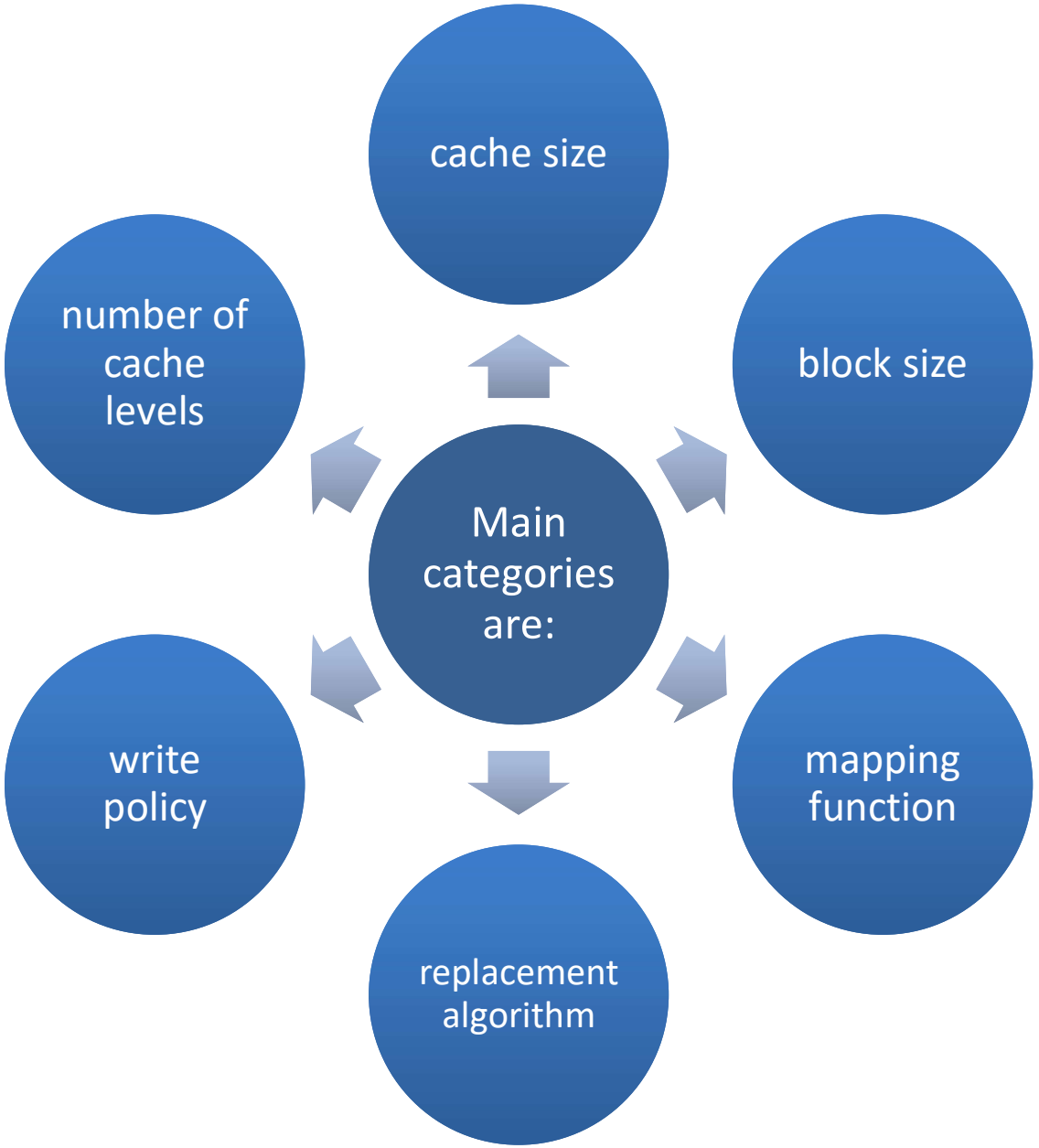


Figure 1.18 Cache Read Operation

CACHE DESIGN

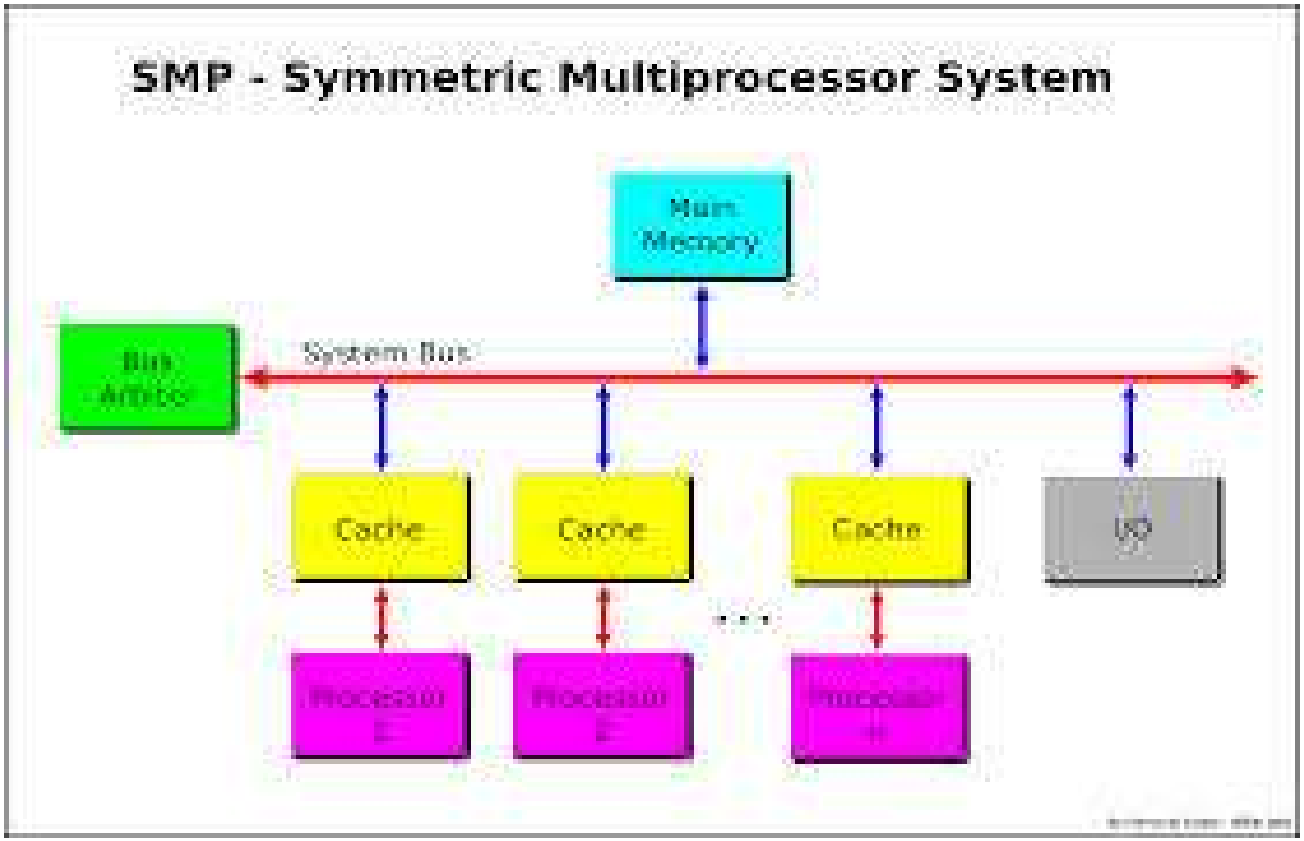


I/O Techniques

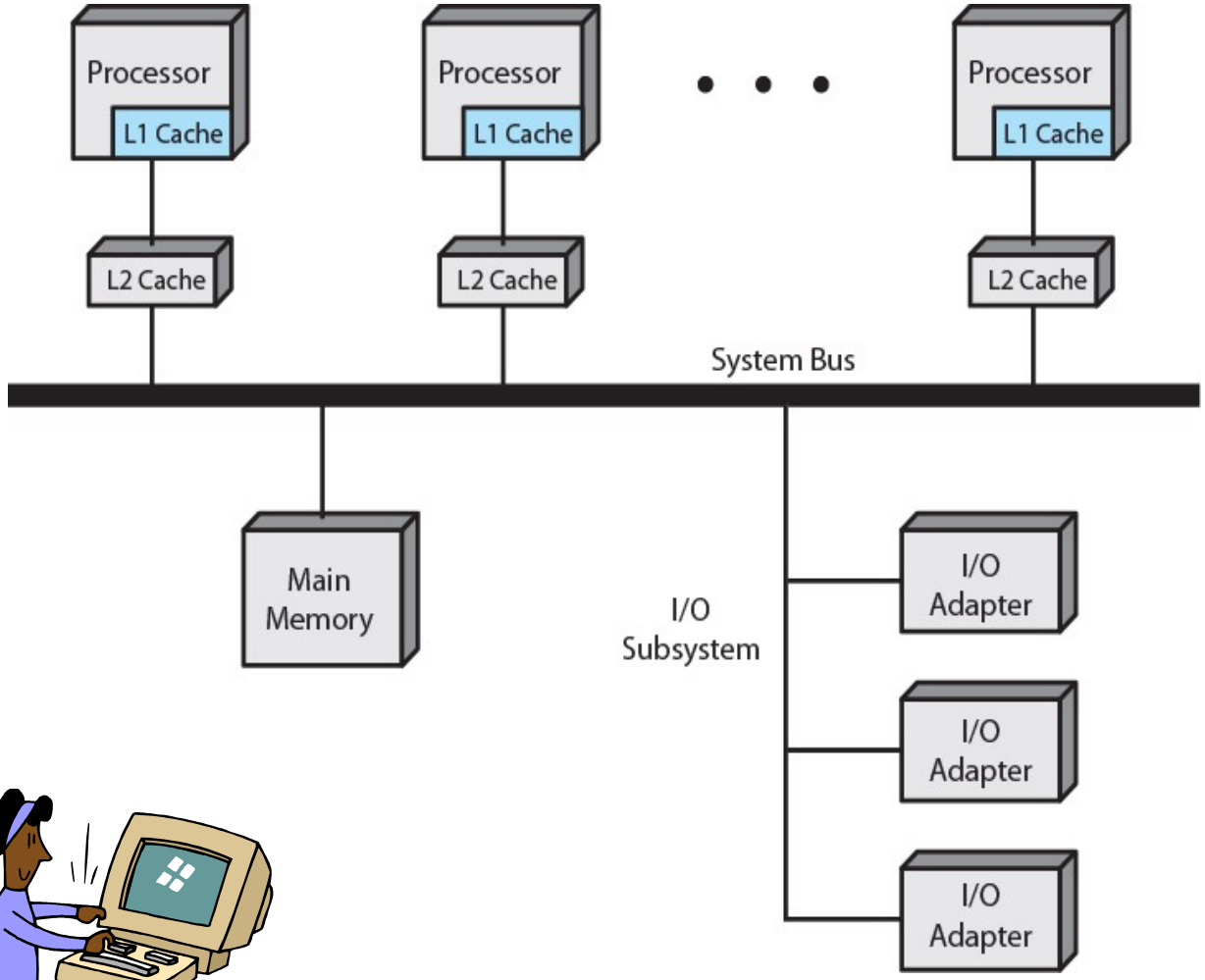
Three techniques are possible for I/O operations:

- Programmed I/O
- Interrupt-Driven I/O
- Direct Memory Access (DMA)

Symmetric Multiprocessors (SMP)



SMP Organization



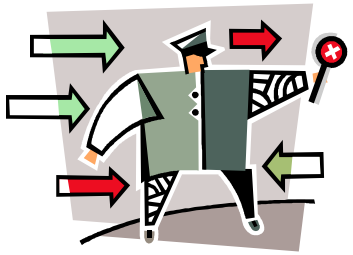


Figure 1.19 Symmetric Multiprocessor Organization

Intel Core i7

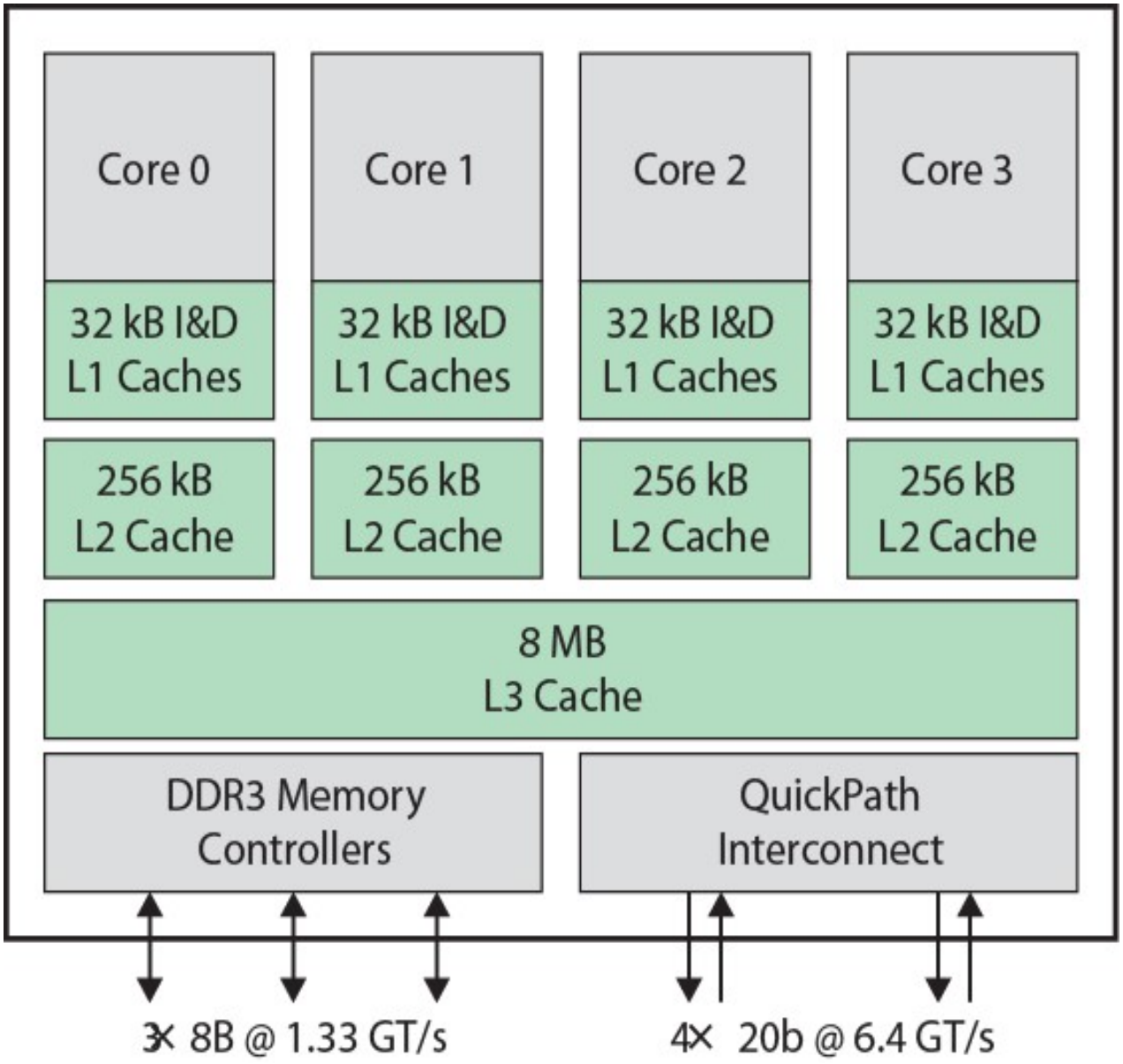


Figure 1.20 Intel Corei7 Block Diagram

Basic Hardware Organization

- Basic Elements
  - processor, main memory, I/O modules, system bus
  - GPUs, SIMD, DSPs, SoC
  - Instruction execution
    - » processor-memory, processor-I/O, data processing, control
  - Interrupt/Interrupt Processing
  - Memory Hierarchy
  - Cache/cache principles and designs
  - Multiprocessor/multicore