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PROFESSIONAL SKILLS

- 10+ years of 32/64 bit RISC(ARM/S+core) **hardware/software co-design and verification experience.**
- 10+ years of Linux Kernel Porting in ARM, MIPS and S+core based SOC and Device Driver Development experience.
- **10+ years of software development (C/C++ compiler, assembler, linker, debugger, instruction set simulator, tiny OS kernel, libraries, tools, etc.) under Linux using C, shell script, etc.**
- **6+ years of 32bit RISC ISA profiling and design experience from scratch**
- **6+ years of 32bit RISC hardware/software co-design and verification experience.**
- 6+ years of Peripheral IP verification experience

CAREER SUMMERY

Full Time Job

2010/07 ~ Present Sr. Staff Software Engineer/ CPU verification design manager of Marvell Semiconductor

- **In house ARMV7/V8 CPU system level verification.**
  System verification, Including kernel/driver/application porting and environment automation. We verifying the FPGA images with thousands test cases integrated in the auto regression system and report the healthiness and reliability ot HW colleagues. we need to analyze the test results and redesign the experiments for narrow down/reproduce/root cause the issue. For complicated issue, it takes several months to root the cause. It needs strong knowledges in computer science, including CPU architecture, operating system, device driver, toolchain and applications.
- **Hardware/software co-verification.**
  Connected FPGA & QEMU by PCIe, co-verifying on the fly based on the program's waypoint. Able to cross-check and find the divergent execution path between QEMU and DUT.

2009/12 ~ 2010/06 Principal Engineer of Nova Technology Corporation:

- **Linux kernel, device driver porting and maintain for DTV, STB SOC**
  I am responsible for porting the Linux kernel to DTV, STB SOCs and help to clarify the issues that colleagues meet in device driver develop. Shared working experience and skill with colleagues in Linux kernel and device driver develop. I ported the Linux 2.6.30 for DTV Soc 72682 and released to Samsung.

2007/10 ~ 2009/12 Manager of Sunplus Core Technology Corporation (Spin off from Sunplus Technology):

- **Porting Linux V2.4/V2.6 to S$^+$core architecture**
  In this project, we tried to port Linux kernel V2.4/V2.6 to a new architecture, S$^+$core. I was asked to lead the team to review the GNU tool chain to fit kernel need, and port the kernel to S$^+$core at the same time. We have also ported a subset of test items of LTP from Linux to verify the ported kernel. The Linux port of S$^+$core architecture has been committed to Linux kernel official release since Version 2.6.32.

- **PC Linux DVR/IPCam system on DSP base H.264 codec**
  The project is developing a DVR/IPCam system on Linux environment, base on a DSP base H.264 codec. My team was asked to define and implement the driver interface and control protocol between Linux driver and the DSP firmware. The driver has been implemented following Video4Linux version 2 (aka V4L2), and, the control protocol has been implemented by packet based mechanism. In the meantime, we also worked on a DVR application for demo, and ported the IPCam system to an embedded system that powered by ARM base SOC. The streaming server of the IPCam is powered by FFMPEG and FFserver.

2000/11 ~ 2007/10 Senior Software Engineer /Project Manager of Sunplus Technology Corporation:

- **System software for In-house 32bit RISC S+core7[1]:**
  S+core 7 is Taiwan's first 32bit embedded processor design and has commercial success. I lead the team development/port the system software from scratch, including C/C++ compiler, assembler, linker, debugger, instruction set simulator, tiny OS and libraries, etc. Finally, we not only ported the GNU tool chain to S+core architecture, but also commit it back to open source community, that we are proud of. The SPG290[2]/ SPIF250[3]/ SPV7050[4] is the product line that commercial success based on the S+Core7.

- **Hardware/Software Co-designed for In-house 32bit RISC S+core7:**
  During hardware designer working on S+core RTL, we are work on a co-verification environment based on the Instruction set simulator, and connected it to the RTL via the PLI interface, compare the behavior of instructions on hardware RTL simulator. Finally, the environment became a random test pattern generator and performed random testing between hardware and software.

- **S+core3(3 pipeline stages) hardware/software co-design and verification:**
  S+core3(3 pipeline stages) hardware/software co-design and verification:
  The project goal is to reduce 30+% code size of S+core , and competed with arm thumb2. I lead the team to perform the ISA profiling on various benchmarks and propose the new ISA for S+core3. We redesigned the 16bit instructions and reduce 30% code size that evaluated on the FPGA base on the new tool-chain/ISA simulator we ported in ISA profiling.

- **Porting Linux V2.4/V2.6 to S+core architecture:**
  I was asked to lead the team to review the GNU tool chain to fit kernel need, and port the kernel to a S+core at the same time. The Linux port of S+core architecture has been committed to Linux kernel official release since Version 2.6.32.

  [1] https://en.wikipedia.org/wiki/S%2Bcore
  [2] http://www.sunplus.com/press/press.asp?id=10338C4323417
  [3] http://www.sunplus.com/press/press.asp?id=1B3D1174A15291
  [4] http://w3.sunplus.com/products/spv7050.asp

1999/06 ~ 2000/9 Software Engineer of ALI Technology Corporation:

- **DVD player system development**
  I was responsible for the VCD navigation, front panel control in DVD player system.

Position Desired

Staff Software/Firmware Engineer

Certification or License

1996

National Senior Examination of Professional and Technical Personnel in the category of Information technology personnel

Education

1995/09 ~ 1997/06
Master in Department of Electrical Engineering, National Taiwan University of Science and Technology

1993/09 ~ 1995/06
Bachelor in Department of Computer Science, Soochow University

1988/09 ~ 1993/06
College Student of Department of Electrical Engineering, Hwa Hsia Institute of Technology

Experience

Full-time Jobs:

2010/07 ~ Present	Sr. Staff Software Engineer/ CPU verification design manager of Marvell Semiconductor
2009/12 ~ 2010/6	Principal Engineer of Nova Technology Corporation
2007/10 ~ 2009/12	Manager of Sunplus Core Technology Corporation
2000/11 ~ 2007/10	Senior Software Engineer /Project Manager of Sunplus Technology Corporation
1999/06 ~ 2000/9	Software Engineer of ALI Technology Corporation

Academic Projects

- Vtrio, a tiny multi-tasking OS kernel base on DOS environment implemented in C++
- Shell enhancement in Minix operating system, implemented in C

Master Thesis

A Study of Fault-Tolerant Routing on Star Graph Using Limited-Global-Information

Abstract

In this thesis, we study the problem of fault-tolerant communication in star graphs multi-computers in which components may fail. We propose the concept of safety levels which respect to the distance to nearest faulty node of each direction. A simple algorithm is presented to calculate the safety levels of each processor that in system. A routing algorithm which based on safety levels is then presented to facilitate efficient fault-tolerant routing. The algorithm route a message in an attempt to minimize misrouting which is undesirable for a communication function. Moreover the fault-tolerant routing algorithm use the information embedded in safety levels to improve the time optimality and reach-ability of a message to its destination. Extensive simulation has been conducted to evaluate the performance of the proposed mechanisms.

References

Available Upon Request