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# Callisto Hardware Board

| Version | Date       | Note                  |
|---------|------------|-----------------------|
| V0.0    | 2020.08.05 | Original version (DH) |
| V1.0    | 2020.09.27 | Revised version       |

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## 1. Callisto hardware board

### 1.1 Introduction

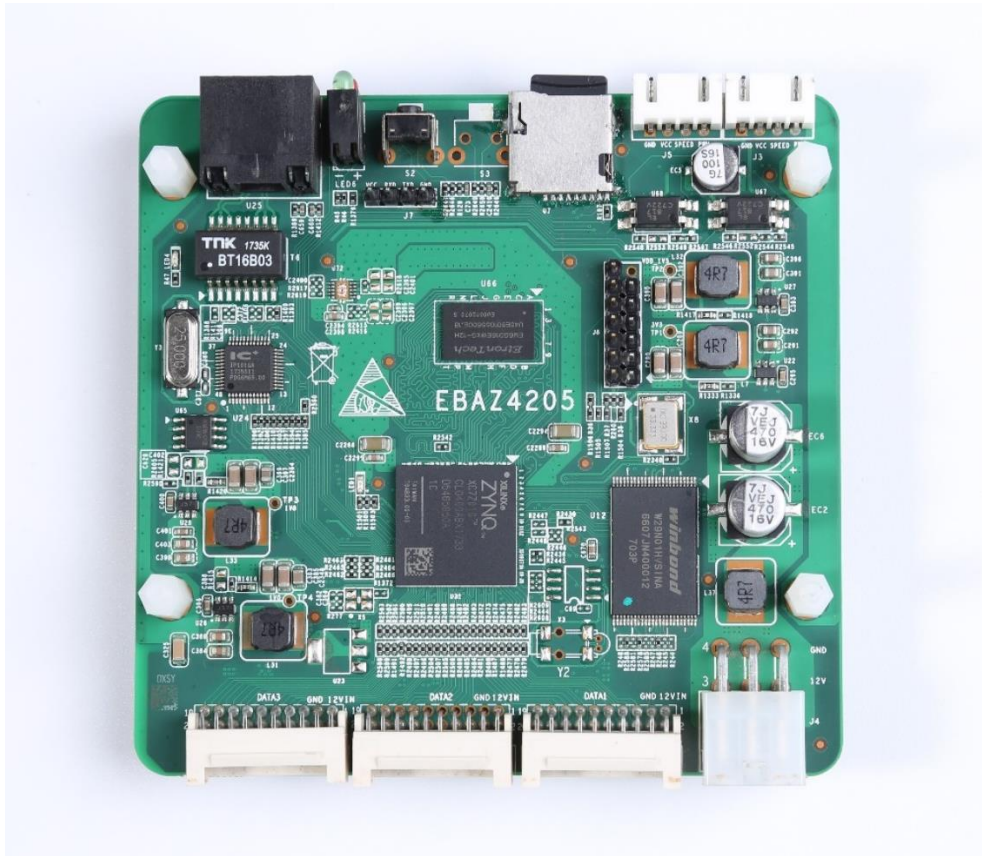
Callisto hardware board is developed by SpaceChain to run on-orbit blockchain applications. The board employs Zynq-7010 as the processor and is integrated with a power supply system, DDR, NAND flash, TF card and ethernet. In addition, the board is equipped with 42-pin I/O ports, allowing advanced users to use Vivado to program the board and extend functions such as UART, I2C and CAN.

### 1.2 Schematics of Callisto Hardware board

We add a protection board for the Callisto hardware board. There are power supply and USB-C port on the protection board.



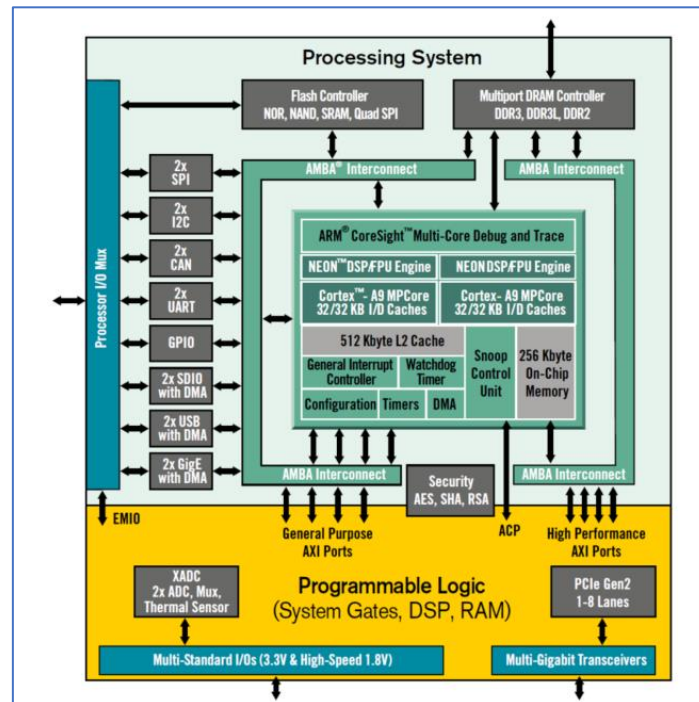
The below figure shows the circuits after removing the protection board.



## 2. Zynq-7000 SOC introduction

### 2.1 SoC

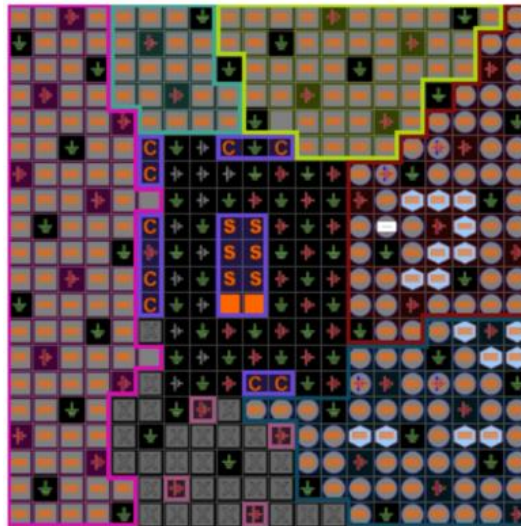
The Zynq-7000 family is based on the Xilinx SoC architecture. These products integrate a feature-rich dual-core ARM Cortex™-A9 based processing system (PS) and 28 nm Xilinx programmable logic (PL) in a single device. The ARM Cortex-A9 CPUs are the heart of the PS and also include on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces. The below figure shows the block diagram of Zynq-7000.



- **Processing system (PS)**
  - **Core:** Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
  - **CPU frequency:** 866 MHz or 667 MHz (This board uses 667 MHz)
  - **L1 Cache:** 32 KB instruction Cache, 32 KB data per processor
  - **L2 Cache:** 512 KB
  - **On-chip RAM:** 256 KB
  - **External memory support:** DDR3, DDR3L, DDR2, LPDDR2
  - **External Static Memory Support:** 2x Quad-SPI, NAND, NOR
  - **DMA channels:** 8 (4 dedicated to programmable logic)
  - **Peripherals:** 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
- **Programmable logic (PL)**
  - **Xilinx 7 series programmable logic equivalent:** Xilinx 7 Series Artix®-7 FPGA
  - **Programmable Logic Cells:** 28K (Around 430K ASIC logic gates)
  - **LUTs:** 17,600
  - **Flip-Flops:** 35,200
  - **RAM:** 240 KB
  - **DSP Slices:** 80

## 2.2 SoC Bank

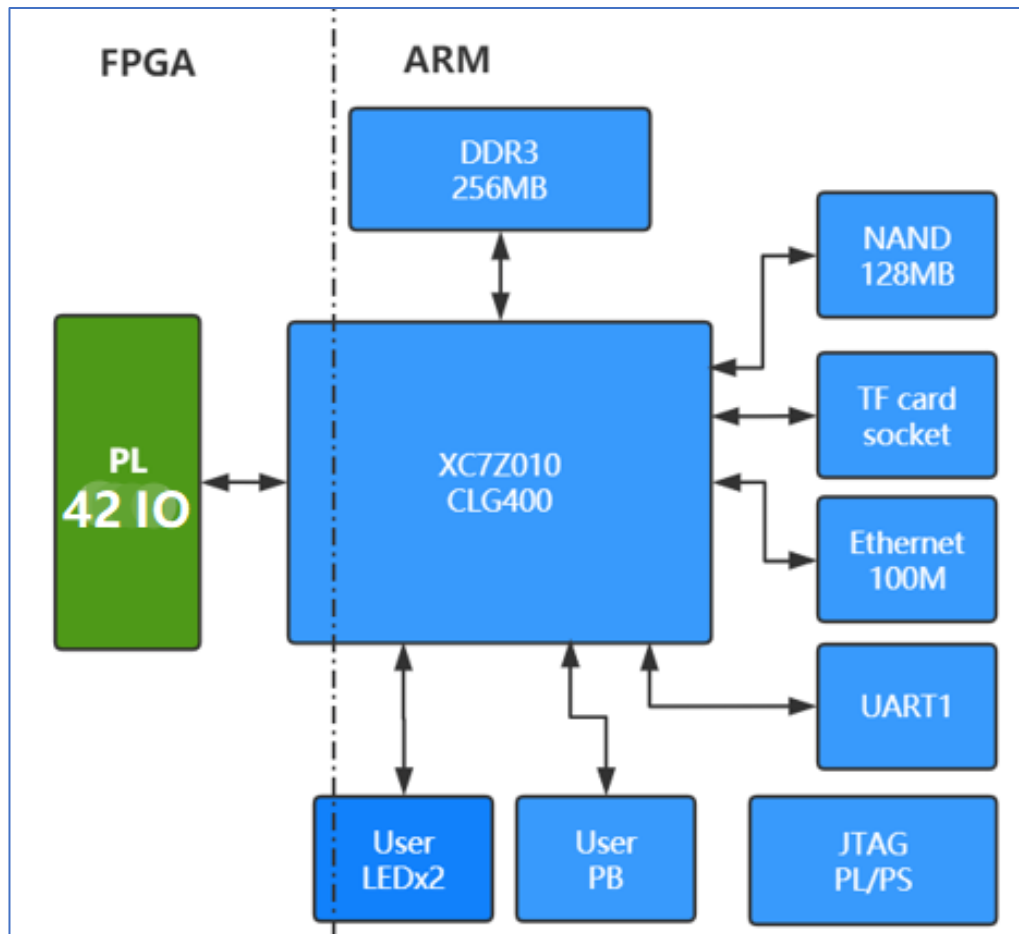
The below figure shows the bank configuration of ZYNQ7000.



- **BANK 0:** JTAG, reset, analog signal
- **BANK 13:** Only for XC7Z020
- **BANK 34:** PL part, 50-pin (24 differential pairs)
- **BANK 35:** PL part, 50-pin (24 differential pairs)
- **BANK 500:** PS part, MIO [0:15], 16-pin, RGMII, USB, SDIO, UART
- **BANK 501:** PS part, MIO [16:53] 38-pin, QSPI, NAND Flash
- **BANK 502:** PS part, DDR pins

### 3. Hardware board configuration

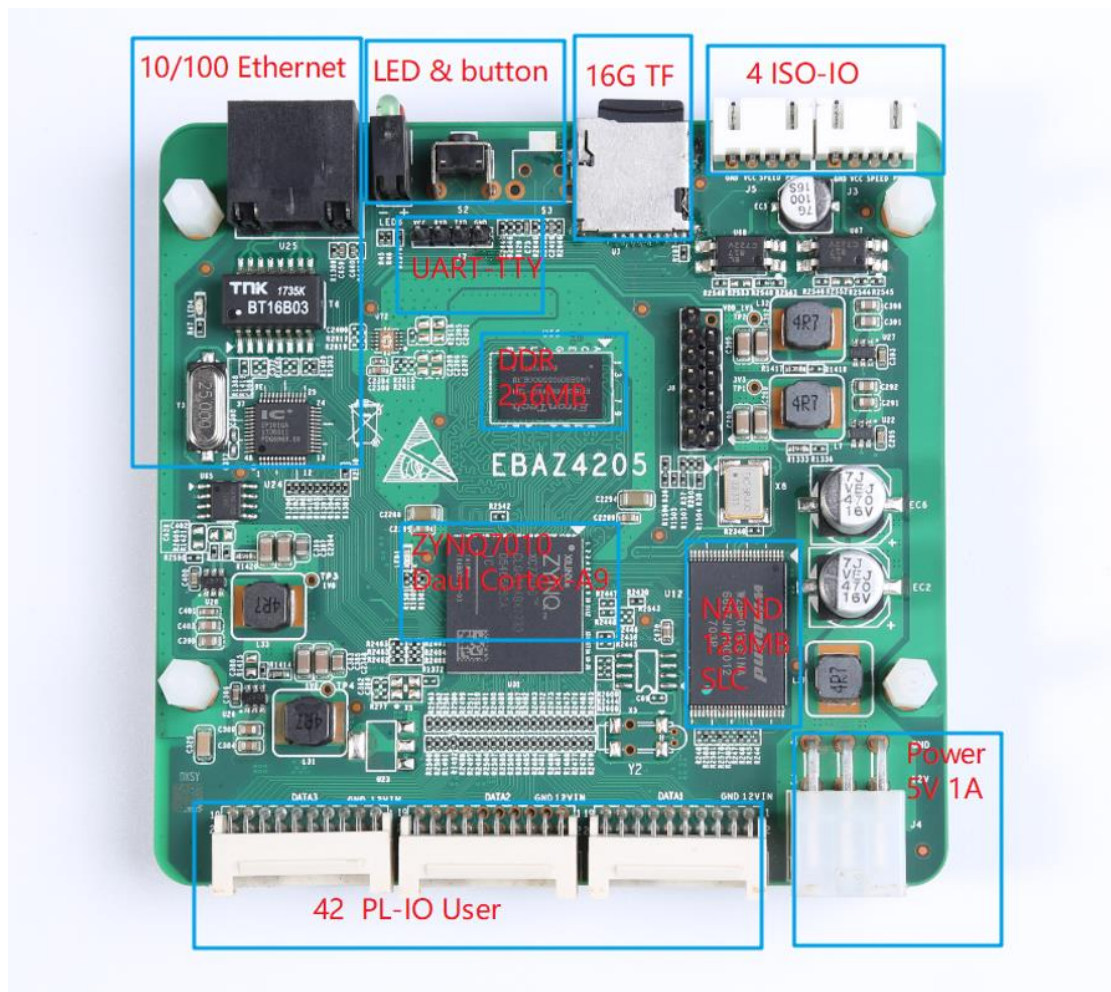
#### 3.1 Hardware board configuration introduction



- Hardware
  - 128MB NAND Flash
  - 256MB DDR3 SDRAM
  - 16-bit data bus
  - 10/100Mb/s Ethernet
- Peripherals
  - TF card port: one TF card port
  - Debugging serial port: one channel, UART1
  - Data transmission channel: One channel, 10/100Mb/s Ethernet port
  - Input: One button
  - LED: 2 LED lights
  - JTAG debugging ports: One 14-pin double-row debugging interface with 2.54 mm spacing
  - Extension ports: 3 × 20-pin (60 pins in total) double-row interfaces with 2 mm spacing



### 3.2 Hardware configuration

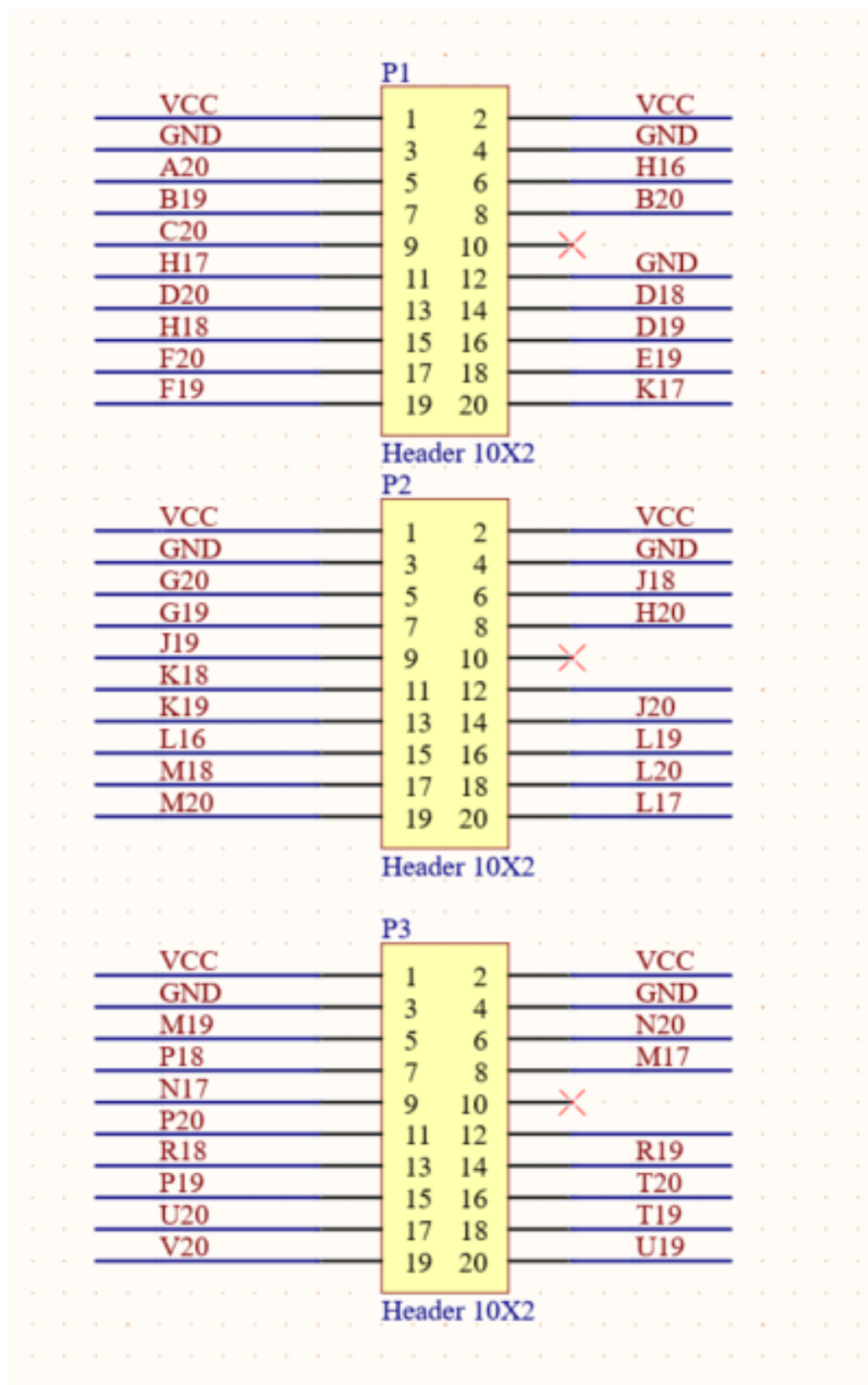


## Table of Interfaces

| Number | Item                | Note          |
|--------|---------------------|---------------|
| J8     | JTAG                | 14-Pin        |
| U25    | 10/100Ethernet      | RJ45          |
| U7     | Micro SD Card slot  |               |
| J7     | Debug UART          | UART1         |
| J4     | 5V DC Power jack    |               |
| LED1   | FPGA DONE LED       |               |
| LED6   | USER LED            | RED and GREEN |
| DATA1  | PL extension port 1 |               |
| DATA2  | PL extension port 2 |               |
| DATA3  | PL extension port 3 |               |

### 3.3 Extension port explanation

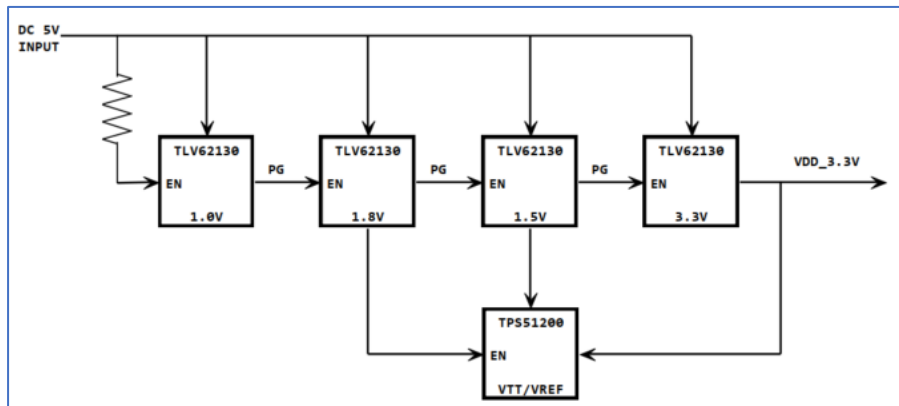
All the extension ports are connected to FPGA of Z7010. The definition of the extension ports is shown in the below figure.





## 4. Other systems on the hardware board

### 4.1 Power supply system



The above figure shows the power supply diagram of the Callisto hardware board. The power-up sequence is 1.0, 1.8, 1.5 and 3.3 V. This 3.3 V also serves as the reset signals. The levels of pins of PL and PS are set by the relevant registers.

The USB-C port for 5 V input voltage is at the side of protection board. The LED will be lit once powering on the hardware board.



### 4.2 Zynq7000 Boot mode

The Callisto hardware board can be booted by two methods: TF card or NAND flash. The boot modes can be selected through resistors R2577 and R2584. Please

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note that the Callisto hardware board has to be booted by TF card such that both Linux and SpaceChain OS can be booted. It is not recommended to change the boot mode to NAND flash.

- Connect a 20 k $\Omega$  resistor to R2584 while leave the position of R2577 empty. The board is booted by NAND Flash.
- Connect a 20 k $\Omega$  resistor to R2577 while leave the position of R2584 empty. The board is booted by TF card.

### **4.3 DDR**

Callisto hardware board is equipped with a MT41K128M16HA-125 DDR3 by Micron or a chip by Etron. The size of RAM is 256 MB. The DDR3 is connected to the ports of PS DDR controller.

### **4.4 NAND Flash**

Callisto hardware board is equipped with 256 MB SLC NAND Flash. The model of the NAND flash is W20N01HISV. The NAND flash is used to store data by the SpaceChain OS.

### **4.5 TF card**

Callisto hardware board is equipped with a 16 GB TF card. The image files of Dual-OS have already been imported to the TF card. The TF card also serves as the system disk for Linux OS, and saves user applications and data.

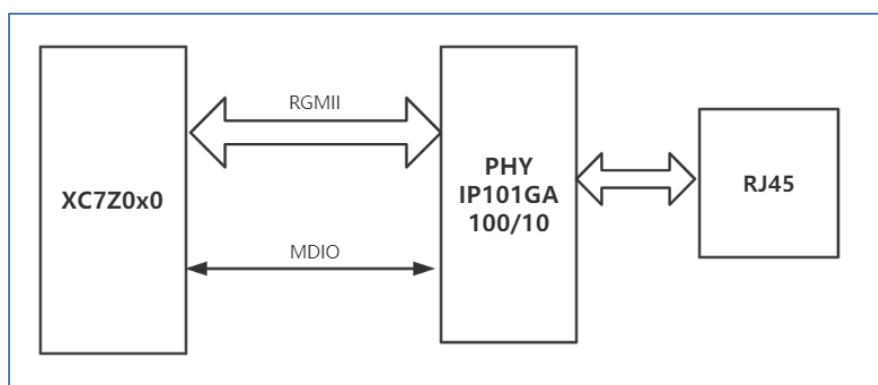
### **4.6 UART-TTY port**

Callisto board is equipped with a UART port which is used for showing messages of Linux and UBoot. Users can use TTY to access the Linux OS by connecting the board with a computer via the USB-C port located at the side of protection board.



#### 4.7 Ethernet

The PS of Zynq-7000 SoC contained two MAC layers of gigabit ethernet. To achieve ethernet communication, Callisto hardware board employs IP101GA as the PHY. In addition, RGMII is used for fast ethernet.



As shown in the below figure, two LEDs have to be lit after the hardware board is successfully connected to the WIFI router.



## 4.8 PL peripherals

Zynq7010 is also equipped with FPGA functions. Users can configure various IP cores , and multi-UART, I2C and CAN controller with FPGA. Please leave your feedback on our GitHub if you are interested in developing FPGA functions with our board.

## 5. Software introduction

### 5.1 Linux software introduction

| Item                | Name                                | Note  |
|---------------------|-------------------------------------|---|
| <b>Tool chains</b>  | arm-linux-gnueabi-hf-gcc            | Download link:<br><a href="https://releases.linaro.org/components/toolchain/binaries/latest-5/arm-linux-gnueabi-hf/">https://releases.linaro.org/components/toolchain/binaries/latest-5/arm-linux-gnueabi-hf/</a> |
| <b>Linux Kernel</b> | Linux 4.14-xlnx-rebase2018.3        | Linux kernel for Dual-OS:<br><a href="https://github.com/Xilinx/linux-xlnx/releases/tag/xlnx_rebase_v4.14_2018.3">https://github.com/Xilinx/linux-xlnx/releases/tag/xlnx_rebase_v4.14_2018.3</a>                  |
| <b>rootfs</b>       | ArchLinux OS image files in TF card | <a href="https://drive.google.com/file/d/1nZVEweYjDNeGtfk2_5h3RNRBrIul3ZHW/view?usp=sharing">https://drive.google.com/file/d/1nZVEweYjDNeGtfk2_5h3RNRBrIul3ZHW/view?usp=sharing</a>                               |

Please refer to the SpaceChain GitHub homepage for more resources.

<https://github.com/spacechain/SpaceChain-Board>

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## 6. Burn OS image files

### 6.1 Hardware preparation

SpaceChain Callisto uses a TF card to burn the system and save data. The below shows the procedures of copying image files to the TF card.

We need the following items: personal computer, SpaceChain Callisto board, Type-C cable, TF card and TF card reader.



### 6.2 Download deployment files

- Baidu Wangpan  
<https://pan.baidu.com/s/1XI8IFhMVNRZ-UEwwza5Byw>  
Password: wjec
- Google Driver  
[https://drive.google.com/file/d/1nZVEweYjDNeGtfk2\\_5h3RNRBrlul3ZHW/view?usp=sharing](https://drive.google.com/file/d/1nZVEweYjDNeGtfk2_5h3RNRBrlul3ZHW/view?usp=sharing)

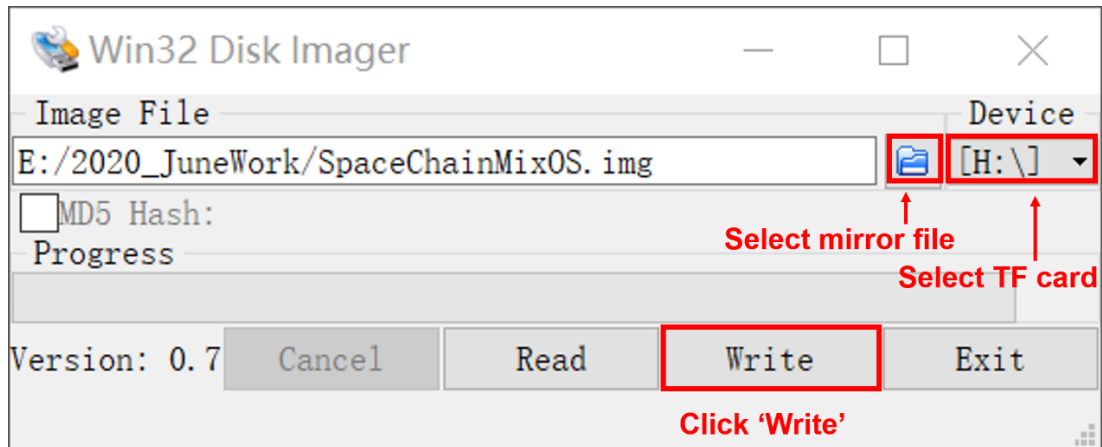
### 6.3 Copy OS mirror file to TF card

Note: we recommend formatting the TF card before copying the mirror files.

Download Win32DiskImager from the below link.

[https://sourceforge.net/projects/win32diskimager/?source=typ\\_redirect](https://sourceforge.net/projects/win32diskimager/?source=typ_redirect)

Open Win32DiskImager, select the mirror files, Choose TF card as the file location, and click 'write'.



#### 6.4 Boot the hardware board

Insert the TF card into the SpaceChain hardware board.

Connect the hardware board with the computer by a Type-C cable. If both red and green LED are on, the system is successfully initialized.



#### 6.5 Log in the hardware board by TTY

The Type-C cable provides both power connections and TTY function to the hardware board. The driver is CH340 chip. If your Win10 computer is unable to automatically install the driver, please download the driver the below link and install the driver properly.

*CH340 Windows version driver*

Link: [http://www.wch.cn/download/CH341SER\\_EXE.html](http://www.wch.cn/download/CH341SER_EXE.html)

*CH340 Linux version driver*

Link: [http://www.wch.cn/download/CH341SER\\_EXE.html](http://www.wch.cn/download/CH341SER_EXE.html)

*CH340 MacOS version driver*

Link: [http://www.wch.cn/download/CH341SER\\_MAC\\_ZIP.html](http://www.wch.cn/download/CH341SER_MAC_ZIP.html)



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We recommend using MobaXterm for TTY related functions. Please download MobaXterm from the below address.

<https://mobaxterm.mobatek.net/download.html>

Install the free version.

Open MobaXterm and select the serial port number of SpaceChain hardware board.  
The Baud rate is 115200.