# MICROPROCESSOR TECHNOLOGY AND SINGLE EVENT UPSET SUSCEPTIBILITY

L.D. Akers
University of Colorado
Colorado Springs, Colorado

## Abstract

Today's small satellites employ powerful microcircuits to control virtually every aspect of the spacecraft. While these small devices are very capable, they are increasingly vulnerable to heavy ion induced Single Event Upset (SEU). Current technology is not very susceptible to SEUs. The evolution of microdevices is toward lower power and higher speed while spacecraft evolve toward smaller and lighter structures. This combination, along with the increased heavy ion particle fluence associated with large solar flares, will cause tomorrow's microdevices to experience SEU at rates approaching 100 upsets per device per day! To ensure mission success, these small satellites must consider implementing one or more SEU mitigation techniques.

## Introduction

Cosmic radiation is composed of both galactic cosmic rays and solar cosmic rays. Galactic cosmic rays are high energy nuclei that propagate through intergalactic space. These particles may originate from stars both within and outside of the Milky Way Galaxy. Solar cosmic rays are high energy particles that originate from our own Sun. Galactic cosmic radiation is most intense during solar minimum while solar cosmic radiation is most intense at solar maximum[1]. SEUs from galactic and solar cosmic radiation can cause many undesirable effects, including[1]: damage to data in memory, damage to software, halting the Central Processing Unit (CPU), writing over critical data tables, and unplanned events including loss of mission.

Some effects of SEUs are easy to correct. Data stored in memory can often be recreated via software re-execution or reading from hardened memory. Volatile software can be reloaded through ground commands, but hard errors in a software storage location may permanently corrupt the software. A halted CPU cycle causes lost operation time, which can have detrimental effects on attitude control or mission data gathering. Some corrupted critical data tables can be recreated, but others may be permanently damaged and can cause serious operational impacts. Anomalies resulting from SEUs can cause flight software to be executed at the wrong time, components to be commanded on or off, or the mission to be unexpectedly terminated.

## Single Event Upsets

In recent years, spacecraft have experienced "bit flips" in memory and processing devices. These state changes are most frequently attributed to the ionizing radiation of a single energetic particle, thus the name Single Event Upset. Galactic and solar cosmic rays composed of nuclei from heavy ions, are most frequently the cause of single event phenomena. When an ionizing particle passes through the depletion region of a semiconductor circuit, the particle deposits charge along its path. The deposited charge is swept up by the electric field in the depletion region and results in a short current pulse in the circuit. If that pulse is large enough and lasts long enough, the feedback will cause a change in the final state of the circuit. This is interpreted by the rest of the electronics as a "bit-flip" because the memory location now reads the opposite of what it did before the particle transit.

Charge deposited in a semiconductor device affects different technologies in different ways, but the net result is an upset of the device causing performance degradation[2]. Flip-flop circuits change logic states when an ionizing particle deposits sufficient charge in the depletion region. For bipolar transistors, ionizing radiation causes a conducting path from the base to the emitter which directs

base current away from the main base current path, resulting in a loss of gain of the transistor. Ionizing radiation affects Junction Field Effect Transistors (JFETs) by increasing the gate to channel leakage current and contributing to noise currents.

SEUs in all types of microprocessor technologies were first predicted in 1962 by Walmark and Marcus[3]. They examined the evolution of microcircuits and predicted that smaller devices of the future would be vulnerable to upset. Because the work was ahead of its time, spacecraft designers ignored the prediction. In 1975, Binder, Smith, and Holman[4] published a paper in which they identified upsets in flip-flop circuits in space using a scanning electron microscope to simulate the ionization caused by iron nuclei. Again, designers ignored the research. Not until upsets due to cosmic rays were seen on GPS spacecraft in 1978 did designers take note[5]. Since that time, SEUs have been observed on nearly all spacecraft.

## Technology Development

The commercialization of space has led spacecraft manufacturers to faster, smaller, cheaper, and more capable spacecraft. Today's spacecraft employ less shielding and faster, smaller microprocessors. While this trend provides more powerful, less expensive spacecraft, it leaves them more susceptible to SEU. Spacecraft microprocessors and memory devices of the early 1970's were large, power consuming devices with limited computing power. With critical charges (minimum charge required to change logic states) as high as fifty to one hundred picocoulombs, these processors had performance drawbacks, but they were well suited for survival in the space environment. As processors evolve toward lower power and faster speed, they allow spacecraft to execute more sophisticated and powerful software with minimal power requirements. This increased performance is possible only through reducing the size of the chip and the amount of charge required to store information. Today's typical processors have a critical charge between three and ten picocoulombs. Figure 1[6] illustrates this evolution in memory and microprocessors. The y axis represents the energy required to operate the device, and the x axis is the particle energy threshold for SEU effects. A similar diagram was used by the Galileo project engineers to show NASA why single event upsets were a design consideration for Galileo and not for Voyager. The Galileo program wanted to estimate, based on previous component performance, where technology was leading with respect to SEU hardness.

Early Complementary Metal Oxide Semiconductor (CMOS) technology was not susceptible to SEU because the devices were large and had high critical charges. As the P-channel Metal Oxide Semiconductor (PMOS), Large Scale Integration (LSI), and Integrated Injection Logic (IIL) technologies were developed, SEU susceptibility increased. The lower critical charges of these devices left them vulnerable to the more prevalent lower energy cosmic rays.

One of the most important factors in determining the SEU rate is the feature size. The smaller the processor size, the faster the processing speed, and the lower power required to maintain or change data in the memory. Processor size can be related to the critical charge, $Q_c$, by:

$$Q_c = 0.023 * L^2 \quad (1)$$

where L is the longest pathlength through the vulnerable cross section. Although actual critical charge and device size must be determined experimentally, this approximation is sufficient for most SEU calculation applications. The critical charge for various depletion depths is plotted in Figure 2[6]. As the device depth decreases, the critical charge also decreases. The equation for $Q_c$ holds true for many types of devices, including CMOS, N channel Metal Oxide Semiconductor (NMOS), and IIL. This analysis uses this relationship to demonstrate the increasing SEU vulnerability of smaller cross section devices.

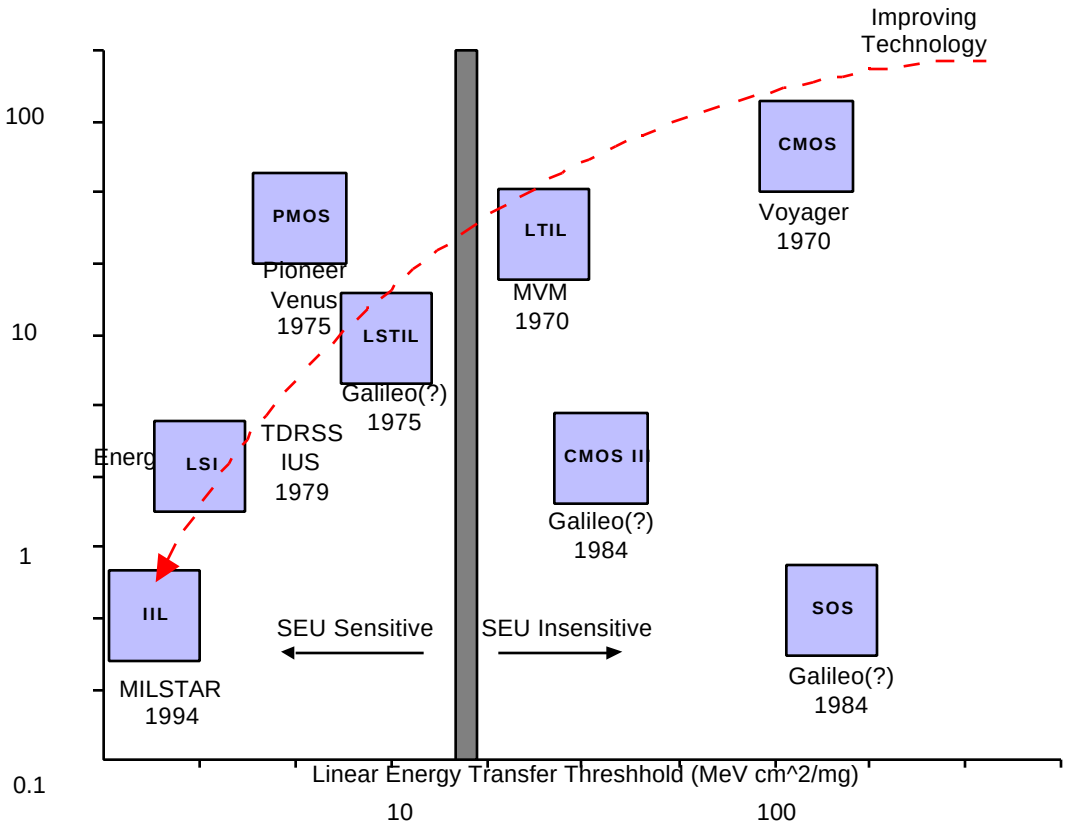


**Figure 1: Technology Development**

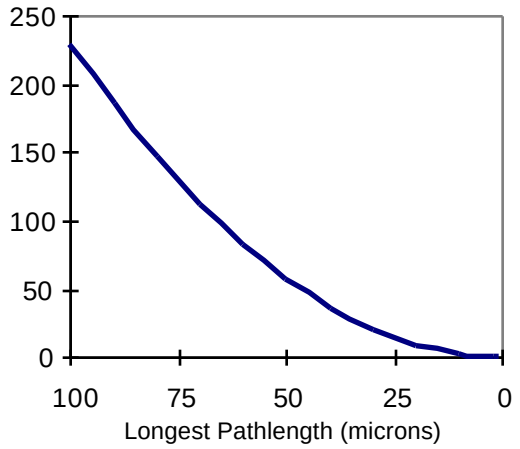


**Figure 2: Critical Charge vs. Device Size**

As a device's critical charge decreases, the circuit can be upset by the more prevalent lower energy cosmic rays which can have energies ranging from nearly 0 to over 20 GeV. The combination of the lower critical charge and the higher particle flux (as energy decreases) makes the smaller processors more susceptible to SEU.

When a cosmic ray particle travels through a device, it loses energy through ionization. Linear Energy Transfer (LET) is the term used to describe the energy depositing capability of the incident particle. It is a convenient metric for calculation because it allows the use of one number to characterize the energies of all ion species. LET is expressed in terms of the energy lost (dE) by the particle in traveling a distance (dx). Typically, LET is divided by the density of the target material, so that it becomes

$$LET = \frac{1}{\rho}\frac{dE}{dx}. \qquad (2)$$

Units are MeV cm$^2$/mg. LET can be related to the charge deposited by the relationship:

$$LET = \frac{225Q}{D\rho} \qquad (3)$$

The particle's pathlength, D, in the target material is measured in centimeters. The charge, Q, (in picocoulombs) is deposited by the particle as it moves through the device. The constant 22.5 is required in the conversion from picocoulombs to electron volts.

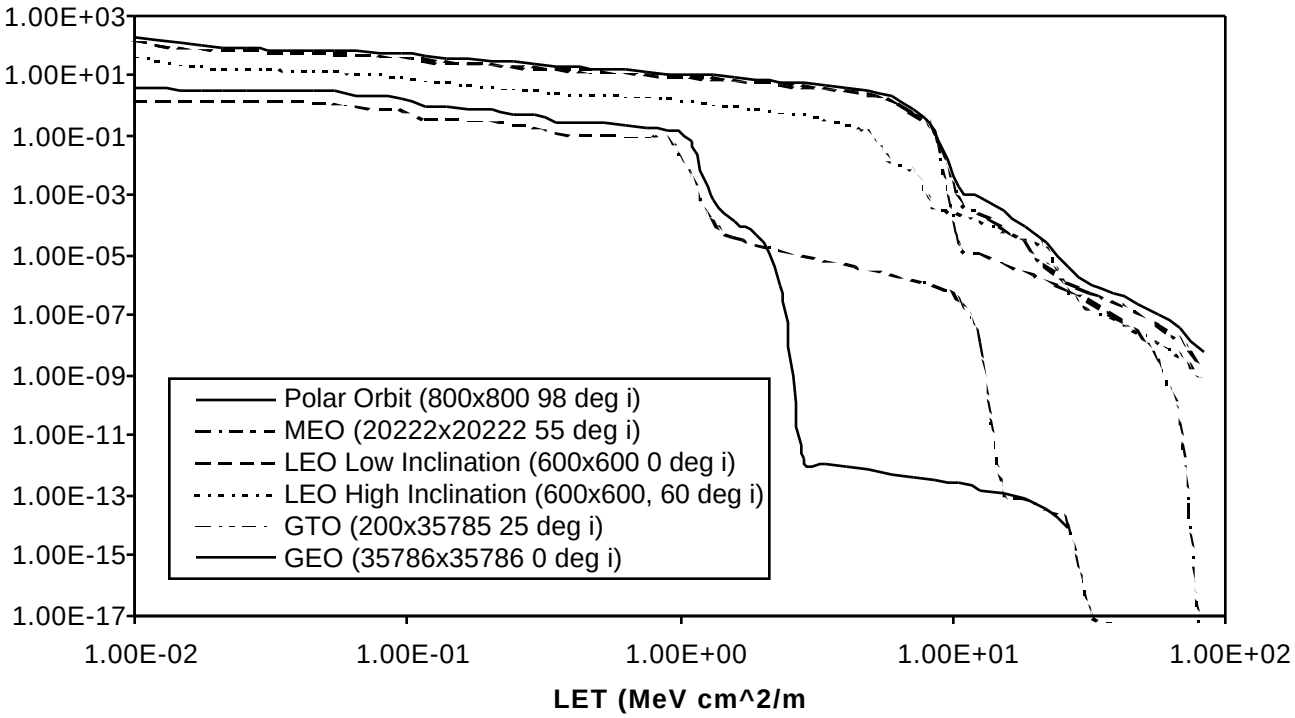


**Figure 3: Solar Minimum LET Spectrum**

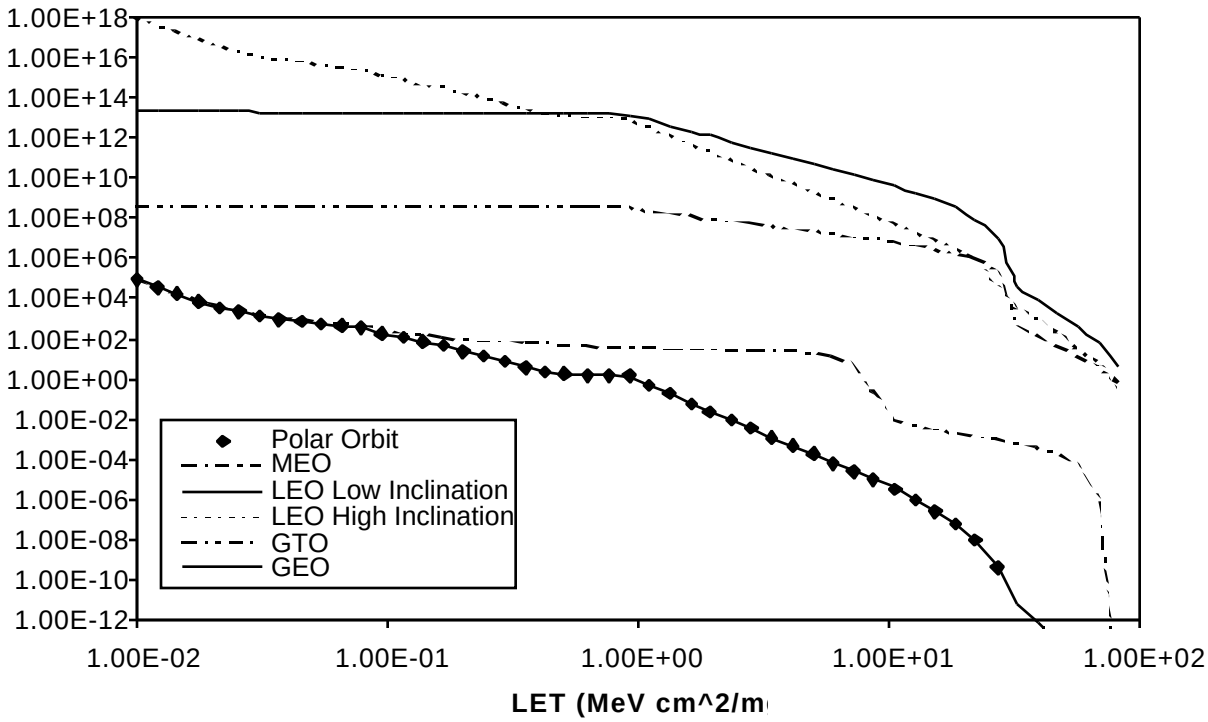


**Figure 4: Solar Flare Environment LET Spectrum**

To show the particle fluence for a given orbit under a specified solar condition, researchers commonly use the integral LET spectrum plot. Figure 3 shows the LET spectrum for various orbits during solar minimum. The high altitude and/or high inclination orbits are exposed to the greatest cosmic ray fluence because of decreased geomagnetic shielding effects. During periods of intense solar activity, the cosmic ray fluence can be much greater. The particle conditions after the March 1991 X9 level solar flare were enhanced by as much as $10^6$ times. This particle fluence (a worst case scenario) is shown in Figure 4. This analysis focuses on the geosynchronous orbit because it presents the overall greatest risk to spacecraft microelectronics.

Single event upsets are not limited to "bit flips." Five levels of single event effects (SEE) can impair circuit performance. An SEU is the most benign of the SEEs. It is caused by a particle capable of depositing charge equal to or greater than the device's critical charge. The LET of these particles is called the threshold LET, and is defined as:

$$LET = \frac{225 Q_c}{D\rho} \qquad (4)$$

where $Q_c$ is the circuit's critical charge and D is the longest pathlength through the device. As the particle energy increases, the particle becomes more likely to cause a more severe SEE, possibly resulting in a circuit failure. Table 1[7] shows the five types of SEE, in order of increasing severity.

**Table 1: Single Event Effects**

| Single Event Effect Type | Circuit Response |
|---|---|
| Single Event Upset | A change of state or transient induced by an energetic particle such as a cosmic ray |
| Single Hard Error | An SEU that causes a permanent change to the operation of a device (a stuck memory bit) |
| Single Event Latchup | A condition that causes the loss of device functionality due to a single event induced high current state. May or may not cause permanent failure, but requires power strobing to return to normal operations |
| Single Event Burnout | A condition which can cause device destruction due to a high current state in a power transistor |
| Single Event Gate Rupture | A single ion induced condition in power MOSFETs that may result in the formation of a conducting path in the gate oxide. |

A decrease in threshold LET increases the device susceptibility to all types of SEE. Because the particle flux decreases with increasing energy, the probability of more severe SEEs is lower than that of SEUs. Only the susceptibility of SEU is addressed in this study, since an increased SEU rate implies an increased rate of other single event effects.

## Upset Rate Calculation

The algorithm used in this analysis is based on Dr. James Adams' Cosmic Ray Effects on Microelectronics (CREME)[8] model and the CRRES/SPACERAD Heavy Ion Model of the Environment (CHIME)[9] model developed jointly by Lockheed Palo Alto, Louisiana State University, and the University of Chicago. The CREME model was developed in 1986 and forms the basis of the upset rate calculation. The CHIME model provides updated LET spectra information based on new measurements of the cosmic ray environment. Recent advances in the knowledge of the space radiation environment showed the CREME model to overestimate the particle fluence in many environments. This contributed to a corresponding overestimation of upset rates.

The upset rate for a microprocessor may be calculated by evaluating an integral containing the target size (cross section), the pathlength distribution through the sensitive region, the ion distribution as a function of LET and spatial parameters, and the device's critical charge. The function is:

$$rate = \sum_{z=1}^{92} \int_0^{2\pi} d\phi \int_0^{\pi} d\theta \int_{E1}^{E2} dE f_z(E,\theta,\phi)\sigma(E,\theta,\phi) \cdot \quad (5)$$

The summation is over all ion species and the integration is over all angles and energies. The flux, $f_z(E,\theta,\varphi)$, is the number of particles of energy E, atomic number z, and moving in the direction indicated by the angles $\varphi$ and $\theta$. The cross section is defined by $\sigma(E,\theta,\varphi)$, and represents the probability that a particle in the given direction with energy, E, will cause an upset. This function can be greatly simplified by the following assumptions[6]: (1) the vulnerable cross section is defined as a function of LET rather that energy and (2) the sensitive region is modeled as a rectangular parallelepiped. The first assumption eliminates the need to sum over ion species and integrate over all energies. The second assumption allows the use of Bradford's[10] pathlength distribution and eliminates the need to integrate over all angles. The resulting equation is:

$$rate = 225\pi\sigma Q_{crit} \int_{\frac{225Q_{crit}}{d_{max}}}^{L_{max}} D(d(L))\, flux(let > L_0) \frac{dL}{L^2} \quad (6)$$

The term D(d(L)) represents the pathlength distribution probability function, flux(let>$L_0$) is the particle flux, $Q_{crit}$ is the circuit's critical charge. The constant is the same as in equation 3. This equation is integrated over the portion of the LET spectrum able to cause upset in the device.

The rate equation yields results of upsets per bit per second. Each bit must be analyzed separately, as different storage areas in the same microprocessor may have different vulnerable cross sections, and the total device upset rate may not be as simple as the upset rate per bit per day times the number of bits.

A weighting factor may be required to compensate for the different upset rates across the microprocessor. For example, the Texas Instruments SBP9989[6] processor has two different vulnerable cross sections. The first section, which contains 70% of the bits is sized at 10x10x1.8 microns per bit. The remaining 30% of the vulnerable cross section is composed of 15% each 100x10x1.8 and 1x1x1.8 microns per bit.

## Model Results

The five microprocessors used in this analysis represent technologies currently on orbit and future developments. Current technology has depletion depths of 2 microns and below. Designers estimate that future technology could have depletion region depths of 0.1 to 0.2 microns[12]. The processor dimensions are for each bit, not the entire device. The five devices are summarized in Table 2. Figure 5 shows the increase in upset rate as device size decreases.

**Table 2: Device Summary**

| Dimensions (microns) | Cross Section (micron$^2$) | Critical Charge (picocoulombs) | $LET_{th}$ (MeV cm$^2$/mg) |
|---|---|---|---|
| 20x20x2 | 960.00 | 18.492 | 6.300 |
| 20x20x1 | 880.00 | 18.423 | 6.289 |
| 15x15x0.5 | 480.00 | 10.356 | 4.715 |
| 10x10x0.2 | 208.00 | 4.061 | 3.142 |
| 5x5x0.1 | 52.00 | 1.150 | 1.571 |

The rates shown in Figure 5 are small; the highest rate converts to more than $3.5x10^{11}$ years between upsets. Although the galactic cosmic ray environment is more dangerous during solar minimum, the upset danger is not as significant as during solar maximum.

With solar minimum expected in 1997, and solar maximum ramping up quickly in the following five years, spacecraft launched today will be subjected to the much more violent particle environment associated with solar flares. A single solar flare can increase the near earth particle fluence by as much as 100,000 times (Mar '91 Flare). The increased particle flux can have a dramatic impact on SEU rates. In a solar flare environment of this magnitude, a microprocessor can experience as many as 0.7 upsets per bit per day. With typical devices having between 100 and 500 sensitive bits, these devices can see 70 to 350 upsets per day. The high upset rate frequency can have a crippling effect on satellite operations.

The March '91 flare represents a severe enhancement of heavy ion fluences. Flares of this magnitude are not common, but large ($10^3$-$10^4$ times enhancement) can occur on an average of once a month. These flares can enhance the near earth particle environment for a period lasting from several hours to several days. Figure 6 shows the upset rates for the five processors in the Mar '91 flare environment. These rates follow the same trend as for a solar minimum environment, but the upset rates are approximately $10^{12}$ times higher.

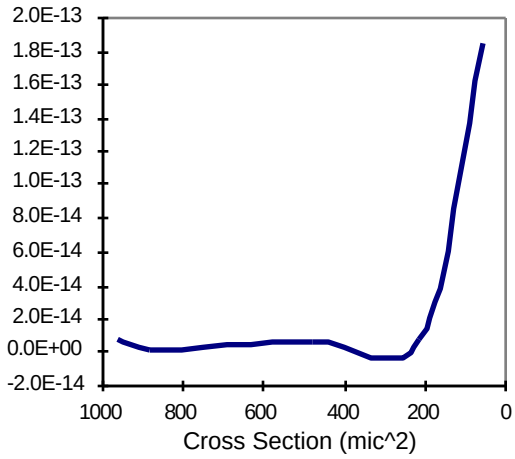


**Figure 5: Upset Rate Vs Device Size (GEO)**

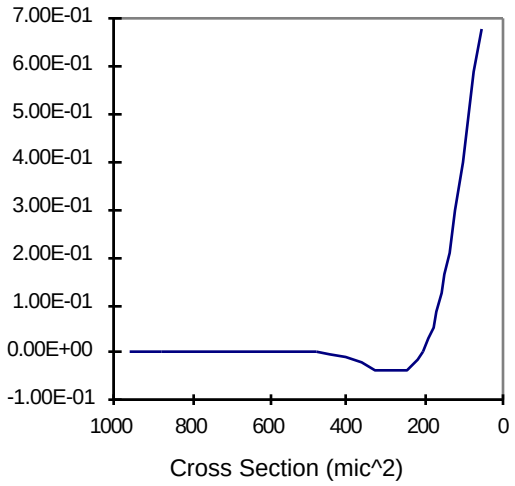


**Figure 6: Upset Rate for Flare**

Actual Device Data

Small satellite programs frequently use the Intel 80x86 family and the R3000 processors. These processors are vulnerable to the cosmic ray environment in varying degrees. Table 3 shows the device parameters such as cross section and critical charge. Figure 7 shows a plot of the upset rates for six typical orbits under both solar minimum and solar flare conditions. Although the readily available technology has not reached the depletion depths and critical charge levels of the representative devices in this study, they are still very susceptible to upset from cosmic rays.

**Table 3: Actual Device Parameters**

| Device/ Manufacturer | Cross Section ($\mu^2$) per bit | Critical Charge (pC) | $LET_{th}$ (MeV $cm^2/mg$) |
|---|---|---|---|
| 8086 / Intel | 600 | 7.186 | 3 |
| 80C86 / Intel | 10000 | 49.630 | 5 |
| 80C186 / Harris | 200 | 11.959 | 9 |
| 80C286 / Harris | 150 | 13.613 | 12 |
| 80386DX / Intel | 100 | 5.430 | 6 |
| 80486DX2 / Intel | 100 | 7.604 | 5 |
| R3000 / LSI | 300 | 4.967 | 3 |
| R3000A / LSI | 100 | 7.624 | 8 |

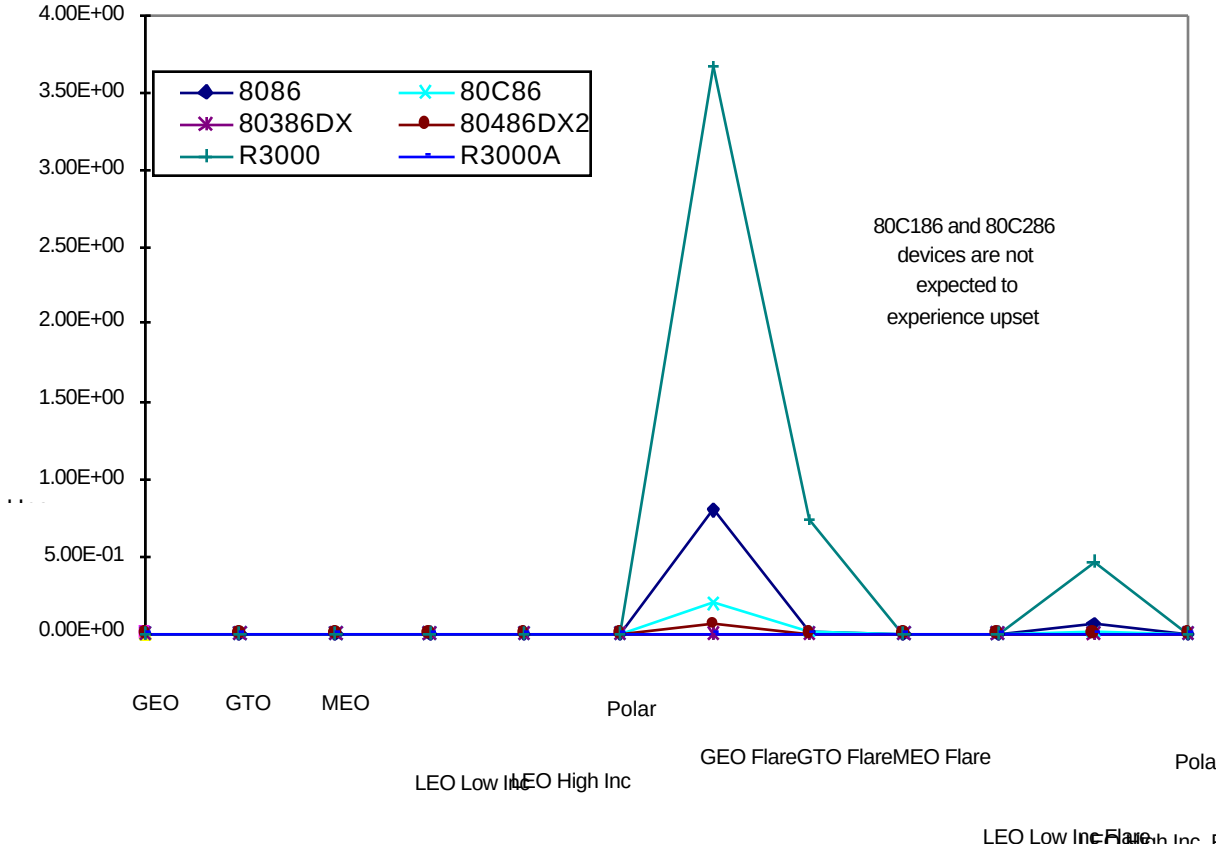


**Figure 7: Actual Device Upset Rates**

## Model Limitations

An important limitation of this model is the requirement to input the dimensions of the vulnerable cross section. In many cases, the cross section can be computed through testing, but the length, width, and depth[12] of the region often cannot be accurately measured. By estimating these values, the probability distribution of chord lengths through the sensitive region can be miscalculated, resulting in false answers. An underestimated depletion depth will result in a higher estimate of the upset rate, while an overestimated depth yields a lower than actual upset rate. The rate calculation is not as sensitive to the length/width ratio, but the sensitivity of the device depends heavily on the thickness[12].

Another limitation is in the rate calculation itself. Adams' CREME model calculates the upset rates for silicon devices only. Semiconductor technology is beginning to use other materials such as GaAs. The material density is an important input to the upset rate model, and calculations for these devices require use of another model for accurate results. The Chenette[11] upset rate model includes a user input option for semiconductor material density.

A third limitation deals with the modeling of the LET spectrum. This analysis models the LET spectra as a step rather than continuous function. The LET spectrum in this analysis used 50 steps between 0.03 and 100 MeV $cm^2/mg$, while the CREME model uses 1000. The increase in LET model accuracy improves the model's prediction capability, but makes the calculation more complex and time consuming. For the most sensitive processor in the study (0.1 micron depth), the upset rate calculated with 100 steps was identical

to the 50 step value to three significant digits. A further limitation of the model is a function of the LET spectrum. According to Adams, the SEU rate calculation tends to be less accurate right below a ledge in the LET spectrum[8]. The rates calculated from these spectra will tend to be more conservative (higher) than actual data. Using multiple prediction methods to calculate SEU rates will help alleviate this inaccuracy.

Mitigation Techniques and Applications

With upset rates as high as 350 per day, designers require a method to mitigate the potentially crippling effects of SEUs. The simplest method is through mass shielding. Increasing the shield thickness around a microprocessor decreases the number of cosmic ray particles that can reach the chip. Only the most energetic particles can actually penetrate the shielding and cause upset. While this method is simple, the additional shielding greatly increases the weight of the spacecraft and can actually increase the rate at which the penetrating high energy particles upset the circuit. Since high energy particles move through interplanetary space at near relativistic speeds, they may not possess sufficient LET to upset a circuit. If these particles are slowed down by a shield, they can deposit more charge per unit time in the depletion region, thus increasing the upset rate.

To protect against SEU effects without shielding, many designers are including software to detect and correct SEU caused errors. A common form for Error Detecting and Correcting (EDAC) code uses a parity checking and memory scrubbing routine to determine if errors occurred, and reads recovery information from a radiation hardened memory location. EDAC code uses parity checks to detect memory errors. If the memory cache is corrupted, the information is re-read from another source, or the CPU is halted and restarted from scratch. Memory scrubbing is a process where all memory locations are accessed and any single bit errors corrected. An SEU rate of one upset every $10^8$ seconds (3.17 years) requires a memory scrub every 0.1 seconds[13]. This scrubbing frequency can have a significant impact on flight software execution because it detracts from the processing time for flight software.

Hardware modifications eliminate many of the problems associated with software error detection and correction. High fault protection can be obtained using a technique known as “lockstepping.” Two processors operate simultaneously, executing identical code, and the software compares the outputs. If there is a discrepancy, the cycle is halted and the software re-executed. The two processors must execute at exactly the same clock speed. This requires a

**Table 4: SEU Mitigation Techniques**

| Technique | Software Impact | Performance Degradation | Physical Modification/Cost | Fault Coverage |
|---|---|---|---|---|
| Shielding | None | None | Weight increased, launch costs | Fair to poor |
| Software Checking | Extreme, bug prone | Moderate | None. Long software development | Poor |
| Lockstep CPUs | Checkpointing required | None | Two CPUs. Moderate Cost | Very high |
| Redundant CPUs | Voting and control handling | None | More hardware | Very high |
| Radiation Hardening | Possibly none | Small | Extreme costs. Custom design | High |

phasing/synchronizing system either on the chip or in external circuitry. To avoid the costly synchronization problems, some designers are implementing redundant CPUs with a voting logic design. In this technique, the outputs of multiple CPUs are compared and the output receiving the majority vote is implemented. This technique usually employs three CPUs.

As technology improves, radiation hardening becomes a more viable option. Hardening significantly increases the cost of the chip, but has a high probability of mitigating and eliminating SEU effects. The most common technique for radiation hardening is to modify the chip's construction by adding layers of radiation hardened materials. This technology is still in development and not yet widely available. As processors decrease in size, critical charge, and upset threshold, radiation hardening may become the only reasonable solution to the SEU problem. Table 4 compares various SEU detection and correction techniques based on cost, impact, and protection[13].

Many commercial and research projects are moving toward smallsat technologies. NASA's smallsat initiatives have recognized the need for high capacity, low power, low cost, radiation hardened memories and processors[14]. As designers select fast processors with minimal shielding, operators will see an increase in the number of single event effects. An accurate SEU rate prediction program allows the designers to include mitigation techniques in the design before the operators become overwhelmed with SEE recovery.

SEU predictions can help optimize spacecraft design in several areas. Some of the areas to consider include[15]:

- Design requirements/specification
- Selection of orbit parameters
- Design concept trade offs
- Semiconductor parts selection
- Evaluation of shielding protection
- Prediction of upset rates
- Selection of upset recovery techniques
- Calculation of system performance
- Qualification and acceptance tests
- Anomaly resolution and investigation

Based on this list, SEU prediction techniques have applicability in all aspects of mission design--from early concepts through mission operations to end of life. Many of the design areas can have a significant impact on the overall design. Orbit selection can drive sensor choices; shielding levels may impact launch vehicle selection, propulsion subsystem design, and attitude control subsystem design. Mission operations design must consider the effectiveness of mitigation techniques and the difficulty of recovery techniques when determining command and control system and staff requirements. SEU rate prediction can help designers best select components and optimize spacecraft performance. Anomalies can often be resolved faster if the operators know and understand the spacecraft's vulnerability to space environmental effects.

## Conclusion

Advances in microprocessor technology provide spacecraft with faster processing of more sophisticated software, but as speed increases, SEU vulnerability also increases. As chips get smaller, their critical charge and SEU threshold decrease. This decrease makes the chip vulnerable to SEU causing ionization from more prevalent lower energy cosmic rays. Designers need an accurate method to estimate the rate of cosmic ray induced upsets. The upset rate is a function of both the particle environment and the chip's critical charge. If the particle environment intensifies or the critical charge decreases, the chip becomes more susceptible to SEU. The higher upset rates associated with newer technology can cause spacecraft to spend as much or more time recovering from upset than executing flight software. This analysis provides an accurate and valid calculation of upset rates for various microprocessor technologies so that spacecraft designers can include the effects of the cosmic ray environment during the entire design process

as ionizing cosmic radiation can be crippling to mission operations.

The calculations for SEU rates are complex and component parameters are frequently unavailable. In most cases, the size of the vulnerable cross section and the critical charge must be determined experimentally. Ground based cyclotron testing is expensive and the waiting lists are often lengthy. Methods used to calculate the upset rate vary widely and each produces slightly different results. The best way to get accurate SEU rate data is to use historical flight data or ground test data. Many devices are catalogued by NASA's Jet Propulsion Lab and can be found on the World Wide Web at URL http://radnet.jpl.nasa.gov/.

Although this research identified electronic component vulnerabilities to heavy ion induced SEU, a host of other space environmental effects may cause small devices to upset. High energy protons emitted during solar flares or coronal mass ejections can cause similar types of upsets. Spacecraft charging can result in discharges through electronic circuits. The Van Allen radiation belts are home to high energy electrons, protons, and ions. The NASA/SAMPEX program recently discovered a third radiation belt within the inner Van Allen belt containing oxygen, nitrogen, and neon ions (anomalous cosmic rays). These effects cannot be ignored in spacecraft design, but many can be reduced through effective mitigation techniques.

## References


[1] Davenport, G., Course Notes-ASE560, University of Colorado at Colorado Springs, June 1994

[2] Stephen, J.H., "Hazards to Electronics in Space," The Behavior of Systems in the Space Environment, Kluwer Academic Publishers, Netherlands, 1993, pp 407-435.

[3] Walmark, J.T. and S. M. Marcus, "Minimum Size and Maximum Packing Density of Non-Redundant Semi-Conductor Devices," Proceedings of the IRE, Mar 1962, p 286.

[4] Binder, D., E.C. Smith, A.B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," IEEE Transactions on Nuclear Science, NS-22, Dec 1975, pp 2675-80.

[5] Pickel, J.C., and J.T. Blandford, "Cosmic Ray Induced Errors in MOS Memory Cells," IEEE Transactions on Nuclear Science, NS-25, Dec 1978, pp 1166-71.

[6] Robinson, P., Spacecraft Environmental Anomalies Handbook, GL-TR-89-0222, AFGL, Hanscom AFB, MA, Aug 1989.

[7] "Single Event Effects Specification," Goddard Space Flight Center, World Wide Web URL: http://flick.gsfc.nasa.gov/seespec.htm/, 1993

[8] Adams, J.H. Jr., "Cosmic Ray Effects on Microelectronics, Part IV," Naval Research Lab., NRL Memorandum Rept-5901, Washington, D.C., Dec 1986.

[9] Chenette, D.L., J. Chen, E. Clayton, T.G. Guzik, J.P. Wefel, M. Garcia-Munoz, C. Lopate, K.R. Pyle, K.P. Ray, E.G. Mullen, D.A. Hardy, "The CRRES/SPACERAD Heavy Ion Model of the Environment (CHIME) for Cosmic Ray and Solar Particle Effects on Electronic and Biological Systems in Space," IEEE Transactions on Nuclear Science, NS-41, Dec 1994, pp 2332-39.

[10] Bradford, J.T., "A Distribution Function for Ion Track Lengths in Rectangular Volumes," Journal of Applied Physics, Vol 50, 1979.

[11] Chenette, D. L. T.L. Schumaker, and A.E. Williamson, "An Accurate and Efficient Method to Calculate the Rate of Single Event Upset from the LET Spectrum and SEU Cross Section Test Results," PL-TR-9202984, Phillips Laboratory, Air Force Systems Command, Hanscom AFB, MA, 1992.

[12] Petersen, E.L., J.C. Pickel, J.H. Adams, Jr., E.C. Smith, "Rate Prediction for Single Event Effects--A Critique," IEEE Transactions on Nuclear Science, NS-39, Dec 1992, pp 1577-99

[13] Kaschmitter, J.L., D.L. Shaeffer, N.J. Colella, "Operation of Commercial R3000 Processors in the Low Earth Orbit (LEO) Environment," IEEE Transactions on Nuclear Science, NS-38, Dec 1991, pp 1415-1420.

[14] Bruner, M.E., "Issues in Spacecraft Technology for Small Spacecraft," Proceedings of the First GSFC Conference on Small Satellites, http://www.gsfc.nasa.gov/c600/workshops/sws1_splinter2.html, 1995

[15] Cunningham, S.S., J.A. Banasiak, C.S. Von Flotow, "Living With Things that go Bump in the Night," AAS Paper 85-056, October 1985.

## Author Biography

The author is a 1992 graduate of the United States Air Force Academy (B.S. English) and a 1996 graduate of the University of Colorado (M.E. Space Operations). She is currently the Chief, Operations Training Section of the 50th Weather Squadron at Falcon AFB, CO. The squadron is the only DoD organization providing space environmental forecasts, warnings, and support to military users worldwide. Recently, she joined forces with the US Air Force Academy small satellite programs to provide the cadets and faculty with space environment impacts information for upcoming missions.