Miniaturized Data Processing Unit for Use on Small Satellites

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Abstract: High density packaging of non rad-hard commercial of the shelf (COTS) components combined with mission specific tailored shielding, error correcting codes and latchup current breakers provides a significant reduction in mass, volume, power and cost compared to the traditional approach using rad. hard components. A prototype development of a miniaturized Data Processing Unit (DPU) exhibits the potential of the approach. The traditional approach for the ROSETTA-OSIRIS DPU is taken as reference.

Introduction

Most today's space instruments rely on an individual DPU providing (1) sufficient computing power (e. g. 100 MIPS), (2) mission specific radiation tolerance, (3) low consumption of power, mass and volume and (4) adequate reliability at (5) moderate single unit costs.

Two contrary approaches are in use. The more traditional approach (a) uses radiation hardened parts of high quality level. This means, that the requirement on both radiation tolerance and reliability are met by a dedicated device technology, traceability of the fabrication process and by screening. The alternative approach (b) uses commercial of the shelf (COTS) components. It meets the requirements in radiation tolerance and reliability by structural provisions. Shielding, error correcting codes and latchup current breakers are applied for protection against radiation induced permanent failures and transient errors. H/W-redundancy as word extension for error correction codes, reconfigurable spares and majority voting are applied for achieving the required probability of survival and also in some cases for graceful degradation of the functional performance.

Apparently approach (a) supports a straight-forward DPU architecture. It minimizes the design costs at the expense of component costs. Besides the argument of cost balancing the questions remains, for which radiation environments approach (b) is competitive or even superior with respect to power, mass and volume.

Rad. hard components suffer from lower integration density, poorer performance and a very restricted parts spectrum compared to state of the art COTS. This leads to less attractive figures for power, volume and mass and provides a mass margin for shielding of the more compact COTS-electronics. Basically, the shielding mass drops with $(volume)^{2/3}$. Therefore, dense packing pays off. This is backed by the general trend to hand-held, battery-operated electronic equipment, which in turn nourishes the rapid progress in high-performance, small size, low power, non rad. hard devices. In contrast, the traditional backup for the development of rad. hard. devices by defense projects is dwindling.

Projecting the current trend into the future, we initiated the development of a prototype small-size COTS-DPU, which follows the structural protection approach and implements (i) the performance of the ROSETTA-OSIRIS-DPU, which is mainly directed to wavelet

image compression and (ii) compliance with the ROSETTA radiation environment at substantially more favourable figures of power, volume and costs.

Shielding

Figure 1 shows the radiation dose at the centre of an aluminum sphere for three representative mission scenarios: ROSETTA, CASSINI / SOLAR PROBE and GALILEO PROBE:
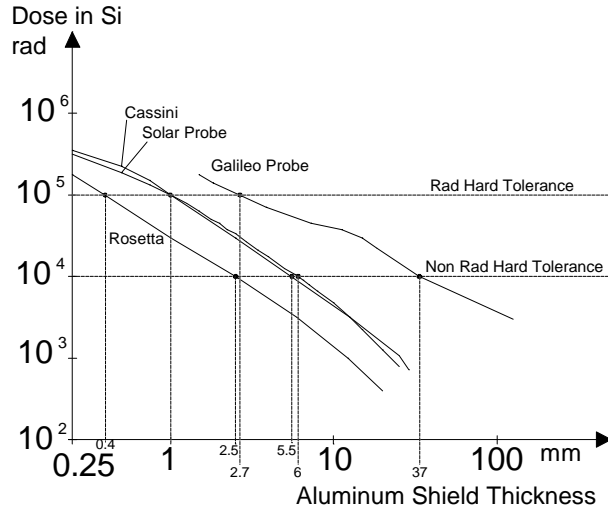

Figure 1: Radiation dose at the centre of an aluminum sphere for representative mission scenarios

Rad. hard. parts tolerate a total dose of 100krad typically and non rad. hard. parts 10krad, respectively. Table 1 shows the required shield thickness d for these three mission scenarios.

Mission	Shield Thickness rad. hard. Electronics d_{RH}	Shield Thickness non rad. hard. Electronics d_N
ROSETTA	0.4 mm	2.5 mm
SOLAR PROBE / CASSINI	1 mm	6 mm
GALILEO PROBE	2.7 mm	37 mm

Table 1: Shield Thickness for representative mission scenarios

The mass increase by the additional shielding should not consumes all the mass savings achieved by use of

COTS. Therefore, the total mass figures of both approaches have to be compared.

Mass Comparison: Rad Hard Components versus COTS plus Shielding

The mass m of the DPU is defined by the volume of the electronics V_E with mass density ρ_E plus the volume of the box V_B with mass density ρ_B:

$$m = V_E \bullet r_E + V_B \bullet r_B \qquad (1)$$

Rad. hard electronics occupy a substantially larger volume than COTS electronics. The lower integration density results in a larger device count, e.g. by a factor of 4 in case of memory devices. Further, hermetic chip packaging imposes in a substantially higher consumption of board area and of board spacing compared to small SMD plastic packages. Depending on the specific device spectrum the volume ratio between rad hard and COTS devices

$$C_v = \frac{V_{E,RH}}{V_{E,N}} \qquad (2)$$

varies between $C_v = 10 \ldots 200$.

The mass ratio between rad. hard- and COTS-electronics is:

$$C_m = \frac{m_{RH}}{m_N} = \frac{V_{E,RH} \bullet r_E + V_{B,RH} \bullet r_B}{V_{E,N} \bullet r_E + V_{B,N} \bullet r_B} \qquad (3)$$

The near optimum configuration of the electronics volume is a cube:

$$V_E = a_E^3 \qquad (4)$$

The volume of the box walls V_B increases with the shield thickness d:

$$V_B = \left(a_E + 2d \right)^3 - a_E^3 = \left(\sqrt[3]{V_E} + 2d \right)^3 - V_E \qquad (5)$$

The combination of the equations (2), (3) and (5) yields:

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$$C_m = \frac{V_{E,RH} \cdot \left(\mathbf{b} \mathbf{r}_E - r_B \mathbf{g} \mathbf{r}_B \cdot \mathbf{d} \sqrt{V_{E,RH}} + 2 d_{RH} \right)^3}{\dfrac{V_{E,RH}}{C_V} \cdot \left(\mathbf{b} \mathbf{r}_E - r_B \mathbf{g} \mathbf{r}_B \cdot \mathbf{G} \sqrt[3]{\dfrac{V_{E,RH}}{C_V}} + 2 d_N \right)^3} \quad (6)$$

Using the density $\rho_B = 2.7 \text{g/cm}^3$ for aluminum box walls and $\rho_E = 1.5 \text{g/cm}^3$ for densely packed electronics, equation (6) delivers the mass ratio C_m as depicted in Fig. 2 through Fig. 4 for three mission scenarios. Each figure shows the mass ratio C_m versus the box volume needed for the rad hard approach, with the volume ratio C_v as parameter. The three curve sets differ in the mission individual shield thickness d.

Of particular interest is that minimum volume of the rad. hard approach, for which a mass advantage ($C_m > 1$) can be achieved. For example, for the Rosetta mission and the extremely conservative volume ratio $C_v = 2$, the break-even point is at 40cm^3 of rad. hard electronics.
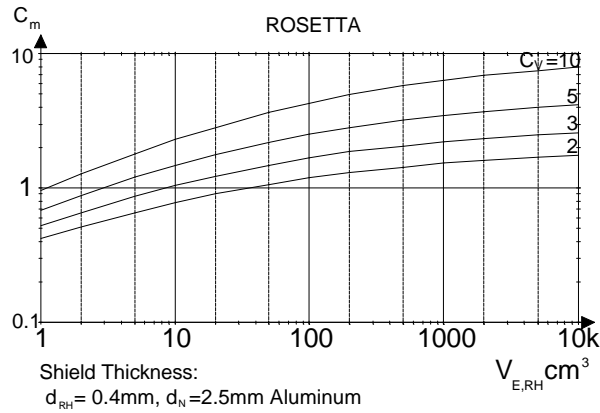

Figure 2 Mass ratio of rad. hard / non rad hard DPU for ROSETTA

Shield Thickness:
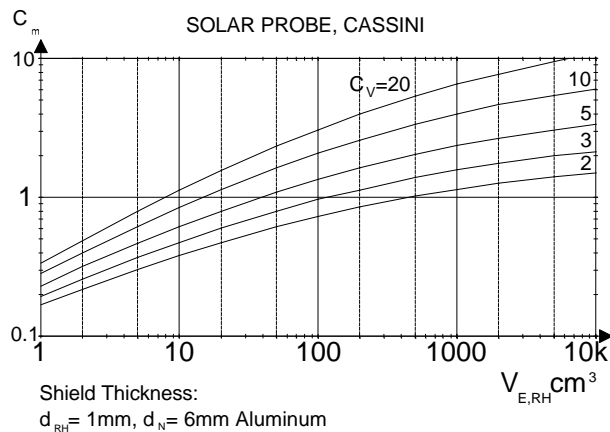$d_{RH} = 0.4 \text{mm}$, $d_N = 2.5 \text{mm}$ Aluminum

Figure 3 Mass ratio of rad. hard / non rad hard DPU for SOLAR PROBE and CASSINI
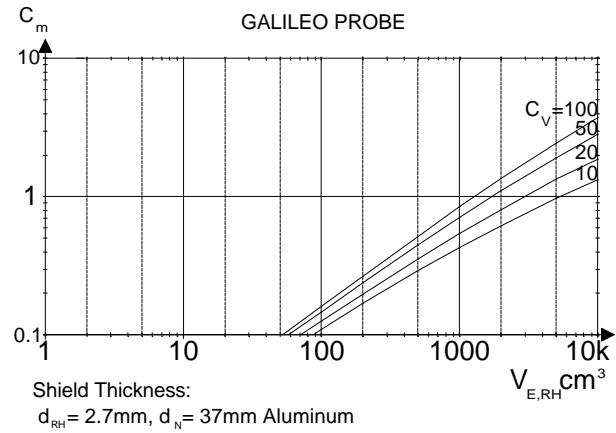
Figure 4 Mass ratio of rad. hard / non rad hard DPU for GALILEO PROBE

Shield Thickness:
$d_{RH} = 2.7 \text{mm}$, $d_N = 37 \text{mm}$ Aluminum

The curves in Fig. 2-4 stretch a wide and potentially unrealistic range of both parameters C_m and $V_{E,RH}$. Taking the OSIRIS DPU as an example, we address the question of the realistic parameter range (Table 2). The actually implemented version (#1) is a mixture of rad. hard electronics and one non-rad. hard mass memory board. Version #2 uses rad. hard parts for the memory, too. Version #3 improves the packaging of the all rad. hard electronics #2. Version #4 reflects the change-over to densely packed non rad. hard COTS electronics.

Shield Thickness:
$d_{RH} = 1 \text{mm}$, $d_N = 6 \text{mm}$ Aluminum

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#	DPU	size [mm*mm*mm]	Electronics volume V_F [cm^3]	Electronics mass m [g]	Electronics volume ratio C_v	Electronics density ρ [g/cm^3]
1	rad hard, except mass memory	190*190*100	3610	3450	58	0.96
2	all rad hard	190*190*288	10397	10000	167	0.96
3	all rad hard, high density packaging	190*190*190	6859	10000	110	1.46
4	all non-rad. hard COTS, high density pack.	38*38*43.2	62.4	100	1	1.6
5	all rad hard, Multi Chip Modules (MCM)	100*100*130	1300	2600	21	2.0

Table 2: Estimation of mass and volume of the ROSETTA-OSIRIS-DPU

Comparing against the COTS version #4 the volume ratio C_v varies between 58 and 167. Thus the even high ratio $C_v \approx 100$ is a first order approximate figure. The non-rad. hard. approach promises a gain in mass, even for the severe Galileo Probe environment (Fig. 4), and even more for the less demanding Rosetta environment (Fig 2).

Version #5 is a rough extrapolation of version #3 for using MCM-technology.[1,2] Even in this case we expect a volume drop by at least C_v=21. This means that even for the harsh Galileo Probe environment the COTS-approach reaches nearly the rad. hard approach.

So we conclude: COTS plus shielding offers a considerable alternative for moderate radiation environments and possibly even for harsh radiation environments as GALILEO PROBE.

Radiation Protection

Typically rad. hard components are characterized by (i) a tolerance dose of 100 krad and more, (ii) immunity against latchups (expressed by a threshold LET of minimum 50 MeVcm^2/mg) and (iii) in some cases a reduced sensitivity against Single Event Upsets (SEU) compared to their commercial counterparts. This means that no shielding and no LU protection circuitry are needed, and that the necessity of protection against SEU-induced faults is relaxed. All this simplifies and shortens the design work.

But, as shown before, the rad. hard approach is prone to end up in a weak compromise between a intolerable high mass figure and a drastic reduction of its functional performance. This is the incentive for looking at the COTS-alternative, despite its need for radiation characterization of COTS devices and its higher complexity of H/W and S/W. But, since the performance of rad. hard devices is falling behind that

of COTS more and more, the brute force straight on route becomes less and less viable and in turn the non rad. hard COTS approach becomes more prospective despite its higher complexity.

The radiation characteristic of COTS will be derived from published data as much as possible. But in most cases a residuum of parts with unknown radiation characteristic will remain. For these parts the tolerance dose and both the SEU and LU cross-section versus LET have to be determined by tests. Compared to tests for general devices use a simplification is possible. The monitored set of functions and parameters can be restricted to those which are relevant for the envisaged application. This is a decisive simplification for complex parts with their huge diversity of operational modes.

Total Dose
Having access to a suitable Co60 source and a device oriented monitoring equipment this test is rather easy. In-situ monitoring of the devices under test is preferable. Fault criterion is either degradation of functionality or an application dependent limit for the increase of the supply current. Most of current digital CMOS devices are qualified to 10 krad or higher. Basically the tolerance dose of MOS devices is improved by shrinking the on-chip structures and in contrast worsened by using lower supply voltages. So, one can expect, that these counteracting effects are nearly in balance and accordingly, that the trend to higher integration density will not affect the currently achieved total dose sensitivity of, typically better than 10 krad by much.

Single Event Tests
These tests create more problems, because they require access to proton and ion accelerators. Roughly a dozen of test runs with different ions have to be performed for a sufficient resolution of both SEU- and LU cross-

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section versus LET plots. Here, in-situ monitoring of the devices under test is mandatory.

Unfortunately, the easy to use Cf252 test gives no definitive answer. The high LET atomic nuclei fragments emitted from this solid particle source are stopped after app. 20µm. Therefore they do not reach structures situated deep under the chip surface (i.e. trench cells, base of stacked elements), which are coming in use more and more for exploiting the third integration dimension.

Knowing both cross-section versus LET and the LET spectrum of the mission dependent particle population the average frequency of SEU and LU occurrence can be calculated.

For the majority of current digital CMOS devices, particularly for those using epitaxial technology, typically no LU occurs during the limited test time. This raises some doubts, whether the device is LU-immune definitely or only very low sensitive.

Raising the particle fluence by extending the exposure time and/or increasing the beam intensity is not practical. Then, we are running into the total dose regime, where the device is prone to become inoperable before the most LU-sensitive chip section has been hit. But, even though very unlikely, just this position can be hit first in space. This uncertainty is embarrassing because the first and only LU can end up in a complete unit loss. To cope with this unlikely, but then catastrophic event, we rely on (perhaps unnecessary) LU current breakers. Apparently, those current breakers introduce another nontrivial design problem, i.e. the dependable discrimination between a LU-induced peak current and an activity-induced peak current.

Since epitaxial technology is used more and more we can expect that the LU situation will improve. In contrast the shrinking of the circuits lowers the charge of the nodes controlling the circuit state. That means that the nodes are becoming more sensitive against the charge deposited along a neighbouring particle track. Consequently we expect to be confronted with an increasing SEU sensitivity.

Structural Protection against Permanent Faults
Shielding is the only practical provision against total dose damages. A first order worst case prediction of the needed shield thickness is based on three facts (1) the dose-depth curve of the envisaged mission, (2) the tolerance dose of the most sensitive device and (3) the dose margin, typically factor of two. Later on in the design process the shielding can be optimized by taking into account: (a) the mass distribution of the mounted boards inside the box, (b) the shadowing of the box by the S/C structure and neighboured units and (c) placement and spot shielding of certain most sensitive devices. Ray-tracing algorithms are used for fine-tuning of shielding efficiency.

Permanent LU-induced device failures can be coped with LU-breakers. Then the affected unit is inoperable for a short time until the automatic reinitialization is completed. If only those devices are used, which did not exhibit a latchup to during test, the LU occurrence will be very rare (e.g. less than once per year). Then the associated short "power down"-periods will not influence the performance, practically

Structural Protection against Transient Faults
The SEU problem is common to both, the rad. hard and the COTS approach. Error correcting codes are very efficient for reducing the frequency of visible errors. Those codes are easily applicable in uniform arrangements of storage cells, as in memories[3,4]. Cyclic background scrubbing over all cells is used to limit the lifetime of single bit errors and so to reduce the probability for non-correctable multi-bit errors drastically. Hamming-Coding is appropriate for single-bit wide devices, where a hit affects only one bit of the respective address. Reed-Solomon-Coding is suited for b-bit wide devices, where a single hit is capable to damage up to b adjacent bits of the respective address.

The problem is more difficult for irregularly distributed arrangements of storage cells, as registers and latches of tailored length, counters, etc., particularly in case of simultaneous access. Here the appropriate design strategy is to allocate as much as possible storage cells in an uniform array, which lends itself to protection by an error correcting code. The remaining amount of storage cells should be equipped with individually tailored protection, as majority voting, parity voting and use of less vulnerable cells (e.g. in FPGAs with FF-modules of different sensitivity). Most probably, a remaining small amount of cells will not be protectable, e.g. registers and memory banks inside of processor devices. There (1) multiple execution of independently stored small program entities plus S/W majority voting, (2) multiple execution in distinct devices plus H/W majority voting and (3) watch-dog protection remain as the last resort.

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In larger systems simulation is the only suitable instrument for numerical assessments of the efficiency of these versatile protection measures. Presently we started such a simulation for the control circuitry of a mass memory module (6 FPGAs plus some discrete logic). Our intention is to extend these efforts to larger systems up to complete DPUs.

Comparative Assessment

The COTS approach implies a lot of additional nontrivial design tasks in comparison to the rad. hard approach. Regarding the SEU issue a problem becomes more visible, which already is existing for the rad. hard approach, even though perhaps with a smaller impact.

But, as much we are in favour of the straight-on rad. hard approach, we don't see, how in the future we will be able to implement lightweight high performance DPUs following the traditional paved way. Instead, we believe that we have to follow the rough way, exchanging vanishing technological support by sophisticated structural provisions. This opens a wide field for the ingenuity of engineers and hopefully results not only in savings of mass but also of costs.

Thermal Aspects

Traditionally rad. hard components for use in space are specified to the military temperature range (-55/+125° C). The COTS component spectrum for this wide temperature range is small, but most components are specified at least to the industrial temperature range (-40/+85°C).

COTS components consume significantly less power as rad. hard devices, because of smaller structures and lower supply voltages. The small board size reduces the thermal resistance between component pins and the box walls, which are rather massive for shielding purposes. On the other hand the heat sources are concentrated in a smaller volume.

Packaging

Traditionally rad. hard components are packed in ceramic packages, which are significantly larger as the chips themselves. To increase the component density, several chips can be packed into one Multi Chip Module (MCM). These MCMs achieve significant reductions of mass and volume compared to the standard ceramic packages. But stiff base plates, electrical connection layers and the hermetically sealed cover occupy much more mass and volume as the chips

themselves. As an example a memory MCM is compared to stacked COTS devices. A sectional view of an 640 Mbit mass memory MCM is shown in Fig. 5. Here 40 non rad. hard 16MBit DRAM chips are mounted on four stacks of 10 devices, each.
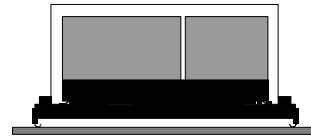

Figure 5: Sectional view of a 640MBit memory MCM

The alternative approach uses COTS components. These plastic moulded components are not significantly larger than bare dies. Laser cut metal leads connect ten 64MBit DRAM devices in Thin Small Outline Packages (TSOP). The devices are glued together to a stack. Four stacks with a total capacity of 2560MBit can be placed on slightly less board space and less volume than the MCM. The sectional view of the COTS stacks is shown in Fig. 6.
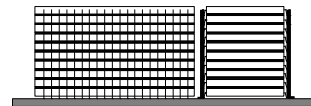

Figure 6: Sectional view of 2560MBit COTS memory stacks

So we claim that high density packaging of COTS components promises more favourable figures for mass and volume and a higher design flexibility than MCMs.

Miniaturized DPU

The goal of our prototype development is to study the potential of the COTS approach with respect to savings of power, mass and volume. The ROSETTA-OSIRIS DPU is taken as reference platform.

This DPU contains two redundant processor systems and a small common core. The processor systems can be operated in parallel or in a Master/Slave configuration. Also a single processor system can be operated, whereas the other represent hot or cold redundancy. Each processor system is based on a Motorola 56302 Digital Signal Processor (DSP). It features the following memory capacities, numbers in brackets include the parity bits: 384kByte (4MBit) PROM and FLASH, 768kByte (8MBit) SRAM and 144MByte (1.5GBit) DRAM. Single bit Error Correction and Double bit Error Detection (SECDED)

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is applied to all memory devices. The DRAM portion is subdivided into 3 banks and provides capacity for 250 compressed images (4M pixel, compression rate 1:14). Eleven latchup detectors protect all devices of the two processor systems and also the common core. The common core provides 48 interface lines (LVDS, RS-422) and is capable to serve the ROSETTA-OSIRIS camera instrument.

Since the DPU is fully static, its clock rate and its associated power consumption are scalable from DC up to 100MHz. This allows the implementation of efficient power saving modes, e.g. for use in specific mission phases as cruise or during pauses within the imaging sequence. All devices operate with 3.3V for power reduction.
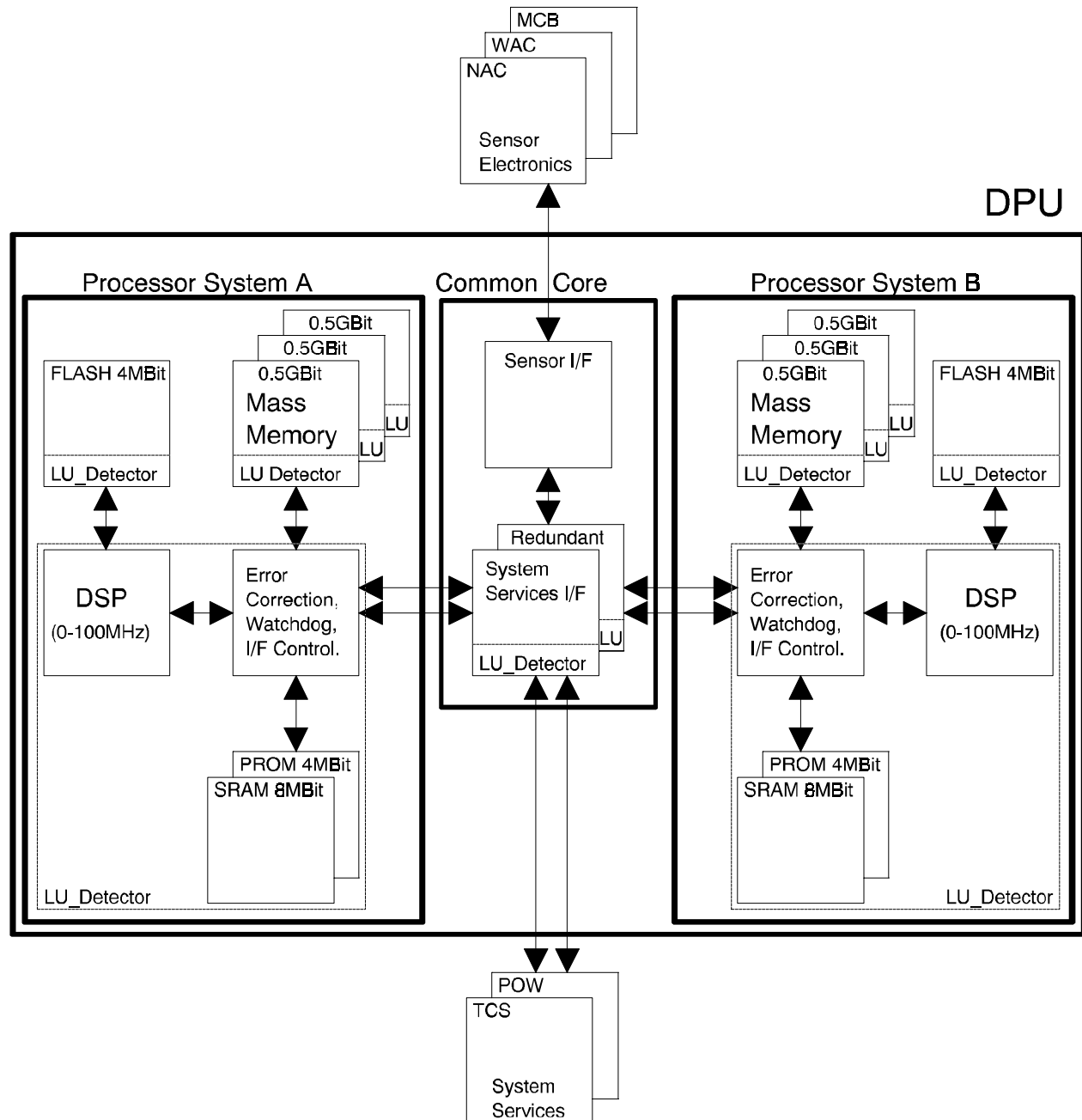

Figure 7: DPU Architecture

Standard components are densely packed on a folded rigid-flexible Multilayer PCB for being competitive to Multi-Chip-Module (MCM) technology at lower costs and substantially higher design flexibility. Only surface mounted devices (SMD) with visually inspectable pins, like Thin-Quad-Flat-Pack (TQFP) and Thin-Shrink-Small-Outline-Package (TSSOP) are used. Further reductions of mass and volume can be achieved by use of smaller packages like Ball Grid Arrays (BGA). But these components require X-ray inspection of the mounted board. The components are placed on five PCB areas sizing 37*37 mm^2. The connectors are located on two small rigid areas, Fig. 8.

The high density packaging requires advanced design rules in line with the current industrial state-of-the-art. The distance between components is 0.4mm and between components and the box wall 0.5mm, respectively. The clearance between boards is 1.0mm. It provides adequate space for random vibration. On the 8-layer Printed Circuit Board (PCB) the track width is 0.13mm (about 5mil) for signals and 0.254mm (10mil) for supply and ground lines. The diameter of the vias is 0.46mm with 0.2mm holes. The minimum radius for the flexible connections is 2mm.

The unfolded board is shown in Figure 8. The mass memory and processor boards are symmetric (i.e. the top side of processor B is identical with the bottom side of processor A). The bottom side of the sensor and S/C interfaces is not shown. It contains additional interface circuitry: receivers, transmitters and some FIFOs. The shaded rectangles represent the flexible connection.
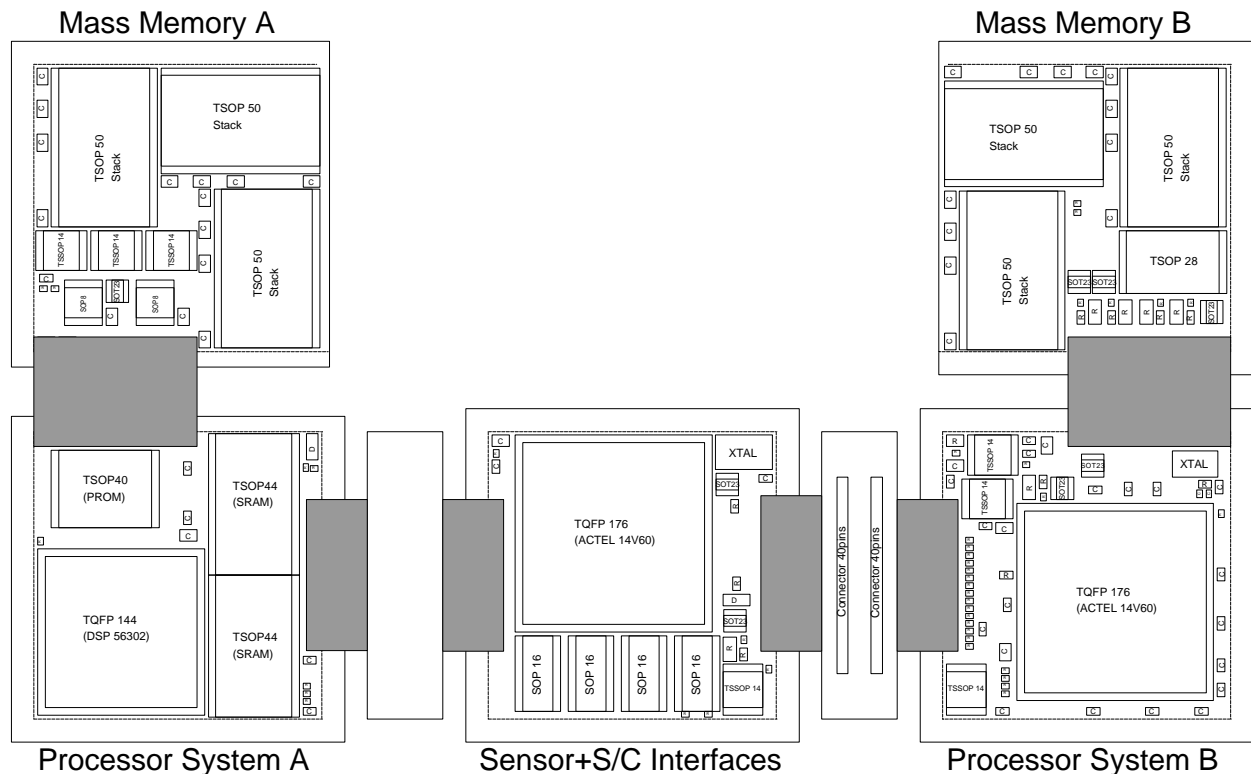

Figure 8: The rigid-flexible PCB

Using these flexible connections the board is folded to a stack of 43.2mm height. The mass of the DPU is less then 300g (50g components, 25g PCB, 203g shielding box structure, 20g coating). The overall dimensions are $50*50*55.2mm^3$ and include the 6mm shield.

Processor System A, Mass Memory A, Sensor and S/C interfaces, Mass Memory B and Processor System B are located from top to bottom in the sectional view of the DPU in Figure 9.
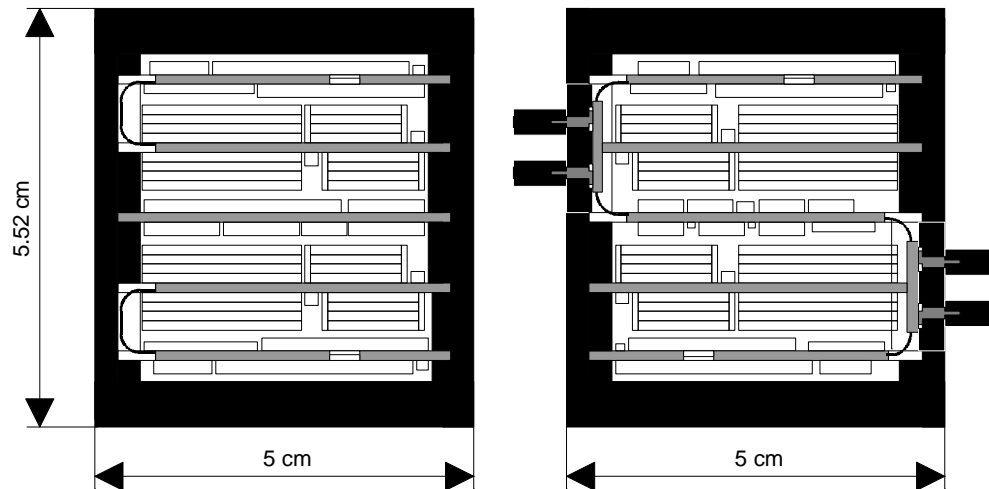

Figure 9: Sectional view of the DPU.

Conclusions

High density packaging of non rad-hard commercial of the shelf (COTS) components combined with mission specific tailored shielding, error correction and latchup protection can be applied on a wide spectrum of missions scenarios. Compared to the traditional rad. hard approach a mass gain of 30 and a volume gain of 100 can be achieved for moderate radiation environments, like ROSETTA or SOLAR PROBE. Even in comparison to the rad. hard MCM technology a gain in mass of roughly 10 can be achieved.

Acknowledgements

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He joined IDA in 1969 and built up a branch directed to the design and development of digital space electronics. He was responsible for the design and implementation of more then 20 instrument DPUs and more than 10 mass memories for missions from HELIOS through CASSINI. He is co-investigator in 8 space experiment teams.