Spacecraft Computers on the SeaStar Satellite

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Abstract

The SeaStar spacecraft requires a high performance computer system to handle its various requirements. It must process not only the high-rate data from the Sea-viewing Wide Field-of-view Sensor (SeaWiFS) instrument, but also the spacecraft ground interface system and the attitude control system data. This paper will describe the spacecraft computer architecture and its hardware. With minimum peripheral changes, the same computer can be configured to perform the payload, or the ground interface, or the attitude control functions. Each flight computer consists of three computer slices and a power module. There are two main flight computers on the SeaStar satellite; the second unit is used as a back-up. To date, the satellite has not required the service of the back-up computer.

Introduction

Orbital Sciences Corporation has developed and used several spacecraft computers with various sizes and performance levels for different satellite applications. In the case of the SeaStar (officially known as OrbView-2) satellite, we decided to upgrade the previous flight computer that was used on the successful DOD's APEX satellite, also an Orbital-built spacecraft. The system engineering team had determined that the APEX computers did not have the throughputs to handle either the SeaWiFS instrument high data rate or the ACS (attitude control system) control loop. To keep the software costs down, we could not afford the migration to another microprocessor architecture. Hence the development of the SeaStar satellite computer was needed.

Functional Description

The SeaStar flight computer system consists of two flight computer units, designated as primary and secondary. Both are identical in term of hardware and software, also they are cross-strapped. The default running computer is the primary unit while the secondary computer is power-off. Each unit consists of three computer slices and a power supply slice which is located on the side contacting the satellite structure panel ensuring better thermal dissipation. There is no motherboard or backplane connecting among the three computer slices but each slice provides two serial ports dedicating for inter-processor communication at the speed of 256 kbps in standard HDLC protocol.

The power supply slice accepts the 28-V DC power and generates the 5-V power supplies for the three computer slices. Two 2805 DC-DC converters are used and a separate 5V DC-DC converter for the watchdog timer circuit. A dedicated watchdog timer circuit is assigned to each of the computer slices. The actual watchdog timer IC is resided on the computer slice.

The circuit toggles its associated 5-V supply off for duration of one second. One 9-pin D-sub connector is provided for 28V input power supplies and a 37-pin D-sub connector for power distribution, watchdog interfaces and power supply status.

The computer slice has the following features:

- Three Radiation-tolerant 68302 microprocessors, operating at 16 MHz
- 64 kB of bootload EEPROM
- 1 MB of application EEPROM
- 4 MB of high-speed Error detection and correction (EDAC) SRAM
  - 2 MB is battery back up
- Programmable watch-dog timer
- Programmable real-time clock
- 16-level priority interrupts
- 9 DMA channels
- 9 RS-422 serial ports with handshakes
- 12 open-collector outputs
- 4 TTL-compatible inputs
- 4 TTL-compatible outputs
- 8 digital I/O channels
- Compact 25 cm. x 17 cm. x 1.8 cm. form factor
- One 37-pin and three 62-pin D-sub connector.

The block diagram of the computer slice is shown on the Figure 1 below.

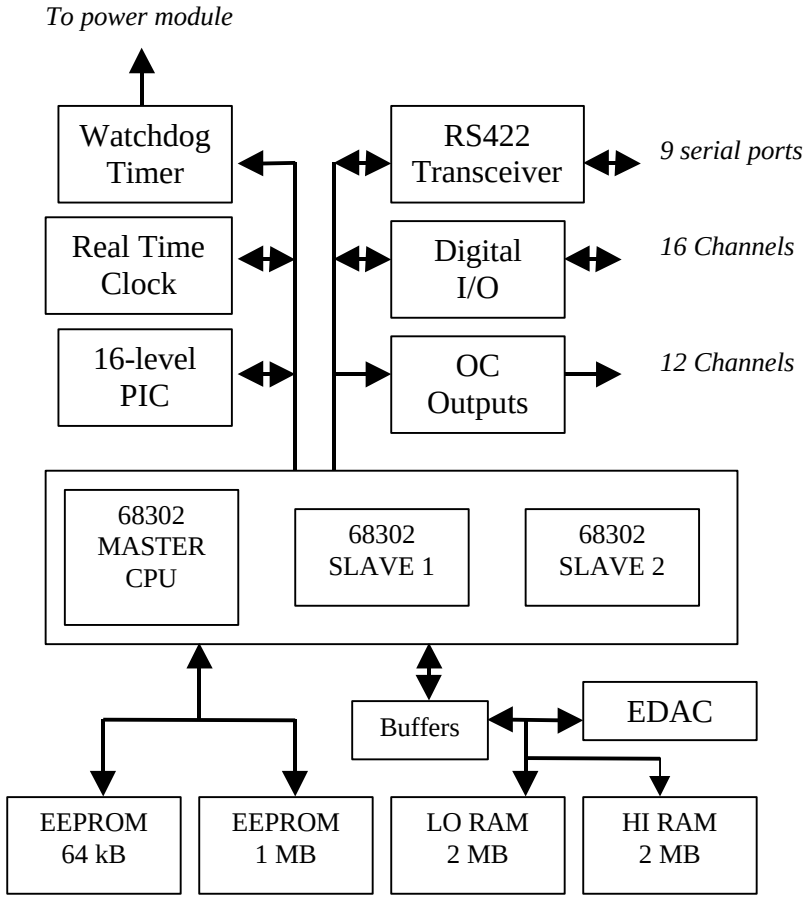

Figure 1. Block Diagram of the Computer Slice.

The computer slice is based on the Motorola MC68302 16-bit multiprotocol microprocessor, operating at 16 MHz. The processor was specially fabricated for Orbital on the epitaxial die for radiation consideration. The slice contains one master and two slave MC68302 processors. Both slave processors had the CPU core disabled. The detailed information about the MC68302 microprocessor can be found on the "MC68302 User's Manual" by Motorola.

The 64-kB bootload EEPROM memory stores the initialization program, operating system kernel and can be re-programmed on-board via external jumper selects at the connector. This feature will not available once the unit was installed on the satellite. In default state, this memory will operate in the read-only mode.

The 1-MB application EEPROM memory contains two copies of the application software that will be loaded into the SRAM memory for execution during the run time. During the mission, an entire new software code can be uploaded to this memory. The internal write-protected EEPROM feature will be used to prevent any accidental writes to this memory.

There are two banks of the on-board EDAC SRAM memory, the low-bank and the high-bank. Each bank contains three 1-MB memory chips with a total of 2-MB usable memory since one chip is used for the check bits. The software will run from the low-bank memory area unless during the initialization. The high-bank memory has battery back-up feature, which is available for storage of status and other long-term data.

The Error Detection and correction (EDAC) function was designed and implemented on an Actel A1020B fpga including the generation of the single bit and multiple bit errors. For single bit error, not only it provides the corrected data to the CPU but also performs the automatic write-back of the corrected data to the same memory location within the same bus cycle. An interrupt is provided to inform the processor when the single bit error occurred. For multiple bit error, it will generate 'bus error' on the BEER signal line resulting in the processor reset. A record of BEER occurrence is stored in the battery back-up memory providing a valuable debugging information. The simple modified Hamming Code is used to generate the 6-bit check bits from a 16-bit word during the write operation and the 6-bit syndrome bits during the read operation. The comparison is accomplished by a set of exclusive-OR gates to detect the single or multiple bit errors. An EDAC disable mode is also provided for testing purpose.

Another A1020B fpga contains the other interface functions including cold/warm boots, power supply status, programmable interrupt controller interface, reset, abort, memory chip selects and watch-dog timer interface.

All input/output (I/O) interfaces are buffered before going out to the connectors. All nine serial ports are RS422 compatible and cross-strapping circuits are provided. One port is normally assigned for the test port, which handles the software upload and test. Two other ports are used for inter-processor communication between the three computer slices. The twelve open-collector outputs have selectable resistor values to accommodate the different current requirements for the three computer slices. The watchdog timer has five jumpers for time duration selection.

On the SeaStar satellite, the three computer slices are configured differently for the three different functions, namely, the Ground

Interface Module (GIM), the Payload Service Module (PSM), and the Spacecraft Control Module (SCM).

The GIM processor handles the interfaces between the satellite and the ground stations including the L-band and S-band communications, launch vehicle interface, command reset decoder interface, and the power module. It also acts as a message router for the communications to other subsystems including the two flight computers on the same unit.

The SCM processor executes the attitude control system software that must be able to stabilize the spacecraft to within one SeaWiFS pixel. Three of its serial ports connect to the Attitude Control System (ACS) subsystem, the Spacecraft Maintenance Unit (SMU), and the GPS receiver.

The PSM processor controls the SeaWiFS instrument and processes all SeaWiFS data before sending to the Solid-state Recorder (SSR) for storage. It also processes the low-rate data at 655.4 kbps, HRPT format, and delivers to the redundant L-band downlink transmitters.

The 2 Mbps high rate data is output from the SSR directly to the redundant S-band transmitters under the command of the PSM processor. Two SSR units are available for the data storage and running continuously for the entire mission.

More details on the SeaStar spacecraft and SeaWiFS instrument can be found under NASA website at http://seawifs.gsfc.nasa.gov/SEAWIFS.html.

Conclusions

The design of the SeaStar Spacecraft Computers is straightforward and successful. According to the report from the NASA's Goddard Space Flight Center, the SeaStar spacecraft has been providing data coverage at 99% of the time since launch on August 1, 1997.