COMMAND AND DATA HANDLING PROCESSOR

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Abstract

This command and data handling processor is designed to perform mission critical functions for the NEAR and ACE spacecraft. For both missions the processor formats telemetry and executes real-time, delayed and autonomy-rule commands. For the ACE mission the processor also performs spin stabilized attitude control. The design is based on the Harris RTX2010 microprocessor and the UTMC Sμmmit MIL-STD-1553 bus controller. Fault tolerant features added include error detection, correction and write protection memory. Components have been selected to minimize the possibility of charged particle induced upset. The processor's architecture and mechanical design are described. The hardware and software test and validation methods are given.

Nomenclature

ACE	Advanced Composition Explorer
EDAC	error detection and correction
EEPROM	electrically erasable programmable read only memory
FIFO	first in first out
KWD	1024 words
NEAR	Near Earth Asteroid Rendezvous
NEPSTP	Nuclear Electric Propulsion Space Test Program
RAM	random access memory
SμMMIT	serial μ-coded monolithic multi-mode intelligent terminal
TIMED	Thermosphere Ionosphere Mesosphere Energetics and Dynamics
TOPEX	Ocean Topography Experiment
UART	universal asynchronous receive transmit
UVPROM	ultra violet erasable programmable read only memory

Introduction

The most important characteristic of a spacecraft embedded processor is that it operate as part of the system through errors induced by the space environment, including solar flares. This, and the other requirements for the processor were established using the experience of the lead hardware and software designers in the APL Space Department. The processor is based on the Harris RTX2010 microprocessor and the UTMC Sμmmit MIL-STD-1553 bus protocol circuit.

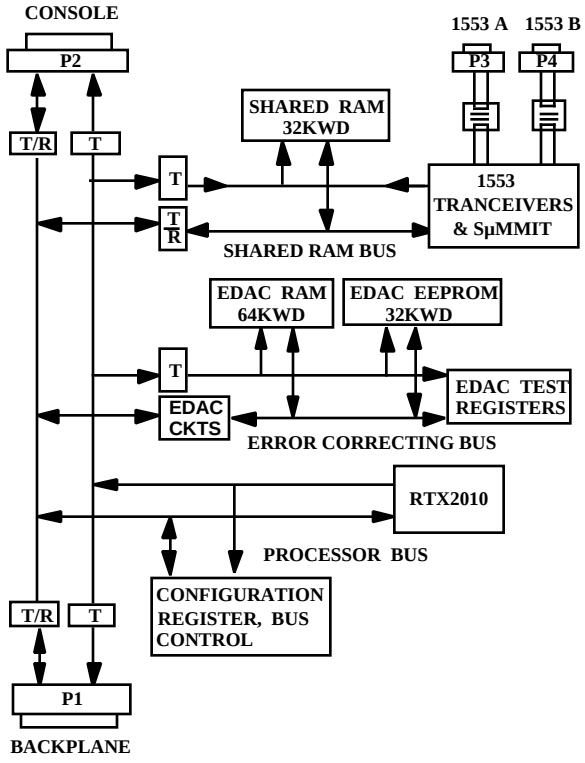

Figure 1. Processor block diagram.

Fault tolerance features must be added. Memory, especially that used for program, is write protected. EDAC is used for the memory bus. A processor wait state time-out interval counter is used. Error flags are brought out to the backplane for off-board action. These flags include an unrecoverable memory error, wait state time out error, 1553 bus error, and the processor boot flag.

Components have been selected to minimize the possibility of charged particle induced upsets. Programmable gate arrays are not used for control because direct logic implementation is too susceptible to upset and triple redundant voting is too slow. Only circuits that require more 45-MeV/mg/cm^2 of ionizing energy transfer to cause an upset are used.

Processor Design

The configuration register and associated logic, Figure 1, controls the data flow through the processor. Bits are allocated for memory segment write protect, error output mask, memory error detection and correction, and test control. The configuration register is write protected when the RTX2010 is brought out of the boot mode.

Error Correcting Bus

The 32-KWD of EEPROM is 22-bits wide and contains 16-data bits and 6-parity bits. A modified Hamming code is used to correct single bit errors and detect double bit errors. EEPROM memory is used to hold program, constants, and spacecraft autonomy rules. Each word read from EEPROM memory can be single error corrected, and double error detected.

Data can be both written into and read out of the 64-KWD of error correcting RAM at high speed. The first 32-KWD are divided into eight, 4-KWD segments. Each segment may be separately write protected. Once the write protect bit for a segment in the processor board configuration register is set, that segment may not be modified. The exception tothis rule is if a single bit error is detected during read, the error control circuitry automatically corrects the bit. This feature is called automatic write-back of the corrected word. If a 4-KWD segment is not write protected, code addressed to that segment is read from EEPROM instead of RAM. The write unprotected RAM segments are free for temporary or scratch pad storage.

A method of testing the EDAC circuitry is provided. When an error occurs, the address of the error is latched into a register. The syndrome bits that are generated in the error detection circuit are also latched. The syndrome bits define the bit position of the error in the word. The processor determines the location of an error by reading the address and syndrome registers. A multibit error flag is bought out to the processor backplane where it is read by the reset logic as a system error. To check the memory error control logic a method is provided to write an error into any data or parity position of either EEPROM or RAM. An error write is accomplished by inhibiting the write of the 6-parity bits. After the errors are induced the error control logic is enabled and the errors are read. A test program is run during board qualification which induces and detects errors in every one of the 22-bit positions of a parity checked word. The test program verifies that the errors are properly corrected. The flags necessary to test the error control logic are contained in the configuration register.

Console

The RTX2010 address and data buses are brought to the console plug via drivers and isolation resistors. The console, Figure 2, contains a logic analyzer monitor interface, UVPROM, EEPROM and a UART interface. The logic analyzer allows real-time capture of the processor instruction and data stream. The UVPROM is loaded with the software development support code. The EEPROM provides a substitute for the flight EEPROM. It holds the flight target program during test and verification. The UART provides an interface to the host software development personal computer.

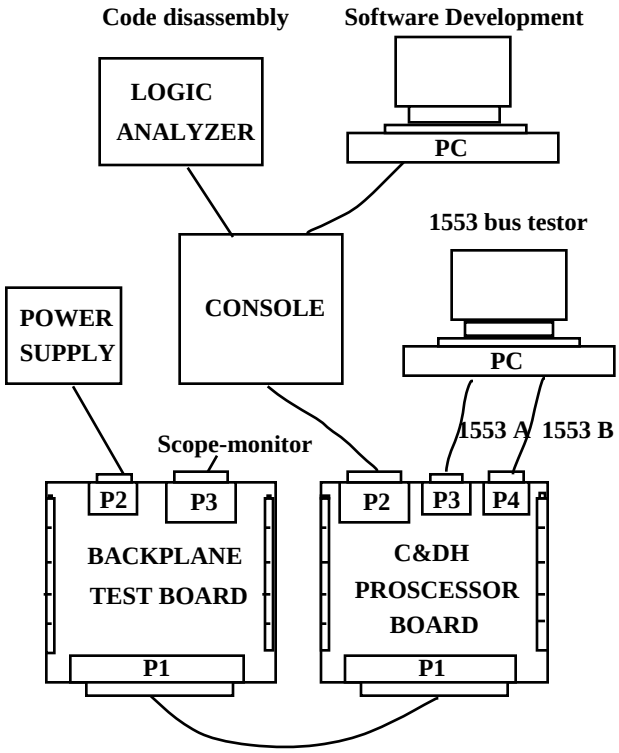

Figure 2. Test setup.

During program development software is loaded into the on board flight RAM. It is executed from RAM while being monitored by the logic analyzer with code disassembly. Next, code is optimally compiled, loaded into the console EEPROM and verified. Last, the code is loaded into the on-board flight EEPROM. The console interface allows execution of code from the console, tracing the code execution with a logic analyzer, loading cross compiled code from the PC, inhibiting of system resets and forcing a console reset. The console also allows running the processor at a higher than nominal clock rate. During normal operation the processor board 24-MHz oscillator, which is also needed for the 1553 bus controller, is divided by two to 12-MHz for the RTX2010 clock input. For clock margin testing a 16 MHz oscillator on the console is used to clock the RTX2010.

Backplane Bus

Backplane cycles run with 2-wait states, unless the backplane wait line is pulled down forcing additional wait states. The backplane cycle control is set up to accommodate slow but space qualified devices including the GEC MA7001 FIFO buffer. Both address and data lines are held stable before the leading edge and after the trailing edge of the backplane write initiate signal. To protect the boards circuitry in the event of a backplane error condition, a 51-ohm series damping resister with a 51-kohm pull up resistor is used with each backplane interface. A custom 18-resistor network flat pack designed by Dale Electric reduces the needed board space for these protection resistors.

The processor communicates over the backplane with five cards in the NEAR configuration, and six cards in the ACE. The other cards provide interfaces to the uplink, downlink, power switching, data recorder, and analog telemetry. In the ACE configuration an attitude control card interfaces with sun sensors and thruster actuators to spin stabilize the spacecraft.

The backplane test board, Figure 2, facilitates loop-back testing of all processor board interfaces including: address, data, and control signals. A test program, written for use with the backplane test board, outputs the results of loop-back test to the console PC where the results are compared with a template. A plug on the backplane test board provides oscilloscope monitor access to the backplane.

MIL-STD-1553 Bus

For NEAR, the MIL-STD-1553 bus provides the interface to its four instruments and attitude subsystem. The UTMC Sμmmit protocol circuit is commanded to a remote terminal on one redundant processor, and a bus controller on the other. When acting as a remote terminal, the 1553 address is determined by the console plug wiring. A flight adapter is used in the launch configuration. The redundant 1553 interfaces are checked during board test by the PC. It contains an Excalibur Systems, Inc. 1553 interface test board. During board test both memory read-write from the RTX2010 and the 1553 bus interface are exercised continuously verifying satisfactory power distribution and memory arbitration.

Mechanical Design

Printed Circuit Board

The processor is packaged on a single conduction cooled 21.6-cm by 20.3-cm printed circuit board. The board weighs 0.5-kg plug-in ready with conformal coat, stiffener, and card locks. The board is designed to withstand launch in any orientation to the thrust axis.

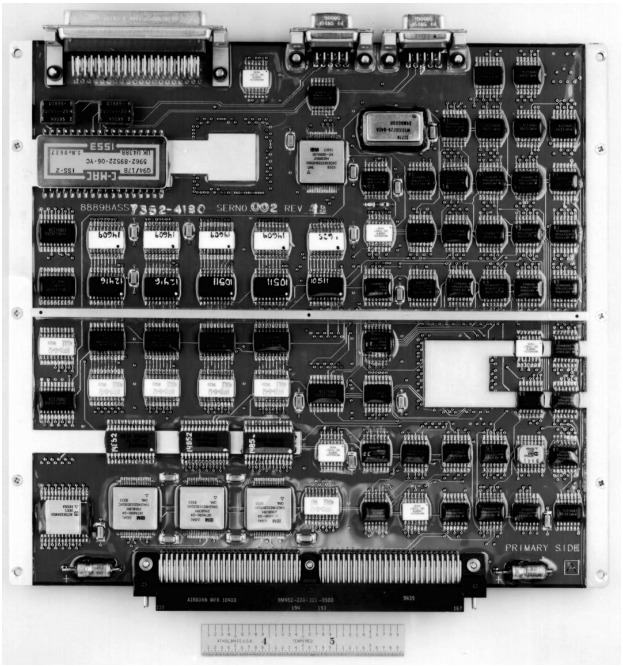

Figure 3. Circuit board front.

The printed circuit board conforms to Mil-P55110. The lines are 0.25-mm with 0.25-mm spacing. Pads are 1.02-mm in diameter with 0.46-mm drill size. The board contains 12 conductor layers, 3 power, 3-ground and 6 signal. Two signal layers are top and bottom and hold the components. The remaining signal layers are stacked between alternating power and ground layers.

Components are mounted on both sides of the board, Figures 3 and 4. Components on the back side of the board have reverse bend leads so that they align with the matching leads of similar components on the front side of the board. This mounting technique is particularly useful with memory circuits. For memories, all leads except one match between components on the front and back of the board. A large number of connections are also saved by having the four buses that interface to the RTX2010 interconnect via components on both sides of the board.

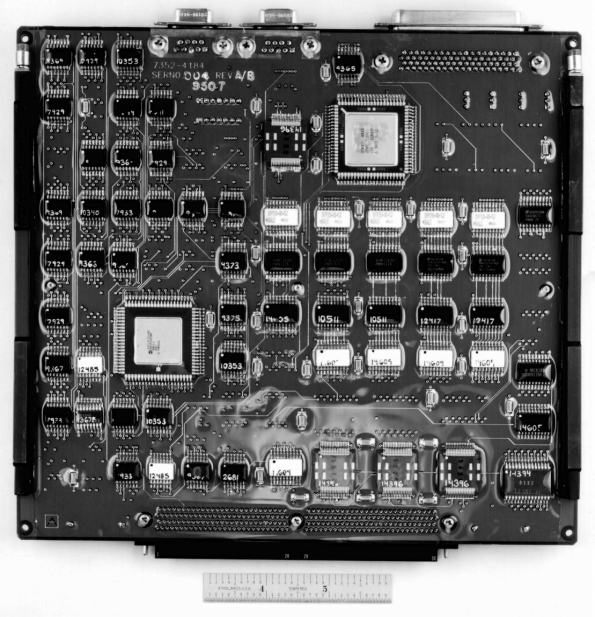

Figure 4. Circuit board back.

Thermal Design

Aluminum is used to heat sink those components that require special attention: The 1553 bus transceivers, the Sµmmit 1553 bus controller, the EEPROMs, and the RTX2010. Although the board typically dissipates less than 2-watts, peak power can exceed 6-watts with an improperly matched MIL-STD-1553 interface in the continues transmit mode. The thermal design allows continues operation at peak power and 65˚ C at the card locks.

Conclusion

A summary of the processor specifications is given in Table 1. The NEAR spacecraft was successfully launched February, 1996. The ACE spacecraft will be launched in August, 1997. The redundant flight processors are operating in the ACE spacecraft.

CPU	RTX2010
Clock input	12 MHz
Memory	64 KWD EDAC RAM
	32 KWD EDAC EEPROM
	32 KWD shared with 1553
IO	Backplane: 20-Addr 16-Data
	MIL-STD-1553: sides A & B
Throughput	0.33-µsec EDAC read/write
	0.50-µsec IO read/write
Size	21.6-cm x 20.3-cm
Weight	0.5-kg
Power	1.5-w typical, 6.0-w max.

Table 1. Processor specifications.

Acknowledgments

A space qualified processor design requires the contribution of many individuals. Much work was done in parts selection and in hardware and software design and analysis. In particular, Dan Rodriguez designed the NEPSTP command processor, the precursor to this board. Dave Artis, Lloyd Linstrom, and Brian Heggestad designed the NEAR software. Steve Williams designed the ACE software. Scott Schlemmer designed the printed circuit board.

Biography

James A. Perschy received a B.S.E.E. degree from The George Washington University in 1958 and an M.S. in physics from the University of Maryland in 1965. In 1958 he joined APL, where he designed the data handling system and memories for the Navy navigation satellites. Recently he led the TOPEX ocean-altimeter signal processor development. He is currently leading the TIMED spacecraft command and data handling system development.