DESIGN OF A LOW-COST SINGLE BOARD COMPUTER SYSTEM FOR USE IN LOW-EARTH ORBIT SMALL SATELLITE MISSIONS

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ABSTRACT

A single-board computer system created specifically to meet the demands of a new generation of small satellite missions is being designed, built and tested by students at the University of New Hampshire. The Satellite Single-Board Computer (SSBC) is an Intel 80C186 based system that is qualified for explicit use in low-earth orbit missions. The SSBC serves as a low-cost, high-c~uality alternative to commercially available systems which are usually very costly and designed for much harsher space environments. These "off-the-shelf" systems are normally out of price range for most very low-cost satellite projects. At the other end of the spectrum, however, are inexpensive commercial-quality computer boards that do not offer any space-hardened characteristics. These systems are typically not designed to survive the cosmic radiation and extreme temperature levels usually found in low-earth orbit. The SSBC fills in the gap between these two alternatives. It offers a flexible design that is based on the industry standard Intel x86 architecture. It can be used in a variety of applications where total dose radiation levels are of concern, but costs must be kept at a minimum. The production cost for a complete SSBC flight board is expected to be under $20,000.

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1.0 INTRODUCTION

The SSBC was originally developed for use onboard the Cooperative Astrophysics and Technology SATellite (CATSAT). The SSBC plays a dual role for CATSAT, acting as the key component of the payload computer as well as the command and control computer for the spacecraft. It has also been adopted by several other satellite projects. In particular, the SSBC is slated to be the main computer system onboard the Joint Air Force Weber SATellite (JAWSAT) scheduled for launch in late 1997.

The board features one Mbyte of memory which is protected by error detection and correction (EDAC) circuitry and 64 Kbytes of rad-hard PROM. The SSBC is capable of surviving radiation levels of at least 5 krads total dose. The board is also latch-up protected and features a redundant watchdog timer. Data storage can be increased to a full 32 Mbytes by adding optional SRAM memory cards. Software development is accomplished using industry standard tools which allows program code to be written in both C and assembly languages.

Real-time software debugging is available by connecting the SSBC to an IBM-compatible computer over a standard serial interface or by using an in-circuit emulator.

2.0 CATSAT MISSION

2. 1 Overview

CATSAT is a small satellite mission being funded by the Universities Space Research Association under the Student Explorer Demonstration Initiative (STEDI) program. CATSAT is being developed jointly by the Institute for the Study of Earth, Oceans and Space at the University of New Hampshire, the Center for Aerospace Technology at Weber State University and the Department of Physics and Astronomy at the University of Leicester. CATSAT is scheduled for a mid-1998 launch on an Orbital Sciences Corporation (OSC) Pegasus XL launch vehicle.

The scientific objective of CATSAT is to study the properties of cosmic gammaray bursts, particularly the nature and distribution of the objects that produce them. To this day, astrophysicists are still speculating as to the origin of these unusual phenomena but have come to no reasonable agreement. Using an extremely sensitive, low-energy sensor system, CATSAT will hopefully shed new light on this hotly debated subject.

A major goal of the STEDI program is to promote student involvement in all aspects of satellite development, and CATSAT has been no exception. A large portion of the spacecraft frame, sensor system, and analog and digital electronics are being designed, built and tested by student engineering teams. These teams are headed by graduate student leaders with faculty and staff at each of the three academic institutions acting as mentors. The STEDI program offers students more than just an educational experience. Real-world engineering challenges, budget constraints, and fixed project deadlines have made working on CATSAT an extremely valuable team-oriented experience.

2.2 CATSATDEURequirements

The Digital Electronics Unit (DEU), which is the back-end of the CATSAT payload instrument electronics, has the SSBC as its core. The DEU also contains several other printed circuit boards, including two addendum memory boards and an input/ output (I/O) board. The two memory boards provide 24 Mbytes of mass data storage and the I/O board contains interfacing hardware and custom circuitry for collecting data from the analog sensor system. The DEU has several major requirements related to the scientific objective. Its first task is to accept digitized pulse-height data from the Analog Electronics Unit (AEU). These digital events are accumulated into a temporary buffer and then transferred to the addendum memory boards where they will be stored and manipulated. The processor needs to examine the stored data and decide whether a gamma-ray burst has occurred or not. If a burst occurred, the data is left unchanged. If a burst has not occurred, the data is timecompressed in memory.
The DEU is also responsible for: EDAC of the program memory; housekeeping chores such as monitoring temperature, voltage, and current levels; communicating with the command and control computer via a serial command interface; managing the system power and powering-up other DEU sub-systems upon startup; processing both immediate and time-tagged commands which are being sent from earth; and sending the stored memory data to the sband transmitter during downlink.
The DEU

also needs to meet vibration, power and total dose radiation requirements specified by the CATSAT Systems Engineering panel. All devices used in the DEU must be able to survive total dose radiation levels of at least 5 krads. This number was derived from a study conducted by a graduate student at the University of Leicester [Whi95]. The 5 krad rating includes a safety factor of two and is based on a two year mission length.

3.0 SSBC HARDWARE DESCRIPTION

3.1 Board Description

The SSBC system is designed around a MIL-STD-883 Intel 80C 186 16-bit microprocessor running at 12.5 MHz. The 80C186 was chosen for its balance of speed, functionality, development tools support, and inherent radiation-hardened properties. Tests have demonstrated that it can tolerate upwards of 8 krads. The microprocessor also has extensive space flight history. It is an ideal candidate for low-earth orbit missions, and as such has been used in numerous satellites designed and built by the AMSAT community

Figure 1 shows a block diagram representation of the SSBC system. The board contains one Mbyte of EDAC SRAM and 64 Kbytes of rad-hard PROM. At the heart of the SSBC is a custom Actel Field Programmable Gate Array (FPGA) chip. The Actel 1280A FPGA contains control logic for the Integrated Device Technology (IDT) 49C465 "Flow-Thru" EDAC unit, a tripleredundant watchdog timer, and interface and glue logic. The FPGA also contains circuitry that increases the 80C186 standard address space from one Mbyte to a full 32 Mbytes. This is accomplished by using a method of paging.

The SSBC includes two independent full-duplex serial ports using the Zilog 85C30 Serial Communications Controller (SCC). The SCC supports most standard synchronous and asynchronous serial transfer protocols, and has built-in CRC and HDLC capabilities. The 85C30 interfaces with two high-speed RS-422 transceivers that are attached to a DB-9 connector at the front of the SSBC printed circuit board. The serial ports can be used for both software debugging and as general purpose ports.

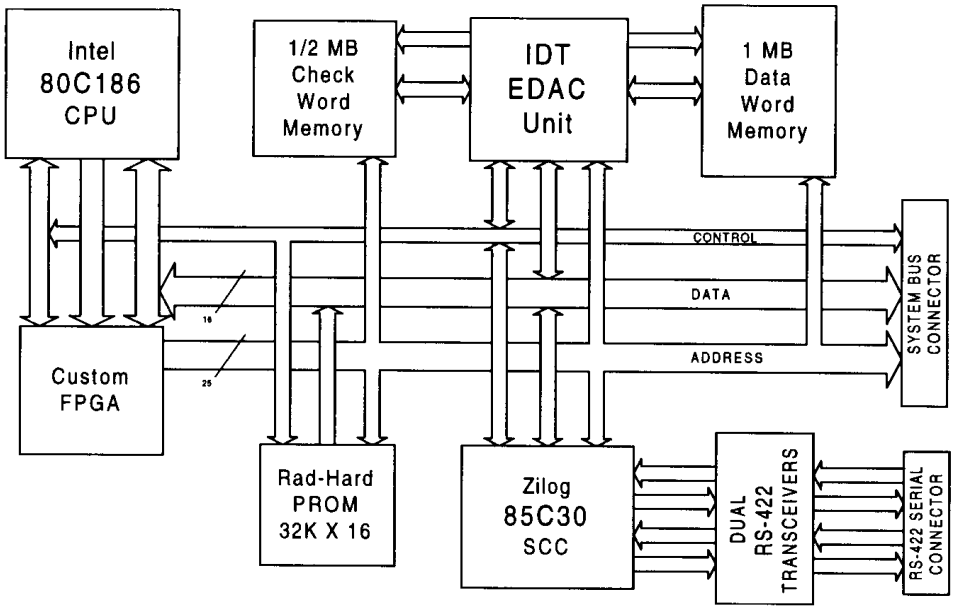

Figure 1. SSBC Block Diagram

All data, address and control signals are routed to the backplane connector for memory expansion and custom options. The backplane bus structure is based on a modified PC-AT design to accommodate for the increased address bus width.

3.2 Board Characteristics

The physical dimensions of the SSBC printed circuit board measure 6 x 7 inches. It is a multi-layer type that was designed and developed by students at the University of New Hampshire and manufactured out-ofhouse at a local facility. The backplane connector is a space-qualified Hypertac model which is manufactured by Hypertronics Corporation. Hypertac (HYPERboloid conTACt) system uses proprietary pin and sleeve designs to increase electrical conductivity and reduce wear and tear on each of the contacts during insertion - extraction cycles. A MIL-SPEC DB-9 connector is used for both serial port communications and as an interface to power and ground signals. The SSBC and optional memory boards require only 5V to operate. The board consumes approximately 3.5 Watts during normal operation. Figure 2 depicts a preliminary board layout design.

DIP packages were chosen for the eight PROMs so that a development version of the SSBC with DIP sockets could be used up to the point of final flight board assembly. This allows software designers to use inexpensive EPROMs during the development stage and requires only one version of the printed circuit board layout. Once the software has been finished, the EPROMs can be replaced with rad-hard PROMs and soldered directly to the flight board.

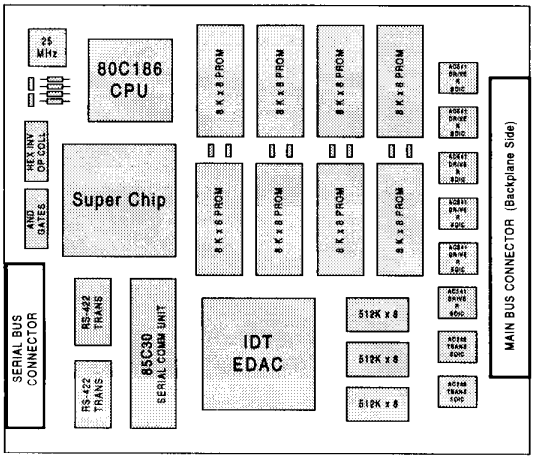

Figure 2. SSBC Board Layout

3.3 Addendum Memory Boards

The one Mbyte storage space of the SSBC can be increased to a full 32 Mbytes by using three addendum memory boards Each board contains up to twenty-four 512K x 8 bit surface-mounted SRAM chips made by Hitachi. An Actel 1020B FPGA contains the address decoding and bus interfacing logic for each board. These bulk memory boards are connected to the backplane connector similar SSBC board.

A new version of the bulk memory board is currently being investigated that would include memory chips on both sides of the printed circuit board. The use of surfacemounted components allows for this type of double-sided assembly. In this manner, as much as 24 Mbytes could be placed on one card, thus reducing the board count and overall weight of the computer system. It would also lower the power requirements since only one FPGA would be needed to support memory on both sides of the board.

3.4 Hardware Development

All aspects of the SSBC design and development were carried out at the University of New Hampshire using state-of-the-art Computer Aided Design (CAD) software by Mentor Graphics. The Mentor Graphics suite of software tools is an

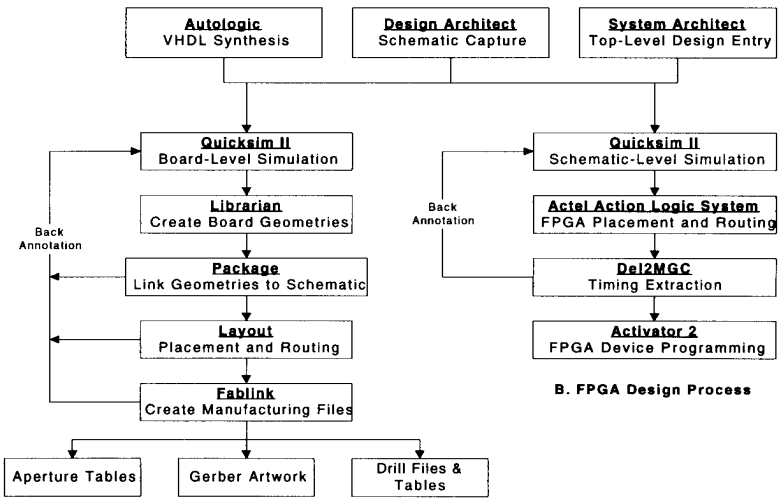

Figure 3. SSBC Mentor Graphics Printed Circuit Board and FPGA Design Processes

industry standard, completely integrated, professional CAD system for electrical and computer engineering design. The CAD system supports analog and digital circuits and includes tools for both schematic entry and simulation. Designs can also be entered using hardware description languages such as VHDL. A complete set of tools for designing printed circuit boards is also part of the package. Thermal analysis tools are available for identifying "hot spots" within a board layout. These tools can be configured to ignore heat convection and depend on conduction and radiation alone. This is an important feature when simulating the space environment.

Mentor Graphics also supports the design and simulation of Actel FPGA devices. Designs can be entered using either schematic capture or VHDL and then simulated. Once a design has been placed and routed in software, timing information can be back annotated into the simulator so that problems due to propagagtion delays can be identified and fixed. This makes troubleshooting a device after programming much easier, since most timing problems have already been found. Actual device programming can be done in-house using an IBM-compatible PC connected to an Actel FPGA programming unit. The flowchart shown in Figure 3 gives an overview of the processes used to create both printed circuit boards and FPGAs using Mentor Graphics and Actel tools.

3.5 PartsSelection

Selecting parts for the SSBC was not an easy task. Each device had to meet the 5 krad total dose requirement set by the CATSAT Systems Engineering panel. If a part did not have test results to prove that it met this requirement, then it needed to have flight history onboard a satellite in a similar low-earth orbit. Finally, if a part could not be justified using either of the above mentioned methods, then at the very least, it needed to be in the same "family" as a known radiation tolerance levels. An

example of a family of devices is the Advanced CMOS (AC) logic series from National Semiconductor, which is used for signal buffering on the SSBC. Goddard uses both AC and ACT family logic on the computer system for the SMEX series of satellites [Ngu95].

3.6 Summary of SSBC Features

The following list summarizes the major features of the SSBC:

- MIL-STD-883 Intel 80C186 16-bit microprocessor running at 12.5 MHz
- Low power - 3.5 Watts typical
- All connectors are high-quality and rated for both launch and space environments
- One Mbyte EDAC SRAM
    - Corrects and logs single-bit errors
    - Detects and logs double-bit errors
- 64 Kbytes Harris rad-hard PROM
- Watchdog timer
- Up to 32 Mbytes of storage memory using optional memory boards
- 2 full-duplex RS-422 serial channels
- All parts have been rated or shown to tolerate at least 5 krads total dose levels.
- Fast, flexible, straight-forward software development / debugging using industry standard languages and tools (including C and assembly).
- All interface and glue logic is condensed into one custom FPGA device.
- Rugged, high-quality, multi-layer printed circuit board with both through-hole and surface-mounted chips. No sockets or jumpers are used throughout the board.
- Designed to meet OSC Pegasus XL launch vehicle vibration specifications
- Current-limiting circuitry for protection against damage due to latchup

4.0 RELIABILITY ANALYSIS

Developing a reliability model is an important consideration when designing a system for a space application. Because of the remote nature of the space environment, it is extremely difficult to repair satellite systems which have experienced a failure of some sort. At the very least, a rudimentary study of the system reliability should be conducted to identify weak links in the

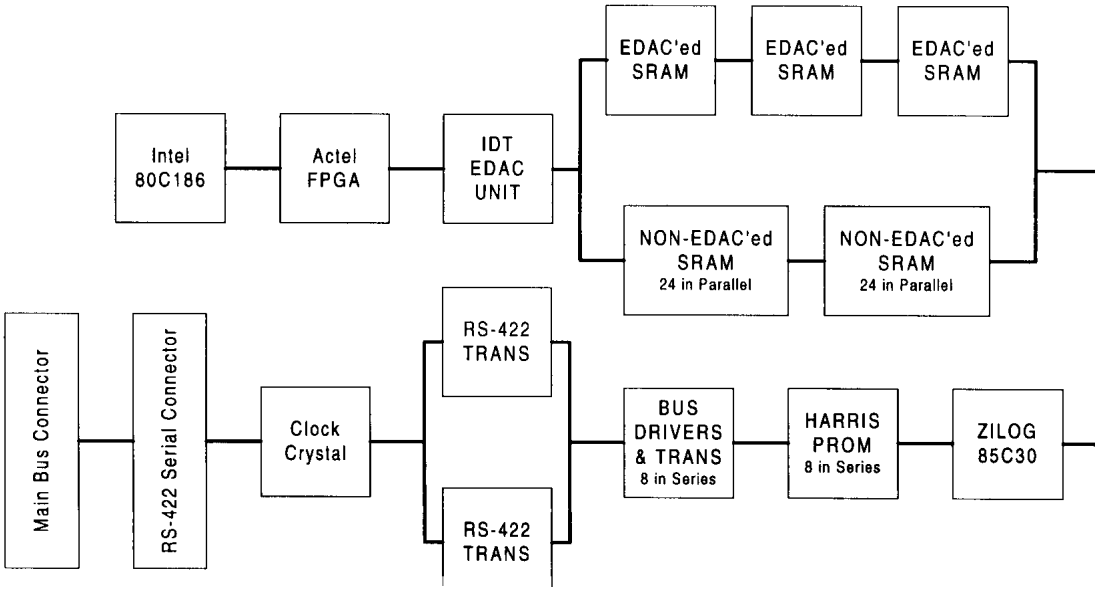

Figure 4. SSBC Reliability Diagram

design. This was the approach that was taken during the reliability analysis of the SSBC.

4.I Reliability Model

The first task was to develp reliability model for the SSBC system. Components were drawn in either series or parallel, depending on whether they existed as a single entity or exhibited some form of redundancy. Next, the failure rates for each of the components were estimated using the
US Air Force Force handbook *Reliability Prediction of Military Equipment Systems* [Mil89]. A reliability analysis software tool called *Sharpe* examined the reliability model that was developed and calculated the failure rate of the SSBC system over a period of six years [Sah96]. The SSBC reliability block diagram is shown in Figure 4. Items which have been identified as "single-point failures" are drawn in series. For example, the Intel 80C186 microprocessor, Actel FPGA, and EDAC unit are all single-point failures. Items that include some form of redundancy are drawn in parallel. An example is the RS-422 transceiver pair. If one transceiver should fail, the SSBC system will still operate with the other. Finally, there are those items that include both serial and parallel configurations. The SRAM subsystem is an example of this situation. If any
one of the EDAC'ed SRAM chips should fail, the program code can be mapped to run out of non-EDAC'ed memory, or vice versa The block diagram shown in Figure 4 is the basis for the reliability analysis. The failure rates for each of the blocks are based on package type, circuit density, quality process, and environmental characteristics. Radiation effects are not taken into account by the Air Force handbook and are therefore not reflected in the failure rate calculations.

4.2 Software Analysis

Sharpe takes a textural description of a reliability model as its input and calculates the failure rate of the system as its output. Generating the input file is quite simple given a reliability block diagram. Once the failure rates have been calculated for each of the devices, the input file can be written. Figure 5 displays a brief portion of the input file used for the SSBC analysis. The file identifies the failure rates for each of the components of the system. These failure rates are expressed in the number of failures per 10^6 hours. The reason for this is that the *Reliability Prediction of Military Equipment Systems* handbook expresses failure rates in this manner. The file also describes the configuration or layout of the components.

```
comp 80C186 exp(0.13)
comp edac exp(0.15)

parallel RS-422s driver driver

series system 80C186 fpga edac
  MEMORY 85C30 PROMs DRIVERS RS-422s
  CRYSTALS main_conn 422_conn
end

cdf(ssbc_rel)
eval(ssbc_rel) 0.0 0.05259 0.000877
end
```

Figure 5. *Sharpe* Input File Excerpt

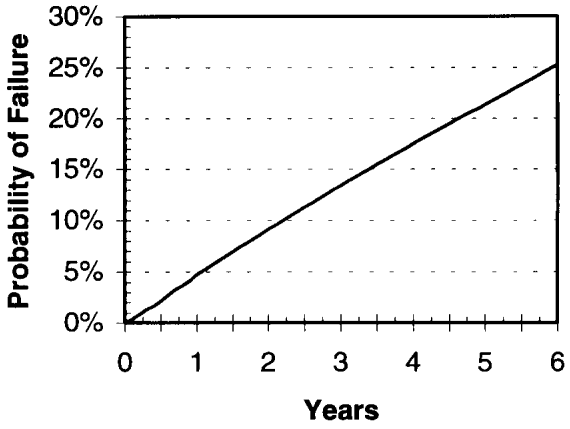

Figure 6. Probability of SSBC Failure

The final portion of the input file instructs *Sharpe* to perform the reliability analysis.

The results from this procedure are presented in Figure 6. The plot represents the probability of the SSBC failing over a six year period of time. Because failure rates were determined using devices with "similar" characteristics, and not from actual device qualification, the accuracy of this plot has a particular level of uncertainty. As stated earlier, the main purpose for conducting this reliability study was to identify "weak links" or single-point failures in the design. With this information, the engineer can concentrate on increasing the quality and level of fault tolerance in these portions of the design.

5.0 SPACE DESIGN CONSIDERATIONS

5.1 Radiation E~ects on Semiconductors

The computer system of a satellite is extremely vulnerable to radiation failure due to the inherent nature of its sub-components. Numerous methods exist that are designed to protect digital circuitry from both hard and soft failures due to radiation. A hard failure is one that is usually characterized by permanent damage to a system. A soft failure is a temporary condition that affects a system only once, and then ceases to cause further problems. It is a goal of the engineer to design a system which is tolerant or hardened to both types of failure [Moo94]. Various techniques were used throughout the design phase of the SSBC in order to decrease the likelihood of failure due to radiation damage.

5.1.1 Radiation and lonization EJ~ects

The low-earth orbit environment is mostly made up of electrons and protons which are trapped by the earth's magnetic field, protons that are produced by energetic solar events, and cosmic rays. Semiconductors are extremely sensitive to these charged particles, and deposited ionizing radiation charge can cause a change in the electrical characteristics under which a solid-state device operates. After a sufficient amount of charge has accumulated, the electronic device may function incorrectly and eventually fail.

The effects of radiation on a semiconductor device are usually a function of what is called the total dose or total accumulated dose, measured in rads. Although some of the radiation dose received by these devices is due to gamma rays, most is a result of neutrons and charged particles that collide with them. A neutron is a high-energy, uncharged particle that can act as a missile, destroying the structure of the solid-state materials that make up integrated circuits. A charged particle is an electron, proton, alpha particle, or ion that can produce a cloud of electrical charge as it passes through an integrated circuit. Serious failure can occur to the device if this charge appears on the gate of a MOS transistor [Moo94].

5.1.2 Single-Event E~ects

High-density integrated circuits, such as the Hitachi 628512 series SRAM used on the SSBC, can experience what are known as single-event effects during the course of their lifetime in space. Single-event effects occur randomly with time and position within an integrated circuit, and can further be divided into two categories, the single-event upset and the single-event latchup. Although single-event upsets can occur in various IC technologies, such as CMOS and TTL bipolar devices, single-event latchup has almost exclusively been observed in CMOS [Ash92].

5.1.2.1 Single-Event Upset

A single-event upset, or SEU, is a non-destructive error which usually affects logic cells (flip-flops, for instance) in such a way that it can cause a bit in a memory device to change logic states (i.e., 0~1, or 1~0). An SEU is caused by a "spurious", or false, charge created by the transit of a single ionizing particle through a IC chip [Ash92]. Because an SEU normally does not cause permanent damage, it is also referred to as a soft error. The SEU frequency is a function of the packing density of the particular IC.

5.1.2.2 Single-Event Latchup

A single-event latchup (SEL), on the other hand, is often a permanent and destructive byproduct of an SEU, and is sometimes referred to as a hard error. The ionizing radiation particle can actually create a direct VDD to ground connection in an IC transistor, effectively short-circuiting the device. If the chips on the SSBC are not protected by some form of current-limitation, such as series resistors connected to their power pins, they may experience permanent damage [Ash92]. If an SEL occurs, an IC protected by a current-limiting resistor needs to have its power turned off in order to clear the latched state. Restoring the power should return the IC to its normal operating mode.

5.2 System Hardening Methods

5.2.1 Watchdog Timer

The 80C 186 may enter into an endless loop due to a corruption of the software program stored in memory or it may have experienced a single-event latchup. To guard against these possible situations, the SSBC uses what is called a watchdog timer. The watchdog timer is simply a hardware counter that is designed to rollover after a three second period of time. The 80C186 must be programmed to reset the watchdog timer often enough so as not to allow the timer to expire. If for any reason the microprocessor enters into an abnormal mode of execution, the watchdog timer will not be restarted properly and it will reset the entire SSBC.

If the watchdog timer itself should ever malfunction, perhaps due to an SEU or SEL, the entire SSBC may become inoperable. Therefore, it was critical that the watchdog be designed with reliability in mind. A form of redundancy called triple modular redundancy was used to address this issue.

5.2.2 Triple Modular Redundancy

Triple modular redundancy, better known as TMR, is a widely used method of protecting a system from both hard and soft failures. The implementation involves using three identical subsystems that are each carrying out the same functions simultaneously. The output from each subsystem is then processed by a voter circuit which outputs the majority of the three inputs. As long as two of the subsystems are functioning properly, the output will be valid [Moo94].

At first it may seem that TMR requires three times as many resources as non-redundant designs, but when it is used in the development of custom FPGAs, creating a triple-redundant circuit is a fairly simple task. Modern FPGAs, like the Actel 1280A that is used on the SSBC, are capable of implementing designs with upwards of 10,000 equivalent gates. The SSBC FPGA contains several subsystems that use TMR configurations.

5.2.3 Error Detection and Correction

The integrity of the program memory is important for proper operation of the SSBC. A single-bit error in one memory location can cause the 80C186 to enter an endless loop or corrupt important scientific data. The CMOS Hitachi memory is much more susceptible to ionizing dose effects than bipolar logic devices, such as Schottky TTL. By using the IDT 49C465 EDAC unit, the reliability of the SRAM is greatly increased.

There are various methods of error detection and correction, but one of the most commonly used is a modified Hamming code. This scheme involves combining an *n*bit data word with a k-bit parity word to form an *(n* + k) composite word [Man88]. The SSBC uses 16-bit data words combined with a 6-bit check word. During memory read and write cycles, the 49C465 can automatically correct single-bit errors and detect double-bit errors. Both single and double-bit errors trigger a custom 16-bit counter on the Actel FPGA. This "error count" can be read by the 80C186 and used for housekeeping data.

5.2.4 ShieldingMethods

The aluminum skin of CATSAT provides very little attenuation of highenergy particles that may cause damage to internal subsystems of the spacecraft at its orbit altitude of approximately 500 km. Therefore, it is important that proper measures be taken to protect many of the SSBC components that may be more prone to radiation failure.

As an extra level of precaution, each of the SSBC commercial SRAM chips may have a small piece of tantalum adhered to its package. This will effectively increases the total dose tolerance of the chip. Shielding will not protect against single-events effects since cosmic-rays are so energetic that they easily pass straight through the shielding. However, since the SSBC uses EDAC and current-limiting circuitry, recovery from an SEU or SEL will usually be possible.

6.0 SOFTWARE DEVELOPMENT CYCLE

A computer system is not complete without software. The SSBC can be used with many off-the-self operating systems that are designed to run on Intel x86 type architectures. The board does not support MSDOS, however, and care must be taken to ensure that developed code does not include system calls to DOS specific functions. Because a multitasking operating system was not needed for CATSAT, it was decided that a custom task scheduler would provide all the functionality needed to support the mission.

Software development for the SSBC is done using industry standard languages and tools. This is an extremely important consideration when students are responsible for writing most of the software. Using tools that students are already familiar with can greatly increase software development speed by reducing the learning curve associated with using new programs. *Microsoft Visual* C++ compiler was chosen for high-level code development on CATSAT. An Applied Microsystems CODE-TAP in-circuit emulator was purchased for real-time processor analysis and debugging. Paradigm Systems *Debug* and *Locate* programs provide all the necessary functions to help the programmer identify and fix software errors.

A ROM-based debugging tool can also be used for developing code on the SSBC. One such product from Paradigm, called a *ROM Monitor, is* basically a segment of code that is programmed into a small portion of the SSBC's PROM address space. Through the use of a standard serial cable, the user can monitor his or her running code and set software breakpoints using a special

version of *Debug*. Because of its low-cost, a number of *ROM Monitors* could be purchased to allow several programmers to develop software simultaneously. Modified versions of the SSBC with non-rad-hard and commercial-quality replacement chips can bring the cost of test and development boards into the thousand dollar range. At this price level, every programmer could realistically have a complete SSBC software development solution on each of their desks.

7.0 CONCLUSION

The SSBC provides a radiationtolerant, low-cost alternative for satellite projects that cannot afford the several hundred-thousand dollar price tags of most off-the-shelf products. The SSBC offers industry-standard hardware that has been designed specifically for low-earth orbit satellite missions. It supports modern tools for software development and can be used with many commercially available embedded operating systems.

A careful study of the environment and the effects of cosmic radiation on digital circuitry has helped to design a system that can endure the harsh environment of space. Many system-hardening techniques were used throughout the development cycle to protect the system from radiation effects. The SSBC is also rugged enough to survive the tremendous vibrations undergone during the launch process.

Two SSBC boards are being built for the CATSAT mission and one is planned for use onboard JAWSAT. The versatile design of the board allows it to be used in a variety of configurations, from scientific analysis and data collection to command and control operations. A small board outline and low power consumption make the SSBC an ideal solution for today' s very low-cost, small satellite missions.

8.0 ACKNOWLEGMENTS

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