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METHOD 2018.5

SCANNING ELECTRON MICROSCOPE (SEM) INSPECTIONS

1. **PURPOSE.** This method provides a means of judging the quality and acceptability of device interconnect metallization on non-planar oxide integrated circuit wafers or dice. SEM inspection is not required on planar oxide interconnect technology such as chemical mechanical polish (CMP) processes. It addresses the specific metallization defects that are batch process orientated and which can best be identified utilizing this method. Conversely, this method should not be used as a test method for workmanship and other type defects best identified using method 2010.

Samples submitted to SEM shall not be shipped as functional devices unless it has been shown that the device structure, in combination with the equipment operating conditions, is nondestructive.

1.1 Definitions.

1.1.1 **Barrier adhesion metal.** The lower layer of multi-layer metal system deposited to provide a sound mechanical bond to silicon/silicon oxide surfaces or to provide a diffusion barrier of a metal into an undesired area such as aluminum into a contact window.

1.1.2 **Cross-sectional plane.** An imaginary plane drawn perpendicular to current flow and which spans the entire width of the metallization stripe as illustrated in figure 2018-1. Metallization stripes over topographical variations (e.g., passivation steps, cross-overs, bird's head), which are nonperpendicular to current flow, are projected onto cross-sectional planes for purposes of calculating cross-sectional area reductions.

1.1.3 **Destructive SEM.** The use of specific equipment parameters and techniques that result in unacceptable levels of radiation damage or contamination of the inspected semiconductor structure.

1.1.4 **Directional edge.** A directional edge (see figure 2018-2) is typically the edge(s) of a rectangular contact window over which metallization may be deposited for the purpose of carrying current into, through, or out of the contact window for device operation. It should be noted that contact geometry, site of concern, or both may vary and if so, the directional edge concept should be modified accordingly.

1.1.5 **General metallization (conductors).** The metallization at all locations including metallization (stripes) in the actual contact window regions with the exception being at areas of topographical variation (e.g., passivation steps, bird's head, cross-overs).

1.1.6 **Glassivation.** Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area (including metallization), except bonding pads and beam leads.

1.1.7 **Interconnection.** The metal deposited into a via to provide an electrical conduction path between isolated metal layers.

1.1.8 **Major current-carrying directional edge.** The directional edge(s) which is designed to provide a path for the flow of current into, through, or out of a contact window or other area(s) of concern (see figure 2018-2).

1.1.9 **Multi-layer metallization (conductors).** Two or more layers of metal used for electrical conduction that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

1.1.10 **Multi-level metallization (conductors).** A single layer or a multi-layer of metal shall represent a single level of metallization. A combination of such levels, isolated from each other by a grown or deposited layer of insulating material, shall comprise the multi-level metallization interconnection system. The use of vias to selectively connect portions of such level combinations through the isolation shall not effect this definition.

1.1.11 Nondestructive SEM. The use of specific equipment parameters and techniques that result in negligible radiation damage, contamination, or both of the inspected semiconductor structure (see 3.10 and 3.11).

1.1.12 Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited on the die prior to metallization.

1.1.13 Passivation steps. The vertical or sloped surface resulting from topographical variations of the wafer surface (e.g., contact windows, diffusion cuts, vias, etc.).

1.1.14 Via. The opening in the insulating layer to provide a means for deposition of metal to interconnect layers of metal.

1.1.15 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group and assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process.

2. APPARATUS. The apparatus for this inspection shall be a scanning electron microscope (SEM) having resolution of 250Å or less as measured on the photograph at use conditions and a variable magnification of 1,000X to 20,000X or greater. The apparatus shall be such that the specimen can be tilted to a viewing angle (see figure 2018-3) between 0° and 85°, and can be rotated through 360°.

2.1 Calibration. The magnification shall be within ± 10 percent of the nominal value when compared with National Institute of Standards and Technology standard 484 or an equivalent at the magnification(s) used for inspection. The resolution shall be 250Å or less as verified with National Institute of Standards and Technology standard SRM-2069 or equivalent. Magnification and resolution verification shall be performed on a frequency defined by the manufacturer based on statistical data for his SEM equipment.

2.2 Operating personnel. Personnel who perform SEM inspection shall have received adequate training in equipment operation and interpretation of the images and resulting photographs prior to attempting certification for metallization inspection. Procedures for certification of SEM operators for metallization inspection shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity. This shall include provisions for recertification procedures once a year as a minimum.

Operator certifications and recertifications shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

2.3 Procedures. There shall be written procedures for metallization inspection. These procedures shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

3. PROCEDURE.

3.1 Sample selection. Statistical sampling techniques are not practical here because of the large sample size that would be required. The wafer sampling requirements defined in table I, taken in conjunction with specific dice locations within the sampled wafers, minimize test sample size while maintaining confidence in test integrity. These dice are in typical or worst case positions for the metallization configuration.

Note: When die or packaged parts are to be evaluated for wafer lot acceptance and the requirements for wafer selection per Table I cannot be met, the following sample size shall be utilized:

- a. If the die/package part is from a known homogeneous wafer lot (traceability specific to the wafer or wafer lot and objective evidence is available for verification), then the sample size shall be 8 devices randomly selected from the population.
- b. If the die/package part is from a non-homogeneous wafer lot (traceability is unknown or no objective evidence is available for verification), then the sample size shall be 22 devices randomly selected from the population.

Die area submitted for SEM evaluation shall not have been or be located immediately adjacent to the wafers edge, and they shall be sufficiently free of smearing, so that the required inspection can be conducted in an area of undisturbed metallization. Acceptance of the interconnect metallization shall be based on examination of selected die area, using either a single wafer acceptance basis or a wafer lot acceptance basis.

Reference to die or dice within this test method implies the evaluation of a complete function or device. When approved by the qualifying activity, this requirement may be satisfied by the evaluation of a special SEM test vehicle existing within the scribe line (kerf), within each die, or within a special process drop in.

3.1.1 Sampling conditions. This sampling condition applies to devices which have glassivation over the metallization. Steps 1 and 2, which follow, both apply when acceptance is on a wafer lot acceptance basis. Step 2 applies only when acceptance is on a single wafer acceptance basis.

3.1.1.1 Step 1: Wafer selection. From each lot to be examined on a wafer lot acceptance basis, wafers shall be selected as defined by table I. If more than one wafer lot is processed through the metallization operation at one time, each wafer lot shall be grouped as defined by table I and a separate set of wafers shall be selected for each wafer lot being examined on a wafer lot acceptance basis.

3.1.1.2 Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer acceptance basis, or with one or more other wafers on a wafer lot acceptance basis), one of the following sampling conditions may be used at the manufacturer's option:

3.1.1.2.1 Sampling quadrants. Immediately following the dicing operation (e.g., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart. The glassivation shall then be removed from the dice using a suitable etchant process(es) (see 3.3) followed by SEM examination.

3.1.1.2.2 Sampling segment, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

Two segments shall be separated from the opposite side of each wafer (i.e., subsequent to metallization and etching but prior to glassivation). These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination.

3.1.1.2.3 Sampling segment, after glassivation. After completion of all processing steps and prior to dicing, two segments shall be separated from opposite sides of each wafer. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination after the glassivation has been removed using a suitable etchant process(es) (see 3.3).

3.1.1.2.4 Sampling whole wafers, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

After completion of the metallization and etching steps and specimen preparation operation, if applicable (see 3.3), the complete wafer shall be placed into the SEM equipment and four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

No die or contiguous die from the inspected wafer shall be shipped as a functional device unless it is shown that the examination is nondestructive (see 3.10 and 3.11).

3.1.1.2.5 Sampling whole wafers, after glassivation. This condition is destructive. The complete wafer shall be subjected to the specimen preparation operation, if applicable (see 3.3), and then placed into the SEM equipment. Four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

TABLE I. Wafer sampling procedures for various metallization chamber configurations.

Metallization chamber configuration <u>1/</u> <u>2/</u>	Number of wafer lots in chamber <u>3/</u>	Required number of samples per wafer lot		Sampling plans per wafer lot
		Evaporation	Sputtering	
Projected plane view of the Wafer-holder is a circle. Wafer-holder is stationary or "wobblates"	<u>1</u> <u>4/</u>	5	2	Four from near the periphery of the wafer-holder and 90° apart. One from the center of holder. See figure 4.
	2	3, 4, or 5	2	See figure 4.
	3	3 or 4	2	See figure 4.
	4	3	2	See figure 4.
Wafer-holder is symmetrical (i.e., circular, square, etc.). Deposition source(s) is above or below the wafer-holder. Wafer-holder rotates about its center during deposition.	1, 2, 3, or 4 <u>4/</u>	2	2	For each wafer lot, one from the periphery of the wafer-holder, and one from close proximity to the center of rotation. See figure 4. <u>5/</u>
Planetary system. One or more symmetrical wafer-holders (planets) rotate about their own axes while simultaneously revolving about the center of the chamber. Deposition source(s) is above or below the wafer-holders.	1, 2, 3, or 4 per planet <u>4/</u>	2	2	For each wafer lot, one from near the periphery of a planet and one from near the center of the same planet. See figure 4. <u>6/</u>
Continuous feed. Wafers are continuously inserted into deposition chamber through a separate pump down of an airlock (25 wafer nominal load)	<u>1</u> <u>1/</u>	2	2	Two randomly selected wafers from each wafer lot.

1/ In this case, a wafer lot shall be defined as a batch of wafers which have received together those common processes which determine the slope and thickness of the passivation steps on these wafers.

2/ If a wafer-holder has only one circular row, or if only one row is used on a multi-rowed wafer-holder; the total number of specified sample wafers shall be taken from that row.

3/ If there is more than one wafer lot in a metallization chamber, each wafer lot shall be grouped approximately in a separate sector within the wafer-holder. A sector is an area of the circular wafer-holder bounded by two radii and the subtended arc; quadrants and semicircles are used as examples on figure 4.

4/ If the wafer lot size exceeds the loading capacity of the metallization system each processed sub-lot will be sampled as if it was a unique lot.

5/ When evaluation data shows that there is no relationship between SEM results and the physical location of the wafers during the metallization process. It shall be permissible to substitute two randomly selected wafers from each wafer lot. This analysis shall be repeated after each major equipment repair.

6/ Sample wafers need be selected from only one planet if all wafer lots contained in the chamber are included in that planet. Otherwise, sample wafers of the wafer lot(s) not included in that planet, shall be selected from another planet(s).

3.1.2 Sampling Destructive Physical Analysis (DPA) evaluation. Finished product, wafers, or die may be subjected to the test conditions and criteria defined within this test method for the purpose of a DPA evaluation.

3.2 Lot control during SEM examination. After dice selection for SEM examination, the manufacturer may elect either of two options:

3.2.1 Option 1. The manufacturer may continue normal processing of the lot with the risk of later recall and rejection of product if SEM inspection, when performed, shows defective metallization. If this option is elected, positive control and recall of processed material shall be demonstrated by the manufacturer by having adequate traceability documentation.

3.2.2 Option 2. Prior to any further processing, the manufacturer may store the dice or wafers in a suitable environment until SEM examination has been completed and approval for further processing has been granted.

3.3 Specimen preparation. When applicable, glassivation shall be removed from the dice using an etching process that does not damage the underlying metallization to be inspected (e.g., chemical or plasma etch). Specimens shall be mounted for examination in a manner appropriate to the apparatus used for examination. Suitable caution shall be exercised so as not to obscure features to be examined.

Specimens may be examined without any surface coating if adequate resolution and signal-to-noise levels are obtained. If the specimens need to be coated, they shall be coated with no more than 100Å of a thin vapor-deposited or sputtered film of a suitable conductive material (e.g., Au). The coating deposition process shall be controlled such that no artifacts are introduced by the coating.

3.4 Specimen examination, general requirements. The general requirements for SEM examination of general metallization and passivation step coverage are specified below in terms of directional edge, magnification, viewing angle, and viewing direction.

3.4.1 Directional edge. All four directional edges of every type of passivation step (contact window or other type of passivation step) shall be examined on each specimen (see table II).

3.4.2 Magnification. The magnification used for examination of general metallization and passivation steps shall be within the range defined by table II.

3.4.3 Viewing angle. Specimens shall be viewed at whatever angle is appropriate to accurately assess the quality of the metallization. Contact windows, metal thickness, lack of adhesion, and etching defects are typically viewed at the angles of 0° to 85° (see figure 2018-3).

3.4.4 Viewing direction. Specimens shall be viewed in an appropriate direction to accurately assess the quality of the metallization. This inspection shall include examination of metallization at the edges of contact windows and other types of passivation steps (see 3.4) in any direction that provides clear views of each edge and that best displays any defects at the passivation step. This may mean that the viewing angle is perpendicular to an edge, or in parallel with an edge, or at some oblique angle to an edge, whichever best resolves any question of defects at the passivation step (see figure 2018-5).

3.5 Specimen examination detail requirements. Examination shall be as specified herein and summarized in table II. The specimen examination shall be documented in accordance with 3.8.

3.5.1 General metallization. At low magnification, inspect at least 25 percent or 10,000 square mils, whichever is less, of the general metallization on each die for defects such as lifting, peeling, blistering, and voiding. Inspection shall be performed for each layer of each level of metallization.

3.5.1.1 Multi-layer and multi-level metal interconnection systems. Each layer of each metallization level that is deposited shall be examined. The current-carrying layer(s) shall be examined with the SEM after removal of the glassivation layer (if applicable) with a suitable etchant (see 3.3).

3.5.1.2 Barrier/adhesion layers. The examination of barrier/adhesion layers designed to conduct less than 10% of the total current is not required as this is considered a non-conduction layer.

3.5.1.2.1 Barrier/adhesion layer as a conductor. The barrier/adhesion layer shall be considered as a conductor (considering the layer thickness and relative conductivity) provided that the following conditions are satisfied: At least ten percent of the current is designed to be carried by this layer; and this layer is used in the current density calculations. When this occurs the barrier/ adhesion layer and/or the principal conducting layer shall satisfy all of the step coverage requirements collectively as baselined by the manufacturer. Specimen examination shall be in accordance with 3.5 and the accept/reject criteria as defined in 3.7.1. The barrier/adhesion layer(s) shall be examined using either the SEM or optical microscope. The following methods may be used to examine these barrier/adhesion layers:

3.5.1.2.1.1 The Etchback procedure. This involves the stripping of each successive unique layer of metal by selective etching, with suitable etchants, layer by layer, to enable the examination of each layer. Typically, each successive layer of metal will be stripped in sequence to expose the next underlying layer for examination. Successive layer removal on a single die area may be impractical. In this case the wafer area or additional die (dice) immediately adjacent on the slice to the original die area shall be stripped to meet the requirement that all unique layers shall be exposed and examined.

3.5.1.2.1.2 In-line procedure. The wafer(s) shall be inspected for the defined accept/reject criteria immediately after being processed through each unique deposition and corresponding etching operation.

3.5.2 Passivation steps. Inspect the metallization at all types of passivation steps in accordance with the requirements of 3.5.1.1 and table II.

TABLE II. Examination procedure for specimens.

Device type	Area of examination	Examination	Minimum-maximum magnification	Photographic documentation <u>1/</u>
Integrated circuit devices	Passivation steps (contact windows and other types of passivation steps) <u>2/</u>	At least one of each type of passivation step present	5,000X to 50,000X	Two of the worst case passivation steps
	General metallization <u>2/</u>	25 percent	1,000X to 6,000X	Worst case general metallization

1/ See 3.8 (an additional photograph may be required).

2/ See 3.7 for accept/reject criteria.

3.6 Acceptance requirements.

3.6.1 Single wafer acceptance basis. The metallization on a single wafer shall be judged acceptable only if all the sampled areas or dice from that wafer are acceptable.

3.6.2 Wafer lot acceptance basis. An entire wafer lot shall be judged acceptable only when all the sampled areas or dice from all sample wafers are acceptable. If a wafer lot is rejected in accordance with this paragraph each wafer from that wafer lot may be individually examined; acceptance shall then be in accordance with 3.6.1.

3.7 Accept/reject criteria. Rejection of dice shall be based on batch process defects and not random defects such as scratches, smeared metallization, tooling marks, etc. In the event that the presence of such random defects obscures the detailed features being examined, an additional adjacent sample shall be inspected. Illustrations of typical defects are shown in figures 2018-6 through 2018-22.

3.7.1 General metallization. Any evidence of poor metallization adhesion shall be unacceptable. Any defects (see figure 2018-18 and 2018-20), such as voids, cracks, separations, depressions, notches, or tunnels, which singly or in combination reduce the cross-sectional area of the general metallization stripe by more than 50 percent shall be unacceptable. Two specific cases of general metallization are specified below:

3.7.1.1 Conductor stripes. In the examination of the other metal layers for the specific case of conductor stripes (exclusive of the contact window area), a defect consuming 100 percent of the thickness of the barrier/adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe (see figure 2018-22).

3.7.1.2 Barrier layers in contact window areas. No defects of any kind in a barrier layer which would bring the overlying metal layer in contact with the semiconductor material surface shall be permitted.

3.7.1.3 Overlying adhesion layers. For the metal layer(s) above the principal conducting layer, a defect consuming 100 percent of the thickness of the adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe.

3.7.2 Passivation steps. Metallization over a passivation step shall be unacceptable if any combination of defects (see figure 2018-23) or thinning of the metal reduces the cross-sectional area of the metallization stripe along any cross-sectional plane in a major current-carrying direction to less than 50 percent of the cross-sectional area of the stripe. A minimum of 20 percent total metallization coverage (barrier metal inclusive, see figure 2018-24) in the primary current carrying direction will be allowed for metallization over a passivation step when the structure involved is a circular or multisided via or contact structure and there is sufficient wrap-around metal (>10 percent of incoming metal line width) to allow for current flow to all sides of the via or contact. The metallization must meet the current density requirements of MIL-PRF-38535. In cases where an absence of visible edge or a smooth transition or taper clearly reveals effective coverage, a cross-section will be performed to verify metal coverage.

3.7.2.1 Nonrejectable cross-sectional area. In the event that the metallization cross-sectional area at a particular directional edge profile is less than as allowed in 3.7.2. This shall not be cause for rejection if the following two conditions occur:

3.7.2.1.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.1.2 Condition 2. Acceptance shall be on a single wafer basis only.

3.7.2.2 Nonrejectable, noncovered directional edge. For passivation steps to be acceptable, all directional edges shall be covered with metallization and be acceptable to the requirements of 3.7.2.1, unless by design. In the event that a directional edge profile of a particular type of passivation step is not covered with metallization, this shall not be cause for rejection if the following two conditions occur:

3.7.2.2.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.2.2 Condition 2. None of the other specimens from the sampled wafers representing the lot exhibit a directional edge profile from which metal is absent in the major current-carrying directional edge.

NOTE: If both 3.7.2.2.1 and 3.7.2.2.2 are satisfied, a wafer lot acceptance basis shall be used. However, if only 3.7.2.2.1 is satisfied, a single wafer acceptance basis shall be used.

3.7.3 Verification of potential rejects. At the option of the manufacturer, it shall be permissible to subject the specimen, or an adjacent sample that exhibits the same reject mode, to a verification test. Given below are some examples of suitable verification tests:

3.7.3.1 Cross-sectioning. A passivated sample shall be cleaved or lapped down to bisect the area of concern. The sample may then be subjected to an etchant that will remove the interconnecting metallization at the inspection surface (i.e., approximately perpendicular to the die surface). Specimens may be examined without any special surface coating if surface charging is not a significant problem and adequate resolution and signal-to-noise levels are obtained. If the specimens are coated, they shall be coated with a thin vapor-deposited or sputtered film of a suitable conductive material (i.e., 100Å gold). The coating deposition processes shall be controlled such that no artifacts are introduced by the coating. The sample shall be prepared (see 3.3) and examined in the SEM for interconnect metallization thickness or percentage coverage at the passivation step, or any other relevant parameter. Note: This cross-sectioning technique is not conclusive for hairline microcracks as they are not adequately filled by the passivation material.

3.7.3.1.1 Dimensional errors. Care must be taken to ensure that the cross-section is close to the center of a contact in order to avoid dimensional errors due to the rounding of the contact corners.

3.7.3.2 Surface etchback. The unpassivated sample surface is subjected to a chemical etch which removes the interconnection metallization from the surface of the die at a known controlled rate. The etching is stopped when the required metal thickness has been removed. The sample is then prepared (see 3.3) and examined within the SEM for residual metal at the passivation step/contact window interface. Photographic evidence shall then be taken of the sample(s) to support the acceptance or rejection of the material.

3.7.3.3 Topographical integration. A graphical representation of the worst case cross-sectional area is drawn to scale on appropriate graph paper from comprehensive photographs taken eucentrically about the directional edge. The cross-sectional area is then graphically integrated. This technique is useful for evaluating metallization with irregular surface topography.

3.8 Specimen documentation requirements. A minimum of three photographs for each layer of each level of metallization inspected per lot shall be taken and retained for a minimum of five years after performance of the inspection. Two photographs shall be of worst case passivation steps and the third photograph of worst case general metallization. If any photograph shows an apparent defect within the field of view, another photograph shall be taken to certify the extent of the apparent defect (see table II).

NOTE: Alternate methods of image storage (e.g., video disk or video tape) shall be acceptable with the prior approval of the qualifying activity.

3.8.1 Required information. The following information shall be traceable to each photograph:

- a. Date of SEM photograph.
- b. Device or circuit identification (type or part number).
- c. Area of photographic documentation.
- d. Electron beam accelerating voltage.
- e. Magnification.
- f. Manufacturer.
- g. Manufacturer's lot identification number.
- h. Record of calculated/measured percentage step coverage.
- i. SEM operator or inspector's identification.
- j. Viewing angle.

3.9 Disposition of inspected specimens. SEM samples and contiguous die shall not be shipped as functional devices unless nondestructive SEM conditions and requirements are met (see 3.10). In order to be considered nondestructive, suitable life-test data (see 3.11) shall be submitted for approval to the qualifying activity to substantiate the nondestructive aspects of the test (e.g., radiation hardness degradation-RHD). Additionally, all of the conditions in 3.10 and 3.11 must be satisfied.

3.10 Nondestructive SEM conditions. For nondestructive SEM, the following conditions shall apply:

3.10.1 Equipment conditions.

- a. The accelerating voltage shall be within the 0.5 kV to 2.0 kV range.
- b. The absorbed specimen current (as measured with a Faraday cup) shall be less than 500 pA.
- c. Total scan time for each test site on the wafer shall not exceed ten minutes.
- d. Resolution for metal inspection shall be in accordance with 2 above at the accelerating voltage of 3.10.1a. When used for other in-line nondestructive SEM evaluations (e.g., photoresist, critical dimension (cd) inspection, etc.) the resolution shall be sufficient to clearly verify the measurement.

3.10.2 Wafer conditions.

- a. The wafer lot shall satisfy the thermal stability criteria defined within MIL-STD-883, method 5007, table I.
- b. Weekly monitoring of particle counts shall be conducted in the SEM inspection area. The particle count limits shall be less than or equivalent to the specified wafer fab limits.
- c. The wafer shall be clean and free of any surface coating.

3.11 Required data for nondestructive SEM validation. Data demonstrating that the method is nondestructive as defined in A.4.3.2.2 of Appendix A of MIL-PRF-38535 shall be submitted to the qualifying activity following the procedure detailed in 3.11.1 through 3.11.3.

3.11.1 Sample conditioning. Expose a sufficient number of devices to the following conditions to yield a quantity of life test samples that meet a quantity (accept number) of 45(0) for each validation sample:

- a. Sample A: Expose at the worst case SEM operating conditions (i.e., accelerating voltage, absorbed specimen current and tilt) and normal SEM metallization inspection procedure for a duration of 10 ± 1 minutes.
- b. Sample B: Expose at the worst case SEM operating conditions and normal SEM metallization inspection procedure for an increased duration of 30 ± 3 minutes.
- c. Sample C: (Optional at the discretion of the manufacturer.) Control group without any SEM exposure.

3.11.2 Procedure. Process test groups through all normal screening steps to complete post burn-in electricals, serialize test samples, and complete 3.11.2a through 3.11.2d.

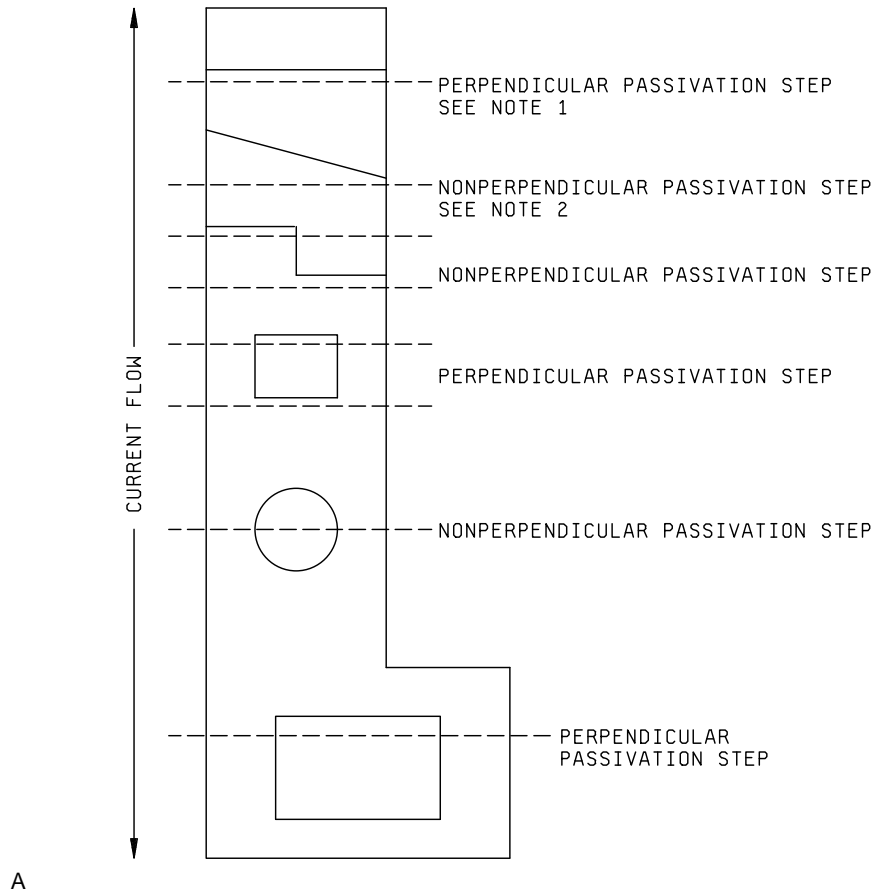
- a. Data log variables on all 25°C dc parameters and record attributes data for all other group A electrical test parameters, conditions and limits specified in the device specification or drawing (i.e., complete group A, not only specified life test endpoints).
- b. Place test samples, including the control group if applicable, on life test in accordance with method 1005 at 125°C minimum for 1630 hours or equivalent (130°C for 1,135 hours, 135°C for 800 hours, 140°C for 565 hours, 145°C for 405 hours, 150°C for 295 hours, 155°C for 215 hours, 160°C for 155 hours, 165°C for 115 hours, 170°C for 85 hours, 175°C for 65 hours) with cooldown under bias using test condition C.
- c. Repeat 3.11.2a for post life test endpoints.
- d. Provide qualifying activity with one set of test results for each sample in terms of variables and attributes data on pre and post life test endpoints plus analysis of mean and standard deviation of variables data and indication of any devices which failed any group A test parameters.

3.11.3 Criteria for validating SEM as nondestructive. If sample A passes single duration and sample B passes triple duration SEM exposure and life test without failing any device specification or drawing parameters, conditions and limits (or delta parameter requirements when they are specified), the SEM procedure shall be validated as nondestructive for the process flow represented by the sample devices and for other devices from the same process flow. With the approval of the qualifying activity, this SEM nondestructive qualification may be performed on appropriate process monitor structures or standard evaluation circuits (SEC's) which represent the process flow.

4. SUMMARY. The following details may be specified in the applicable acquisition document:

4.1 Detail 1. Single wafer acceptance basis when required by the acquiring activity.

4.2 Detail 2. Requirements for photographic documentation (number and kind) if other than as specified in 3.8.



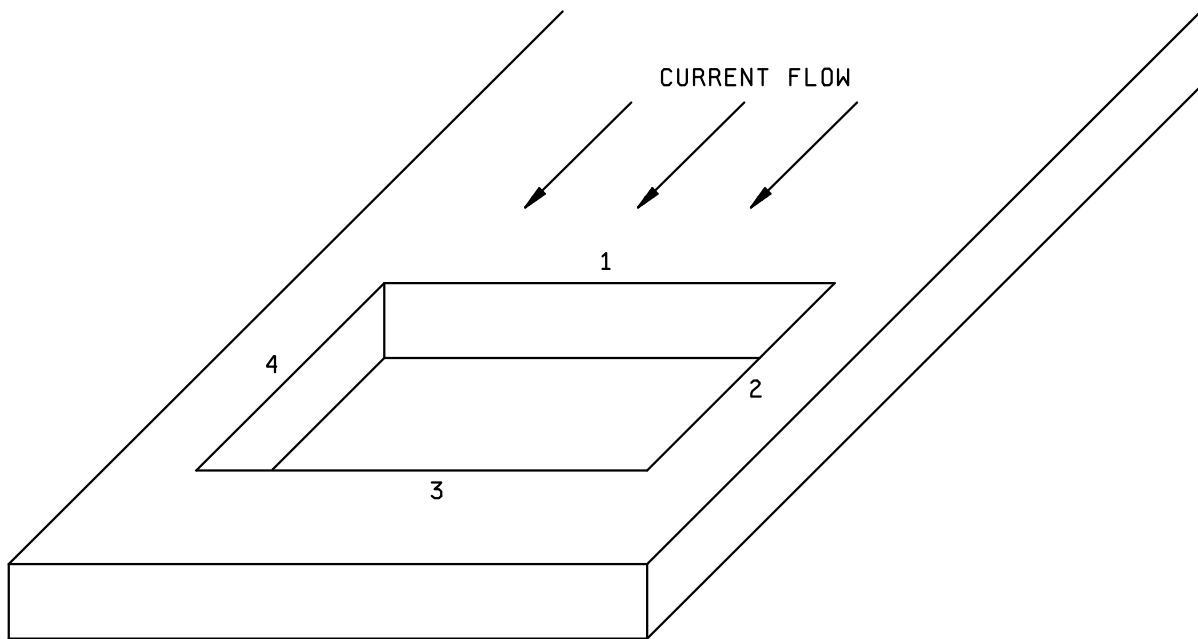
NOTES:

1. Cross-sectional planes are denoted by dashed lines.
2. All passivation steps nonperpendicular to current flow must be projected onto cross-sectional planes perpendicular to current flow for purpose of cross-sectional area calculations.
3. The purpose of this cross-sectional plane illustration is two-fold:

To provide a consistent and convenient means to facilitate the calculation of the appropriate cross-sectional area.

To insure that the cross-sectional area of the metallization in a major current carrying direction is reduced to no more than 50 percent (30 percent when appropriate) for the topographical variation under consideration.

FIGURE 2018-1. Cross-sectional planes at various passivation steps.



NOTES:

1. 1, 2, 3, and 4 are directional edges.
2. 1 is a major current carrying edge.

FIGURE 2018-2. Directional edge.

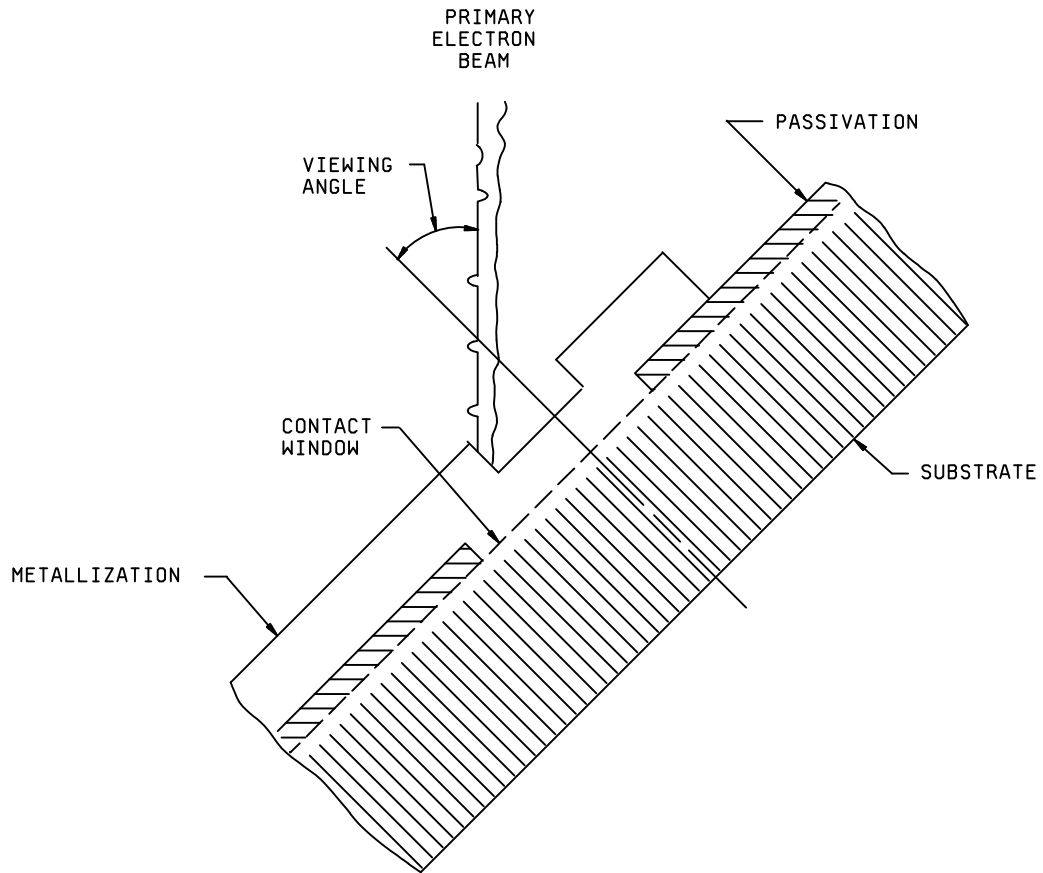
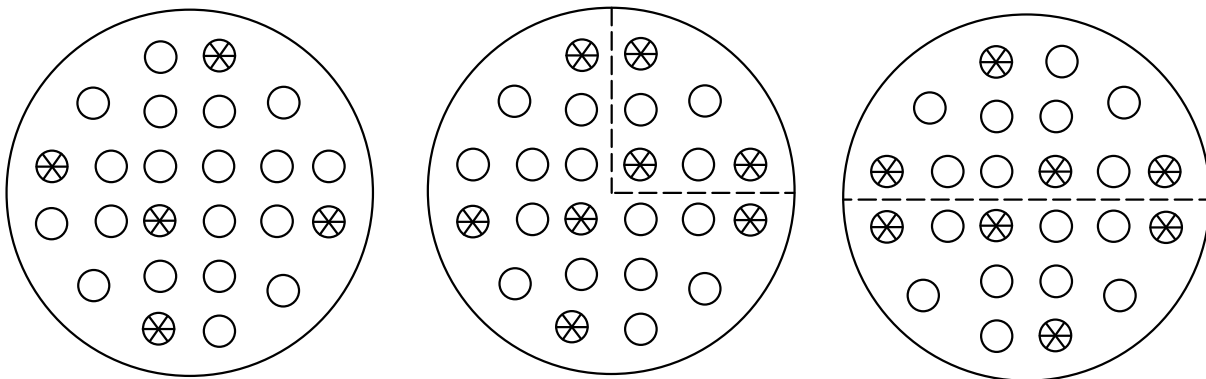


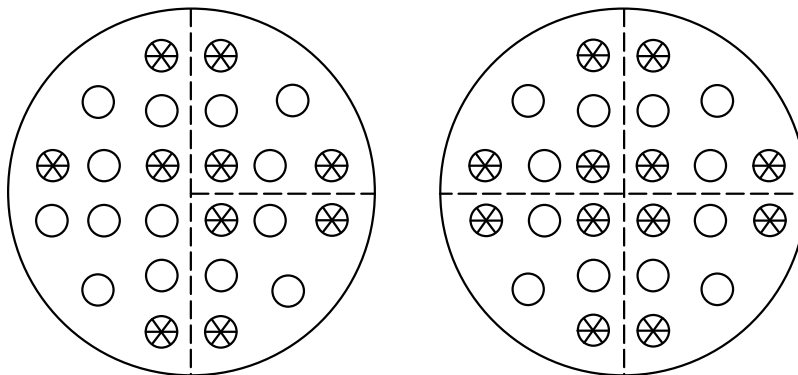
FIGURE 2018-3. Viewing angle.



One wafer lot

Two wafer lots, one
lot considerably larger
than the other

Two wafer lots,
approximately equal
in size

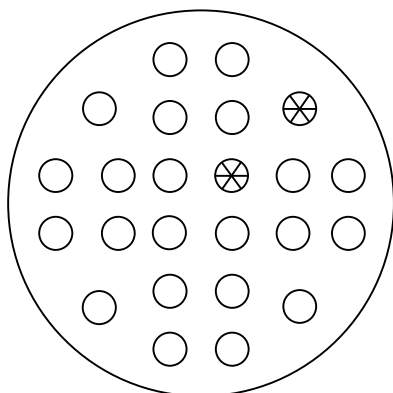


Three wafer lots

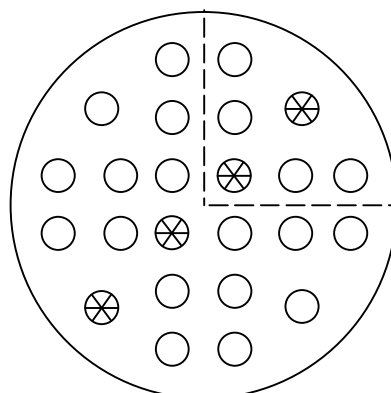
Four wafer lots

STATIONARY (EVAPORATION) WAFER-HOLDER SYSTEM

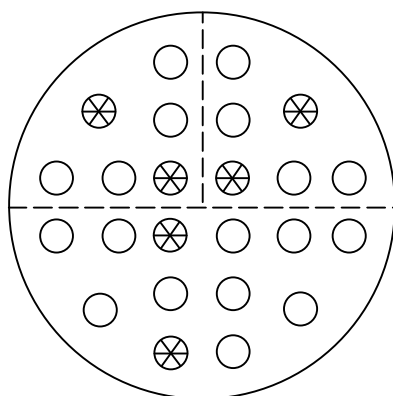
FIGURE 2018-4. Wafer sampling procedures (see table I).



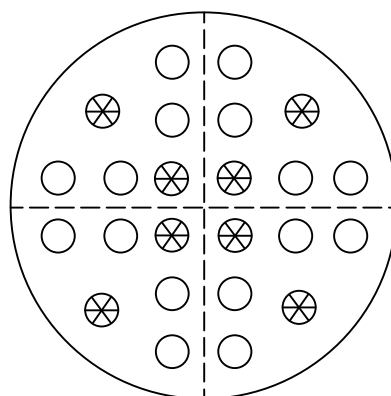
One wafer lot



Two wafer lots



Three wafer lots



Four wafer lots

ROTATING STATIONARY (SPUTTERING) PLANETARY OR CONTINUOUS FEED WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I) - Continued.

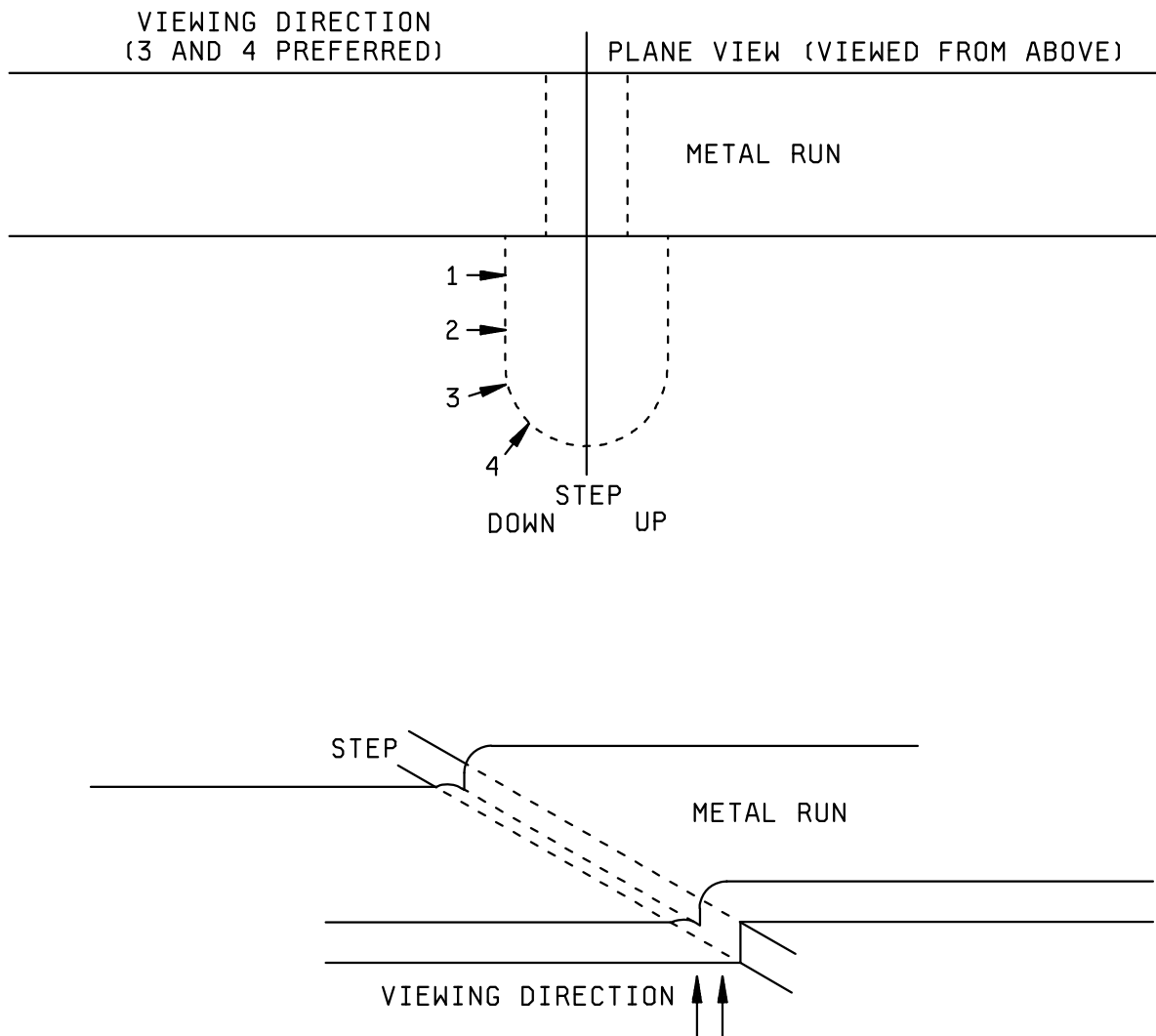


FIGURE 2018-5. Viewing direction.

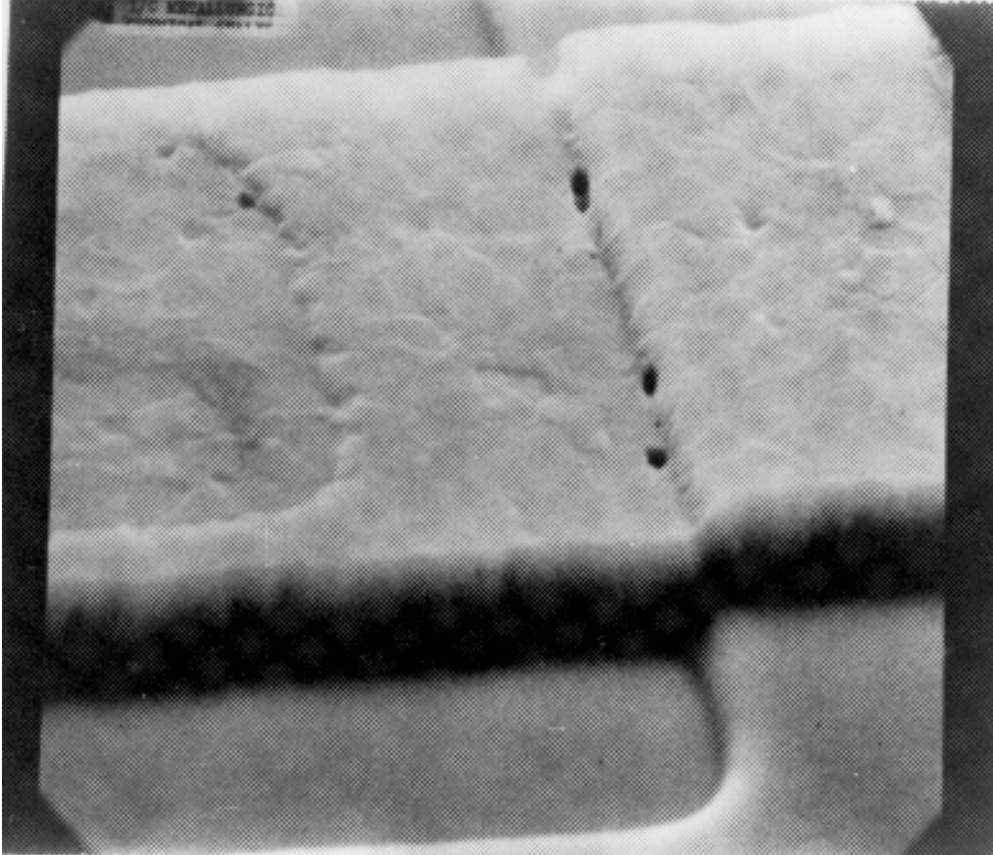


FIGURE 2018-6. (3,400X).
Voiding at passivation step (accept).

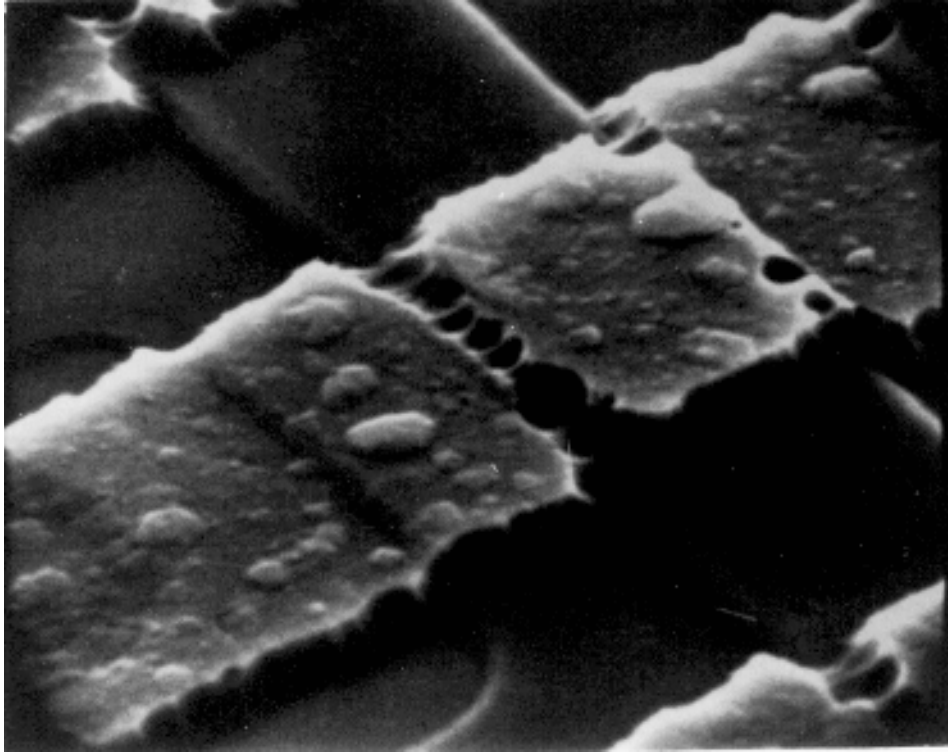


FIGURE 2018-7. 5,000X.
Voiding at passivation step (reject).



NOTE: Tunnel does not extend to surface
of metal; does not reduce cross-sectional
area more than 50 percent.

FIGURE 2018-8. (10,000X).
Tunnel/cave at passivation step (accept).



FIGURE 2018-9. 5,000X.
Tunnel/cave at passivation step (reject).

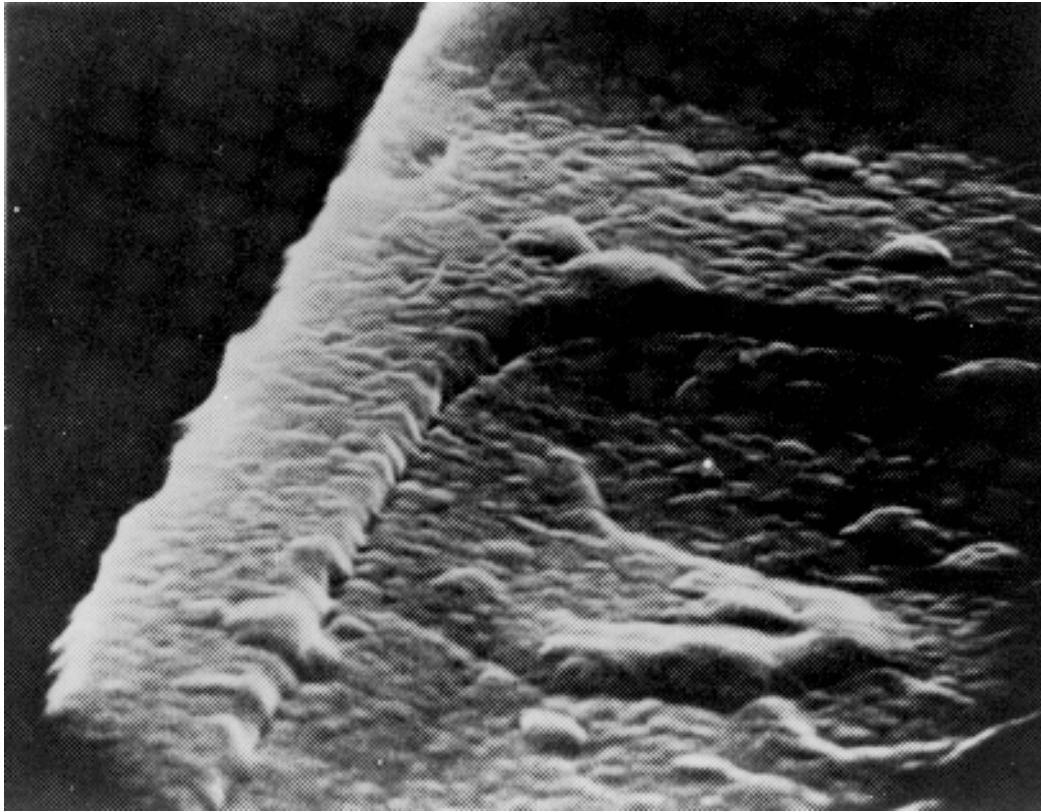


FIGURE 2018-10. (10,000X).
Separation of metallization at
passivation step (base contact) (accept).

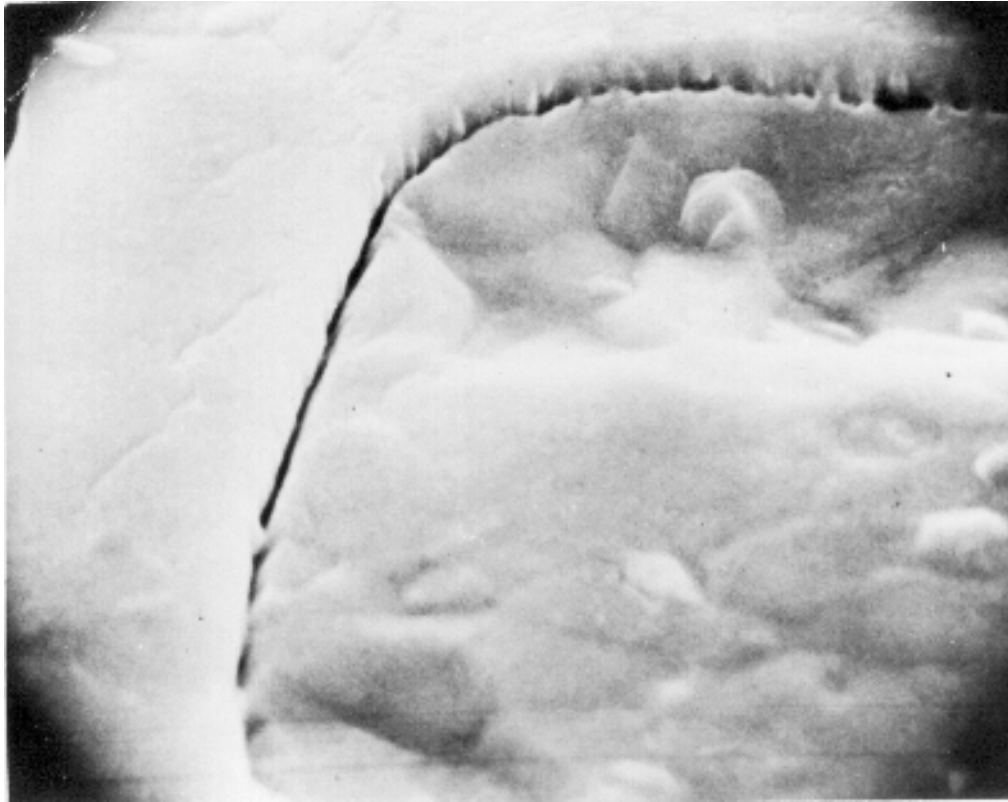


FIGURE 2018-11. 7,000X.
Separation of metallization at
passivation step (base contact) (reject).

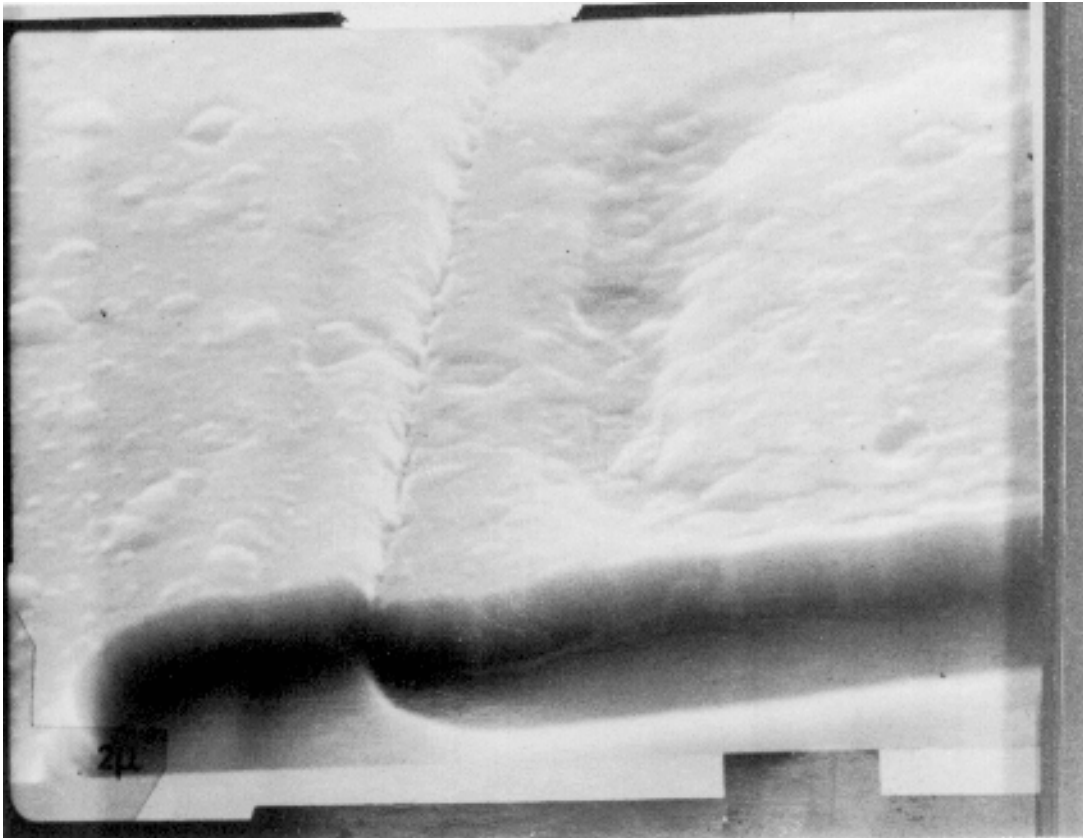


FIGURE 2018-12. (6,000X).
Crack-like defect at passivation step (accept).

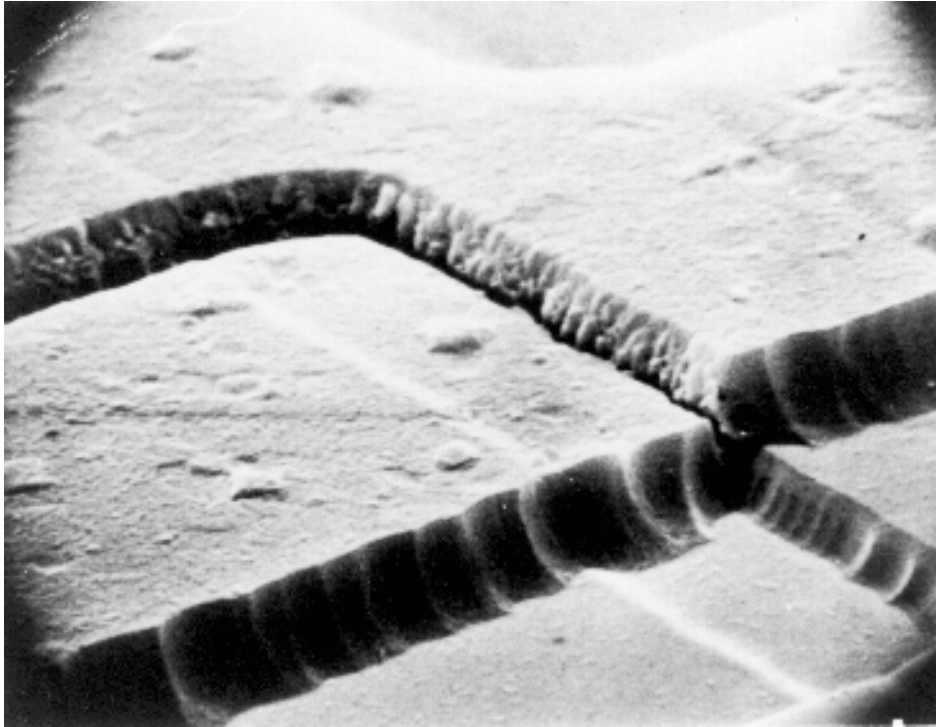


FIGURE 2018-13. 6,000X.
Crack-like defect at passivation step (reject).

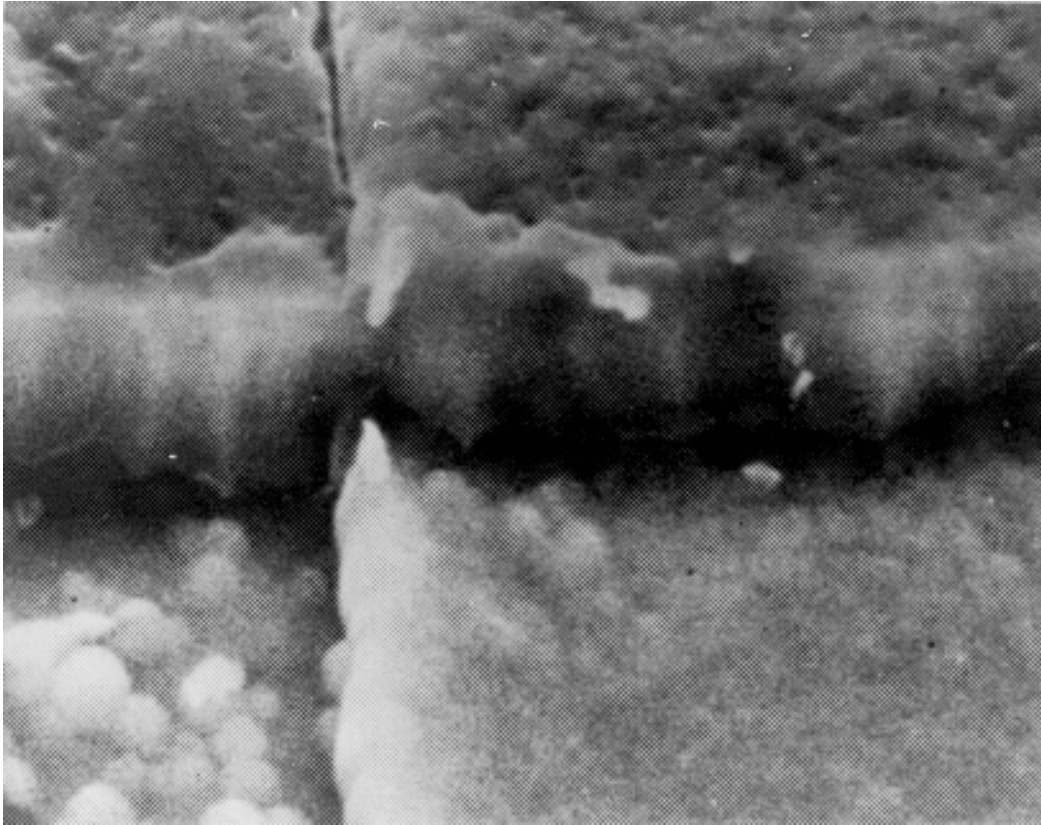


FIGURE 2018-14. (7,200X).
Thinning at passivation step with more than 50
percent of cross-sectional area remaining at
step (multi-level metal) (accept).

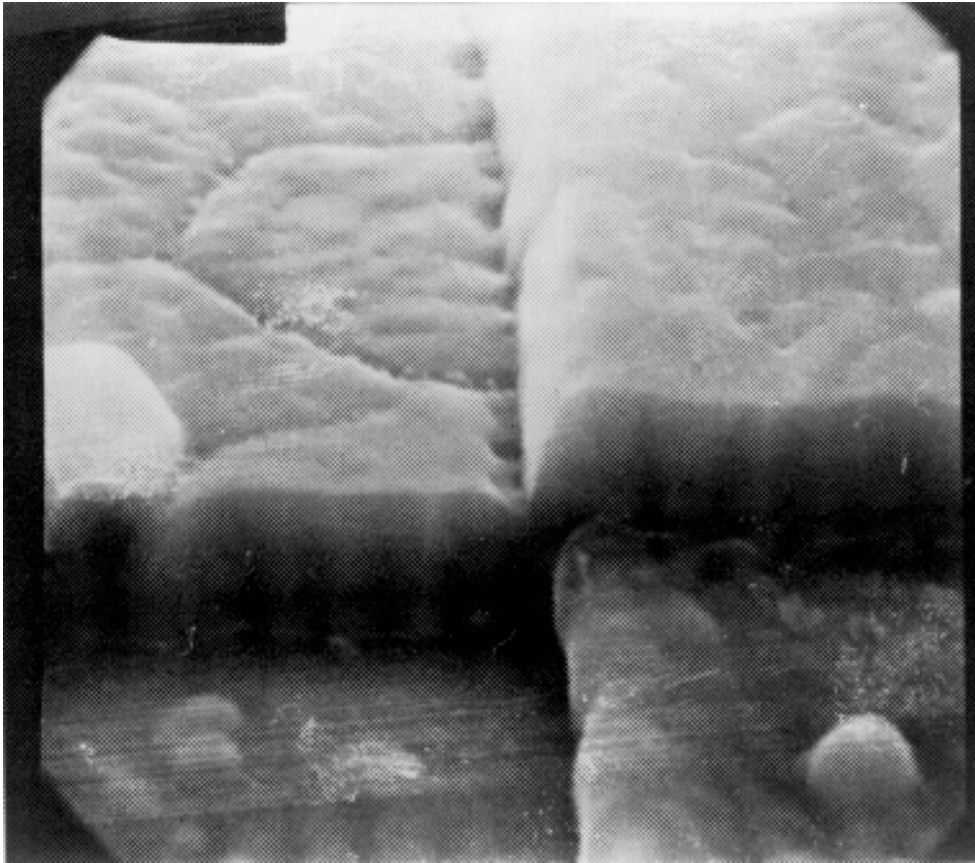


FIGURE 2018-15. 7,200X.
Thinning at passivation step with less than 50
percent of cross-sectional area remaining at
step (multi-level metal) (reject).

*

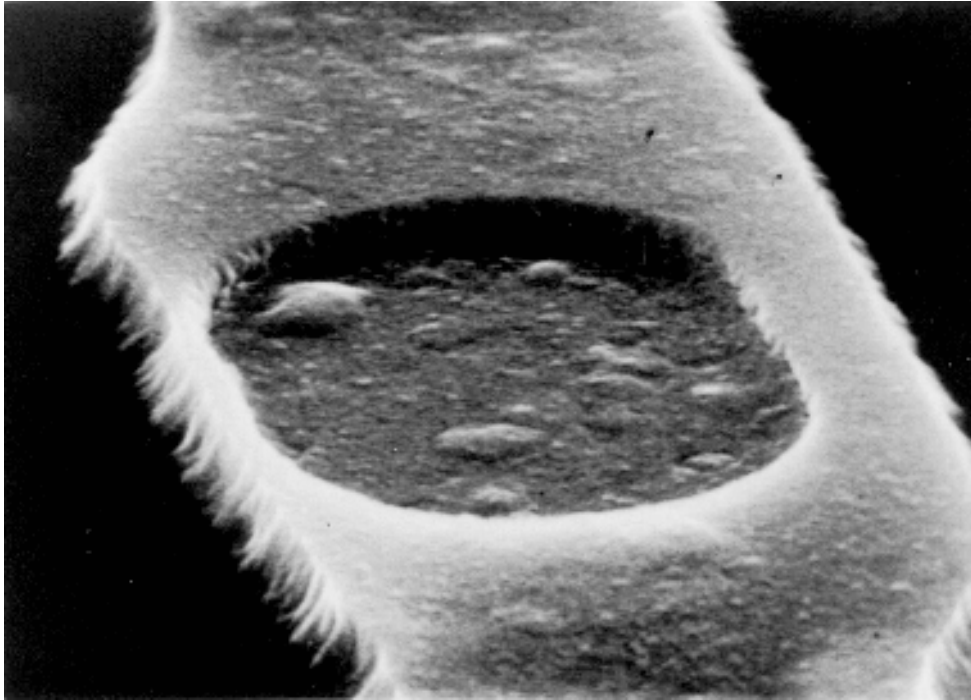


FIGURE 2018-16. (6,000X).
Steep passivation step (MOS) (accept).

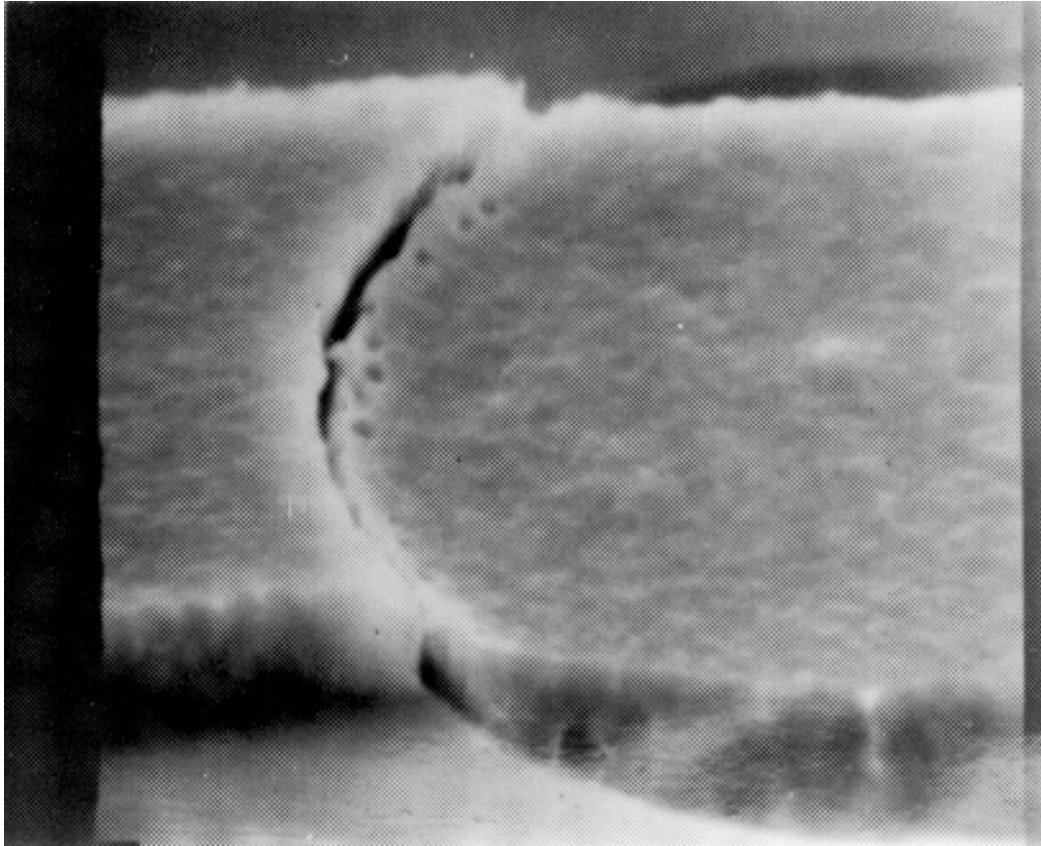


FIGURE 2018-17. 9,500X.
Steep passivation step (MOS) (reject).



FIGURE 2018-18. (5,000X).
Peeling or lifting general metallization
in contact window area (reject).

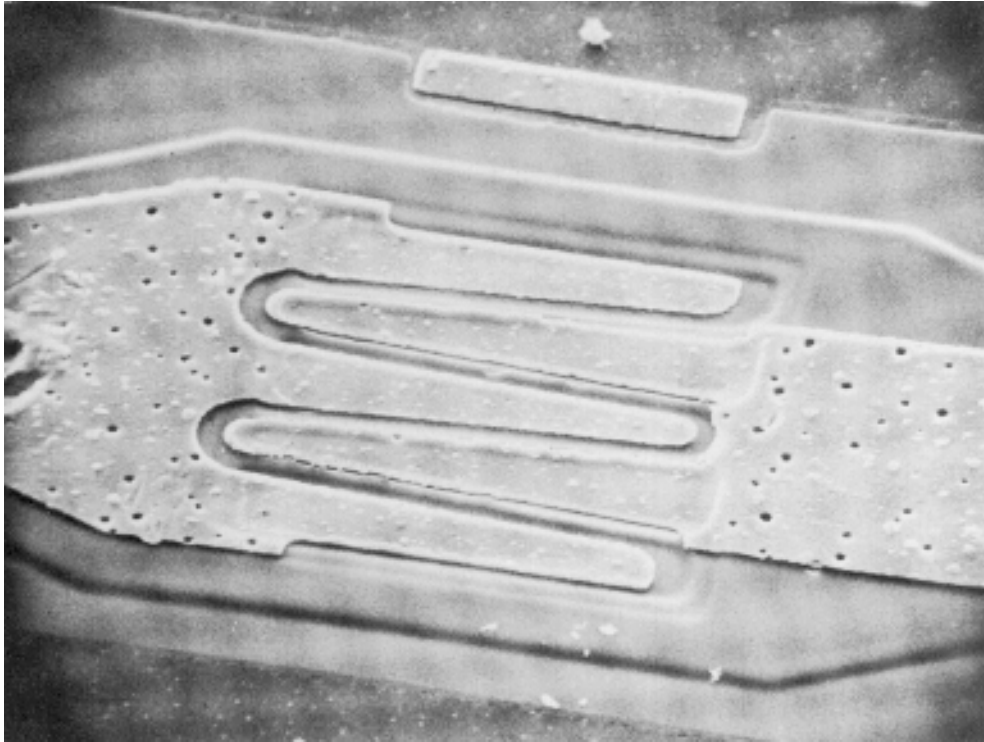


FIGURE 2018-19. 10,000X.
General metallization voids (accept).



FIGURE 2018-20. (5,000X).
General metallization voids (reject).

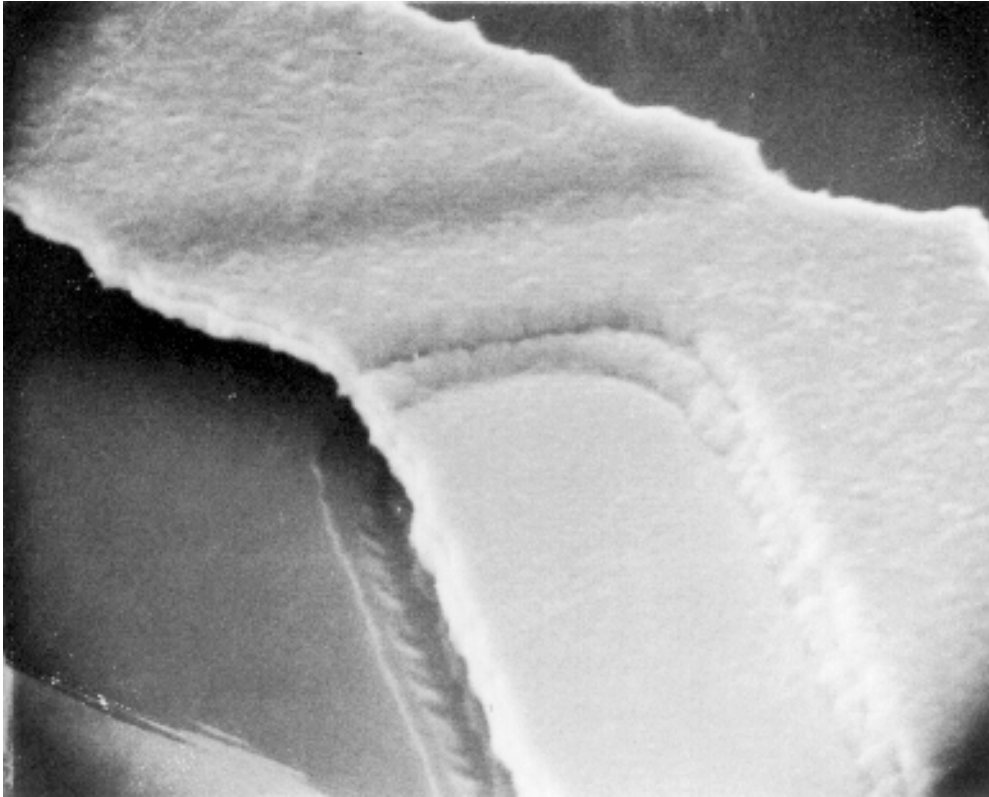


FIGURE 2018-21. 5.000X.
Etch-back/undercut type of notch at
passivation step (multi-layered metal) (accept).

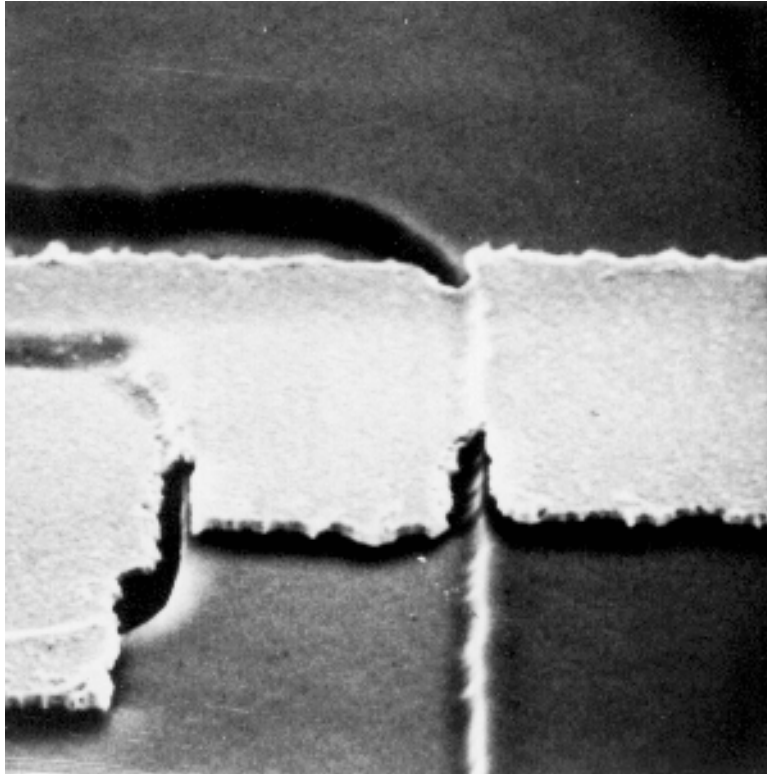
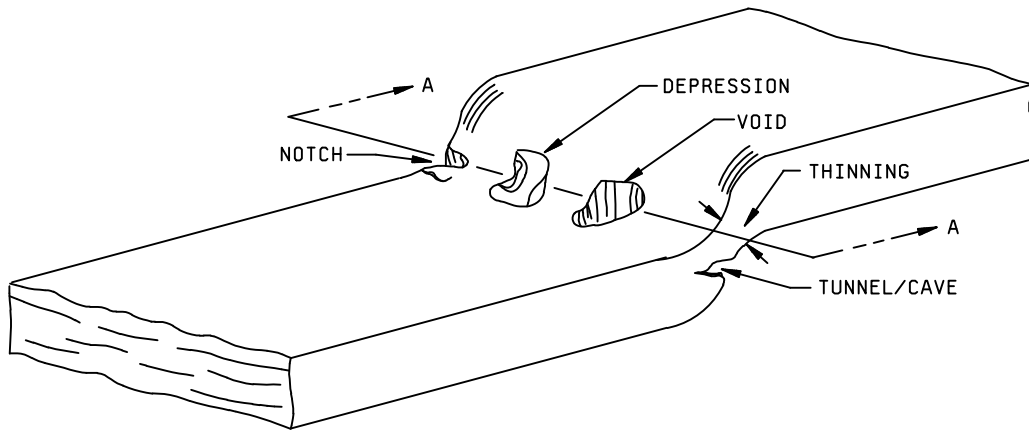
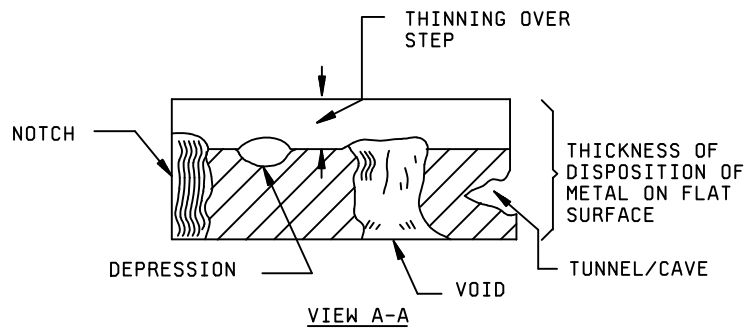


FIGURE 2018-22. (5,000X). Barrier or adhesion layer etch-back/undercut type of notch at passivation step (multi-layered metal) (accept).



METALLIZATION AT PASSIVATION
STEP SHOWING TYPICAL DEFECTS



CROSS-SECTION AREA (ENLARGED) OF METALLIZATION
AT PASSIVE STEP SHOWN ABOVE

FIGURE 2018-23. Concept of reduction of cross-sectional area of metallization as accept/reject criteria (any combination of defects and thinning over a step which reduces the cross-sectional area of the metal to less than the percentage defined within 3.7.2 of metal cross-sectional area as deposited on the flat surface) is cause for rejection.

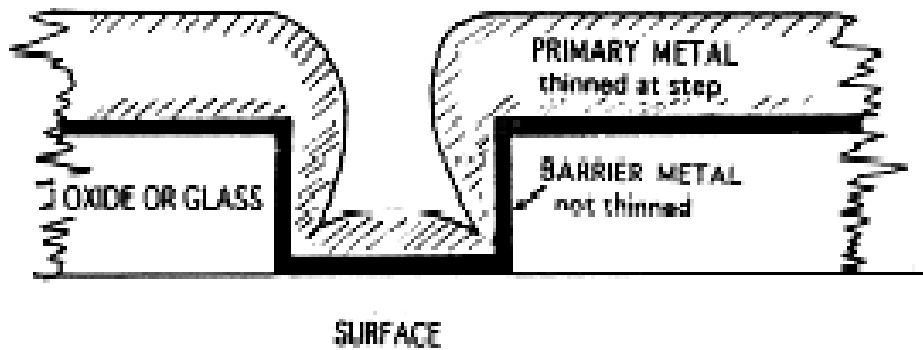
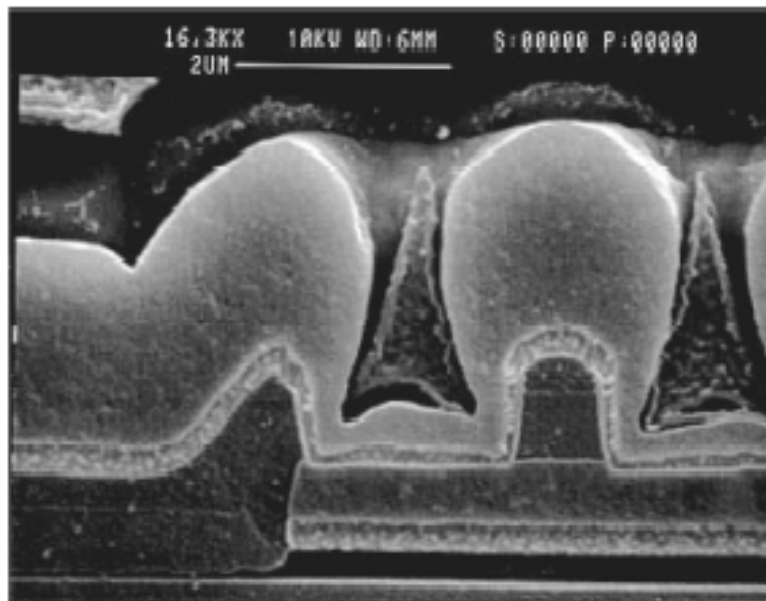


Figure 2018.24 20% metallization coverage (barrier metal inclusive)

APPENDIX A

Metal integrity alternate to SEM inspection

10. PURPOSE. Metal integrity is achieved through a system of designing and building in quality and reliability. It is not practical or cost effective to rely solely on end-of-line testing to ensure metal integrity. This procedure provides a system for designing, building, and monitoring a metal system that withstands the operating conditions of the device for the specified lifetime.

20. SCOPE

20.1 Utilization of this method provides an alternate to the requirements defined in TM2018. This procedure must be used in conjunction with the requirements of alternate 2 of TM5004, paragraph 3.3.1 as it applies to metallization.

20.2 This procedure describes a method by which metal integrity is assured through a combination of design rules and techniques, process development, manufacturing controls and end-of-line screening and reliability testing.

20.2.1 Design controls.

- a. Reliability rules.
- b. Layout rules.
- c. Rules checking.
- d. Process development.

20.2.2 Manufacturing controls. Statistical control of the manufacturing process and equipment defect and foreign material control.

20.2.3 Reliability testing. Accelerated tests.

30. DEFINITIONS

Lifetime. The mean time to failure of a technology at operating conditions defined to be normal. The mean time to failure is measured on a large sample of devices stressed at temperatures and current densities well above the normal operating conditions and extrapolated to normal operating temperature and current density.

Current density. The maximum allowable current density calculated as described in appendix A of MIL-PRF-38535.

Specification limits. Minimum or maximum boundaries for the value of a measured parameter. Material whose measured values are beyond these boundaries must be reviewed and dispositioned.

Worst case operating conditions. Conditions of current and temperature at which a device would normally operate, that would result in the greatest likelihood of failure.

APPENDIX A

40. REQUIREMENTS

40.1 Design controls. Design includes device design and process development. Device design includes all steps and supporting systems needed to translate a functional description for a device into a pattern generating data base. Process development includes selection of materials, tooling, and process conditions that may significantly affect metal integrity. The design process is a major consideration in establishing metal integrity.

40.1.1 A manufacturer's design system must include controlled, documented rules based on the manufacturer's processing capabilities. These rules shall specify feature size and spacing requirements, taking into account size changes that occur during processing. Manufacturers shall be able to justify their rules based on expected process variations. In addition, documented reliability rules shall exist which establish the electrical characteristics for each technology, taking into account processing materials, tolerances and limitations. The manufacturer shall have a system for checking designs for rule violations, and a system for correcting violations. Design rules shall consider the maximum current density (calculated as described in appendix A of MIL-PRF-38535) which shall be determined using worst case operating conditions and taking into consideration current crowding at contacts and vias. The manufacturer shall ensure that worst case processing conditions (such as alignment, metal thickness, line width, and contact/via size) do not result in violation of current density. Current density for a technology shall be at a level such that there is sufficient margin to ensure that failure will not result from electromigration in the specified lifetime of the device.

40.1.2 Process development. The manufacturer's design must take into consideration known levels of defects in the process. The process developed by the manufacturer must produce metallization that has the electrical and mechanical properties consistent with the design rules of 40.1.1, and reliability goals for the technology. Mechanical stress in the metal after final processing shall be understood. The manufacturer shall demonstrate, with results from appropriate designed experiments, that the desired electrical and mechanical properties have been achieved, and that the interaction of other process parameters on metal integrity parameters (minimum list in 40.2) is understood. The initial process specification limits shall be chosen such that metal integrity parameters are within the capability of the process. The manufacturer shall have a change control system in place such that new or changed processes are not put into production without the appropriate reliability evaluation.

40.2 Manufacturing controls. The manufacturer shall establish manufacturing controls in order to achieve uniformly good quality and reliability in their metal system, and to assure that the product is being manufactured according to the assumptions made during design. The manufacturer shall determine which parameters are critical to metal integrity and control those parameters in accordance with EIA-557-A. The manufacturer shall be able to demonstrate control of metal thicknesses, step coverage and cross-sectional areas, metal line width, contact and via sizes, contact and via resistance, and sheet resistance as a minimum, and show that they are being controlled to limits that are consistent with the way the metal system was designed. Specification limits shall be established for these parameters. In addition, defects that threaten metal integrity must be controlled in accordance with the alternate visual procedure (alternate 2) in appendix A of TM5004.

40.3 Reliability testing. While it is desirable to design in and build in reliability rather than to achieve reliability by screening finished product, there is valuable information to be gained from screening and reliability testing. Screening test such as burn-in not only eliminate the weaker parts in a population, but also provide information on failure mechanisms which can be used to improve design, materials, processes, or electrical test. Similarly, accelerated testing is used to speed up failure mechanisms likely to occur under normal operating conditions of a device. These failure mechanisms can then be analyzed to provide a basis for improvement. Accelerated test that a manufacturer may use to this end include but are not limited to electromigration testing, life testing, temperature-humidity-bias testing, and temperature cycling. Structures used in accelerated test must be typical of the technology represented. Failure mechanisms experienced during accelerated testing must be typical of those experienced during normal use of the device.

APPENDIX A

40.3.1 Reliability evaluating. The manufacturer must have in place a system for evaluating the reliability of the metal system. The system shall enable the manufacturer to determine the probability of failure in a given lifetime. The lifetime and failure rate data of the metal system associated with a given technology shall be made available to the customer. The manufacturer's systematically collected data must indicate that there is a high probability of meeting the specified lifetimes and/or failure rates.

50. DOCUMENTATION

NOTE: Certain information considered proprietary may only be available under non-disclosure agreement.

50.1 The manufacturer must have available for customer review controlled reliability rules, layout rules, and current density for each technology for which this procedure is used. In addition, the manufacturer must have available for review the method by which the above rules are checked and verified.

50.2 The manufacturer shall be able to demonstrate the manufacturing controls and system for disposition of out of control occurrences that are in place to control the processes determined critical to metal integrity.

50.3 The manufacturer must have available for customer review any testing performed to evaluate the reliability of the metal system.

50.4 The manufacturer shall specify the metal lifetime to the customer upon request.

*

METHOD 2019.8

DIE SHEAR STRENGTH

1. **PURPOSE.** The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. **APPARATUS.** The test equipment shall consist of a load-applying instrument with an accuracy of ± 5 percent of full scale or 50 grams, whichever is the greater tolerance. A circular dynamometer with a lever arm or a linear motion force-applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

- a. A die contact tool which applies a uniform distribution of the force to an edge of the die (see figure 2019-1). A compliant (conforming) material (e.g., nail polish, tape, etc.) may be applied to the face of the contact tool to ensure uniform force distribution on the edge of the die.
- b. Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate.
- c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die; i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2019-2).
- d. A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing.

3. **PROCEDURE.** The test shall be conducted, as defined herein, or to the test conditions specified in the applicable specific acquisition document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

3.1 **Shear strength.** A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (figure 2019-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

NOTE: For passive elements only attached at the end terminations, the area used to determine the force applied shall be the total area of the mounting surface of the end terminations. An area between and terminations filled with non-adhering filler shall not be used to determine the force applied. However, any adhering material applied between the end terminations shall be used in the shear calculation. If the area between end terminations contains an adhering material, then the area of the adhering material shall be added to the area of the mounting surfaces of the end terminations and that total area shall be used to determine the force applied.

- a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.
- b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.
- c. The die contact tool shall apply a force gradually from zero to a specified value against an edge of the die which most closely approximates a 90° angle with the base of the header or substrate to which it is bonded (see figure 2019-3). For rectangular die, the force shall be applied perpendicular to the longer side of the die. When constrained by package configurations, any available side of the die may be tested if the above options are not available.
- d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.c are met.

3.2 Failure criteria. A device which fails any of the following criteria shall constitute a failure.

NOTE: (See examples for determining DIE AREA following figure 2019-4.)

3.2.1 Epoxy attach.

- a. Fails die strength requirements (1.0X) of Figure 2019-4.
- * b. Separation occurs with a strength greater than the minimum (1.0X) specified in Figure 2019-4, but with less than 2.0 times that strength and evidence that less than 75 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both.

NOTE: Residual element material (silicon or other) attached in discrete areas of the die attach medium shall be considered as evidenced of adhesion.

3.2.2 Eutectic, solder, and other attach.

- a. Fails die strength requirements (1.0X) of Figure 2019-4.
- * b. Separation occurs with a strength greater than the minimum (1.0X) specified in Figure 2019-4, but with less than 1.25 times that strength and evidence that less than 50 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both.
- * c. Separation occurs with a strength greater than the minimum (1.0X) specified in Figure 2019-4, but with less than 2.0 times that strength and evidence that less than 10 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both

NOTE: Residual element material (silicon or other) attached in discrete areas of the die attach medium shall be considered as evidence of adhesion. For metal glass die attach, die attach material on the die and on the package base shall be considered as evidence of acceptable adhesion.

3.2.3 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be recorded.

- a. Shearing of die with residual silicon remaining.
- b. Separation of die from die attach medium.
- c. Separation of die and die attach medium from package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

- a. Minimum die attach strength if other than shown on figure 2019-4.
- b. Number of devices to be tested and the acceptance criteria.
- c. Requirement for data recording, when applicable (see 3.2.1).

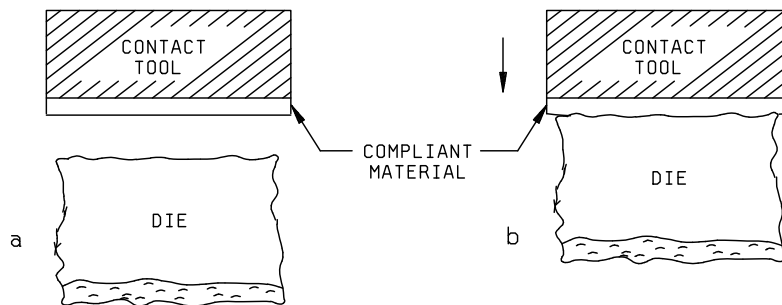


FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

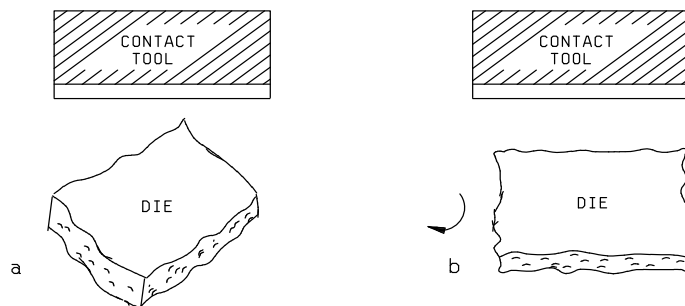


FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

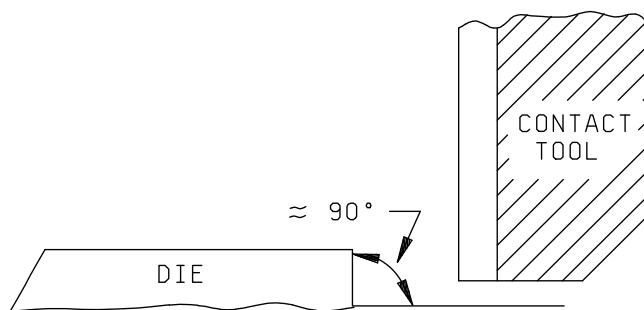
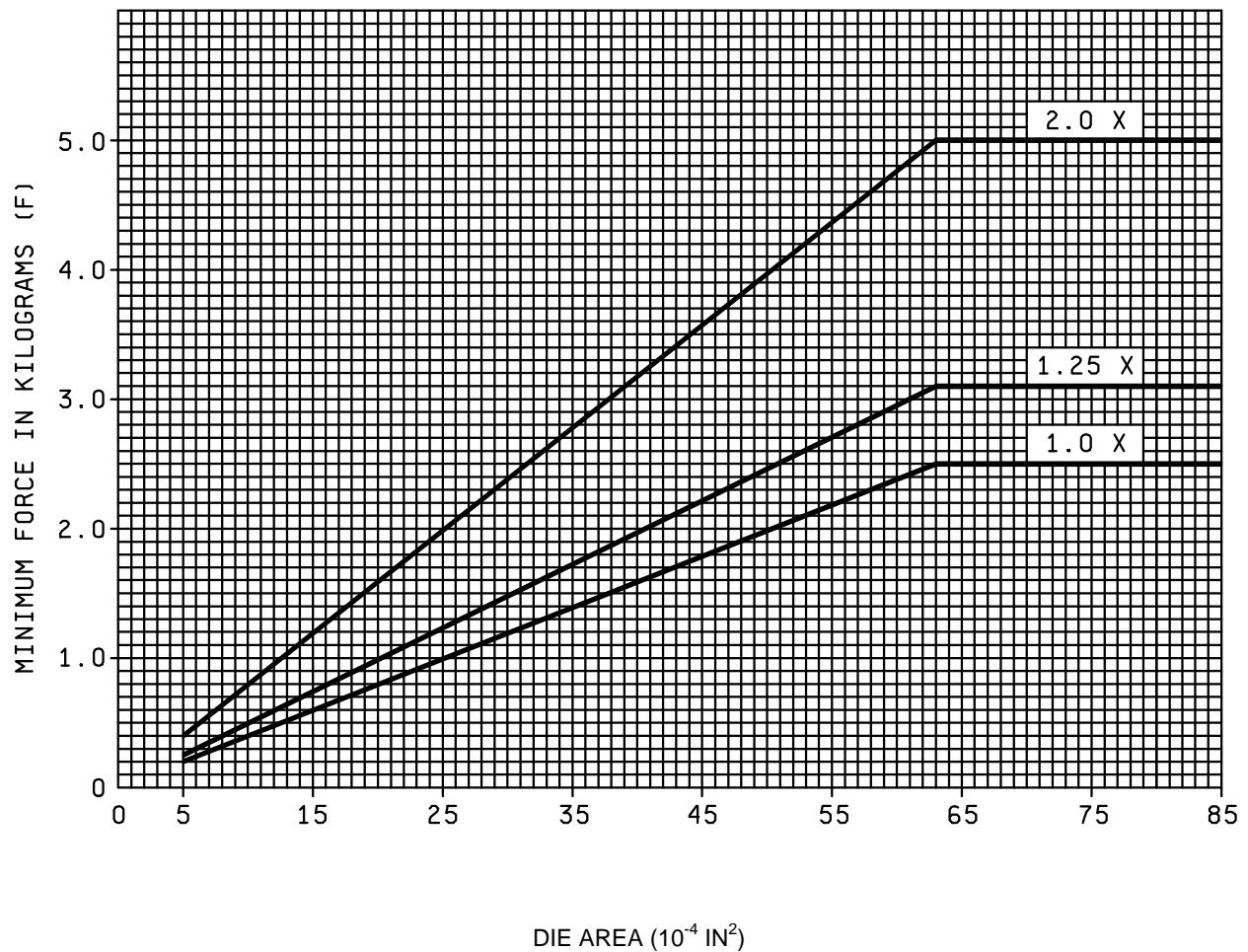


FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle $\approx 90^\circ$ with the header/substrate.



NOTES:

1. All die area larger than $64 \times 10^{-4} (\text{IN})^2$ shall withstand a minimum force of 2.5 kg or a multiple thereof (see 3.2).
2. All die area larger than or equal to $5 \times 10^{-4} (\text{IN})^2$ but smaller than or equal to $64 \times 10^{-4} (\text{IN})^2$ shall withstand a minimum force as determined from the chart of Figure 2019.4. The chart is based on a force of 0.04 kg for every one ten-thousandth (10^{-4}) square inch at (1X) level. Similarly, the required minimum force is 0.05 kg for every 10^{-4} IN^2 at (1.25X) level and is 0.08 kg for every 10^{-4} IN^2 at (2X) level.
3. All die area smaller than $5 \times 10^{-4} (\text{IN})^2$ shall withstand a minimum force (1.0X) of $0.04 \text{ kg}/10^{-4} (\text{IN})^2$ or a minimum force (2X) of $0.08 \text{ kg}/10^{-4} (\text{IN})^2$.

FIGURE 2019-4. Die shear strength criteria (minimum force versus die attach area).

Examples of determining die strength requirements based on die area.

Example 1:

Die Area of device measuring .02 inches by .02 inches.

$$\text{Die Size} = .02 \times .02 = .0004 \text{ IN}^2 = 4 \times 10^{-4} (\text{IN}^2).$$

Because die size is less than $5 \times 10^{-4} (\text{IN}^2)$ use Note 3 which states the value of minimum force required is 0.04 kg/ $10^{-4} (\text{IN}^2)$ at (1X), 0.05 kg/ $10^{-4} (\text{IN}^2)$ at (1.25X), or 0.08 kg/ $10^{-4} (\text{IN}^2)$ at (2X). Thus the associated minimum forces required are 0.16 kg, 0.20 kg and 0.32 kg, respectively.

Example 2:

Die Area of device measuring .04 inches by 0.04 inches.

$$\text{Die Size} = .04 \times .04 = .0016 \text{ IN}^2 = 16 \times 10^{-4} (\text{IN}^2).$$

Because die size is between $5 \times 10^{-4} (\text{IN}^2)$ and $64 \times 10^{-4} (\text{IN}^2)$ use Note 2 which states the value of minimum force required is to be determined based on the chart. The values for die size $16 \times 10^{-4} (\text{IN}^2)$ are found on the chart by reading 16 on the (10^{-4} IN^2) scale, then finding the coordinating force value on the (F) scale. Doing so provides minimum forces required as .64 kg at (1X), .80 kg at (1.25X), and 1.28 kg at (2X).

* Alternately: The chart is based on using .04 kg/ $10^{-4} (\text{IN}^2)$ at (1X), .05 kg/ $10^{-4} (\text{IN}^2)$ at (1.25X), and .08 kg/ $10^{-4} (\text{IN}^2)$ at (2X). Thus: the minimum forces required are $16 \times .04 = .64$ kg (1X), $16 \times .05 = .80$ kg (1.25X), and $16 \times .08 = 1.28$ kg (2X).

Example 3:

Die Area of device measuring .09 inches by .09 inches.

$$\text{Die Size} = .09 \times .09 = .0081 \text{ IN}^2 = 81 \times 10^{-4} (\text{IN}^2).$$

Because die size is larger than $64 \times 10^{-4} (\text{IN}^2)$ use Note 1 which states the value of minimum force required is 2.5 kg or a multiple thereof. Therefore, the minimum forces required are 2.5 kg at (1X), 3.125 kg at (1.25X), and 5.0 kg at (2X).

MIL-STD-883H

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METHOD 2020.9

PARTICLE IMPACT NOISE DETECTION TEST

1. PURPOSE. The purpose of this test is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer.
2. APPARATUS. The equipment required for the particle impact noise detection (PIND) test shall consist of the following (or equivalent):
 - a. A threshold detector to detect particle noise voltage exceeding a preset threshold of the absolute value of 15 ± 1 millivolt peak reference to system ground.
 - b. A vibration shaker and driver assembly capable of providing essentially sinusoidal motion to the device under test (DUT) at:
 - (1) Condition A: 20 g peak at 40 to 250 Hz.
 - (2) Condition B: 10 g peak at 60 Hz minimum.
 - c. PIND transducer, calibrated to a peak sensitivity of -77.5 ± 3 dB in regards to one volt per microbar at a point within the frequency of 150 to 160 kHz.
 - d. A sensitivity test unit (STU) (see figure 2020-1) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ± 20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.
 - e. PIND electronics, consisting of an amplifier with a gain of 60 ± 2 dB centered at the frequency of peak sensitivity of the PIND transducer. The noise at the output of the amplifier shall not exceed 10 mV peak.
 - f. Attachment medium. The attachment medium used to attach the DUT to the PIND transducer shall be the same attachment medium as used for the STU test.
 - g. Shock mechanism or tool capable of imparting shock pulses of $1,000 \pm 200$ g peak to the DUT. The duration of the main shock shall not exceed 100 μ s. If an integral co-test shock system is used the shaker vibration may be interrupted or perturbed for period of time not to exceed 250 ms from initiation of the last shock pulse in the sequence. The co-test duration shall be measured at the 50 ± 5 percent point.
3. PROCEDURES.
 - 3.1 Test equipment setup. Shaker drive frequency and amplitude shall be adjusted to the specified conditions based on cavity size of the DUT (for condition A, see table 1 herein). The shock pulse shall be adjusted to provide $1,000 \pm 200$ g peak to the DUT.
 - 3.2 Test equipment checkout. The test equipment checkout shall be performed a minimum of one time per operation shift. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.
 - 3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency and the shaker amplitude specified. The drive system shall be calibrated so that the frequency settings are within ± 8 percent and the amplitude vibration setting are within ± 10 percent of the nominal values. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between 0.04 and 0.12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of 0.040 inch (1.02 mm).

3.2.2 Detection system checkout. With the shaker deenergized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the attachment medium used for testing the devices. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope. Not every application of the STU will produce the required amplitude. All pulses which are greater than 20 mV shall activate the detector.

3.2.3 System noise verification. System noise will appear as a fairly constant band and must not exceed 20 millivolts peak to peak when observed for a period of 30 to 60 seconds.

3.3 Test sequence. The following sequence of operations (a through i) constitute one test cycle or run.

- a. 3 pre-test shocks.
- b. Vibration 3 ± 1 seconds.
- c. 3 co-test shocks.
- d. Vibration 3 ± 1 seconds.
- e. 3 co-test shocks.
- f. Vibration 3 ± 1 seconds.
- g. 3 co-test shocks.
- h. Vibration 3 ± 1 seconds.
- i. Accept or reject.

3.3.1 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT.

Batch or bulk testing is prohibited.

Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the largest flat surface against the transducer at the center or axis of the transducer for maximum sensitivity. The DUT shall be placed such that the geometric center of the surface contacting the transducer is centrally located on the transducer to within approximately 2 mm of the transducer surface's geometric center. Where more than one large surface exists, the one that is the thinnest in section or has the most uniform thickness shall be mounted toward the transducer, e.g., flat packs are mounted top down against the transducer. Small axial-lead, right circular cylindrical parts are mounted with their axis horizontal and the side of the cylinder against the transducer. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

- (1) Low mass.
- (2) High acoustic transmission (aluminum alloy 7075 works well).
- (3) Full transducer surface contact, especially at the center.
- (4) Maximum practical surface contact with test part.
- (5) No moving parts.
- (6) Suitable for attachment medium mounting.

3.3.2 Test monitoring. Each test cycle (see 3.3) shall be continuously monitored, except for the period during co-test shocks and 250 ms maximum after the shocks. Particle indications can occur in any one or combinations of the three detection systems as follows:

- a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.
- b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.
- c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.

3.4 Failure criteria. Any noise bursts as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods shall be cause for rejection of the device. Rejects shall not be retested except for retest of all devices in the event of test system failure. If additional cycles of testing on a lot are specified, the entire test procedure (equipment setup and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

3.5 Screening lot acceptance. Unless otherwise specified, the inspection lot (or subplot) to be screened for lot acceptance shall be submitted to 100 percent PIND testing a maximum of five times in accordance with condition A herein. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices in that run is less than 1 percent and the cumulative number of defective devices does not exceed 25 percent. All defective devices shall be removed after each run. Resubmission is not allowed.

* Note: If the lot count is 100 devices or fewer, or reaches 100 devices or fewer following a run, then no failures are allowed for any subsequent runs to be acceptable.

TABLE I. Package Height vs. Test Frequency for 20g Acceleration (condition A).

Note: The shaker drive test frequency (F) for condition A (see 3.1) is determined by the package internal cavity height using the following formula:

$$F = \sqrt{20 / [(D) \times (0.0511)]}$$

where: D = Average internal package height (in inches).

20 is a constant in this application and is equal to sinusoidal acceleration of 20g.

F is the shaker drive test frequency (in Hz)

Note: The use of this formula is to be limited to frequencies in the range of 40 - 150 Hz and should not be used for package heights giving frequencies outside this range unless a frequency outside this range is approved by the acquiring activity.

Based on the formula above, the following table is generated to show some typical values:

Average Internal Cavity Height (D)			Test Frequency
Mils	mm	inches	Hz
18	.46	0.018	147
30	0.76	0.030	114
40	1.02	0.040	99
50	1.27	0.050	88
60	1.52	0.060	81
70	1.78	0.070	75
80	2.03	0.080	70
90	2.29	0.090	66
100	2.54	0.100	63
110	2.79	0.110	60
250	6.35	0.250	40

Note: The approximate average internal package height (D) shall be measured from the floor of the package cavity or the top of the major substrate for hybrid or multi-chip assemblies and shall exclude the thickness of the die mounted inside the package.

Example calculation: Assume an average internal cavity height of 70 Mils.

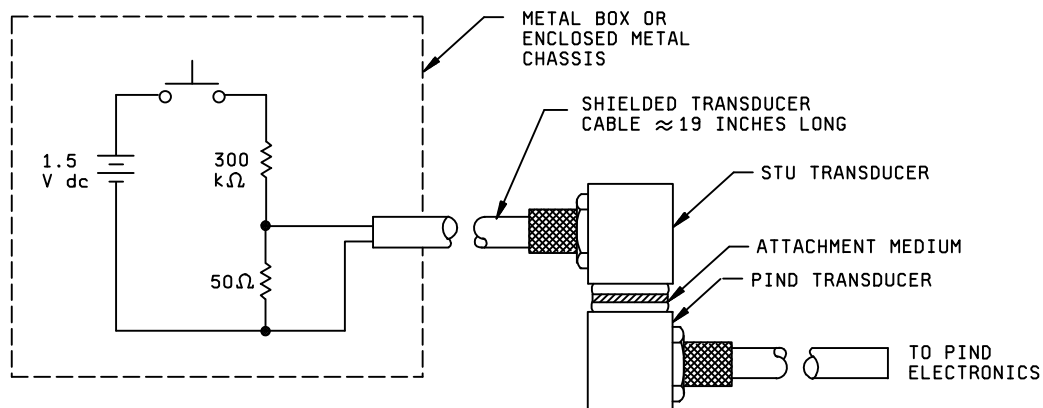
$$F = \sqrt{20 / [(D) \times (0.0511)]}$$

D = 70 Mils converted to inches = .070 inches.

$$F = \sqrt{20 / [(0.070) \times (0.0511)]} = \sqrt{20 / [0.00358]} = \sqrt{5586} = 75 \text{ Hz}$$

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- Test condition letter A or B.
- Lot acceptance/rejection criteria (if other than specified in 3.5).
- The number of test cycles, if other than one.
- Pre-test shock level and co-test shock level, if other than specified.



NOTES:

1. Pushbutton switch: Mechanically quiet, fast make, gold contacts. E.G. T2 SM4 microswitch.
2. Resistance tolerance 5 percent noninductive.
3. Voltage source can be a standard dry cell.
4. The coupled transducers must be coaxial during test.
5. Voltage output to STU transducer 250 microvolts, \pm 20 percent.

FIGURE 2020-1 Typical sensitivity test unit.

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METHOD 2021.3

GLASSIVATION LAYER INTEGRITY

1. PURPOSE. The purpose of this test is to assess the structural quality of deposited dielectric films (e.g., CVD, sputtered or electron beam evaporated glass or nitride, etc.) over aluminum metallized semiconductor devices or microcircuits. The test is directed at identifying process and materials related glass layer defects which result in localized contamination buildup and loss of the advantage given to properly glassivated devices in terms of electromigration behavior at elevated temperature and current density. This is a destructive test.

2. APPARATUS. The apparatus for this test shall consist of suitable sample handling and chemical etching facilities as required for personnel safety. Standard optical microscopes such as those employed in method 2010 shall be used for device inspection. Standard A.C.S. Reagent Grade chemicals shall be used as etchant materials.

3. PROCEDURE. Unless otherwise specified, this test shall be applied to devices which have been through the complete assembly cycle including final package seal. Packaged devices shall be mechanically delidded with minimum thermal stresses applied. Unless otherwise specified, the test sample shall consist of a minimum of one device selected randomly from the inspection lot. One of the following etching procedures shall be used.

3.1 Procedure A. Delidded sample devices shall be completely immersed in the following aluminum etch:

40 Volumes H_3PO_4 (85%)

19 Volumes H_2O

4 Volumes HNO_3 (70%)

This solution shall be maintained at a temperature of $50^\circ\text{C} \pm 5^\circ\text{C}$.

Devices shall be examined during the etching procedure with an optical system, such as a monocular, binocular or stereomicroscope compatible with observation of the immersed samples. Devices shall be etched for twice the amount of time required to completely remove aluminum metallization from exposed bonding pads.

Properly etched devices shall be removed from the heated solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

3.2 Procedure B. Delidded sample devices shall be completely immersed for 20 to 30 minutes at room temperature in the following aluminum etch:

5 Volumes HNO_3 (70%)

80 Volumes H_3PO_4 (85%)

5 Volumes Acetic Acid

10 Volumes Deionized Water

NOTE: The use of a commercial equivalent (e.g., Mity Etch 2) is acceptable.

Properly etched devices shall be removed from the solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

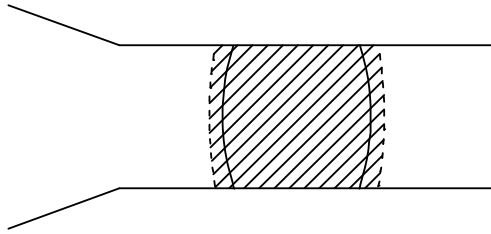


FIGURE 2021-1. Category A - missing glassivation over aluminum.

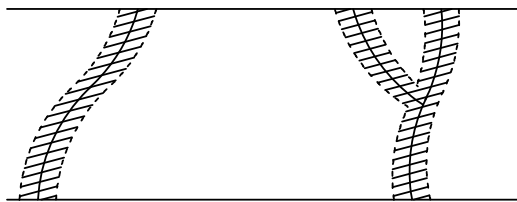


FIGURE 2021-2. Category B - cracks in glass over aluminum.

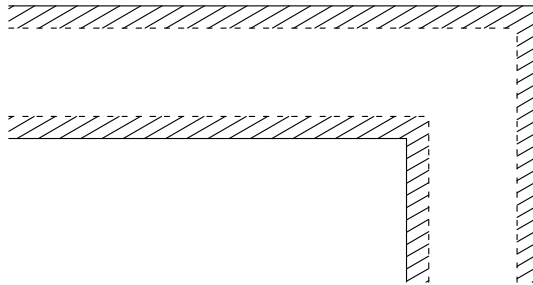


FIGURE 2021-3. Category C - cracks in glass or improper glass coverage along edge of aluminum.

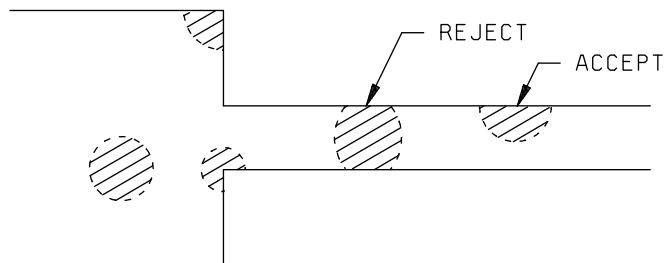


FIGURE 2021-4. Category D - pinholes in glass on top surface and edges of aluminum.

3.2.1 Failure criteria. Lot rejection shall be based on the appearance of etched aluminum, as shown on figures 2021-1 to 2021-7, at any location other than along the edges immediately adjacent to intentionally unglased areas (e.g., bonding pads, die edge, scribe line, etc.) (see 4). This criteria shall be applied only to the interconnect levels which exceed a calculated current density of 2×10^5 A/cm². Category C and D defects, shown on figures 2021-3, -4, -6, and -7 shall not be a cause for rejection unless aluminum is completely removed from the entire width of the conductor stripe. Etched aluminum is determined by changes in the reflecting properties or transparent appearance of areas normally covered with glassivated aluminum.

Failures shall be recorded in terms of the number of devices tested (if other than one) and the number of failures by failure category as defined below:

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- a. When applicable, any intentional omission of glass over the aluminum metallization layer (see 3.1).
- b. If applicable, specific magnification requirements other than as stated in 3.
- c. Sample size if other than one (see 3).
- d. If applicable, special reporting requirements (see 3.1).

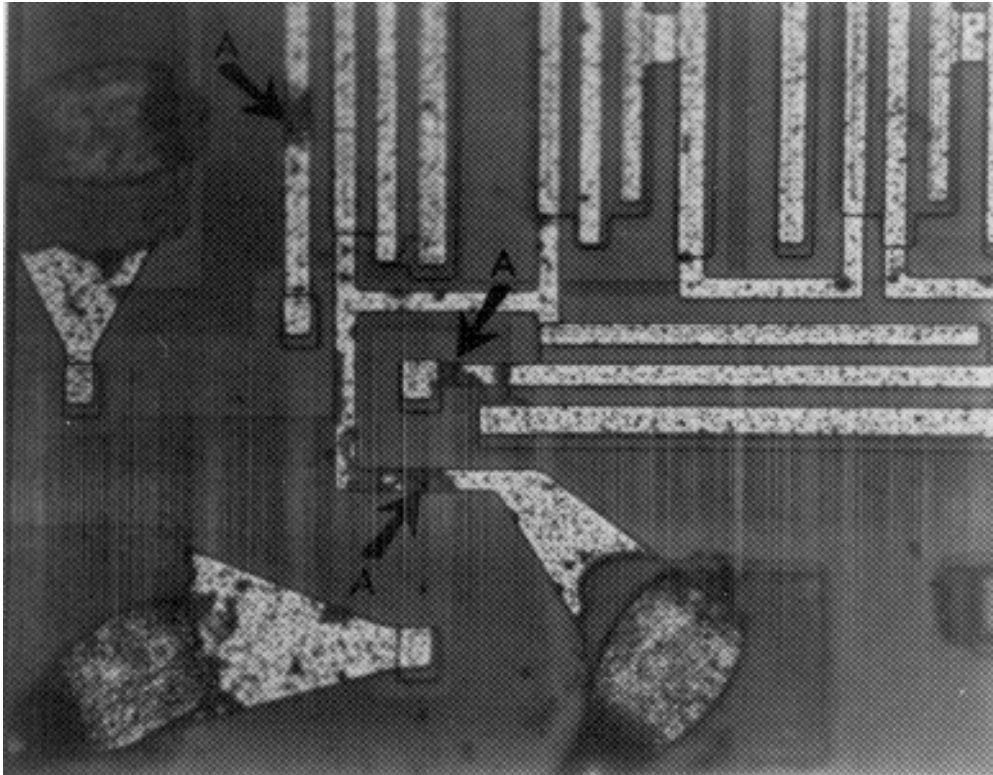


FIGURE 2021-5. Etched device exhibiting failure category A
missing glass over aluminum.

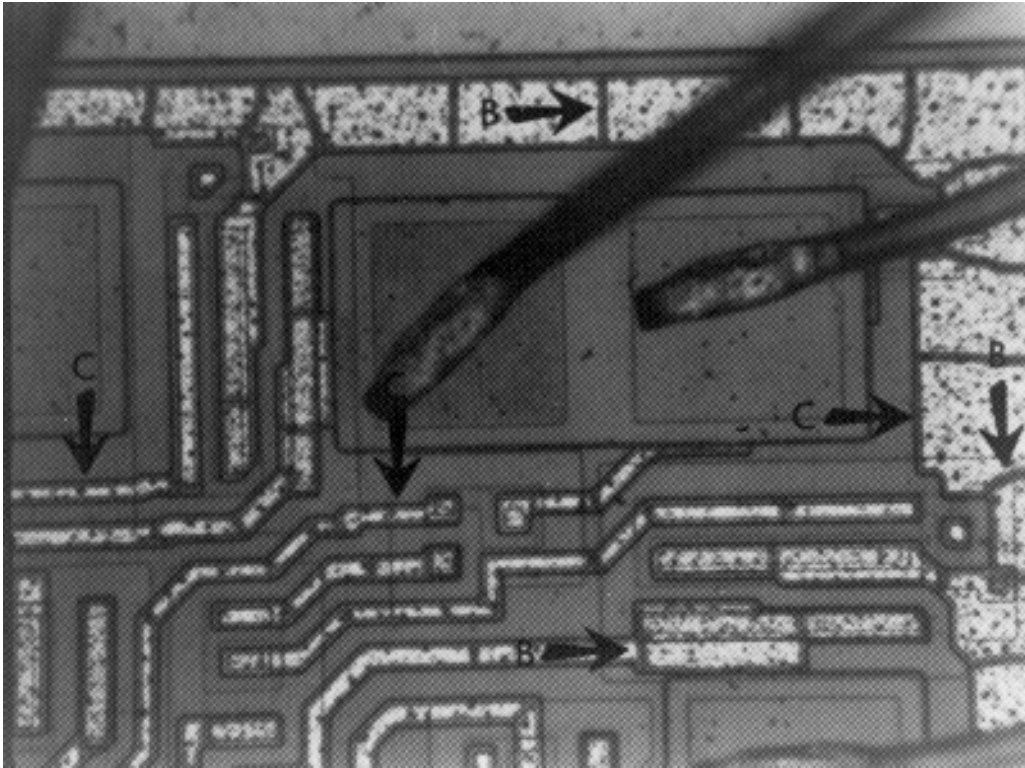


FIGURE 2021-6. Etched device exhibiting failure categories.
B - Cracks in glass over aluminum.
C - Cracks in glass or improper glass
coverage along edge of aluminum.

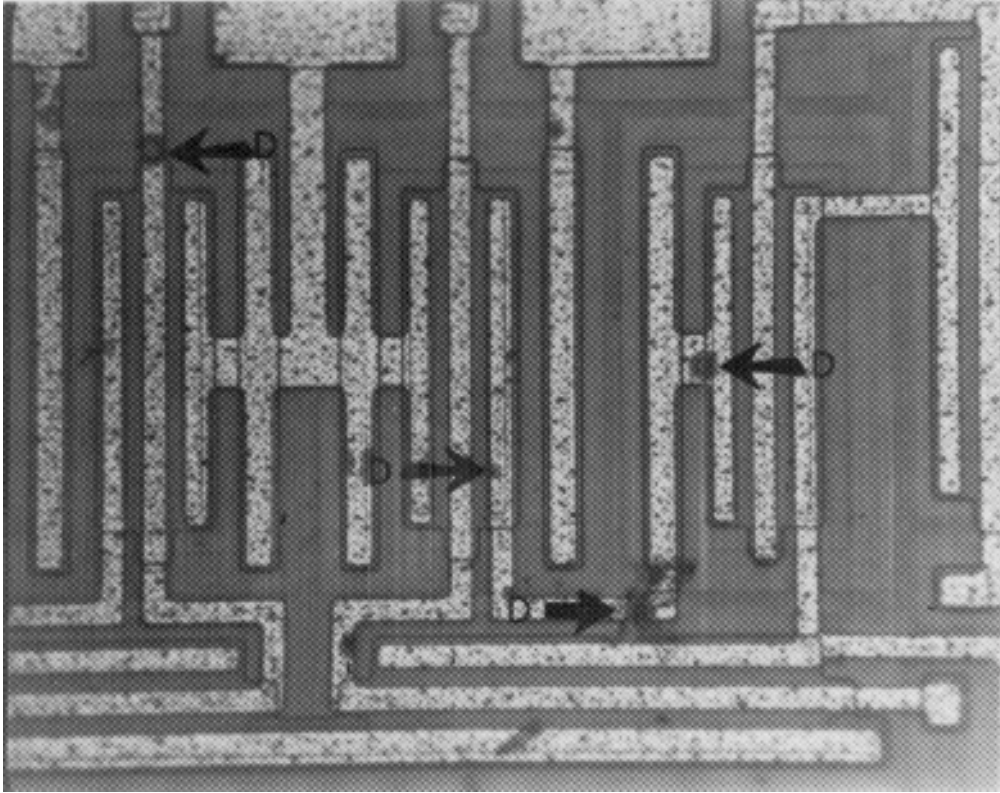


FIGURE 2021-7. Etched device exhibiting category D defects
pinholes in glass over aluminum.

WETTING BALANCE SOLDERABILITY

1. PURPOSE. The purpose of this test method is to determine the solderability of all ribbon leads up to 0.050 inch (1.27 mm) in width and up to 0.025 inch (0.64 mm) in thickness which are normally joined by a soldering operation and used on microelectronic devices. This determination is made on the basis of the wetting time and wetting force curve produced by the specimen while under test.

These processes will verify that the treatment used in the manufacturing process to facilitate soldering is satisfactory and that it has been applied to the required portion of the part which is designated to accommodate a solder connection.

2. APPARATUS.

2.1 Solder meniscus force measuring device (wetting balance). A solder meniscus force measuring device (wetting balance) which includes a temperature- controlled solder pot containing approximately 750 grams of solder shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified in 3.4. The meniscograph apparatus also includes a strip chart recorder which records the force curve for the device tested.

2.2 Dipping device. A mechanical dipping device is incorporated in the Meniscograph, and is preset to produce an immersion and emersion rate as specified in 3.4. The specimen dwell time is operator controlled to the time specified in 3.4.

2.3 Container and cover. A noncorrodable container of sufficient size to allow the suspension of the specimens 1.5 inches (38.10 mm) above the boiling distilled or deionized water shall be used. (A 2,000 ml beaker is one size that has been used satisfactorily for smaller components.) The cover shall be of one or more noncorrodable plates and shall be capable of covering approximately .875 of the open area of the container so that a more constant temperature may be obtained. A suitable noncorrodable method of suspending the specimens shall be improvised. Perforations or slots in the plates are permitted for this purpose.

2.4 Materials.

2.4.1 Flux. The flux shall conform to flux type symbol "A" (flux type "L0") of ANSI/J-STD-004 (previously designated as type "R" of MIL-F-14256).

2.4.2 Solder. The solder shall conform to type Sn63A or Pb37A (previously designated as Sn63 in QQ-S-571) or type Sn60A or Pb40A (previously designated as Sn60 in QQ-S-571).

3. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the applicable acquisition document. During handling, care shall be exercised to prevent the surface to be tested from being abraded or contaminated by grease, perspirants, etc. The test procedure shall consist of the following operations:

- a. Proper preparation of the terminations (see 3.1), if applicable.
- b. Aging of all specimens (see 3.2).
- c. Application of flux and immersion of the terminations into molten solder (see 3.3 and 3.4).
- d. Examination and evaluation of the recordings upon completion of the solder-dip process (see 3.5).

3.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the applicable acquisition document.

3.2 Aging. Prior to the application of the flux and subsequent solder dips, all specimens assigned to this test shall be subjected to aging by exposure of the surfaces to be tested to steam in the container specified in 2.3. The specimens shall be suspended so that no portion of the specimen is less than 1.5 inches (38.10 mm) above the boiling distilled or deionized water with the cover specified in 2.3 in place for 4 to 8 hours. In effect while the manufacturer may accept on the basis of 4 hours aging, the customer/user shall be able to reject on the basis of results after 8 hours aging. Means of suspension shall be a nonmetallic holder. If necessary, additional hot distilled water may be gradually added in small quantities so that the water will continue to boil and the temperature will remain essentially constant.

3.3 Application of flux. Flux, type R shall be used (see 2.4.1). Terminations shall be immersed in the flux, which is at room ambient temperature, to the minimum depth necessary to cover the surface to be tested. Unless otherwise specified in the applicable acquisition document, terminations shall be immersed to 0.16 inch (4 mm) from end of lead. The surface to be tested shall be immersed in the flux for a period of from 5 to 10 seconds.

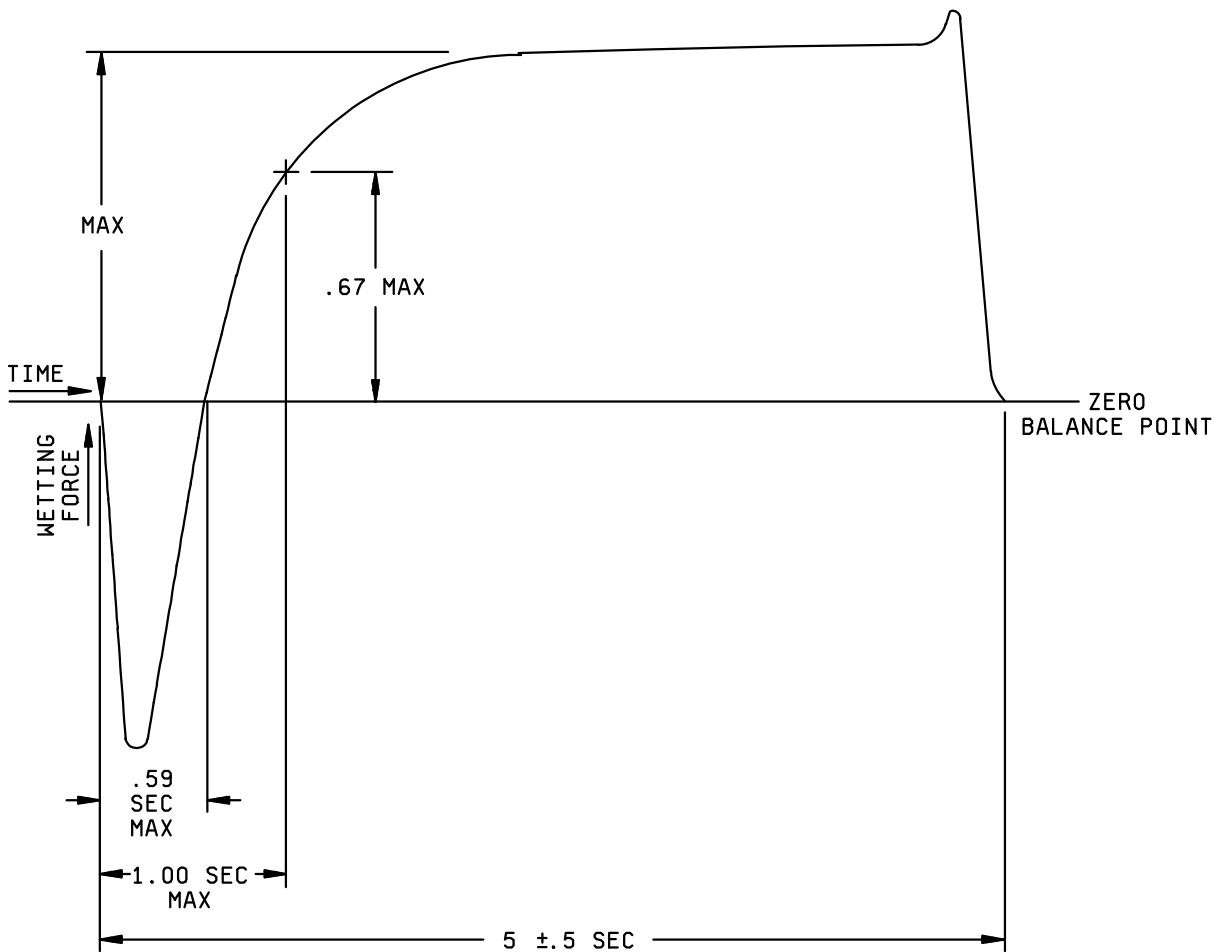
3.4 Solder dip. The dross and burned flux shall be skimmed from the surface of the molten solder specified in 2.4.2. The molten solder shall be maintained at a uniform temperature of $245 \pm 5^\circ\text{C}$. The surface of the molten solder shall be skimmed again just prior to immersing the terminations in the solder. The part shall be attached to a dipping device (see 2.2) and the flux-covered terminations immersed once in the molten solder to the same depth specified in 3.3. The immersion and emersion rates shall be 1 ± 0.25 inches (25.40 \pm 6.35 mm) per second and the dwell time in the solder bath shall be 5 ± 0.5 seconds.

3.5 Evaluation of resultant meniscograph curves from testing of microelectronic leads. The criteria for acceptable solderability during the evaluation of the recordings are:

- a. That the recorded signal trace crosses the zero balance point at or before 0.59 seconds of test time.
- b. That the recorded signal trace reaches two-thirds of its maximum value in 1 second or less of test time (see figure 2022-1).

4. SUMMARY. The following details must be specified in the applicable acquisition document:

- a. The number of terminations of each part to be tested (see 3).
- b. Special preparation of the terminations, if applicable (see 3.1).
- c. Depth of immersion if other than 0.16 inch (4 mm) (see 3.3).
- d. Solder dip if other than specified in 3.4.
- e. Evaluation of meniscograph curves if other than specified in 3.5.
- f. Solder composition, flux, and temperature if other than those specified in 2.4 and 3.4.
- g. Number of cycles, if other than one. Where more than one cycle is specified to test the resistance of the device to heat as encountered in multiple solderings, the examinations and measurements required shall be made at the end of the first cycle and again at the end of the total number of cycles applied. Failure of the device on any examination and measurement at either the one-cycle or the end-point shall constitute failure to meet this requirement.

FIGURE 2022-1. Wetting balance curve evaluation criteria.

MIL-STD-883H

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METHOD 2023.6

NONDESTRUCTIVE BOND PULL

1. **PURPOSE.** The purpose of this method is to reveal nonacceptable wire bonds while avoiding damage to acceptable wire bonds. This procedure is applicable for all bonds made by either ultrasonic or thermal compression techniques, except those larger than 0.005 inch diameter (or equivalent cross section area) that do not have sufficient clearance to permit use of a hook.

The alternate procedure defined in 3.2 may be used for devices with packages having 84 or more external terminations and with nominal bonding wire pitch at the package post of less than or equal to 12 mils.

2. **APPARATUS.** The apparatus of this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ± 5 percent or ± 0.3 gf, whichever is greater.

- a. The diameter of the wire used to make the hook utilized to apply force to the interconnect wire shall be as follows:

<u>Wire diameter</u>	<u>Hook diameter (x wire dia)</u>
≤ 0.002 inch	2.0 x min
> 0.002 inch - ≤ 0.005 inch	1.5 x min
> 0.005 inch	1.0 x min

For ribbon wire, use the equivalent round wire diameter which gives the same cross sectional area as the ribbon wire being tested. Flat portion of hook (horizontal) shall be ≥ 1.25 x the diameter of the wire being tested.

- b. The hook shall be smooth and free of defects which could compromise the test results or damage the wire being pulled.
- c. Travel speed of the hook shall be controlled to that impact loading as the hook initially contacts the wire shall be no more than 20 percent of the specified nondestructive bond pull force.
- d. Final hook placement shall be accomplished under observation at 15X minimum magnification. A microscope with a zoom capability may be used for indexing the hook.
- e. The fixturing which holds the package shall allow positioning the hook for optimum force application to the wire.
- f. An indicator shall either (1) measure the force required to cause failure of the interconnect; or (2) provide visual indication that the predetermined load has been applied.
- g. The hook shall be in a fixed position which restricts motion along a straight line between each bond, so that it will not rise to the highest point which could result in a test for only one bond (e.g., as for a ball bond).

3. PROCEDURE. The test shall be conducted as specified in the applicable acquisition document, as a sample or as a screen, and shall be consistent with the particular bond materials and construction. All bond wires in each device shall be pulled and counted, and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Where there is any adhesive, encapsulant or other material under, on, or surrounding the wire such as to increase the apparent bond strength, the test shall be performed prior to the application of the material.

- a. Set the rate of force application.
- b. Mount the specimen to be tested and set the lifting mechanism to apply the specified force for the appropriate wire size and material.
- * c. The device shall be rotated and positioned such that the hook contacts the wire between midspan and loop apex without causing adverse wire deformation (for forward wedge and ball bonding, this would be between midspan and die edge; for reverse bonding, this would be between midspan and package edge) and the pulling force is applied in a perpendicular direction to the die or substrate surface. See Figure 2023-1.
- * d. The lifting mechanism shall be actuated to stress the wire bond such that the specified stress is applied with minimum impact loading and with no overshoot greater than specified accuracy of the indicator at any time during the bond pull. The dwell time of maximum force application shall be a maximum of one second.
- e. Observe whether the bond breaks.
- f. If the bond breaks, reject the device and proceed to the next device, unless rework is acceptable. If so, record the identification of the broken bond and the device containing the bond. If rework is permitted, all bonds shall be tested prior to any bond rework and reworked bonds shall be tested.
- g. If no bonds on the device break, accept the device as satisfactory.
- h. Repeat a through g for all bonds to be tested.
- i. Record the total number of wires or wire bonds that fail when subjected to the predetermined stress.
- j. Record the number of devices that failed the test.

* 3.1 Failure criteria. Any bond pull which results in separation (of bonds at the bond interface or breakage of the wire or interconnect anywhere along the entire span including bond heels) at an applied stress less than the specified stress for the applicable material and construction shall constitute a failure. Unless otherwise specified, the applied nondestructive pull stress shall be 80 percent of the preseat minimum bond strengths for the applicable material, size and construction given in table I of method 2011 or figure 2011-2 of method 2011. Table I herein lists pull force values for commonly used wire sizes.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$$V_1 = V_2 \sin \theta$$

Where: V_1 = New value to pull test.

V_2 = Table I value for size wire tested.

* θ = Greatest calculated wire loop angle (figure 2023-2).

Also, RF/microwave hybrids that contain tuning wires (designated wires that will alter RF performance when moved) or wires that cannot be accessed with a pull hook must be simulated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, schedule, and elements (electrical rejects may be used). The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2023-3).

*

TABLE I. Nondestructive pull forces.

AL and AU wire diameter (inches)	Pull force (gf) AL	Pull force (gf) AU
0.0007	1.2	1.6
0.0010	2.0	2.4
0.00125	2.5	3.2
0.0013	2.5	3.2
0.0015	3.0	4.0
0.0030	9.5	12.0

NOTES:

1. Nondestructive pull force values for wire sizes not specified shall be 80 percent of the preseat pull forces for aluminum or gold wire given in method 2011.
2. Tolerances shall be ± 0.3 gf for pull forces up to 6 gf and ± 5 percent for pull forces above 6 gf.
3. Any bond subjected to a nondestructive pull force exceeding the specified pull force and the positive tolerance shall be eliminated and not counted toward the PDA failures.

3.2 Alternative procedure. This alternate procedure may be used where 100 percent non-destructive bond pull cannot be performed because of high pin count (greater than or equal to 84 terminals) and small bonding wire pitch at the package post (less than or equal to 12 mils).

*

3.2.1 In-process controls. In order for a manufacturer to use the alternate procedure, a SPC program shall be implemented for the wire bond operation in accordance with EIA-557, Statistical Process Control Systems. Any change in the various effects shown to be significant by the characterization with respect to wire bond strength shall require a re-characterization of the wire bonding process for the changed effect(s) on wire bond integrity. For QML, the SPC program and the requirements listed herein shall be approved by the qualifying activity and may be subject to an audit at any time by the government qualification activity. For Non-Jan devices, the SPC program and the requirements listed herein are subject to review by the government agency responsible for the acquisition or their designee. All statistical evaluation, characterizations, and designed experiments shall be available for review.

3.2.1.1 Applicable incoming materials. Applicable incoming materials including wafer pad metallization targets, package bonding post, and bonding wire shall have their critical characteristics determined and made requirements for acceptance using either incoming inspection or vendor SPC data. Critical characteristics shall include possible sources of material contamination (e.g. excessive carbon content in aluminum wire). Also, the applicable incoming inspection requirements of MIL-PRF-38535 or MIL-PRF-38534 shall apply.

3.2.1.2 Applicable manufacturing processes. Applicable manufacturing processes including bond pad metal disposition, glassivation etch, and worst case package seal excursion shall have their critical characteristics determined and placed under SPC control. Also, the process control requirements of the applicable general specification shall apply for these operations including contamination controls, preventative maintenance procedures and schedules, and complete removal of glassivation from the bonding pad.

3.2.1.3 For packages with gold plated posts. For packages with gold plated posts, the device manufacturer shall perform a bake test on one device from each incoming package lot. This test shall evaluate for basic plating or contamination anomalies of the package post. The package shall be wire bonded post-to-post. The wire bonded package shall be baked at 300 degrees Celsius for 1 hour in either air or inert atmosphere. Bond strength shall then be tested in accordance with MIL-STD-883, method 2011, using a sample size number = 45, C = 0 on the number of wires pulled. If any bond strength failure is determined to be package plating or contamination related then the package lot shall not be used for this alternative unless the defect can be effectively screened and the package lot resampled to a tightened sample size number = 76, C = 0 for the number of wires pulled.

3.2.1.4 An active foreign material control program. An active foreign material control program shall be in accordance with MIL-STD-883, method 2010 or method 2017. A procedure and system for storing and handling wafers, packages, related piece parts, and unsealed devices that will prevent contamination through package seal including face masks, lint free gloves, restrictions on particle generating make-up, hair covers, and cleanroom gowns.

3.2.1.5 A 100 percent pre-bond visual inspection procedure. A 100 percent pre-bond visual inspection procedure of the die pads and package post shall be documented. The visual inspection shall be performed at 100-200X in a class 100 environment. Cleaning to remove rejectable contamination is allowed. No device shall exhibit evidence of the following criteria:

- a. Glassivation on the designed open contact area of the bond pads.
- b. Chemical, film, photoresist or liquid contamination on the pads or posts.
- c. Particulate and /or foreign material contamination on the pads or the critical bond area of the posts greater than 0.25 mils in diameter.
- d. Die pads and package posts that do not meet all applicable requirements of MIL-STD-883, method 2010, condition A or method 2017.

NOTE: 100 percent pre-bond visual inspection may be waived by the qualifying activity provided a 100 percent pre-clean of pads and posts is performed, and all pads and posts for five (5) randomly selected devices pass the inspection criteria. Precleaning may also be waived by the qualifying activity if historical data demonstrates the cleaning is unnecessary. No cleaning is allowed during sample inspection. A 100 percent pre-clean and sample inspection of 5(0) may be repeated a maximum of two times. Rejection of the sample after the second pre-clean shall result in a 100 percent pre-bond inspection of the lot in accordance with 3.2.1.5. An investigation of the rejects in the lot and sample shall be required and corrective action, as necessary shall be instituted. Until then, 100 percent pre-bond inspection is required. Once the effectiveness of any corrective action has been determined, the 100 percent pre-bond inspection may be eliminated.

3.2.1.6 Bonding machine parameters. Bonding machine parameters (e.g., temperatures, pressure, timing, fixtures, wire size, wire material, height settings, etc.) must be defined for each die/package combination. The bonding equipment parameters ranges shall be optimized by designed experiments. The experiments shall consider variations in bonding wire geometry (e.g., loop height, wire length, shelf height, etc.). The experiments shall establish the predicted strength and tolerance of the bonding operation. The allowable performance ranges of the bonding parameters determined by controlled experiments shall be documented. Equipment parameter changes outside the allowable limits must be evaluated and documented as to still meeting the predicted wire pull strength and tolerance.

Note: ASTM Standards F 458 and F 459 may be used as guideline documents.

3.2.1.7 Process capability study. After the wirebond process has been demonstrated to be in a condition of stability and statistical control, a process capability study shall demonstrate that the probability of any device failing the minimum post-seal bond strength is $P < .0001$. The probability must meet the accumulative probability at the device level and not at the individual wire level. The distributional form of the post-seal bond strengths shall be statistically evaluated for conformance to the selected sampling distribution (e.g., Gaussian, lognormal, Weibull, etc.). The capability study sample size shall be sufficient to detect a shift in the distribution of the worst case package/die combination to a 100 parts per million level. The beta risk to the consumer shall be .001 or less. (See Appendix A for normal distribution example.) The process capability study shall be performed periodically. The capability study may be accomplished by characterizing the wire pull strengths of one or more worst case package/die combinations. Selection of the worst case package/die combinations should consider wire geometry, number of wires, pads and post sizes, etc. The characterization results from worst case package/die combinations must be readily extended to all devices.

3.2.1.8 Control limits and action procedures. The results of the evaluations in 3.2.1.6 and 3.2.1.7 shall be used in determining control limits and action procedures for the wire bond operation. A destructive wire bond strength sampling plan for each wire bonder shall include start and completion of each assembly lot, frequency of sampling the assembly lot, and changes in operators (manual wire bonding only), wire spools, package lots, or setup conditions. The bond strength data shall include the force required for failure, the physical location of failure, and the nature of the failure. Electrical rejects from the same wafer lot may be used for the destructive wire bond pulls. In the event that bond wire strengths are outside the predicted values for the wire, or class of wires with similar geometry, the bonder shall be inactivated immediately and not returned to production until tests show that the operation is back under statistical control. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test is required.

3.2.1.9 Time and temperature characterization. Initially, a time and temperature characterization shall be performed for each major type of wire bond metallurgical interface (e.g., gold/aluminum, etc.) to determine the electrical and mechanical integrity of the wire bonds with respect to such factors as; flexing of wire bonds due to thermal expansion, and microcracks or microvoids at the metallurgical interface. Evidence from the characterization shall demonstrate that the integrity of the bonds is sufficient for a device to function over its expected life. Life usage conditions shall exceed 50,000 cycles from a 0 - 85 degree Celsius temperature range at the bonds. Time and temperature degradation factors for accelerated testing must be justified against these minimal life usage conditions.

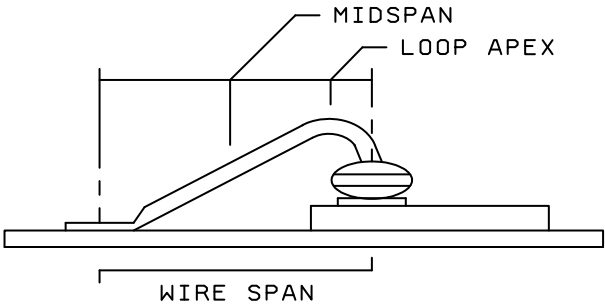
3.2.1.10 Wire bond integrity. If pre-burn-in, interim and post burn-in electrical failures (opens/shorts), qualification, or quality conformance inspection failures indicate questionable wire bond integrity then an analysis is required to verify the bond integrity. If any bond is confirmed to be defective; the applicable inspection lot or subplot will be rejected, an evaluation performed to determine the cause of the bond failure, corrective actions implemented based on the evaluation, and disposition of other affected inspection lots or sublots. The failure analysis and corrective actions will be retained and made available to the qualifying activity upon request.

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3.2.2 Lot acceptance procedure. Each assembly lot shall receive a post-seal bond wire integrity acceptance test. A separate assembly lot acceptance test is required for each wire bonder, and for any changes in setup conditions, wire spool, package lot, or wafer lot, unless such differences have been demonstrated to be statistically insignificant. A post-seal destructive wire bond sampling and test plan with the following minimum requirements shall be documented.

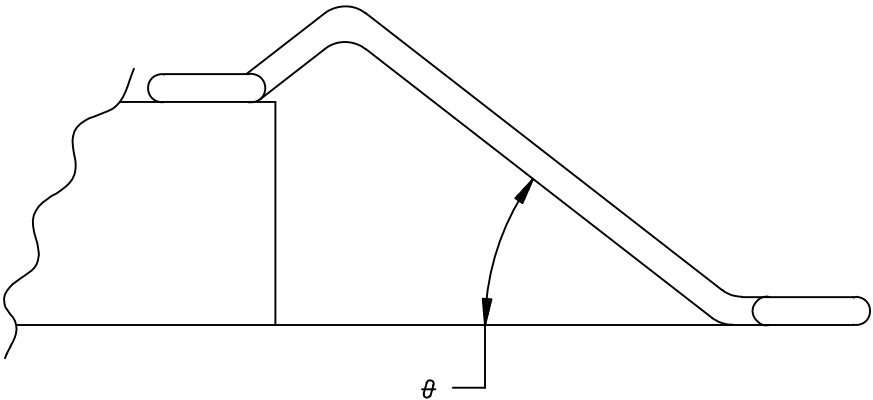
- a. More than one device shall be subjected to the acceptance test. Electrical, non-wire bond related visual, or package seal rejects may be used for the post-seal wire bond test.
 - b. The destructive wire pulls shall be evaluated in meeting the post-seal bond strength limits in MIL-STD-883, Method 2011, or as established in 3.2.1.7. The assembly lot shall be accepted if the wire bond strengths meet the requirements of sections c, d, and e below.
 - c. All wires or a minimum of 50 randomly selected wires shall be pulled from each sampled device. The post-seal bond strength distribution(s) must demonstrate that the wire bond process is in statistical control, has not changed with respect to the distribution characterized for a one-sided lower control limit, and no single destructive pull is less than the specified post-seal bond strength limit. The sample size shall be sufficient to demonstrate that the statistical distribution of all wires pulled has not changed with respect to central tendency or dispersion in such a way as to violate a $p < .0001$ at the device level. The beta risk to the consumer shall be .01 or less. The method of statistical analysis shall be documented and approved by the qualifying activity.
 - d. A minimum of 8 wires shall be evaluated from each sampled device to represent the worst case wires as determined to potentially violate the lower specification limit. Their wire pull strengths shall be within the predicted tolerances established in 3.2.1.6. Any wire pull strengths outside the predicted tolerance in the characterized distribution shall require evaluation as to the cause of the out of control condition, and additional worst case wires shall be pulled to determine whether the wire bond strength distribution meets a probability at the wire level of $P < 1 - [.9999^{**}(1/n)]$ (n = number of bonding wires in the package). The lot is rejected if this criteria is not met.
 - e. If any bond fails the acceptance criteria, a documented action plan shall be followed to determine the cause of the failure. Wire bond failures verified as non-bond related shall be documented, and additional post-seal wire bond pulls shall be conducted to demonstrate statistical control as described in 3.2.2.1.c and d. If a failure is verified as bond integrity related (e.g., contamination on wire, glassivation on the bonding pad, etc.), all devices within the applicable assembly lot shall be rejected. Wire bonding shall be suspended on the applicable bonding equipment until a failure analysis, MIL-STD-883, method 5003, of the failed bond is performed and corrective action is implemented and recorded.
4. SUMMARY. The following details shall be specified in the applicable acquisition document:
- a. The applied lifting force if other than as specified in 3.1.
 - b. The sampling, acceptance, or screening requirements.
 - c. The percent defective allowable (PDA) as applied to the number of failures with respect to the number of wires tested.
 - d. The requirements for reporting of failure categories, when applicable.

*



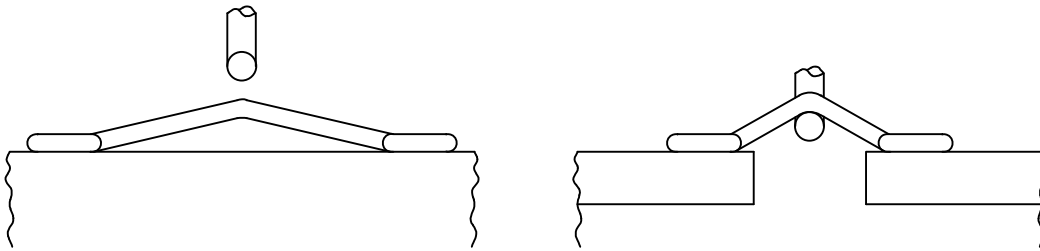
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Figure 2023-1. Bond pull hook placement location.



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FIGURE 2023-2. Wire loop angle.



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FIGURE 2023-3. Flat loop wire pull testing.

APPENDIX A

Capability Study Example

The worst case die/package combination for the example product line is a 100 wire package with the smallest die. The worst case die/package combination is based on the characterized worst case wire geometry and number of bonding wires. A post seal bond pull of 2 grams or less is considered unacceptable for 1.25 mil diameter aluminum wire. The proposed military standard requires a failure rate of no greater than 100 parts per million.

The distribution of bond pulls across devices is examined for each wire length. A statistical test is done for normality and in this example there is no reason to reject the assumption of normality. The worst case wire length in terms of variability and closeness to the specification of 2 grams is identified. The mean of this worst case distribution is found to be 4.26 grams with a standard deviation of .5 grams.

Thus, for this distribution the 2 gram specification is 4.52 standard deviations away $[(4.26-2)/(.5)]$ and corresponds to a ppm level of approximately 3.1. If the distribution was to shift to the 100 ppm level such that 2 grams corresponds to 100 ppm (i.e., the 2 gram spec is now only 3.719 standard deviations below the mean), a shift of about .8 sigma $[4.52-3.719]$ from the present bond pull mean of 4.26 would be required. This information is used to determine the number of devices needed for the capability study.

The following table can be used where the data is normally distributed:

<u>Sigma shift to 100 ppm level</u>	<u>Devices needed</u>
.4	140
.5	90
.6	62
.7	46
.8	35
.9	28
1.0	22
1.1	19
1.2	16
1.3	13
1.4	11
1.5 or greater	10

$$n = [(Z_{\alpha} + Z_{\beta})^2] / (d^2)$$

d = standard deviation shift = 0.8

alpha = .05 ; $Z_{\alpha} = -1.645$

beta = .001 ; $Z_{\beta} = -3.09$

[see Diamond, 1989, Practical Experiment Designs, pages 45-47]

Therefore, $n = [(1.645 + 3.09)^2] / (.8)^2 = 22.42 / .64 = 35$. Thirty five devices are used in this capability study.

Using the standard bonding process, the 35 devices (each having 100 wires) are submitted to package seal, and post-seal bond strength measured.

For each wire position a mean and standard deviation is calculated across the 35 devices.

mean = \bar{x}

standard deviation = sd

The distributions are evaluated and show no significant departure from normality.

The lower spec limit is determined: Here a lower bond pull of 2 grams.

APPENDIX A

For each wire position a "Z" is calculated:

$$Z = (\bar{x} - LSL) / sd$$

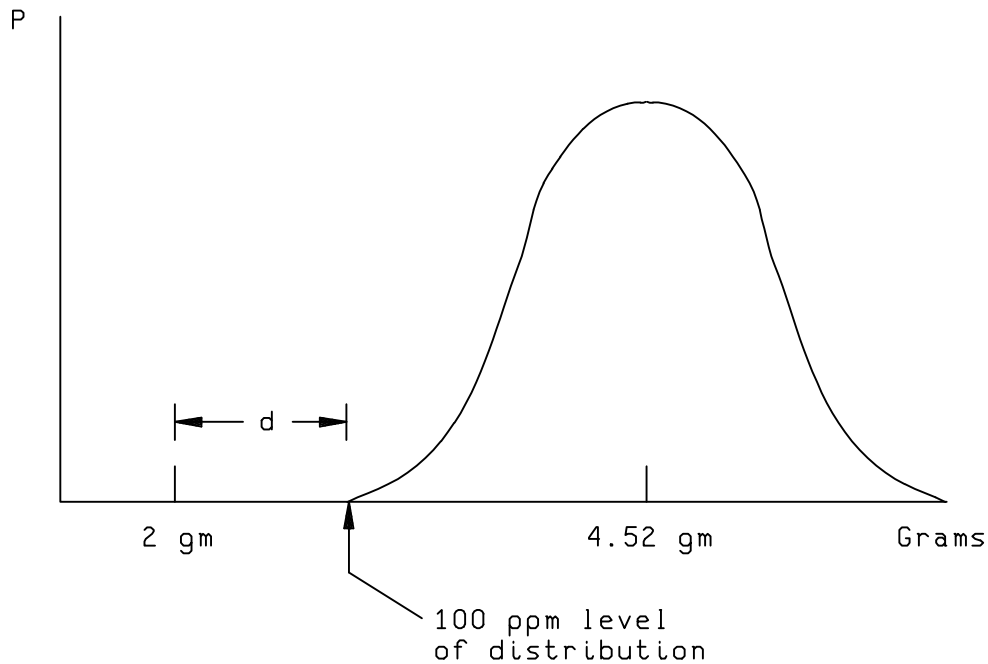
For each wire position a probability of wire failure is determined by finding the probability of being below the Z value. Use of normal probability tables are utilized in this example because of the distributions being normally distributed. For this example there will be 100 values.

The probability of device failure is calculated by summing the 100 p values for failure of a wire position.

$$P(\text{Device Failure}) = \text{Summation of } P(\text{failure of wire position})$$

$$= .00005 \text{ for this example or 50 parts per million}$$

For this example it has been demonstrated that the probability of any device failing the minimum post-seal bond strength is less than .0001.



*

FIGURE 2023-4. Bond strength versus probability.

METHOD 2024.2

LID TORQUE FOR GLASS-FRIT-SEALED PACKAGES

1. **PURPOSE.** The purpose of this test is to determine the shear strength of the seal of glass-frit-sealed microelectronic packages. This is a destructive test.

2. **APPARATUS.** The test equipment shall consist of suitable fixed or adjustable clamps and fixtures to secure devices while applying a torque to the seal area. The torque mechanism and holding fixtures should provide adequate support to the base and lid (especially for flat packs, chip carrier packages, or other thin profile packages) to assure that the torque is applied predominantly to the seal area without significant bending, warping or displacement of the package being tested. A torsion wrench or torque-applying mechanism capable of applying a torque of at least 12.8 newton meter (114 in-lbf) with a gauge capable of measuring the force with an accuracy and precision of ± 5 percent of the reading or ± 0.2 newton meter, whichever is greater, shall be used to apply torque to the lid. For smaller seal area packages a torsion wrench or torque-applying mechanism with sufficient capacity to separate the package and with an accuracy and precision of ± 5 percent of the reading or ± 0.2 newton meter whichever is greater, may be used to allow for a more accurate reading. The torque mechanism shall have a peak indicator for retaining the maximum stress applied or other equivalent stress recording system.

3. **PROCEDURE.** The device shall be held by the device body and torque applied to the lid of the device or vice versa. The lid torque fixtures shall be placed to assure that it only applies torque to the side area of the package lid, base, or spacer. Contact to the sealing glass should be avoided. The lid torque fixture may touch the package leads but not in such a way that significant torque is transferred directly through the leads. The torque shall be applied gradually and smoothly until package separation occurs, or the reaching of the 12.8 newton meter torque limit. The torque required for package separation or the reaching of the 12.8 newton meter torque limit shall be recorded. The torque shall be applied such that the axis of rotation is perpendicular to the sealing plane and the axis of rotation shall be located at the geometric center of the sealing area (see figure 2024-2).

3.1 **Separate glass seals.** For packages with more than one glass-frit-seal (e.g., separate glass-frit-seals for the lid and the lead frame), each seal shall be torqued and rated separately against the failure criteria. A failure of either seal shall constitute failure of the test. Alternatively, the two seals may be simultaneously stressed by holding only the lid and base and applying the torque specified for the larger seal area.

3.2 **Failure criteria.** Failure criteria are based on not achieving the designated torque without breakage or lid separation. The designated torque is a function of the device seal area, as illustrated in Figure 2024-1. A device where package separation or breakage occurs at a torque value less than specified in table I shall constitute a failure. If the entire package (lid, seal, and base) breaks in a direction normal to the plane of the applied torque (i.e., showing evidence of improperly applied torque) with parts of lid and base still fused together, the package may be discarded without counting as a failure and a replacement sample substituted to complete the required testing.

4. **SUMMARY.** The following details shall be specified in the applicable acquisition document:

- a. The minimum torque if other than the value specified in table I.
- b. Number of devices to be tested.
- c. Requirement for data recording where applicable.

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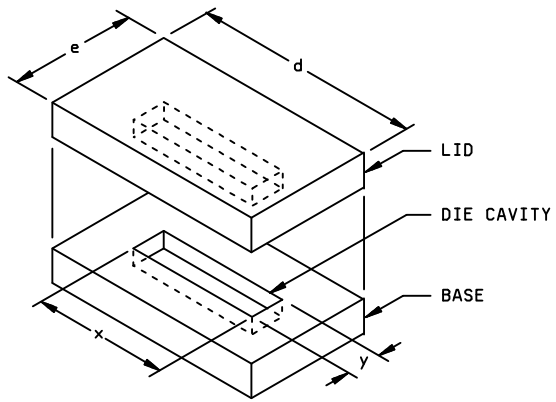
TABLE I. Minimum torque limits versus design seal area.

Design seal area (cm ²)	Torque		
	Newton meter (N-m)	Inch-pounds force (in-lbf)	Meter-grams force (m-gf)
<0.22	0.5	4	50
0.221-0.32	0.7	6	70
0.321-0.47	1.0	9	100
0.471-0.65	1.7	15	170
0.651-0.85	2.5	22	250
0.851-1.08	3.4	30	350
1.081-1.41	4.4	39	450
1.411-1.73	5.9	52	600
1.731-2.05	7.4	65	750
2.051-2.50	8.8	78	900
2.501-3.00	10.8	96	1100
>3.00	12.8	114	1300

Various units are presented for the convenience of those using conventional torque wrenches scaled in metric or English system units. All values have been rounded off from the direct conversion values beginning with N-m and are acceptable for use in quality conformance and qualification inspection.

$$1 \text{ m-gf} = 0.009807 \text{ N-m}$$

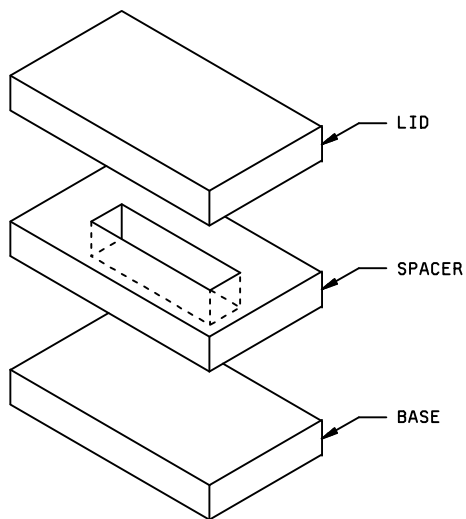
$$1 \text{ in-lbf} = 0.1130 \text{ N-m}$$



a. TWO PIECE PACKAGE

$$\text{Seal area} = ed - xy$$

If the cavities in the lid and base are not equal, the area "XY" shall be determined from the larger of the cavities in the lid or base.



b. THREE PIECE PACKAGE

FIGURE 2024-1. Design seal area.

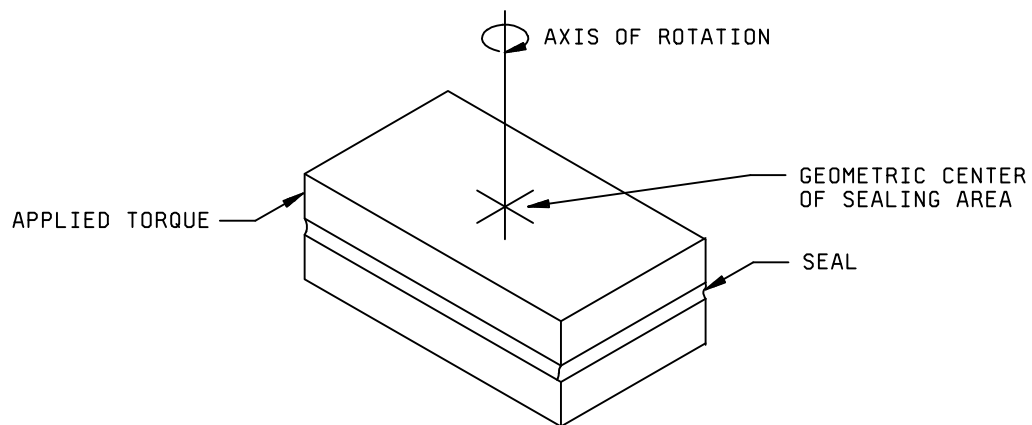


FIGURE 2024-2. Application of torque.

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METHOD 2025.4

ADHESION OF LEAD FINISH

1. PURPOSE. This destructive test is intended to determine the integrity of all primary and undercoat lead finishes.
2. APPARATUS. This test requires suitable clamps and hardware necessary to apply the bending stress through the specified bend angle. Optical equipment capable of magnification of 10X to 20X.
3. PROCEDURE. Unless otherwise specified, the bend stress shall be applied to randomly selected leads from each device selected for test and shall be performed after application of the primary finish and after sealing. Unless otherwise specified, the sampling shall be sample size number = 15, C = 0 based on the number of leads tested chosen from a minimum of three devices. The leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. The coated lead shall be bent repeatedly in the same direction (or plane) through an angle of at least 90° at a radius of less than four times the lead thickness or diameter at approximately the mid point of the lead lengths until fracture (i.e., lead breaks off) of the base metal occurs.

3.1 Failure criteria. No cracking, flaking, peeling, blistering, loosening, or detachment of the coating(s) at the interface(s) shall result from probing the bend/break area with a sharp instrument. Cracks in the base metal shall not be considered a failure unless accompanied by cracking, flaking, peeling, blistering, loosening, or detachment of the primary coating(s) or undercoating(s).

NOTE: In tin lead or heavy tin coatings, the failure criteria listed should not be confused with shearing and tearing associated with fatigue fractures and slip-planes which develop into cracks and result in rupture.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:
 - a. Sampling criteria, if other than specified (see 3).
 - b. Failure criteria, if other than specified (see 3.1).

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RANDOM VIBRATION

1. PURPOSE. This test is conducted for the purpose of determining the ability of the microcircuit; to withstand the dynamic stress exerted by random vibration applied between upper and lower frequency limits to simulate the vibration experienced in various service-field environments. Random vibration is more characteristic of modern-field environments produced by missiles, high-thrust jets, and rocket engines. In these types of environments, the random vibration provides a more realistic test. For design purposes, however, a swept frequency sinusoidal test may yield more pertinent design information.

2. APPARATUS.

2.1 Vibration system. The vibration system, consisting of the vibration machine, together with its auxiliary equipment shall be capable of generating a random vibration for which the magnitude has a gaussian (normal) amplitude distribution, except that the acceleration magnitudes of the peak values may be limited to a minimum of three times the rms (three-sigma (α) limits). The machine shall be capable of being equalized so that the magnitude of its spectral-density curve will be between specified limits (for example, see figures 2026-1 and -2). When the test item, or a substitute equivalent mass, is appropriately secured to the vibration machine. The equalization of an electrodynamic vibration machine system is the adjustment of the gain of the electrical amplifier and control system so that the ratio of the output-vibration amplitude to the input-signal amplitude is of a constant value (or given values) throughout the required frequency spectrum.

2.1.1 Control and analysis of vibration.

- a. Spectral-density curves. The output of the vibration machine shall be presented graphically as power-spectral density versus frequency. ^{1/} The spectral-density values shall be within +40 and -30 percent (± 1.5 dB) of the specified values between a lower-specified frequency and 1,000 Hz, and within +100 and -50 percent (± 3 dB) of the specified values between 1,000 and an upper-specified frequency (2,000 Hz). A filter bandwidth will be a maximum of one-third-octave or a frequency of 25 Hz, whichever is greater.

^{1/} Power-spectral density is the mean-square value of an oscillation passed by a narrow-band filter per unit-filter bandwidth. For this application it is expressed as G^2/f where G^2/f is the mean-square value of acceleration expressed in gravitational units per number of cycles of filter bandwidth. The spectral-density curves are usually plotted either on a logarithmic scale, or in units of decibels (dB). The number of decibels is defined by the equation:

$$dB = 10 \log \frac{G^2 / f}{G_r^2 / f} = 20 \log \frac{G / \sqrt{f}}{G_r / \sqrt{f}}$$

The rms value of acceleration within a frequency band between f_1 and f_2 is:

$$G_{rms} = \left[\int_{f_1}^{f_2} G^2 / f df \right]^{1/2}$$

where G_r^2/f is a given reference value of power-spectral density, usually the maximum specified value.

- b. Distribution curves. A probability density-distribution curve may be obtained and compared with a gaussian-distribution curve. The experimentally-obtained curve should not differ from the gaussian curve by more than ± 10 percent of the maximum value.

2.2 Monitoring. Monitoring involves measurements of the vibration excitation and of the test-item performance. When specified, the device shall be monitored during the test. The details of the monitoring circuit, including the method and points of connection to the specimen, shall be specified.

2.2.1 Vibration input. The vibration magnitude shall be monitored on a vibration machine, on mounting fixtures, at locations that are as-near as practical to the device mounting points. When the vibration input is measured at more than one point, the minimum input vibration shall be made to correspond to the specified test curve (see figures 2026-1 and 2026-2). For massive test-items and fixtures, and for large-force exciters or multiple-vibration exciters, the input-control value may be an average of the average magnitudes of three or more inputs. Accelerations in the transverse direction, measured at the test-item attachment points, shall be limited to 100 percent of the applied vibration.

3. PROCEDURE. The device(s) shall be rigidly fastened on the vibration platform and the leads adequately secured. The vibration machine shall then be operated and equalized or compensated to deliver the required random frequencies and intensities conforming to the curves specified in test condition I, figure 2026-1 or test condition II, figure 2026-2. The device(s) shall be subjected to a random vibration specified by the test condition letter (see tables I and II) for a duration of 15 minutes in each of the orientations X, Y, and Z. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- a. Test condition (see 3).
- b. Measurements after test (see 3 and 3.1).
- c. Test condition I or II and letter (A-K).
- d. Test duration if other than specified.
- e. Requirement for test to be conducted with device powered up, when applicable.

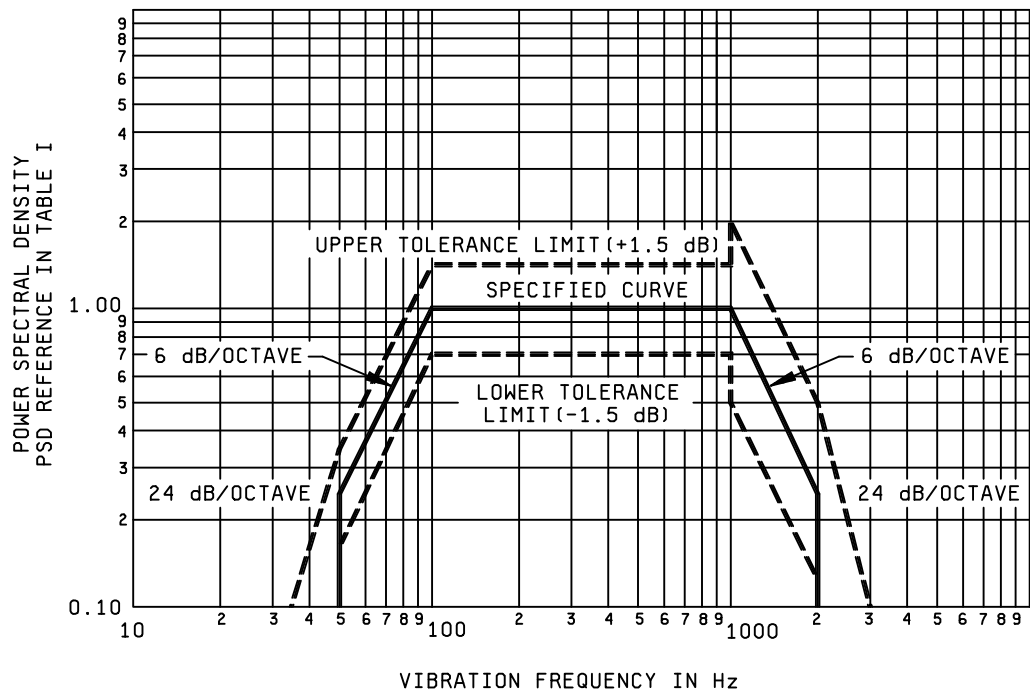


FIGURE 2026-1. Test condition I, random vibration test-curve envelope (see table I).

TABLE I. Values for test condition I. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.2
B	.04	7.3
C	.06	9.0
D	.1	11.6
E	.2	16.4
F	.3	20.0
G	.4	23.1
H	.6	28.4
J	1.0	36.6
K	1.5	44.8

1/ For duration of test, see 4.

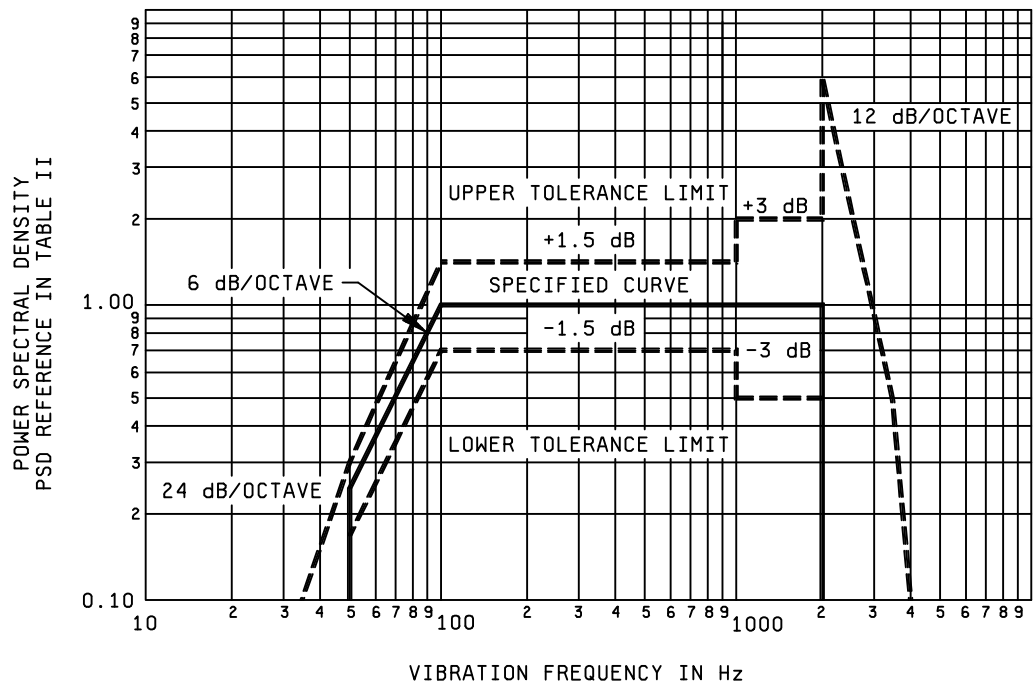


FIGURE 2026-2. Test condition II, random vibration test-curve envelope (see table II).

TABLE II. Values for test condition II. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.9
B	.04	8.3
C	.06	10.2
D	.1	13.2
E	.2	18.7
F	.3	22.8
G	.4	26.4
H	.6	32.3
J	1.0	41.7
K	1.5	51.1

1/ For duration of test, see 4.

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METHOD 2027.2

SUBSTRATE ATTACH STRENGTH

1. PURPOSE. The purpose of this test is to determine the strength of the element attachment system when subjected to force in the Y1 axis. This method is applicable to semiconductor die attached to headers or substrates by means of organic materials. Uses include material evaluations and process control.

2. APPARATUS. The test equipment shall consist of a tensile strength tester capable of applying a force equal to 1,000 psi (6895 kpa) times the area of the largest die to be tested with an accuracy of ± 5 percent or 1.75 ounces (50 gm) force, whichever is less. The test equipment shall have the following capabilities.

- a. A range of replaceable die contact tools such that each contacting surface shall be 60 to 100 percent of the area of the die under test.
- b. Provision to assure that the die contact tool is held perpendicular to the die mounting plane of the header or substrate.
- c. A rotational capability between the die contact tool and the header/ substrate holding fixture.

3. PROCEDURE. The test shall be conducted by placing a small amount of a quick setting adhesive on the contacting tool which is then attached to the die surface (figure 2027-1). After sufficient adhesive curing the sample is subjected to a vertical pull force as defined herein.

3.1 Force applied. A force sufficient to lift the die from its mounting or equal to twice the minimum specified tensile strength (figure 2027-2) whichever occurs first, shall be applied to the die using the apparatus of 2 above.

3.2 Failure criteria. If the separation occurs between the die surface and the die contacting tool at less than twice the minimum specified tensile strength, the particular die pull test will not be counted in the sample as either passing or failing. When this occurs, the DUT may either be retested or replaced with a substitute device to be tested in its place. The following criteria constitute a failure when the die is lifted from the header/substrate:

- a. Separation at less than the minimum die tensile strength (1.0X) as shown on figure 2027-2).
- b. Separation at less than 200 percent of the minimum die attach strength (2.0X) as shown on figure 2027-2 and no evidence of attachment at the interface between the die attach medium and the die or header/substrate.

3.2.1 Recording. When specified, the force required to achieve separation will be recorded with the failure category.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- a. Minimum die pull strength if other than that shown on figure 2027-2.
- b. Number of die to be tested and the acceptance number.
- c. Requirements for data recording.

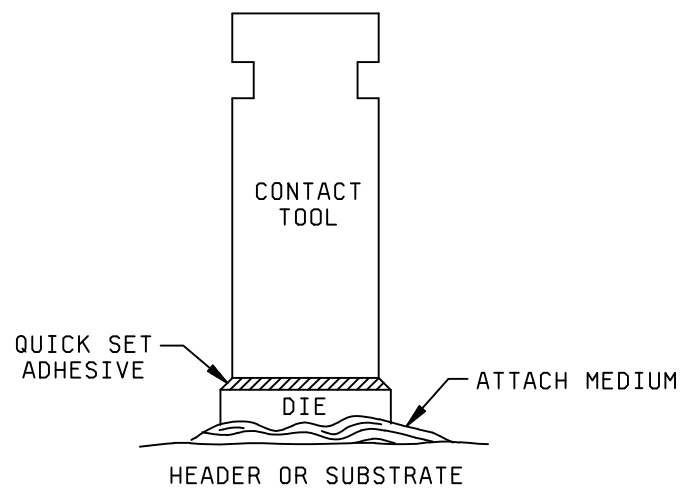
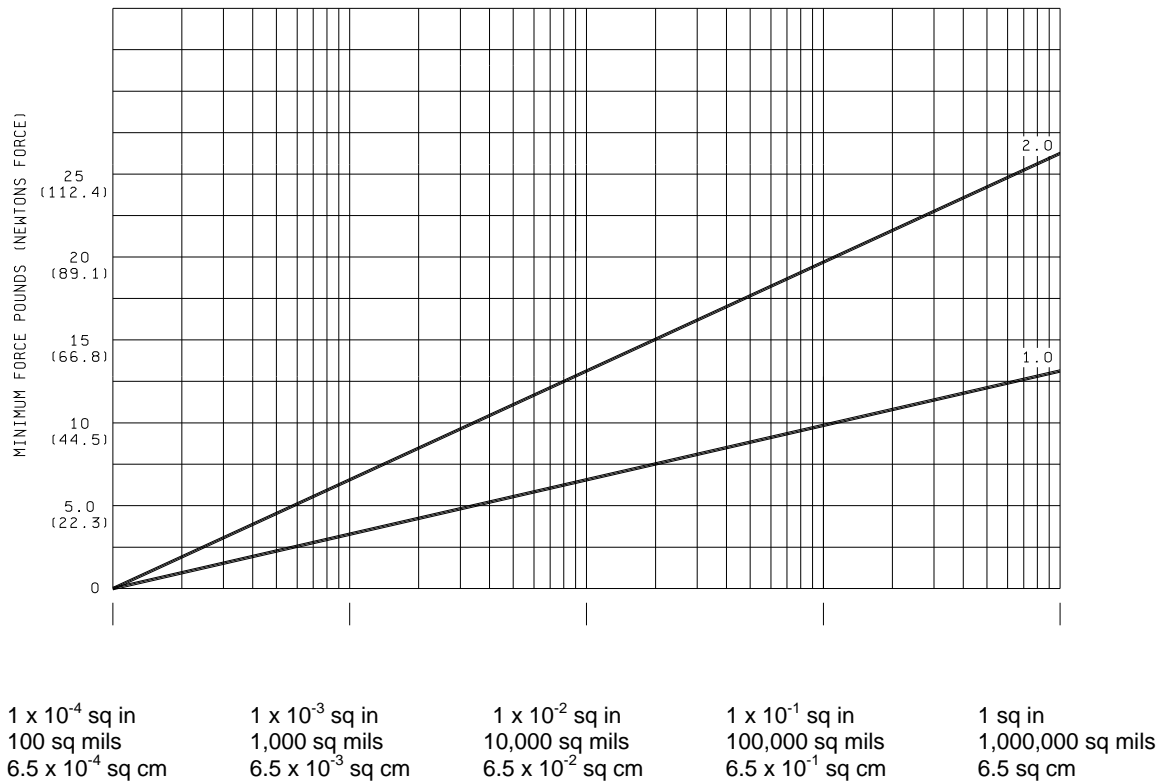


FIGURE 2027-1. Die contact tool adhered to die top surface prior to lift off.



NOTE: The X-axis is a log scale and intermediate points not shown must be calculated based on the formulas, (1.0 X: $y = 3.32 \log x + 13.3$, 2.0 X: $y = 6.63 \log x + 26.6$) not extrapolated from the graph.

Sample 1: English calculation:

Assume a die measurement of 0.25 inches by 0.25 inches.

$$x = 0.25 \text{ in times } 0.25 \text{ in} = 0.0625 \text{ sq in.}$$

Then $y = 3.32 \log x + 13.3$

$$= 3.32 \log (0.0625) + 13.3$$

$$= 3.32 (-1.204) + 13.3$$

$$= -4.0 + 13.3$$

$$= 9.3$$

Hence: $X = 9.3 \text{ lbs}$ and $2X = 18.6 \text{ lbs}$

Sample 2: Metric calculation:

Assume a die measurement of 0.8 cm by 0.8 cm.

$$x = 0.8 \text{ cm times } 0.8 \text{ cm} = 0.64 \text{ sq cm}$$

Then $y(\text{in pounds}) = 3.32 \log x(\text{in sq in}) + 13.3$

Because 1 pound = 4.45 newtons, and 1 sq in = 6.45 sq cm, then $y_{\text{newtons}} = 4.45 \text{ times } y_{\text{pounds}}$ and $x_{\text{sq in}} = x_{\text{sq cm}} / 6.45$

Thus: $y_{\text{newtons}} = 4.45 [3.32 \log (x_{\text{sq cm}} / 6.45) + 13.3] = 14.8 \log x_{\text{sq cm}} + 47.2$

Or $y_{\text{newtons}} = 14.8 \log (0.64 \text{ sq cm}) + 47.2$

$$= 14.8 (-0.194) + 47.2$$

$$= -2.9 + 47.2$$

$$= 44.3 \text{ Newtons}$$

Hence $X = 44.3 \text{ newtons}$ and $2X = 88.6 \text{ newtons}$

FIGURE 2027-2. Die attach strength criteria (minimum force versus die attach area).

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METHOD 2028.4

PIN-GRID PACKAGE DESTRUCTIVE LEAD PULL TEST

1. PURPOSE. This method provides a test for determining the integrity of pin-grid type package leads by measuring the capability of the package leads to withstand an axial force.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for supplying the specified stress to the package lead. A calibrated measurement and indication of the applied stress in grams-force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ± 5 percent or ± 0.25 kgf, whichever is greater.

3. PROCEDURE. The stress shall be applied to the leads to be tested randomly selected from a minimum of 3 devices prior to start of the test. Tension only shall be applied, without shock, to each lead to be tested in a direction parallel to the axis of the lead. The tension shall be increased until the minimum acceptable pull strength is reached or upon separation of the lead from the braze pad. The tension shall be applied as close to the end of the lead as possible.

3.1 Failure criteria. The minimum acceptable lead pull strength shall be 1.70×10^7 grams-force per square inch of cross-sectional lead area (e.g., the minimum pull strength of a lead with an average cross-sectional area of 2.5×10^{-4} in² will be 4.3 kgf.)

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- a. Number and selection of leads, if different from above.
- b. Measured lead pull strength and minimum required pull strength, if different from above.

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METHOD 2029

CERAMIC CHIP CARRIER BOND STRENGTH (DESTRUCTIVE PUSH TEST)

1. PURPOSE. The purpose of this test method is to measure strengths of bonds external to leadless microelectronic packages (e.g., solder bonds from chip carrier terminals to substrate or wiring board).

2. APPARATUS. The apparatus for this test method shall consist of suitable equipment for applying the specified stress to the device terminals. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ± 5 percent or ± 0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the following test procedure. All push tests shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. A minimum of 4 chip carriers (or use all chip carriers if 4 are not available) on each of a minimum of 2 completed substrates or wiring boards shall be used. Where there is any adhesive, encapsulant, or other material under, on, or surrounding the chip carrier such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

3.1 Test samples. When packages are bonded to substrates or wiring boards other than those in completed devices, the following conditions shall apply:

- a. The sample of packages for this test shall be taken at random from the same chip carrier population as that used in the completed devices that they are intended to represent.
- b. The packages for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.
- c. The test package substrates shall be processed and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1.1 Sample preparation. Substrates must be prepared as follows:

- a. A roughly circular area comprising 50 percent, +5 percent, -0 percent of the bonded side of each package to be tested shall be exposed by either end-mill drilling of the test substrate or other suitable means. If it is not possible to expose the ceramic in this manner, the packages shall be bonded onto test substrates into which the proper hole(s) and hole size(s) has (have) been manufactured, providing all other conditions of 3.1 have been met.
- b. Suitable support must be provided for the test substrate so that there is a minimum of flexure of the substrate during the test. This support, if necessary, may be provided by bonding the substrate to a rigid metal plate having a hole pattern matching that of the test substrate.
- c. A cylindrical rigid metal test post must be prepared for each hole size, which will be inserted through the support plate and test substrate holes. The post will be used to transmit the specified stress from the stress-source equipment to the exposed package surface. The diameter of the post shall be 85 percent (+5 percent, -0 percent) of the corresponding test hole diameter. The length of the post shall be sufficient to extend 1 inch (+100 percent, -0 percent) from the open end of the test hole when the post is inserted completely into the hole.

3.2 Testing. The test shall be performed in the following manner:

- a. A single package shall be pushed during each test sequence.
- b. A layer of teflon tape in accordance with MIL-T-27730 or equivalent shall be placed between the exposed chip carrier surface and the test post prior to testing.

- c. Insert test post into test hole. The contact of the test post to the ceramic chip carrier shall be made without appreciable impact (≤ 0.1 inch/minute). With the stressing element of the test equipment traveling at a constant rate of 0.02 ± 1 percent inch/second, apply sufficient force to chip carrier (through test post) to break all chip carrier to substrate bonds on at least three edges of chip carrier under test. When failure occurs, the force at the time of failure and the failure category shall be recorded. Any test resulting in the fracturing of either the chip carrier or test substrate shall be considered unacceptable. The data from the test shall be discarded, and the test performed again.

3.3 Failure criteria. Any push test which results in separation with a bond strength of less than 30 kg-force per linear inch (1180 g-force per linear mm) of solder pad width shall constitute a failure. The bond strength shall be determined by dividing the separating force by the total of the solder pad widths as measured on the substrate at the package edge, in a direction parallel to the package edge.

3.3.1 Failure category. Failure categories are as follows. When specified, the stress required to achieve separation and the predominant category of separation shall be recorded.

- a. Device fracture.
- b. Failure in package-bond interface.
- c. Terminal break at point not affected by bonding process.
- d. Failure in bond-substrate conductor interface.
- e. Conductor lifted from board or substrate.
- f. Fracture within board or substrate.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

- a. Minimum bond strength if other than specified in 3.3 or details of required strength distributions if applicable.
- b. Sample size number and accept number and selection and number of devices to be tested on each substrate, if other than 4.
- c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.3.1).

*

METHOD 2030.1

ULTRASONIC INSPECTION OF DIE ATTACH

1. PURPOSE. The purpose of this examination is to nondestructively detect unbonded regions, delaminations and/or voids in the die attach material and at interfaces within devices through the measurement of acoustic continuity. It establishes methods and criteria for ultrasonic inspection of devices.

For certain device structures or die attach materials, a dramatic distinction between well-bonded and poorly bonded conditions may be difficult to achieve. This factor should be considered in relation to the design of each device when application of this test method is specified.

2. DEFINITIONS.

2.1 The term "die attach interface" as used in this test method refers to the entire bulk area between the die and the substrate to which it is bonded. For die attach interfaces, this includes the interface between the die attach material and the die, the interface between the die attach material and the substrate, plus the die attach material itself.

2.2 The term "bulk material" as used in this test method refers to the entire thickness within a specific layer of material. For die attach, the attachment material by itself is considered a bulk material.

2.3 The term "ultrasonic inspection" as used in this test method refers to high frequency ultrasonic visualization (imaging) which produces a gray or color scale output such as may be provided by ultrasonic scanning (US) or acoustic microscope (AM) techniques. The most common mode utilized for die attach inspection is an X-Y plane scan at specified depth(s) in Z, which is commonly referred to as C-Scan or C-mode imaging. Other ultrasonic techniques may also be utilized to obtain the die attach integrity data.

2.4 The term "reflected" as used in this test method refers to the change in direction of an ultrasound wave front at an interface between two different media so that the wave front returns via the medium from which it originated.

2.5 The term "reflection mode" as used in this test method refers to an ultrasonic scan or acoustic microscope that uses one transducer as both the pulser and receiver. (This is also known as a pulse/echo system.)

2.6 The term "transmitted" as used in this test method refers to the propagation of an ultrasound wave through a media or an interface between media that allows it to continue through the structure.

2.7 The term "transmission mode" as used in this test method refers to an ultrasonic scan or an acoustic microscope that transmits ultrasound completely through the sample from a sending transducer to a receiver on the opposite side.

3. APPARATUS. The apparatus and materials for this test shall include:

3.1 Ultrasonic inspection equipment: The ultrasonic inspection equipment shall have a test frequency sufficient to penetrate to the die attach material interface. In the case that the opening of a sealed hermetic or non-hermetic device with a known air cavity is undesirable, the ultrasonic equipment shall be capable of detecting an acoustic signal that enters the top and bottom or back of a package and is reflected by or transmitted through to the desired material interface. The test frequencies and focal distances shall be adequate to achieve a resolution capable of detecting voids as small as 0.0254 mm (0.001 inch) in diameter, when inspecting through the die is desired, but this may not be feasible due to the construction of the device. In such cases, the test frequency and focal distance shall be chosen to ensure penetration down to the desired material interface with the achievable resolution being a secondary consideration.

3.2 Output device: A hard copy gray or color scale recording unit or other direct recording device (computer storage) shall be used to produce an image for analysis (manual or automated). The dynamic range of the output image shall be at least 256 discernible colors or levels of gray scale. The appropriate gray/color scale shall be included in each image. The image, hard copy or digital, shall be large enough to achieve a resolution capable of detecting a void as small as 0.0254 mm (0.001 inches) in diameter, when inspecting through the die, or the best feasible resolution for that application.

3.3 Holding tank: A holding tank for containing the coupling fluid and locating fixtures (as needed) to ensure accurate and repeatable placement of the devices inspected. The holding tank, locating fixtures and any auxiliary supporting hardware shall be constructed of materials that will be unaffected by corrosion or other reactivity in the presence of the coupling fluid.

3.4 Ultrasonic detector: Reflection mode imaging shall be used when the opening of a sealed, hermetic device is undesirable. For inspection of the die attach interfaces within a sealed device, as an example, it shall be capable of detecting an acoustic signal which enters the back or bottom of the package and is reflected by the material interface(s). The reflection and/or transmission modes of imaging shall be used when inspecting a non-hermetic or the opening of a sealed hermetic device is allowable.

4. PROCEDURE. The ultrasonic inspection instrument shall be selected or adjusted as necessary to obtain satisfactory images and achieve maximum image details within the sensitivity requirements for the device or defect features the test is directed toward. In the case of reflection mode or transmission mode images, care must be exercised to insure that the ultrasound penetrates and is sensitive to the entire die attach interface or bulk material area of interest

4.1 Mounting and handling. The devices shall be mounted in the holding tank so that the devices are not damaged or contaminated and are in the proper plane for inspection. The devices may be mounted in any type of fixture providing the fixtures do not block the view from the ultrasonic transducer to any portion of the body of the device in the region of interest. The coupling fluid in the holding tank shall be distilled water or other suitable noncorrosive liquid. The devices shall remain in the coupling fluid for as short a time as possible. Subsequent to the ultrasound inspection, proper cleaning and drying of the samples are required. Refer to J-STD-033 for the recommended bake out times and procedures to remove any ingressed moisture within a non-hermetic surface mount devices.

4.2 Views. All devices, shall have at least one image view made with the ultrasound penetrating the device in a direction perpendicular to the plane of the material interfaces, and for which there is acoustic continuity from the device exterior surface to the die attach interface(s) (Note: Generally, the Z-axis direction with the die attach parallel to the X-Y plane). For devices with no sealed air gap above the die (unlidded or non-hermetic devices), an image view made with the ultrasound directed from (reflected) or through (transmitted) the surface of the die to the material interface(s) may be specified (see figure 2030-1 for examples).

4.3 Recording and marking. The ultrasonic image shall be printed using paper and with at least a resolution of 300 data elements per inch nominal or stored in a digital file format by the equipment. The image shall be identified by unambiguously marking the paper on which the image is printed or stored within the digital file format with, but not limited to the following information:

4.3.1 Device manufacturer's name or code identification number.

4.3.2 Device type or part number.

4.3.3 Production lot number or date code or inspection lot number.

4.3.4 Ultrasonic image view number and date.

4.3.5 Device serial or cross reference numbers, where applicable.

4.3.6 Ultrasonic laboratory identification, if other than device manufacturer.

4.3.7 Mounting material utilized for the die attachment, if known.

4.4 Recording with nonprint techniques. The use of documentation techniques, other than paper recording techniques is permitted (e.g., computer records, digital data files) provided that the equipment is capable of storing results of at least equal quality when compared to printed recording techniques, and all requirements specified herein, except those pertaining to the actual paper recording. If possible, the digital file name should incorporate a unique device identifier, such as a serial number, as part of the file name.

4.5 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number.

4.6 Set up verification. When imaging lidded (sealed) devices, one open lid device of the same type and construction should be available to set up the equipment. The device may be a scrapped, nonoperational device or a known set up sample with known voids which will be used to identify internal landmarks and insure the equipment is properly operating.

4.7 Tests. Ultrasonic frequency gate settings, receiver attenuation, and other equipment settings shall be selected to achieve the resolution desired for the type of inspection being accomplished, in the example of die attach a resolution of 0.0254 mm (0.001 inch) in diameter, when inspecting through the die. Optimize the ultrasonic signal reflected from the material interface of interest, and distinguish image features with as great a contrast as possible. Ultrasonic images shall be made for each view required.

4.8 Operating personnel. Personnel who will perform ultrasonic inspection shall have training in ultrasonic imaging procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards.

4.9 Interpretation of ultrasonic images. Ultrasonic images shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected. Interpretation of the image shall be made under moderate light level conditions without a glare on the recording paper's surface or the display monitor. The image shall be viewed at an appropriate magnification to determine acceptance as specified herein. Automated percentage void or bond area calculations can be utilized instead of visual analysis upon confirming that the automated method is at least equal to the accuracy of the visual method (see figure 2030-2 for example of automated method).

4.10 Reports of records.

4.10.1 Reports of inspection. When specified, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the ultrasonic inspection, and list the purchase order number or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

4.10.2 Ultrasonic image and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report. These shall be retained for the period specified by the procuring activity in the acquisition document.

4.11 Examination and acceptance criteria for die attach. In the examination of devices, the following aspects shall be considered unacceptable die attach interface, and devices that exhibit any of the following defects shall be rejected. If heat transfer is a concern, defects directly under the "hot" regions of the attach interface may be an issue and should be evaluated further with reliability testing.

4.12 Void and Unbonded Area. When imaging devices ultrasonically, certain types of mounting material may not give true representation of voids; therefore the mounting material shall be noted on the inspection report, when known.

4.12.1 Total of voids in excess of 50 percent of the total intended interface region (see figure 2030-3).

4.12.2 A single void in excess of 15 percent of the total intended interface region (see figure 2030-3).

4.12.3 A single corner void in excess of 10 percent of the total intended interface region (see figure 2030-3).

4.12.4 When the interface region of interest is divided into four equal quadrants by bisecting both pairs of opposite edges, any quadrant exhibiting interface region voids in excess of 70 percent of the intended interface quadrant region (see figure 2030-3).

In case of dispute, the percent of voiding shall be determined by actual measurement from the digital image using percentage void and bond image analysis functions with at least two threshold levels, i.e. B&W.

5. SUMMARY. The following details shall be specified in the applicable acquisition document:

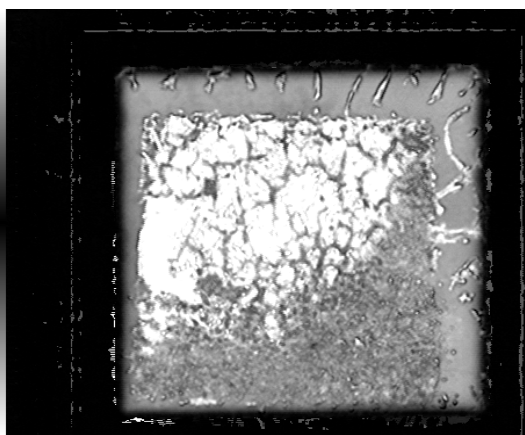
5.1 Number of views, if other than indicated in 4.2.

5.2 Image marking, if other than indicated in 4.3 or marking of samples to indicate they have been ultrasonically imaged, if required.

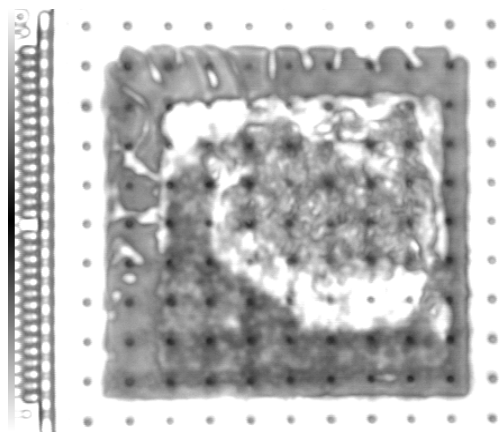
5.3 Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 4.12.

5.4 Image and report retention per 4.10.2, if applicable.

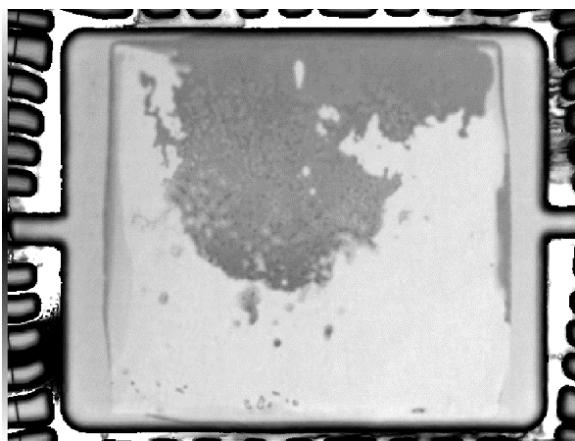
5.5 Test reports, if other than indicated in 4.10.1.



Example 2030-1a: Unlidded device reflection mode image through the die to die attach interface.



Example 2030-1b: Unlidded device reflection mode image through substrate side to die attach interface.



Example 2030-1c: Non-hermetic device reflection mode image through substrate side to die attach interface (see figure 2030-2 for example automated method analysis).

FIGURE 2030-1. Example Reflection Mode Grayscale Images of Die Attach Interface

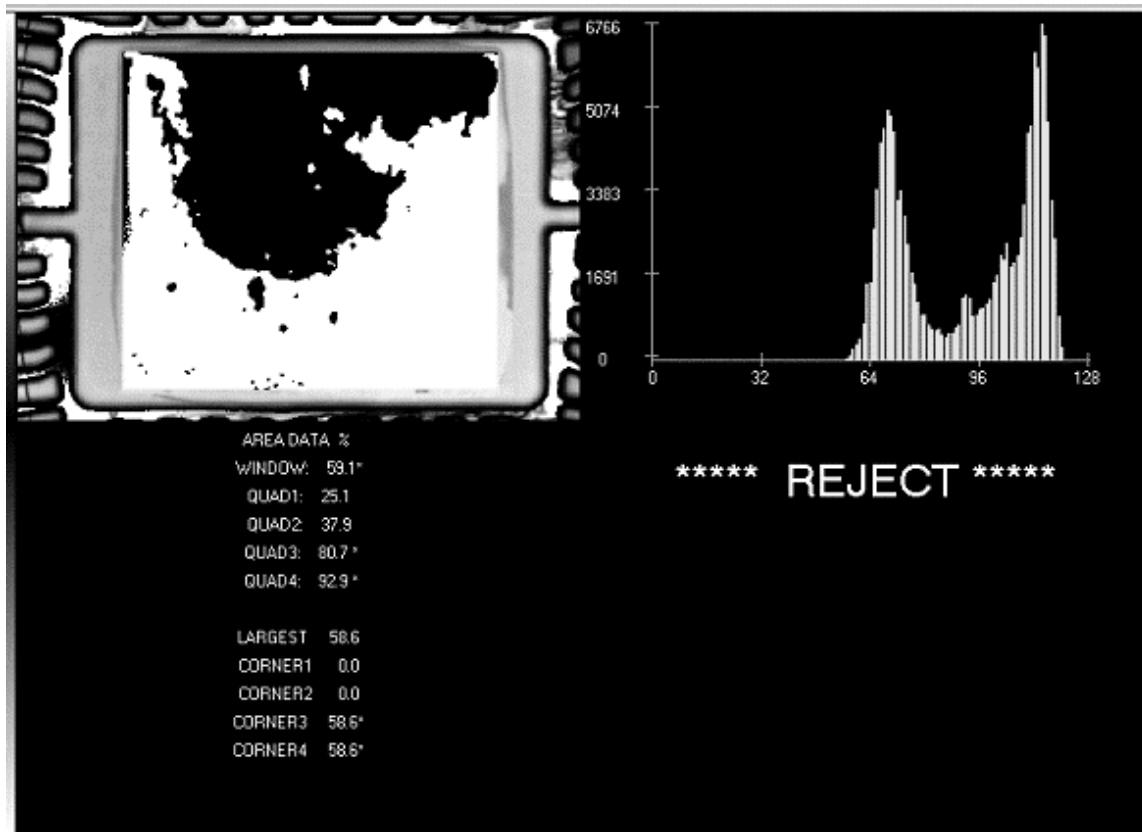


FIGURE 2030-2. Example Automated Method Analysis Report for Die Attach Interface

Typical Transmission Mode Image Analysis
(Two threshold levels – B&W)



Typical Reflection Mode Image Analysis
(Two threshold levels – B&W)



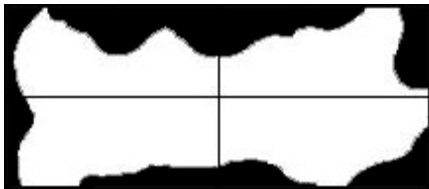
Reject: Single void larger than 15 percent (%) of total intended interface.
Reject: Corner void larger than 10 percent (%) of total intended interface.



Accept: No single void larger than 15 percent (%) of total intended interface.
Accept: Corner void of area less than 10 percent (%) of total intended interface.



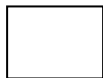
Reject: Quadrant more than 70 percent (%) unbonded.



Accept: All quadrants less than 70 percent (%) unbonded.



= Void or Unbonded area



= Void or Unbonded area

FIGURE 2030-3. Void criteria for die attach material interface inspection.

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METHOD 2031.1

FLIP-CHIP PULL-OFF TEST

1. PURPOSE. The purpose of this test is to measure the strength of internal bonds between a semiconductor die and a substrate to which it is attached in a face-bond configuration.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bonds. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ± 5 percent or ± 0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the following procedure. All die pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. The sample size number and accept number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices, a minimum of 4 die or all die if four are not available on a minimum of 2 completed devices shall be used. All pull tests shall be performed prior to the application of encapsulants, adhesive, or any material which may increase the apparent bond strength.

When flip chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

- a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.
- b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.
- c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Testing. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) having a cross-sectional area of 75 percent, $+3$ percent, -5 percent of the chip surface area. The rod shall make connection with a hard setting adhesive material (for instance, a cyanoacrylate or other adhesive possessing high tensile strength) on the back of the flip chip. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The die shall be pulled without shock, within 5° of the normal at a rate of 500 grams ± 100 grams per second, until the die separates from the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any flip-chip pull which results in separation under an applied stress less than $500 \text{ kg/in}^2 \times \text{average solder bump area (in}^2) \times \text{number of solder bumps}$ shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the predominant category of separation or failure shall be recorded.

- a. Silicon broken.
- b. Lifted metallization from chip.
- c. Separation at bond-chip interface.
- d. Failure within bond.

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- e. Separation at bond-substrate interface.
 - f. Lifted metallization from substrate.
 - g. Substrate broken.
4. SUMMARY. The following details shall be specified in the applicable acquisition document.
- a. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.
 - b. Sample size number and accept number and selection and the number of die to be tested, if other than 4
 - c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

METHOD 2032.2

VISUAL INSPECTION OF PASSIVE ELEMENTS

1. PURPOSE. The purpose of this test is to inspect passive elements used for microelectronic applications, including RF/microwave, for the visual defects described herein. This test can be performed at the unmounted element level, or prior to sealing or encapsulation, on a 100 percent inspection basis, to detect and eliminate elements with visual defects that could lead to failure in normal application. It may also be performed on a sample inspection basis at the unmounted element level, or prior to sealing or encapsulation, to determine the effectiveness of the manufacturer's quality control and handling procedures for passive elements. Visual inspection criteria are presented in four sections. The first (see 3.1), concerns planar thin film elements (resistors, capacitors, inductors, single-level patterned substrates and multilevel patterned substrates). The second (see 3.2), concerns planar thick film elements (resistors, capacitors, single-level patterned hard substrates, and multilevel patterned hard substrates). The third (see 3.3), concerns nonplanar elements (ceramic chip capacitors, tantalum chip capacitors, parallel plate chip capacitors, chip resistors, inductors, and transformers). The fourth (see 3.4) concerns surface acoustic wave (SAW) elements. The inspection criteria contained in each section define the visual requirements for class H and class K elements (classes of passive elements refer to screening requirements of MIL-PRF-38534).

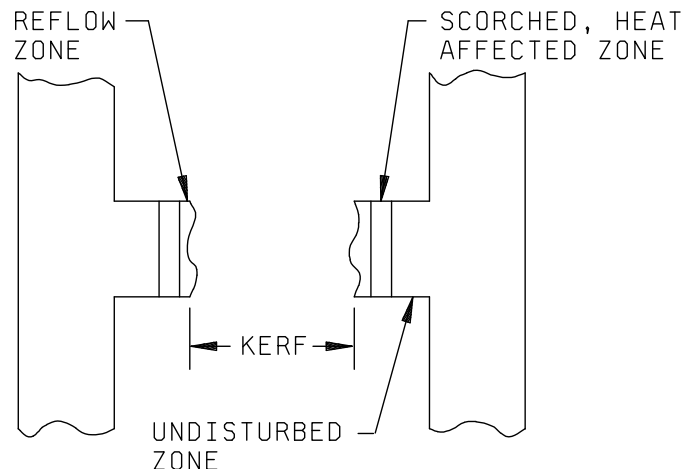
2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (drawings, photographs, etc.) necessary to perform effective inspection and to enable the operator to make objective decisions as to the acceptability of the element being inspected. Adequate fixturing shall be provided for handling elements during inspection to promote efficient operation without inflicting damage to them.

3. PROCEDURE.

- a. General. The element shall be inspected in a suitable sequence of observations within the specified magnification ranges to determine compliance with class H or class K visual requirements. If a specified visual inspection requirement is in conflict with element design, topology or construction, it shall be documented and specifically approved by the acquiring activity. Inspection for all of the visual defect criteria in this test shall be performed on all elements to which they are applicable. Where a criterion is intended for a specific element type, process, or technology, it has been so indicated.
- b. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.
- c. Inspection control. In all cases, inspections prior to the final pre-seal inspection shall be performed under the same quality program that is required at final pre-seal inspection. Care shall be exercised after unmounted element inspection to prevent any handling induced defects from occurring and to insure that defects created during such handling will be detected and rejected at final pre-seal inspection. If an element is electrostatic discharge (ESD) sensitive, then appropriate precautions shall be taken.
- d. Inspection environment. Unmounted element inspection shall be conducted in a 100,000 (0.5 μ m or greater) particles/cubic foot controlled environment (class 8 of ISO 14644-1), except that the maximum allowable relative humidity shall not exceed 65 percent. Mounted element inspection shall be conducted in a 100,000 (0.5 μ m or greater) controlled environment (class 8 of ISO 14644-1) for class H and a 100 (0.5 μ m or greater) controlled environment (class 5 of ISO 14644-1) for class K. During the time interval between final pre-seal inspection and preparation for sealing, mounted elements shall be placed in a controlled environment (see 3.i (7)). Both mounted and unmounted elements shall be in covered containers when transported from one controlled environment to another.

- e. Magnification. "High magnification" inspection shall be performed perpendicular to the element with illumination normal to the element surface. Other angles at which the inspection can be performed, and at which the element can be illuminated, may be used at the option of the manufacturer if the visual presentation is the same as used in the originally specified conditions. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereo microscope with the element under suitable illumination, tilted at an angle not greater than 30° from the perpendicular. The magnification ranges to be used for inspection are specified at the start of each section and are called out at the start of each major criteria grouping.
- f. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection shall be performed at the magnification specified herein, unless a specific magnification is required by the acquisition document.
- g. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly drawing.
- h. Format and conventions. For ease of understanding and comparison, visual criteria are presented side-by-side in a columnar format. Class H criterion are presented in the left column and class K criterion are presented in the right column. When there are differences, the applicable parts of the class H criterion are underlined, for ease of comparison and clarity, and the differences only are shown in the class K column. When there are similarities, the phrase "same as class H" is used with no underlining of the class H criterion. If a requirement is not applicable to either product class, this is indicated by "N/A." A note in the class H column is applicable to class K unless otherwise specified in the class K column. A note in the class K column is applicable to class K only. Two kinds of notes are used herein, regular notes (NOTE:) and precautionary notes (PRECAUTIONARY NOTE:). A regular note is an integral part of a criterion. A precautionary note is not an integral part of the criterion but serves to alert the user to a requirement of the General Specification for Hybrids, MIL-PRF-38534. The phrases "except by design," "intended by design," "by design," or "unless otherwise specified by design" require that the element drawing be referenced to determine intent. For inspections performed at 100X, the criteria of "0.1 mil of passivation, separation, or metal" is satisfied by a "line of passivation, separation, or metal." Reference herein to "that exhibits" is satisfied when the visual image or visual appearance of the element under examination indicates a specific condition is present that does not require confirmation by any other method of testing. When other methods of test are used to confirm that a defect does not exist, they shall be approved by the acquiring activity. In the figures, cross-hatched areas represent metallization, blank areas represent resistor material and shaded areas represent exposed underlying material. The letters "x", "y", or "z" represent the dimension of interest and the letter "d" represents the original dimension. Most figures show the reject condition only.
- i. Definitions:
 - (1) Active circuit area is all functional circuitry, operating metallization, or any connected combinations of these. In the case of resistors, it includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads).
 - (2) Block resistor is a solid, rectangularly shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.
 - (3) Bonding pad is a metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element.
 - (4) Bridging is complete connection between circuit features not intended to be connected.
 - (5) Conductive substrate is one that can conduct electricity. Copper or doped silicon, for example, are conductive substrates. Alumina and quartz, for example, are nonconductive (insulating) substrates.

- (6) Contact window is an opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate.
- (7) Controlled environment is one that has 1,000 or fewer (0.5 μ m or greater) particles/cubic foot in a controlled environment in accordance with the requirements of ISO 14644-1 for a class 6 clean environment, except that the maximum allowable relative humidity shall not exceed 65 percent.
- (8) Corrosion is the gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product.
- (9) Crazing is the presence of numerous, minute, interconnected surface cracks.
- (10) Crossover is the transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing.
- (11) Detritus is fragments of original or trim-modified resistor or conductor material.
- (12) Dielectric is an insulating material that does not conduct electricity but may be able to sustain an electric field. It can be used in crossovers, as a passivation or a glassivation, or in capacitors.
- (13) Foreign material is any material that is foreign to the element or any nonforeign material that is displaced from its original or intended position in the element. It is considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of color fringing around the periphery of the particle.
- (14) Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads. Crazing is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.
- (15) Kerf is the clear area in a trimmed resistor resulting from the removal of resistor material by the trimming operation. In laser trimming, the kerf is bounded by the reflow zone (which is characterized by adherent, melted resistor material), the scorched heat-affected zone (which is characterized by discoloration of the resistor film without alteration of its physical form), and the undisturbed zone.



- (16) Mar is a nontearing surface disturbance such as an indentation or a buff mark.
- (17) Metallization, multilevel (conductors) is alternate layers of metallization, or other material used for interconnection, that are isolated from each other by a grown or deposited insulating material. The term "overlying metallization" refers to any metallization layer on top of the insulating material.
- (18) Metallization, multilayered (conductors) is two or more layers of metallization, or other material used for interconnection, that are not isolated from each other by a grown or deposited insulating material. The term "underlying metallization" refers to any metallization layer below the top layer of metallization.
- (19) Metallization, operating (conductors) is all metallization (gold, aluminum, or other material) used for interconnection. Bonding pads are considered to be operating metallization. Alignment markers, test patterns, and identification markings are not considered to be operating metallization.
- (20) Narrowest resistor width is the narrowest portion of a given resistor prior to trimming; however, the narrowest resistor width for a block resistor may be specified in the approved manufacturer's design documentation.
- (21) Neck-down is tapering of a resistor line at a metallization interface. Resistor material taper is typically equal on both sides of the line and is less abrupt than a void.
- (22) Nicking (partial cut) is incomplete or inadvertent trimming of a resistor adjacent to the one being trimmed or of the next ladder rung of the same resistor.
- (23) Nonplanar element is one that is essentially three-dimensional.
- (24) Original separation is the separation dimension or space that is intended by design.
- (25) Original width is the width dimension that is intended by design.
- (26) Oxide defect is an irregularly shaped defect in the oxide characterized by two or three colored fringes at it edges.
- (27) Passivation is the silicon oxide, silicon nitride, or other insulating material, that is grown or deposited directly on the element prior to the deposition of metal.
- (28) Passivation step is a change in thickness of the passivation layer by design.
- (29) Passive elements are planar resistors, capacitors, inductors, and patterned substrates (both single-layer and multilayer), and nonplanar chip capacitors, chip resistors, chip inductors, and transformers.
- (30) Patterned substrate is a substrate on which conductors, and components such as resistors or capacitors, are formed using thick or thin film manufacturing techniques.
- (31) Planar element is one that is essentially two-dimensional with all points in a common plane.
- (32) Protrusion is a jutting-out of a circuit feature. Protrusion is typically caused by a photolithographic or screening defect.
- (33) Resistor ladder is a resistor structure resembling a ladder in appearance that can be trimmed in incremental steps. A coarse ladder structure is one in which trimming of a rung results in a large incremental resistance change (one that can cause an out-of-tolerance condition to occur). A fine ladder structure is one in which trimming of a rung results in a small incremental resistance change (one that can not cause an out-of-tolerance condition to occur).

- (34) Resistor ladder rung is that portion of a resistor ladder structure intended to be laser trimmed to result in an incremental change in resistance.
- (35) Resistor loop is a resistor structure resembling a loop in appearance that can be trimmed. A coarse loop structure is one in which trimming results in a large resistance change (one that can cause an out-of-tolerance condition to occur). A fine loop structure is one in which trimming results in a small resistance change (one that cannot cause an out-of-tolerance condition to occur).
- (36) Resistor material, self passivating is one on which a conformal insulating layer can be thermally grown (such as tantalum nitride on which tantalum pentoxide is grown).
- (37) Scorching is discoloration of laser trimmed thin film resistor material without alteration of its physical form.
- (38) Scratch, metallization is any tearing defect, including probe marks, in the surface of the metallization. A mar on the metallization surface is not considered to be a scratch.
- (39) Scratch, resistor is any tearing defect in the resistor film. A mar on the resistor surface is not considered to be a scratch.
- (40) Sidebar is that portion of a resistor ladder structure to which rungs are attached. Sidebars are not intended to be laser trimmed.
- (41) Substrate is the supporting structural material into or upon which, or both, functional circuits are formed.
- (42) Surface Acoustic Wave (SAW) element is a planar element fabricated typically using thin film manufacturing techniques on various substrate materials. Size varies as a function of frequency and design features include interdigitated fingers.
- (43) Terminal is a metal area used to provide an electrical access point to functional circuitry.
- (44) Thick film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.
- (45) Thin film is conductive, resistive or dielectric material, usually less than 50,000Å in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.
- (46) Underlying material is any layer of material below the top-layer metallization. This includes metallization, resistor, passivation or insulating layers, or the substrate itself.
- (47) Via is an opening in the insulating material in which a vertical conductive electrical connection from one metallization layer to another is made.
- (48) Vitrification is conversion into glass or a glassy substance by heat and fusion.
- (49) Void, metallization is any missing metallization where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.
- (50) Void, resistor is any missing resistor material where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

- (51) Wraparound conductor is one which extends around the edge of the substrate by design.
- (52) Coupling (air) bridge is a raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material.
- (53) Pit is a depression produced in a substrate surface typically by nonuniform deposition of metallization or by nonuniform processing such as excessively powered laser trim pulses.
- (54) Substrate, hard is the inorganic, rigid material into or upon which or both, functional circuits are formed. Typical materials are alumina and silicon.
- (55) Blister, metallization is a hollow bump that can be flattened.
- (56) Nodule, metallization is a solid bump that cannot be flattened.
- (57) Substrate plug via is a cylinder-like volume in the substrate material filled with conductive material which makes electrical connection from contact areas on the top surface to the back surface of the substrate..

3.1 Thin film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thin film passive element. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 30X to 60X for both class H and class K. When inspection is performed prior to mounting, then elements utilizing ceramic or glass type substrates, without backside metallization, shall be inspected using backlighting for conditions of hair-line voiding or bridging. Patterned substrates that have geometries of 2.0 mils or greater shall be inspected at 10X to 60X magnification.

Class H

Class K

- 3.1.1 Operating metallization defects "high magnification". No element shall be acceptable that exhibits:
 NOTE: The metallization defect criteria contained in this section apply to operating metallization only.

3.1.1.1 Metallization scratches.

- a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes under-lying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see 2032-1h).
 NOTE: These criteria do not apply to capacitors (see 3.1.1.1e).
 NOTE: Underlying material does not have to be exposed along the full length of the scratch.

- a. Same as Class H.

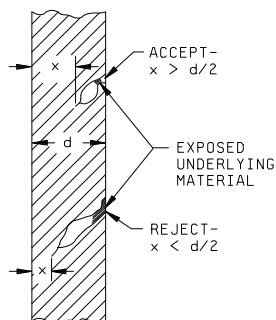


FIGURE 2032-1h. Class H metallization scratch criteria.

Class H

- 3.1.1.1 b. Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, and leaves less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-2h).

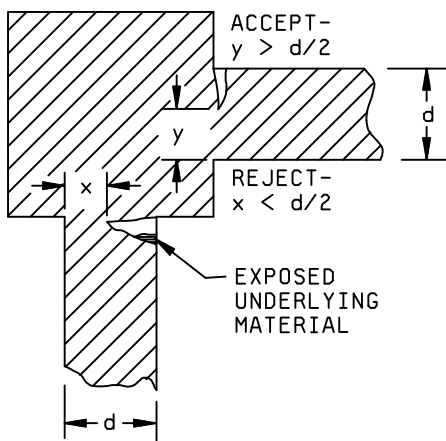


FIGURE 2032-2h. Class H metallization width reduction at bonding pad criteria.

- 3.1.1.1 c. Scratch that completely crosses a Metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side.
- d. Scratches or probe marks in the bonding pad area that expose underlying material over greater than 25 percent of the original unglassivated metallization area.
- e. For capacitors only, a scratch in the metallization, other than in the bonding pad area, that exposes the dielectric material.

Class K

- 3.1.1.1 b. Less than 75 percent (see figure 2032-2k).

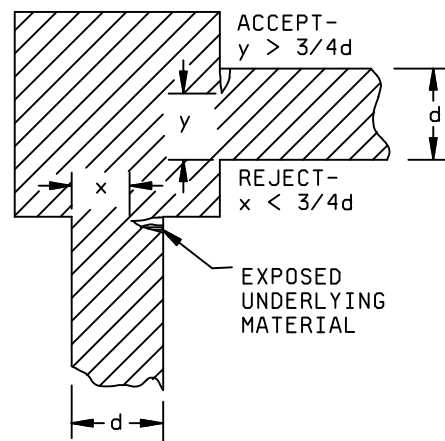


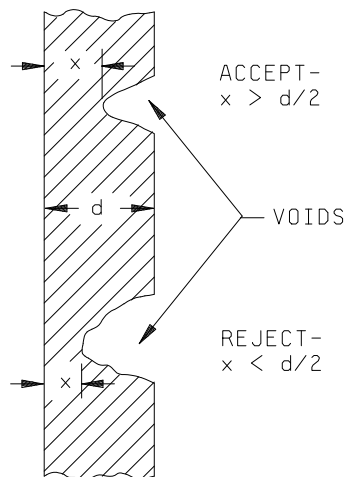
FIGURE 2032-2k. Class K metallization width reduction at bonding pad criteria.

- c. Same as class H.
- d. Same as class H.
- e. Same as class H.

Class HClass K3.1.1.2 Metallization voids.

- a. Void(s) in the metallization, excluding bonding pads, that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-3h).

- a. Same as Class H

FIGURE 2032-3h. Class H metallization void criteria.

- b. Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately.

NOTE: Figures 2032-2h and 2032-2k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.

- b. Less than 75 percent

Class H

- 3.1.1.2 c. Void(s) in the bonding pad area that expose underlying material over greater than 25 percent of the original unglassivated metallization area.

NOTE: For RF/microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.

- d. For capacitors only, void(s) in metallization, other than in the bonding pad area, that reduces the metallization to an extent greater than an area equivalent to 25 percent of the capacitor metallization.
- e. For interdigitated capacitors only, void(s) in the metallization that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-4h).

Class K

- 3.1.1.2 c. Same as class H.

- d. Same as class H.

- e. Less than 75 percent (see figure 2032-4k).

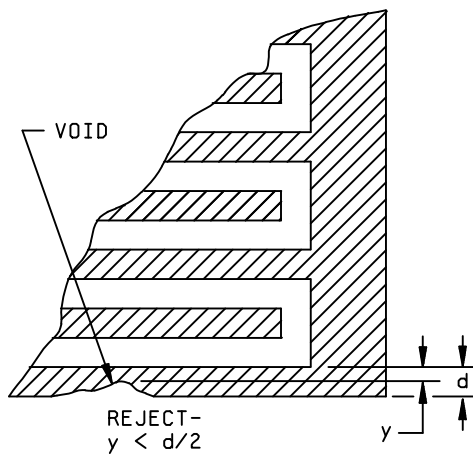


FIGURE 2032-4h. Class H interdigitated capacitor metallization void criterion.

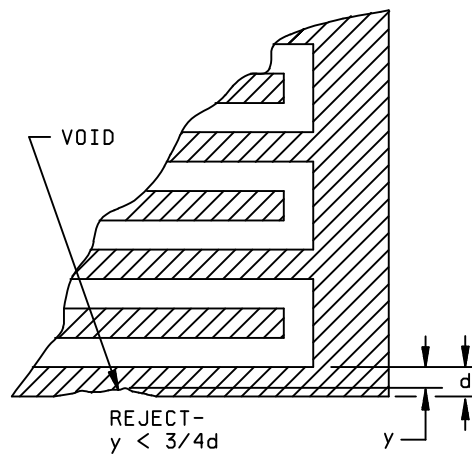


FIGURE 2032-4k. Class K interdigitated capacitor metallization void criterion.

Class HClass K3.1.1.3 Metallization corrosion.

- a. Any metallization corrosion.

- a. Same as class H.

NOTE: Metallization having any localized discolored area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

3.1.1.4 Metallization adherence.

- a. Any metallization lifting, peeling, or blistering.
NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister.
NOTE: These criteria are not applicable to undercutting or separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.

- a. Same as class H.

3.1.1.5 Metallization protrusion.

- a. Protrusion of metallization that reduces the original separation between adjacent operating metallization by greater than 50 percent (see figure 2032-5h).

- a. Same as class H.

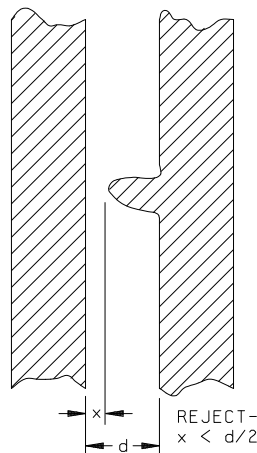


FIGURE 2032-5h. Class H operating metallization protrusion criterion.

Class H

- 3.1.1.5 b. For interdigitated capacitors only, protrusion of metallization that reduces the original separation by greater than 50 percent (see figure 2032-6h).

Class K

- 3.1.1.5 b. Same as class H.

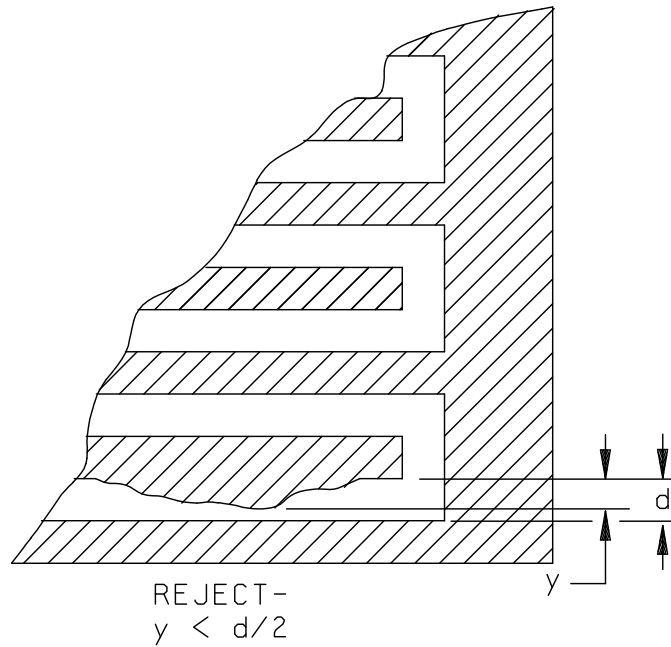


FIGURE 2032-6h. Class H interdigitated capacitor metallization protrusion criterion.

3.1.1.6 Metallization alignment.

- a. A contact window that has less than 50 percent of its area covered by metallization.

- a. Less than 75 percent.

Class H

- 3.1.1.6 b. A contact window that has less than a continuous 40 percent of its perimeter covered by metallization (see figure 2032-7h).

NOTE: When, by design, metallization is completely contained in a contact window, or does not cover the entire contact perimeter, 3.1.1.6a, area coverage, or 3.1.1.6b, perimeter coverage, can be deleted as applicable provided that the design criteria are satisfied.

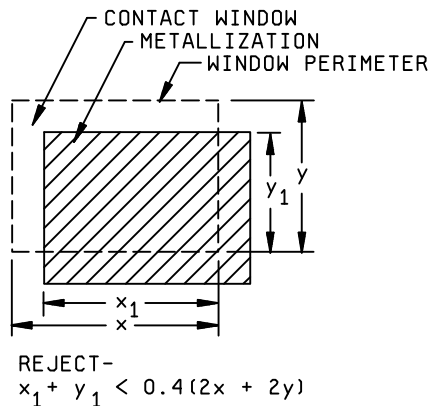


FIGURE 2032-7h. Class H metallization alignment criteria.

- c. A metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil unless by design.

3.1.1.7 Metallization bumps or indentations.

- a. For capacitors only, a bump or indentation in the overlaying metallization.

Class K

- 3.1.1.6 b. 50 percent of its perimeter (see figure 2032-7k).

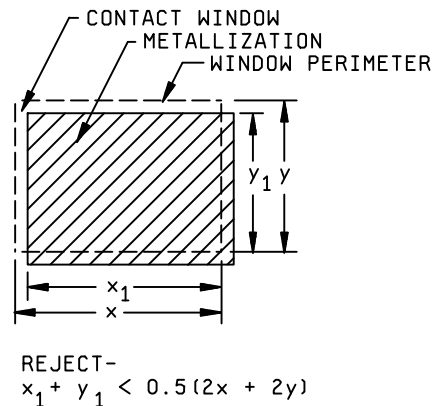


FIGURE 2032-7k. Class K metallization alignment criteria.

- c. Same as Class H.

- a. Same as class H.

Class H

Class K

- 3.1.1.8 Metallized through-hole defects.
"high magnification". No element shall be acceptable that exhibits:

- a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.

- a. Same as class H.

- 3.1.1.9 Wrap-around connection defects, "high magnification". No element shall be acceptable that exhibits:

- a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-8h).

- a. Same as class H.

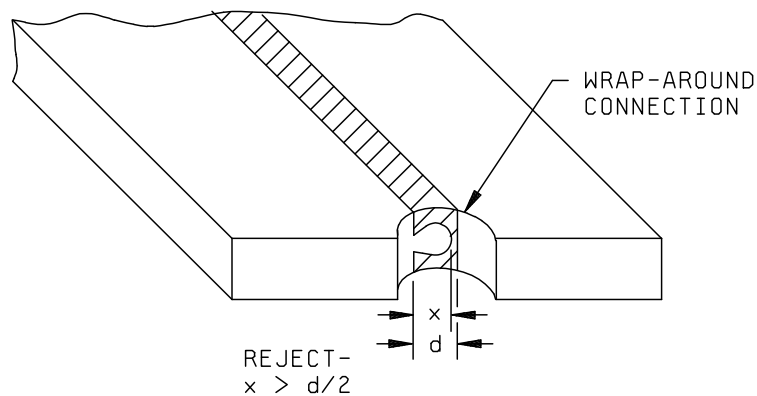


FIGURE 2032-8h. Class H wrap-around connection unmetallized area criterion.

3.1.1.10 Substrate plug via defects, "low magnification". When inspected from each side of the substrate, no element shall be acceptable that exhibits:

- A complete void through the via.
- Any lifting, peeling, or blistering of the via metallization.
- Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.

NOTE: These are minimum requirements. Via flatness and other requirements shall be in accordance with the applicable detail drawings. The via fill may consist of thick film metallization.

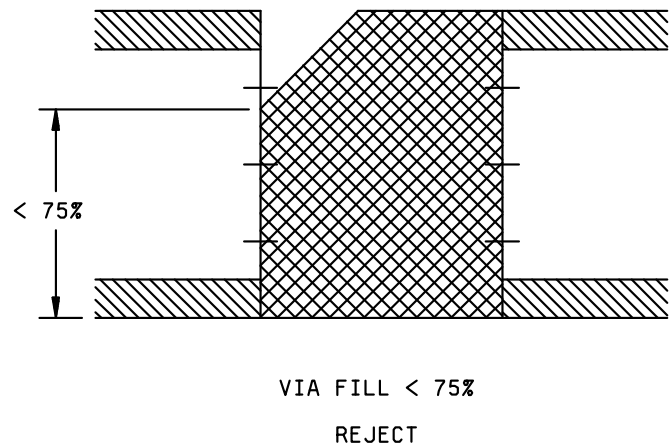
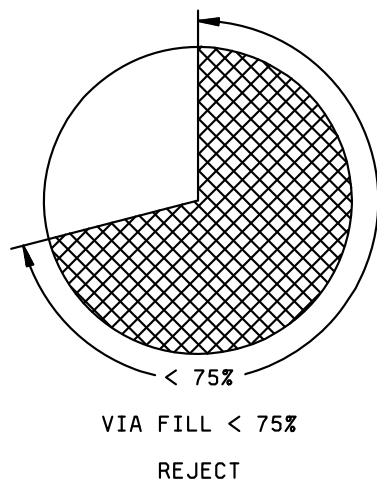


FIGURE 2032-8Bh. Classes H and K via plug fill criteria

Class HClass K3.1.2 Passivation defects "high magnification".

No element shall be acceptable that exhibits:

- a. Either multiple lines (color fringing) or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2032-8Ah). A passivation defect that exhibits a line of separation from the metallization is acceptable.
- NOTE: These criteria apply to conductive substrate elements only.
- NOTE: Double or triple lines at the edge of the passivation defect indicate it can have sufficient depth to penetrate down to the bare substrate.

- a. Same as class H.

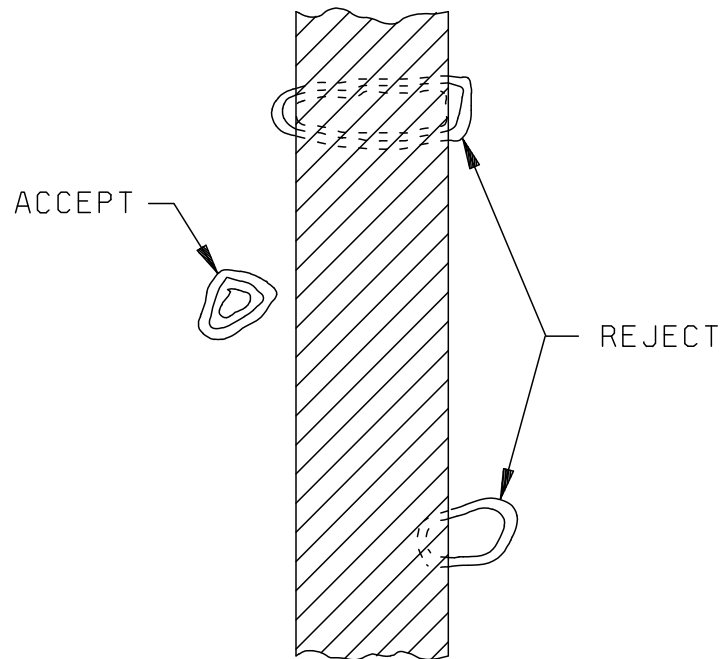


FIGURE 2032-8Ah. Class H passivation defect criteria.

Class HClass K3.1.3 Glassivation defects, "high magnification".

No device shall be acceptable that exhibits:

NOTE: Criteria of 3.1.3 can be excluded when the defects are due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation defects, equal to or greater than 50 percent of the narrowest resistor width, (see figure 2032-9h).

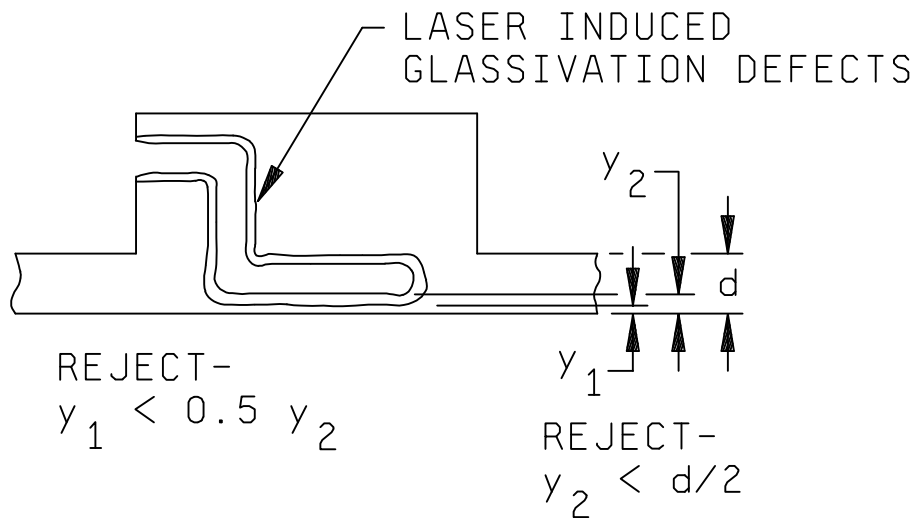


FIGURE 2032-9h. Class H laser trimmed glassivation defect criteria.

a. Glass crazing or damage that prohibits the detection of visual criteria contained herein.

a. Same as class H.

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	<u>Class H</u>		<u>Class K</u>
3.1.3	<p>b. Any lifting or peeling of the glassivation. NOTE: Lifting or peeling of the glassivation is acceptable when it does not extend more than 1.0 mil from the designed periphery of the glassivation, provided that the only exposure of metallization is of adjacent bonding pads or of metallization leading from those pads.</p> <p>c. A void in the glassivation that exposes two or more adjacent operating metallization paths, excluding bonding pad cutouts, unless by design.</p> <p>d. Unglassivated nonactive circuit areas greater than 5.0 mils in any dimension, unless by design.</p> <p>e. Unglassivated areas at the edge of a bonding pad exposing the conductive substrate.</p> <p>f. Glassivation covering more than 25 percent of a bonding pad area.</p> <p>g. Crazing in glassivation over a resistor.</p> <p>h. Misalignment of the glassivation that results in incomplete coverage of a resistor, unless by design.</p> <p>i. Glassivation scratches or voids that expose any portion of a resistor or fusible link except for polycrystalline silicon links where the glassivation is opened by design.</p> <p>j. Scratches in the glassivation that disturb metallization and bridge metallization paths.</p> <p>k. Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallization paths.</p>	3.1.3	<p>b. Same as class H.</p> <p>c. Same as class H.</p> <p>d. Same as class H.</p> <p>e. Same as class H.</p> <p>f. Same as class H.</p> <p>g. Same as class H.</p> <p>h. Same as class H.</p> <p>i. Same as class H.</p> <p>j. Same as class H.</p> <p>k. Same as class H.</p>

Class HClass K3.1.4 Substrate defects "high magnification".

No element shall be acceptable that exhibits:

- a. Less than 0.1 mil of separation between the operating metallization and the edge of the element unless by design (see figure 2032-10h).

NOTE: For elements containing wraparound conductors or for bonding pads of RF/microwave elements that are coincident with the element edge (as documented on the design drawing) this criteria does not apply. When bond pad metallization is coincident with the element edge, a minimum separation of 1.0 mil shall exist between the bonding pad metallization at the element edge and any noncommon conductive surface.

- b. A chipout that extends into the active circuit area (see figure 2032-10h).

- a. Same as Class H.

- b. Same as class H.

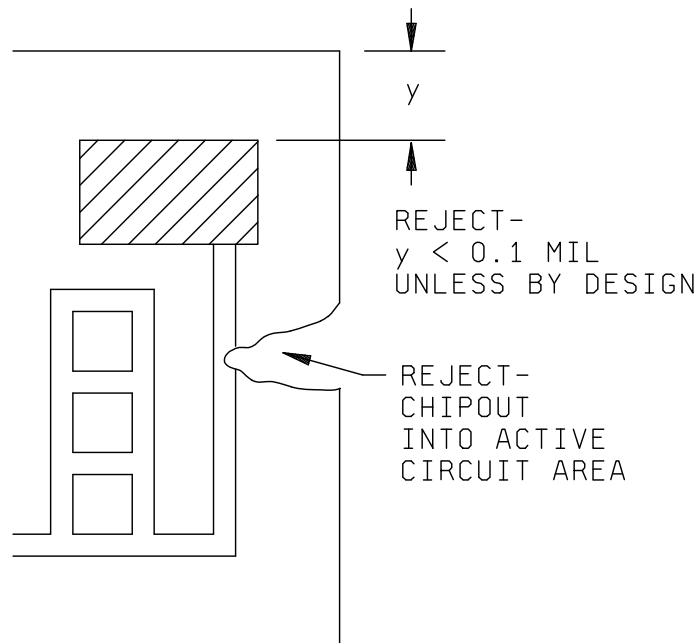
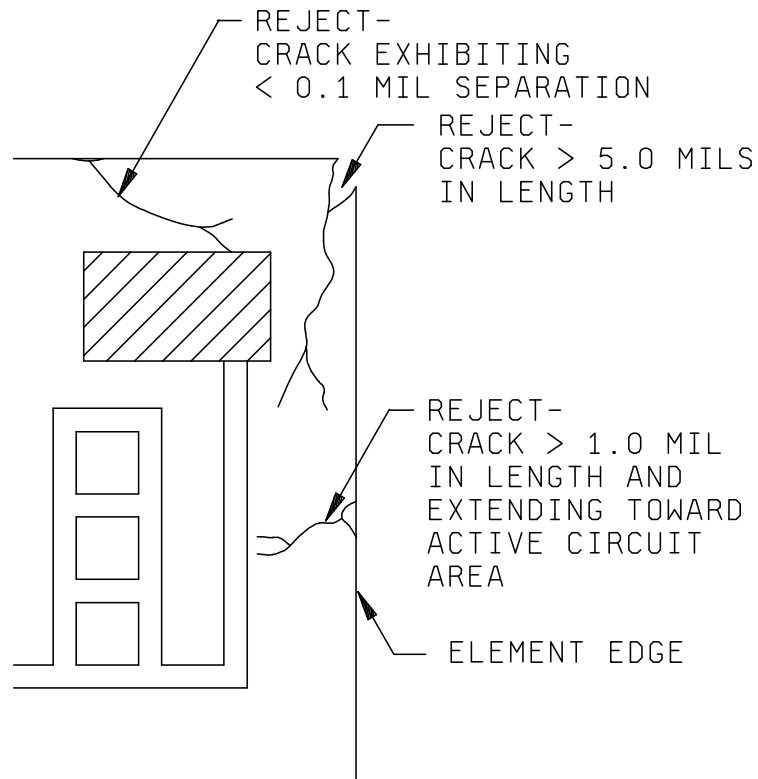


FIGURE 2032-10h. Class H separation and chipout criteria.

- | <u>Class H</u> | <u>Class K</u> |
|--|---|
| <p>3.1.4 c. Any crack that exceeds <u>5.0 mils in length</u> (see figure 2032-11h).
NOTE: For fused quartz or crystalline substrates, no cracking is allowed.</p> <p>d. Any crack that does not exhibit <u>0.1 mil</u> of separation from any active circuit area or operating metallization (see figure 2032-11h).</p> <p>e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-11h).</p> | <p>3.1.4 c. Same as Class H.</p> <p>d. 0.25 mil (see figure 2032-11k).</p> <p>e. Same as class H.</p> |

FIGURE 2032-11h. Class H crack criteria.

Class H

3.1.4 f. N/A

Class K

3.1.4 f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-12k).

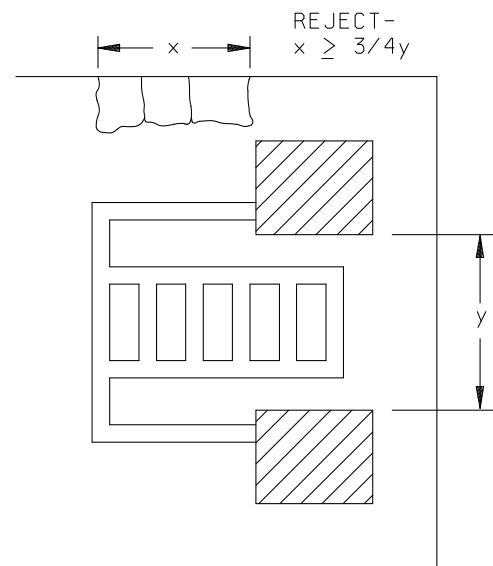


FIGURE 2032-12k. Class K semicircular crack criterion.

- g. An attached portion of an active circuit area from an adjacent element.
- h. Any crack that does not originate at an edge.
- i. Holes through the substrate, unless by design.

- g. Same as class H.
- h. Same as class H.
- i. Same as class H.

Class HClass K3.1.5 Foreign material defects "low magnification".

No element shall be acceptable that exhibits:

- | | |
|---|----------------------------|
| <p>a. For mounted elements, unattached, conductive foreign material on the surface of the elements. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization paths, active circuitry, or any combination of these.
NOTE: If an element has an insulating layer (such as glassivation or self-passivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of unattached, conductive foreign material, that is large enough to bridge these features, is acceptable since the features are protected by the insulating layer.
NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.), or by a suitable cleaning process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 20 psig).
NOTE: Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.
NOTE: Semiconductor particles are considered to be foreign material.</p> | <p>a. Same as class H.</p> |
| <p>b. Attached, conductive foreign material that bridges metallization paths, active circuitry, or any combination of these.</p> | <p>b. Same as class H.</p> |
| <p>c. Liquid droplets, ink drops, or chemical stains that appear to bridge any unglassivated or unpassivated active circuit areas.</p> | <p>c. Same as class H.</p> |
| <p>d. Attached foreign material that covers greater than 25 percent of a bonding pad area.</p> | <p>d. Same as class H.</p> |

Class HClass K

3.1.6 Thin film resistor defects, "high magnification".
 No element shall be acceptable that exhibits:

- a. Voids at the terminal that reduces the resistor width to less than 50 percent of the original resistor width (see figure 2032-13h).

- a. Same as Class H

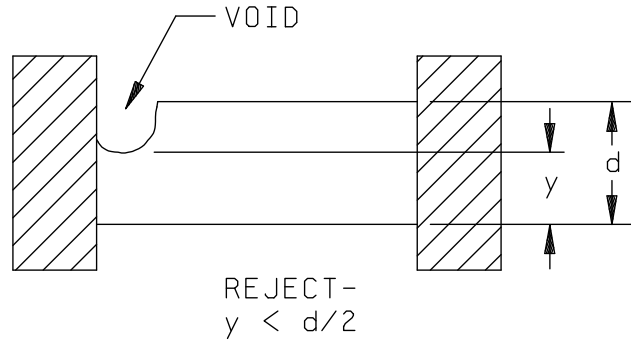


FIGURE 2032-13h. Class H film resistor width reduction at terminal by voids criterion.

- b. Neckdown at the terminal that reduces the resistor width to less than 75 percent of the original resistor width (see figure 2032-14h).

- b. Same as Class H.

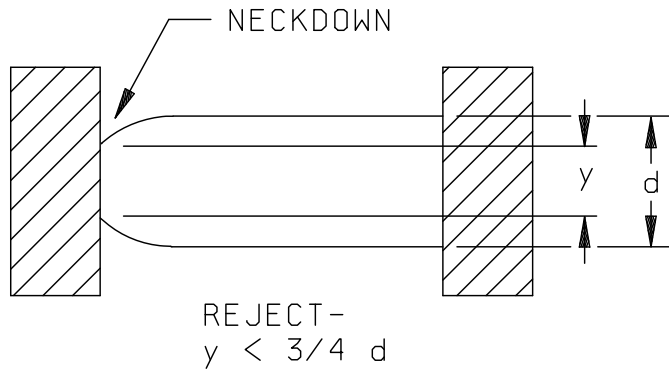


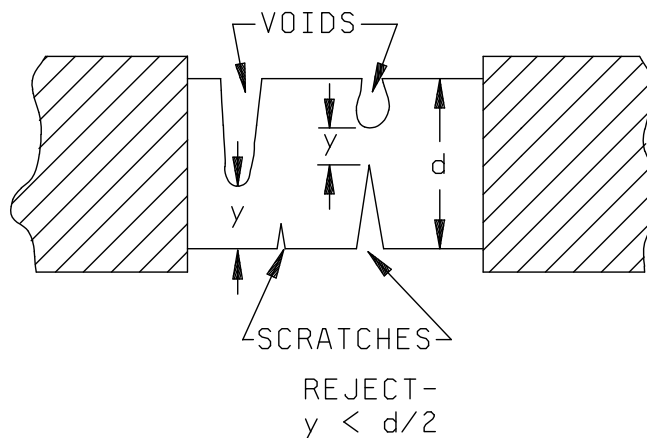
FIGURE 2032-14h. Class H film resistor width reduction at terminal by necking criterion.

Class H

- 3.1.6 c. Any sharp (clearly defined) color change within 0.1 mil of the terminal.
NOTE: A sharp color change close to the terminal usually indicates an abrupt reduction of resistor film thickness. This color change usually occurs in a straight line parallel to the terminal. A gradual color change, or a nonuniform or mottled color anywhere in the resistor, is not cause for rejection.
- d. Any resistor film lifting, peeling or blistering.
- e. Reduction of resistor width, resulting from voids, scratches, or a laser trim kerf or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-15h).
PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.

Class K

- 3.1.6 c. Same as class H.
- d. Same as class H.
- e. Same as class H.

FIGURE 2032-15h. Class H resistor width reduction by voids and scratches criteria.

Class H

- 3.1.6 f. Contact overlap between the metallization and the resistor in which the width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-16h).

Class K

- 3.1.6 f. Same as Class H.

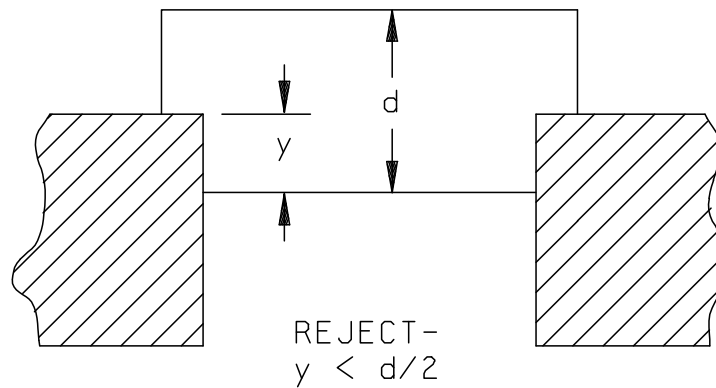


FIGURE 2032-16h. Class H metal/resistor overlap criterion.

- g. Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 0.25 mil (see figure 2032-17h).

- g. Same as class H.

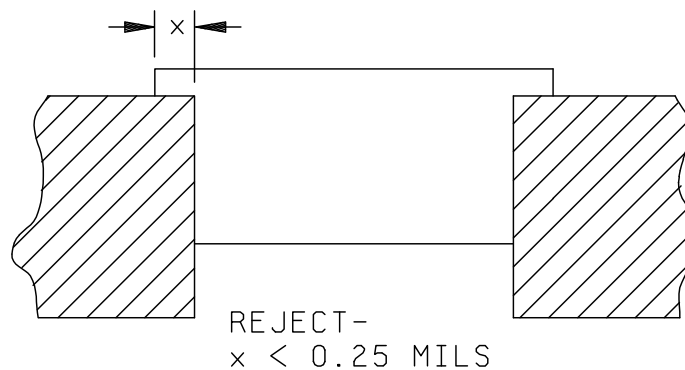


FIGURE 2032-17h. Class H contact overlap criterion.

Class H

- 3.1.6 h. More than a 50 percent reduction of the original separation, between any two different resistors, or a resistor and metallization not associated with it (see figure 2032-18h).

Class K

- 3.1.6 h. Same as class H.

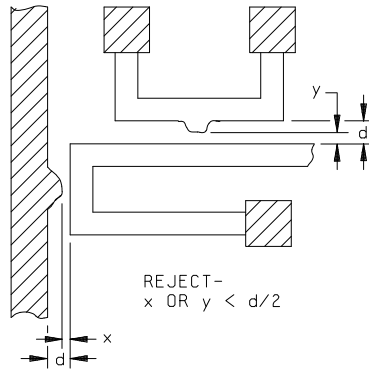


FIGURE 2032-18h. Class H resistor separation criteria.

- i. Any resistor that crosses a substrate irregularity (such as a void or scratch) (see figure 2032-19h).
NOTE: This criterion is applicable to conductive substrates only.

- i. Same as class H.

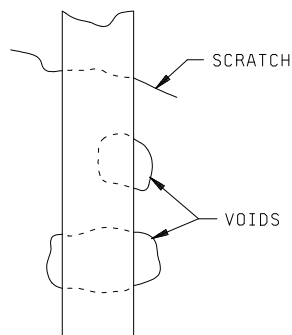


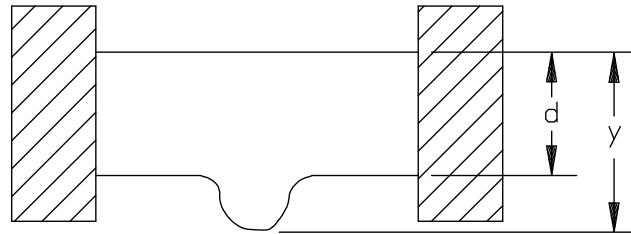
FIGURE 2032-19h. Class H substrate irregularity criterion.

Class H

- 3.1.6 j. Any increase in resistor width of a block resistor greater than 25 percent of the original resistor width (see figure 2032-20h).

Class K

- 3.1.6 j. Same as class H.



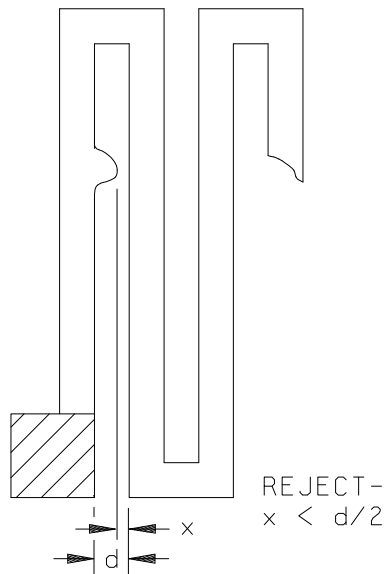
REJECT -
 $y > 5/4 d$

FIGURE 2032-20h. Class H resistor width increase criterion.

- k. Protruding resistor material within the same resistor structure that reduces the original separation to less than 50 percent (see figure 2032-21h).

NOTE: This criteria applies to protrusion of resistor material resulting from a photo-lithographic defect.

- k. Same as class H.



REJECT -
 $x < d/2$

FIGURE 2032-21h. Class H protrusion of resistor material criterion.

Class H

- 3.1.6 I. Bridging within the same resistor pattern where the width of the bridge is less than 50 percent of the narrowest line being bridged (see figure 2032-22h).

Class K

- 3.1.6 I. Same as class H.

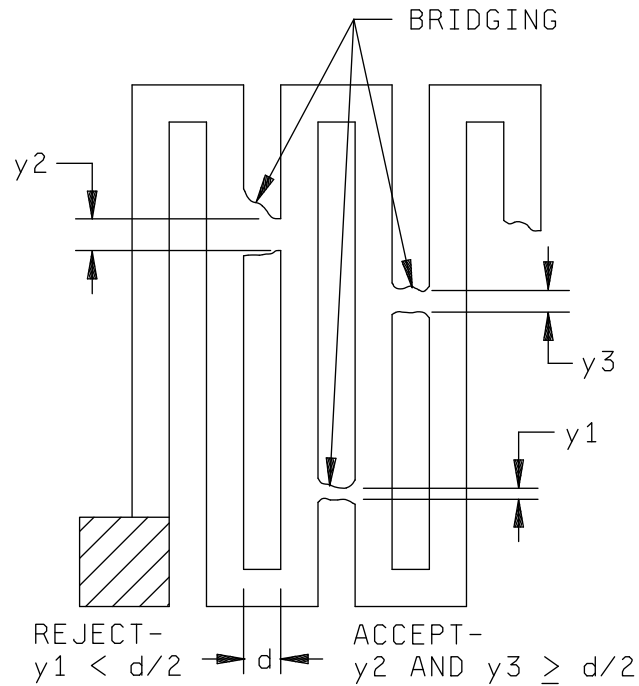


FIGURE 2032-22h. Class H bridging of resistor material criteria.

- 3.1.7 Laser trimmed thin film resistor defects.
"high magnification". No element shall be acceptable that exhibits:
 NOTE: The laser trim defect criteria contained in this section apply to active resistor areas only.

Class H

- 3.1.7 a. A kerf width less than 0.1 mil (see figure 2032-23h).
NOTE: This does not apply to edge trimming.

Class K

- 3.1.7 a. Same as class H.

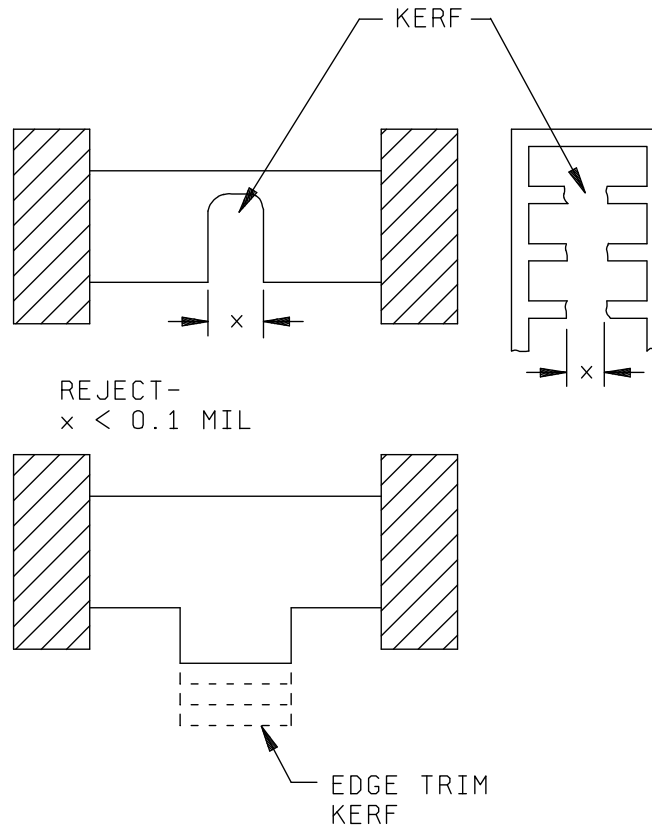


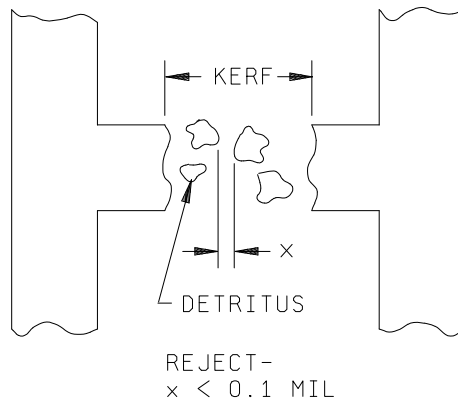
FIGURE 2032-23h. Class H kerf width criteria.

- b. A kerf containing particles of detritus.
NOTE: For resistor materials that are self-passivating (such as tantalum nitride), detritus in the kerf is allowed provided that a clear path of at least 0.1 mil in width exists in the kerf. Such detritus shall be attached. Verification of attachment shall be accomplished using the techniques described in 3.1.5a (see figure 2032-24h).
NOTE: This does not apply to edge trimming.

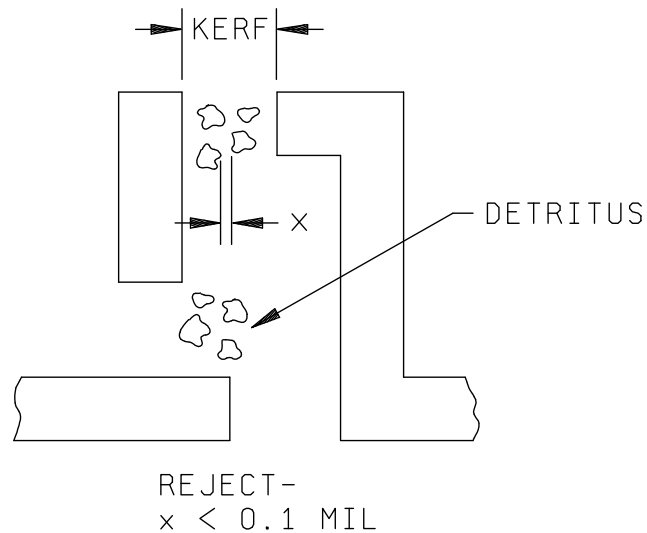
- b. Same as class H.

Class HClass K

3.1.7 b. (Continued.)

FIGURE 2032-24h. Class H detritus criterion for self-passivating resistor materials.

NOTE: In the case of a resistor loop made with self-passivating resistor material which is similar in configuration to the one shown in figure 2032-25h, there shall be at least one kerf that contains a clear path of at least 0.1 mil in width; otherwise, the element shall be rejected.

FIGURE 2032-25h. Class H resistor loop element detritus criterion for self-passivating resistor materials.

Class H

- 3.1.7 c. Bridging of detritus between rungs in the active area of a resistor ladder structure (see figure 2032-26h).
NOTE: Bridging of detritus in inactive areas is acceptable.

Class K

- 3.1.7 c. Same as class H.

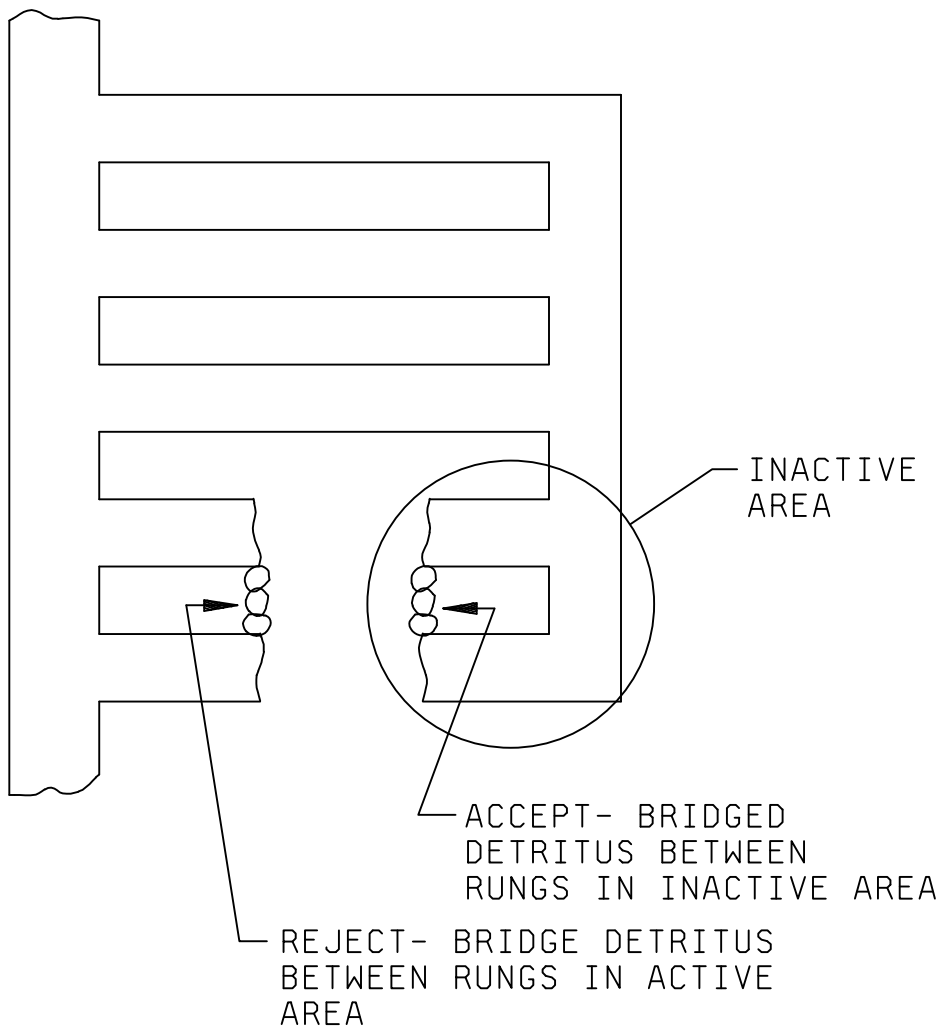


FIGURE 2032-26h. Bridging of detritus between rungs in the active area of a resistor ladder structure criterion.

Class H

Class K

- 3.1.7

d.

No nicking or scorching is allowed except as permitted below.
NOTE: This does not apply to rungs in a fine resistor ladder structure (see figure 2032-27h).
NOTE: See 3.i.(33) for a definition of coarse and fine resistor ladder structures.
The element drawing must be referenced to determine if a given resistor ladder structure is coarse or fine.
- 3.1.7

d.

Same as class H.

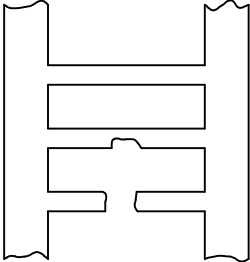
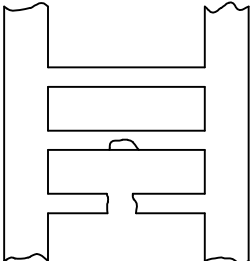
	COARSE LADDERS	FINE LADDERS
<div>NICKING</div> 	REJECT	ACCEPT
<div>SCORCHING</div> 	REJECT	ACCEPT

FIGURE 2032-27h. Class H resistor ladder structure nicking and scorching criteria exceptions.

Class H

Class K

- 3.1.7
- d.
- (Continued.)
- NOTE: This criteria does not apply to the second rung of a resistor loop since the second rung is inactive. This criteria does not apply to a fine loop or to a resistor structure that is comprised of fine loops (see figure 2032-28h).
- NOTE: See 3.i.(35) for a definition of coarse and fine resistor loop structures. The element drawing must be referenced to determine if a given resistor loop structure is coarse or fine.

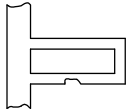
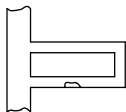
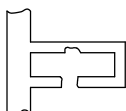
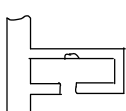
		COARSE LOOPS	FINE LOOPS
NICK IN FIRST (ACTIVE) RUNG		REJECT	ACCEPT
SCORCH IN FIRST (ACTIVE) RUNG		REJECT	ACCEPT
NICK IN SECOND (INACTIVE) RUNG		ACCEPT	ACCEPT
SCORCH IN SECOND (INACTIVE) RUNG		ACCEPT	ACCEPT

FIGURE 2032-28h. Class H resistor loop nicking and scorching criteria exceptions.

Class HClass K

- 3.1.7 d. (Continued.)
 NOTE: This criterion does not apply to the last rung of a resistor ladder if the last rung is inactive (see figure 2032-29h).

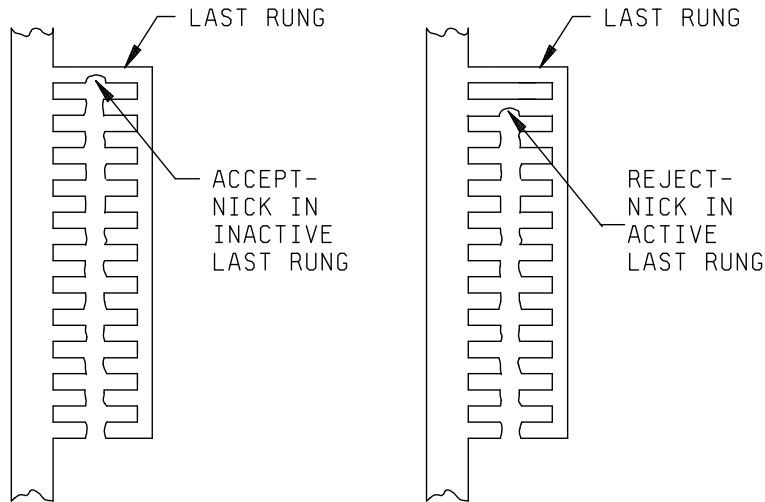


FIGURE 2032-29h. Class H laser nicking criteria exception for the last rung of a resistor ladder.

- e. A kerf or scorch which extends into a resistor ladder sidebar (see figure 2032-30h).
 e. Same as class H.

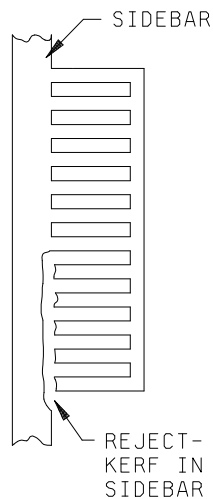
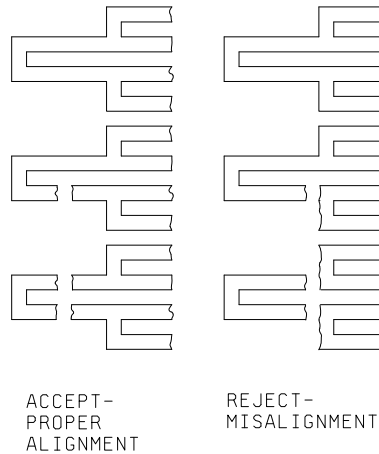
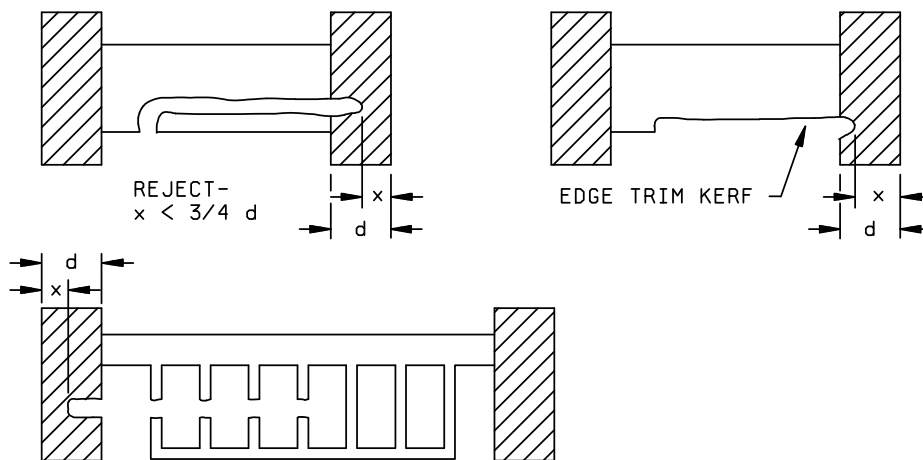


FIGURE 2032-30h. Class H resistor ladder sidebar trim criterion.

- | | <u>Class H</u> | | <u>Class K</u> |
|-------|---|-------|---------------------|
| 3.1.7 | f. Kerf or scorch misalignment (see figure 2032-31h). | 3.1.7 | f. Same as class H. |

FIGURE 2032-31h. Class H laser trim misalignment criteria.

- | | | | |
|----|--|----|------------------|
| g. | A kerf which extends into metallization and leaves less than 75 percent of the metallization width undisturbed (see figure 2032-32h).
NOTE: Opening a metallization link by design is acceptable. | g. | Same as class H. |
|----|--|----|------------------|

FIGURE 2032-32h. Class H laser trim kerf extension into metallization criteria.

Class H

- 3.1.7 h. A kerf in a resistor, at the interface of the resistor material with the metallization, that leaves less than 50 percent of the original resistor width, unless by design.
 PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded. (see figure 2032-33h).

Class K

- 3.1.7 h. Same as class H.

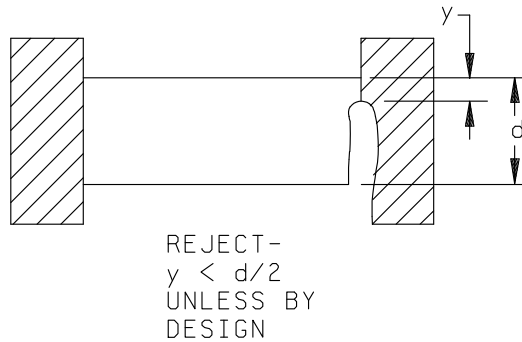


FIGURE 2032-33h. Class H resistor width reduction at metallization interface criteria.

- i. A kerf in a resistor that leaves less than 50 percent of the original resistor width, unless by design.
 PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded (see figure 2032-34h).

- i. Same as class H.

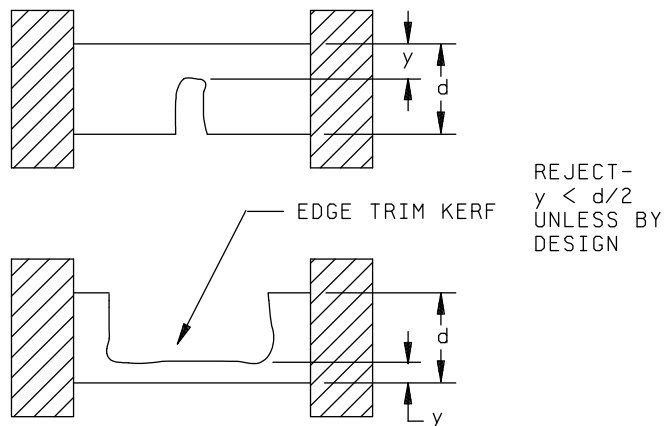


FIGURE 2032-34h. Class H resistor width reduction by trimming criteria.

Class H

- 3.1.7 j. A kerf in a resistor that leaves less than 50 percent of the narrowest resistor width unless by design (see figure 2032-35h).
 NOTE: A floating kerf (one that is completely contained within the resistor) must meet this criteria.
 PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.

Class K

- 3.1.7 j. Same as class H.

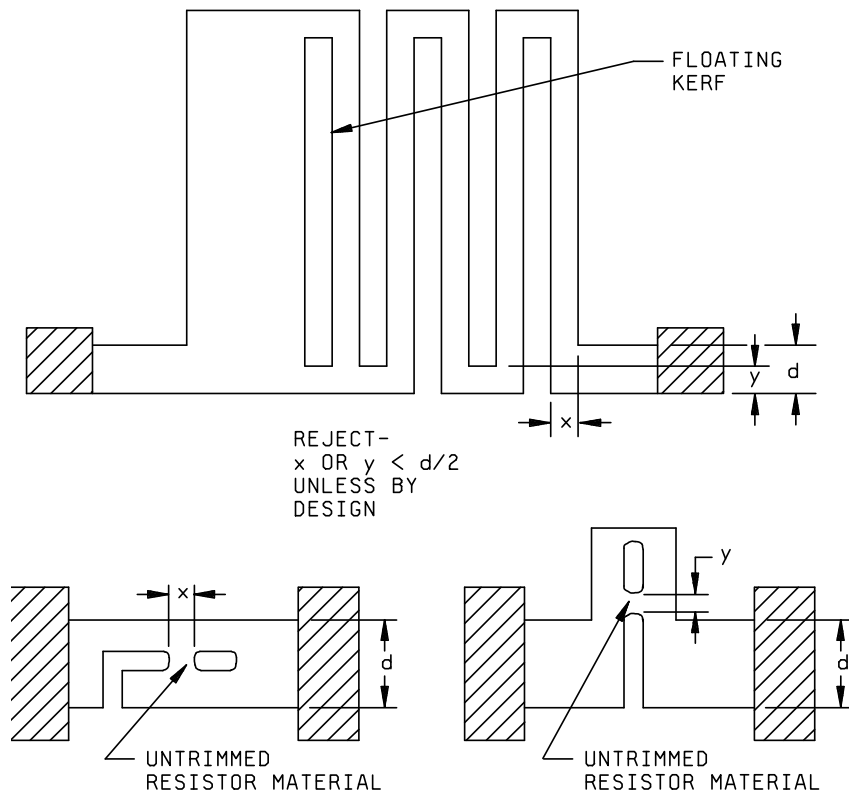


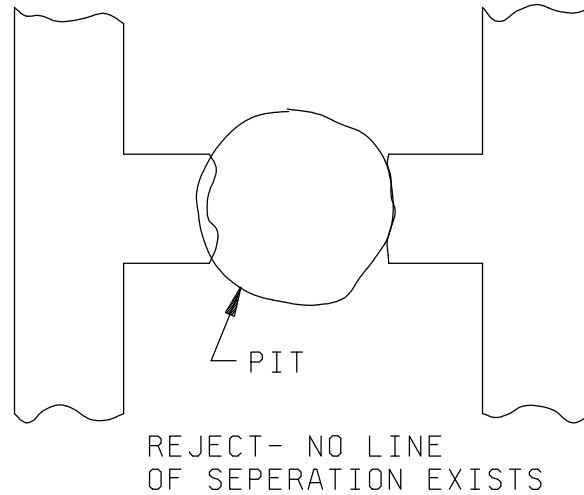
FIGURE 2032-35h. Class H resistor width reduction and untrimmed resistor material criteria.

- k. Pits into the silicon dioxide of conductive substrate elements in the kerf which does not show a line of separation between the pit and the resistor material (see figure 2032-36h).

- k. Same as class H.

Class HClass K

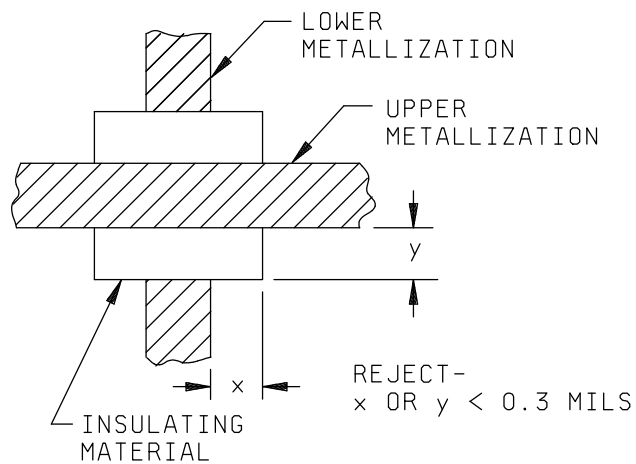
3.1.7 k. (Continued.)

FIGURE 2032-36h. Class H laser trim pitting criterion.

3.1.8 Multilevel thin film defects, "high magnification". No element shall be acceptable that exhibits:

- a. Insulating material that does not extend beyond the width of the upper and lower metallization by 0.3 mil minimum (see figure 2032-37h).

- a. Same as class H.

FIGURE 2032-37h. Class H insulating material extension criteria.

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	<u>Class H</u>		<u>Class K</u>
3.1.8	b. Voids in the insulating material.	3.1.8	b. Same as class H.
	c. A bump or indentation in the upper (overlying) metallization. NOTE: This criteria is not applicable to coupling (air) bridges.		c. Same as class H.
	d. Scratch that completely crosses the metallization and damages the insulating material surface on either side.		d. Same as class H.

3.1.9 Coupling (air) bridge defects "high magnification". No element shall be acceptable that exhibits:

	<u>Class H</u>		<u>Class K</u>
	a. A void in the coupling (air) bridge metallization that leaves less than 50 percent of the original metallization width undisturbed. (See figure 2032-37Ah).		a. Same as class H.
	b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2032-37Ah).		b. Same as class H.
	c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2032-37Ah).		c. Same as class H.
	d. Attached, conductive foreign material that is greater, in any dimension, than 50 percent of the original coupling (air) bridge metallization width.		d. Same as class H.
	e. No visible separation between the coupling (air) bridge and the underlying operating metallization. NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2032-37Ah).		e. Same as class H.
	f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2032-37Ah).		f. Same as class H.
	g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.		g. Same as class H.

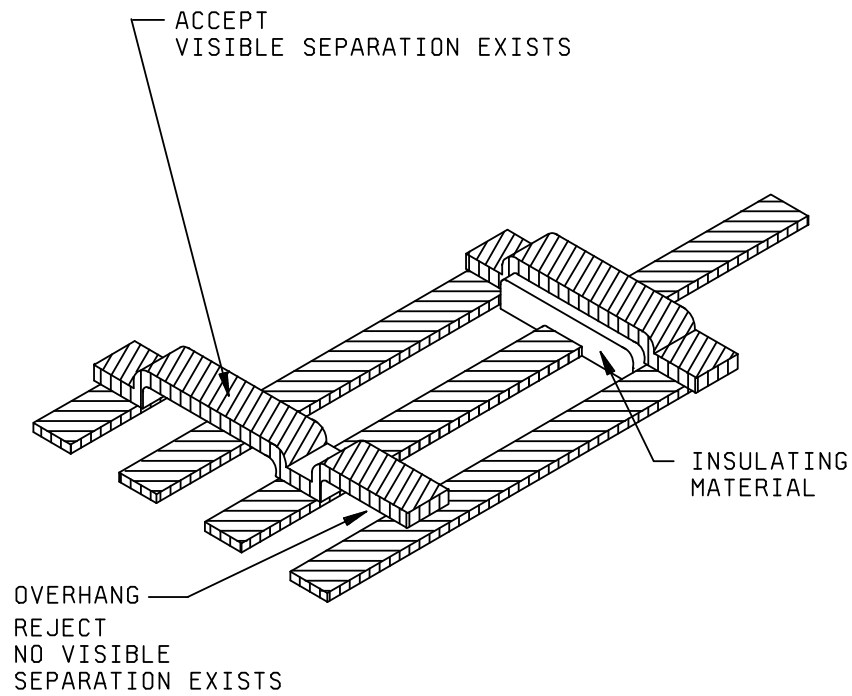
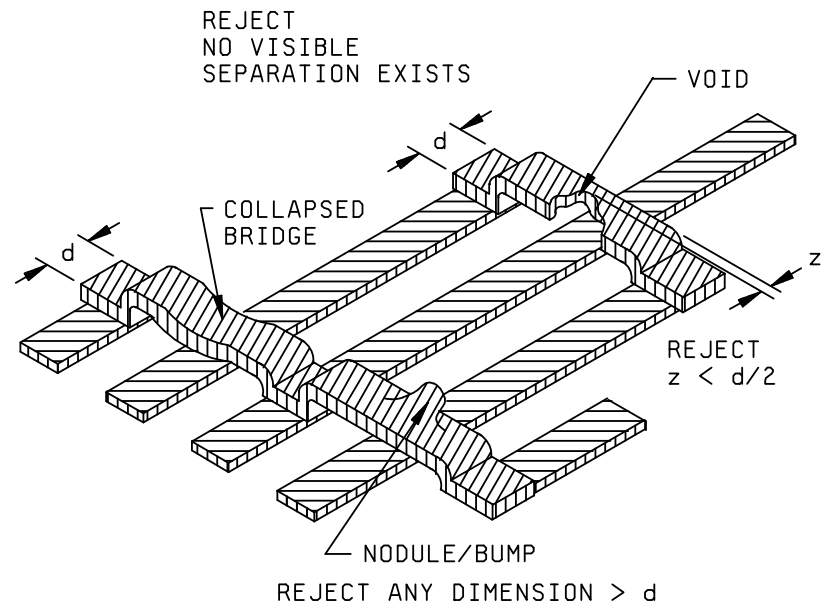


FIGURE 2032-37Ah. Class H and class K coupling (air) bridge criteria.

3.2 Planar thick film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thick film passive element. All inspection shall be performed at "low magnification" within the range of 10X to 60X magnification for both class H and class K.

Class HClass K

3.2.1 Operating metallization defects "low magnification". No element shall be acceptable that exhibits:
 NOTE: The metallization defect criteria contained in this section apply to operating metallization only.

3.2.1.1 Metallization scratches

- a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-38h).
 NOTE: Underlying material does not have to be exposed along the full length of the scratch.
 NOTE: This criteria does not apply to capacitors.

- a. Same as Class H.

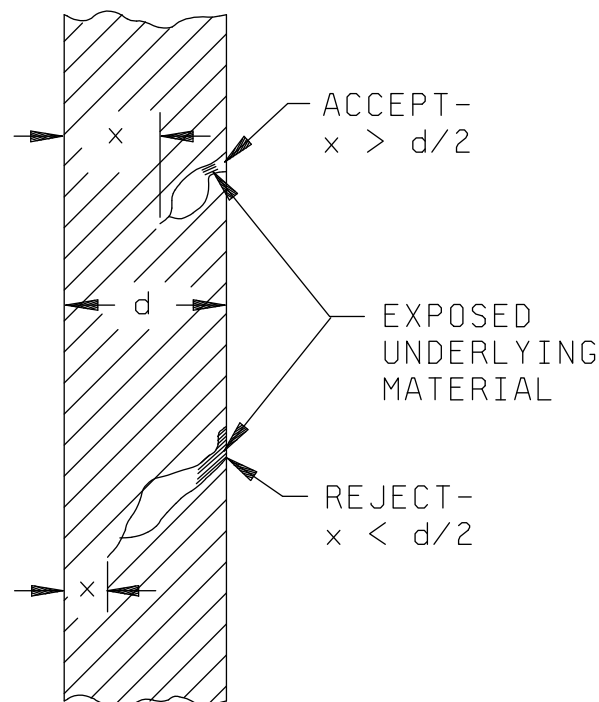


FIGURE 2032-38h. Class H metallization scratch criteria.

Class H

- 3.2.1.1 b. Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, to less than 50 percent its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-39h).

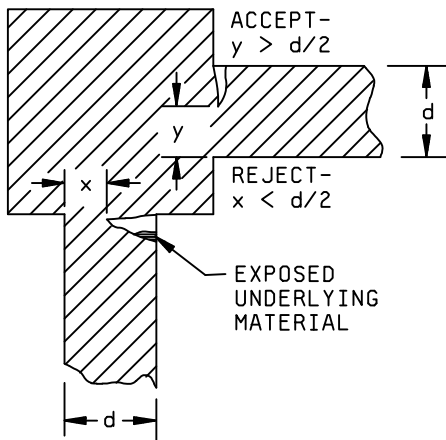


FIGURE 2032-39h. Class H metallization width reduction at bonding pad criteria.

- c. Scratch or probe marks in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area.

Class K

- 3.2.1.1 b. Less than 75 percent (see figure 2032-39k).

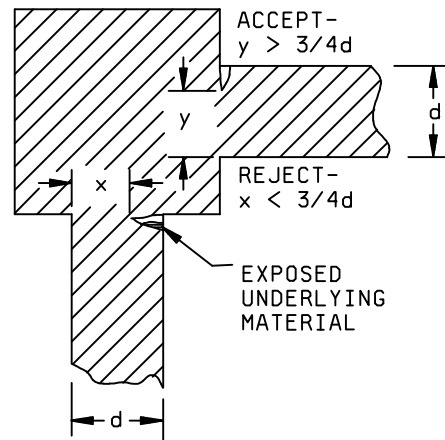


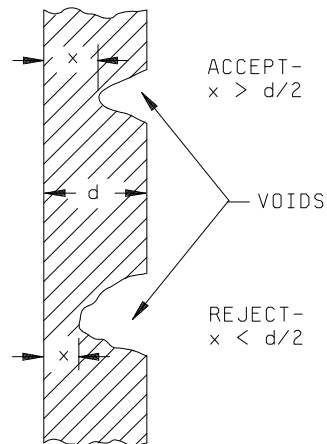
FIGURE 2032-39k. Class K metallization width reduction at bonding pad criteria.

- c. Same as class H

Class HClass K3.2.1.2 Metallization voids.

- a. Void(s) in the metallization, excluding bonding pads, that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-40h).

- a. Same as Class H.

FIGURE 2032-40h. Class H metallization void criteria.

- b. Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately.
NOTE: Figures 2032-39h and 2032-39k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.
- c. Void(s) in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area.
NOTE: For RF microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.

- b. Less than 75 percent.

- c. Same as class H.

Class HClass K3.2.1.3 Metallization corrosion.

- a. Any metallization corrosion.

- a. Same as class H.

3.2.1.4 Metallization adherence.

- a. Any metallization lifting, peeling, or blistering.
 NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister.
 NOTE: These criteria are not applicable to separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.

- a. Same as class H.

3.2.1.5 Metallization protrusion.

- a. More than 50 percent reduction of the original design separation, between any protruding metallization and adjacent metallization paths (see figure 2032-41h).

- a. Same as class H.

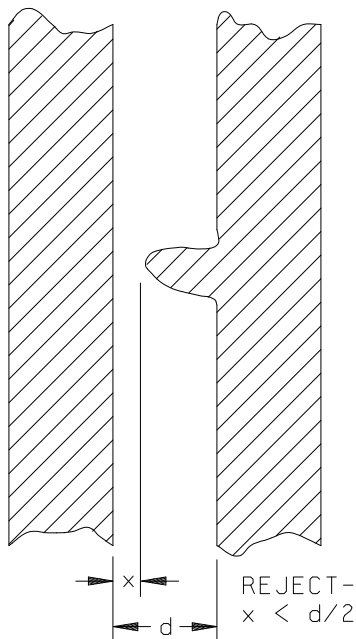


FIGURE 2032-41h. Class H metallization protrusion criterion.

Class HClass K3.2.1.6 Metallization overlap.

- a. Contact overlap between the upper and lower metallizations that is less than 50 percent of the designed contact overlap area (see figure 2032-42h).
 NOTE: The overlap area is that area in which the upper metallization actually contacts the lower metallization.

- a. Same as class H.

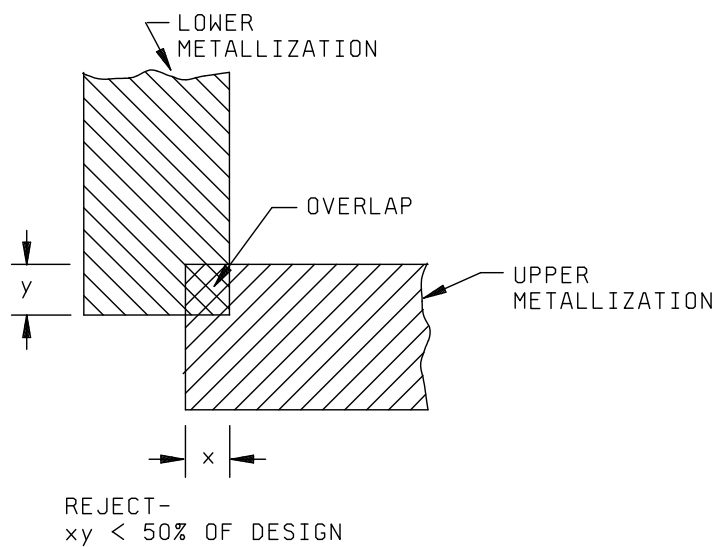


FIGURE 2032-42h. Class H metallization overlap criterion.

Class HClass K3.2.1.7 Metallized through-hole defects, "low magnification".

No element shall be acceptable that exhibits:

- a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.

- a. Same as class H.

3.2.1.8 Wrap-around connection defects, "low magnification".

No element shall be acceptable that exhibits:

- a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-43Ah).

- a. Same as class H.

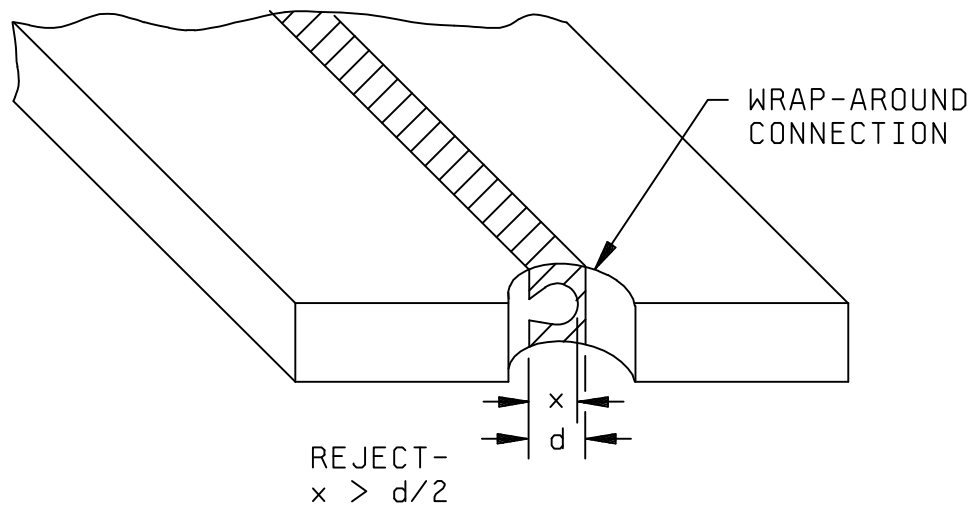


FIGURE 2032-43Ah. Class H wrap-around connection unmetallized area criterion.

3.2.1.9 Substrate plug via defects, "low magnification". When inspected from each side of the substrate, no element shall be acceptable that exhibits:

- A complete void through the via.
- Any lifting, peeling, or blistering of the via metallization.
- Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.

NOTE: These are minimum requirements. Via flatness and other requirements shall be in accordance with the applicable detail drawings.

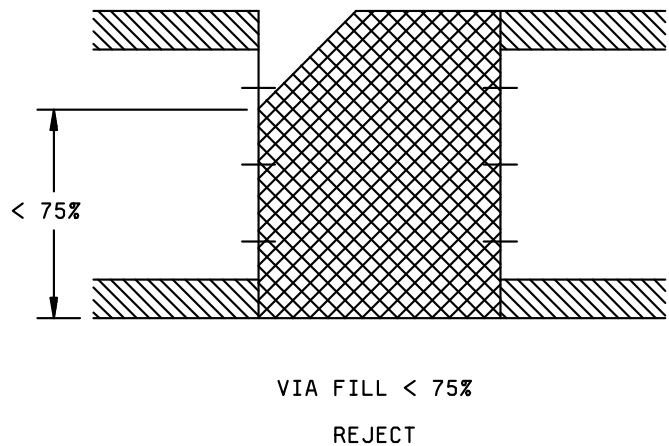
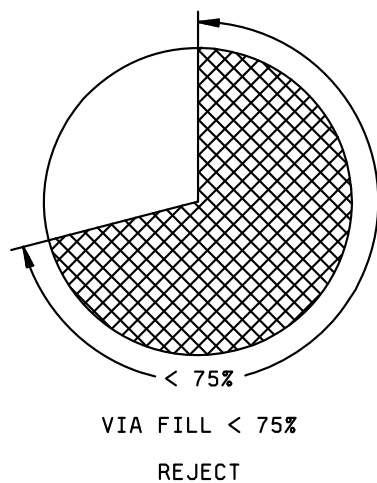


FIGURE 2032-43Bh. Classes H and K via fill criteria.

Class HClass K3.2.2 Substrate defects, "low magnification".

No element shall be acceptable that exhibits:

- | | |
|--|----------------------------|
| <p>a. Less than 1.0 mil separation between the operating metallization and the edge of the element unless by design (see figure 2032-43h).
NOTE: This criterion does not apply to substrates designed for wraparound conductors.</p> | <p>a. Same as class H.</p> |
| <p>b. A chipout that extends into the active circuit area (see figure 2032-43h).</p> | <p>b. Same as class H.</p> |

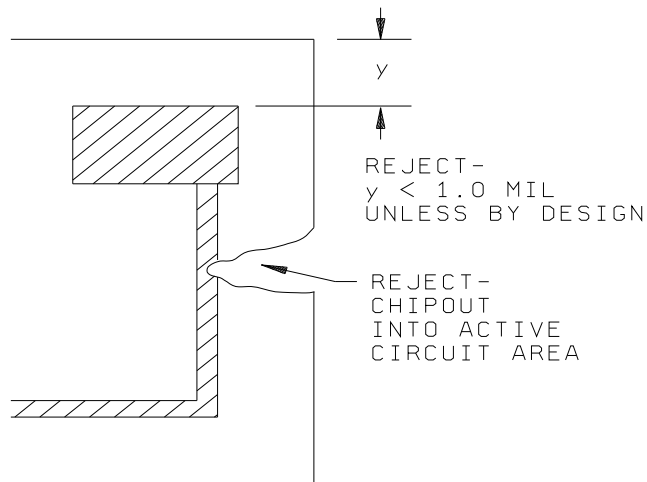


FIGURE 2032-43h. Class H separation and chipout criteria.

- | | |
|--|----------------------------|
| <p>c. Any crack that exceeds <u>5.0 mils in length</u> (see figure 2032-44h).

NOTE: For fused quartz or crystalline substrates, no cracking is allowed.</p> | <p>c. Same as Class H.</p> |
| <p>d. Any crack that does not exhibit 1.0 mil of separation from any active circuit area or operating metallization (see figure 2032-44h).</p> | <p>d. Same as class H.</p> |

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Class H

Class K

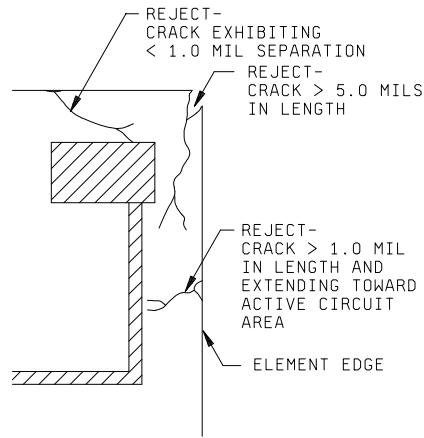


FIGURE 2032-44h. Class H additional crack criteria.

- 3.2.2 e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-44h).

f. N/A

- 3.2.2 e. Same as class H.

- f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-45k).

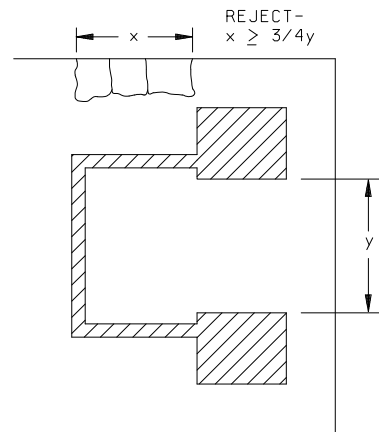


FIGURE 2032-45k. Class K semicircular crack criterion.

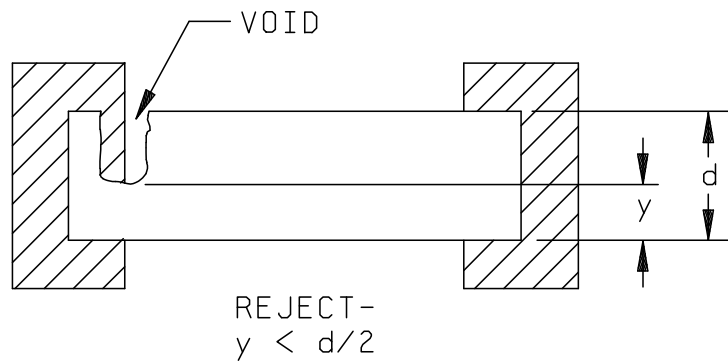
MIL-STD-883H

	<u>Class H</u>		<u>Class K</u>
3.2.2	g. An attached portion of a circuit area from an adjacent element.	3.2.2	g. Same as class H.
	h. Any crack that does not originate at an edge.		h. Same as class H.
	i. Holes through the substrate, unless by design.		i. Same as class H.
	j. Patterned substrates having a section broken out around a substrate mounting hole (intended for substrate-to-post attachment) that is greater than 25 percent of the mounting hole circumference.		j. Same as class H.

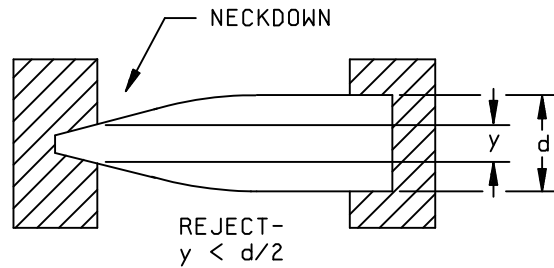
Class HClass K3.2.3 Thick film resistor defects, "low magnification".

No element shall be acceptable that exhibits:

- | | |
|---|---------------------|
| a. A reduction of the resistor at the terminal due to voids to less than 50 percent of the original resistor width (see figure 2032-46h). | a. Same as Class H. |
|---|---------------------|

FIGURE 2032-46h. Class H resistor width reduction at terminal caused by voids criterion.

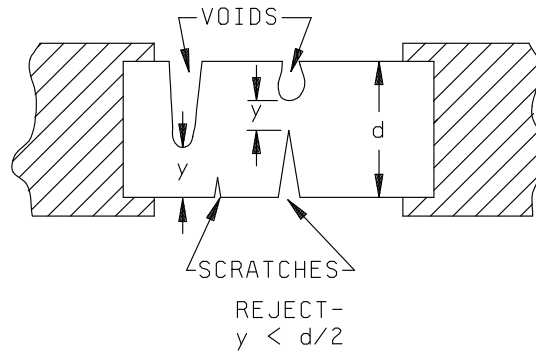
- | | |
|--|---------------------|
| b. Reduction of the resistor at the terminal, due to neckdown less than 50 percent, to of the original resistor width (see figure 2032-47h). | b. Same as Class H. |
|--|---------------------|

Class HClass KFIGURE 2032-47h. Class H resistor width reduction at terminal by neckdown criterion.

- | | | | | | |
|-------|----|--|-------|----|------------------|
| 3.2.3 | c. | Any resistor film lifting, peeling, or blistering. | 3.2.3 | c. | Same as class H. |
| | d. | Crack in the resistor greater than 1.0 mil in length.
NOTE: Irregularities such as fissures in resistor material that are created during firing, and that do not expose the underlying material, are not considered to be cracks. | | d. | Same as class H. |
| | e. | Evidence of resistor repair by overprinting or any other means. | | e. | Same as class H. |
| | f. | Separation between any two resistors that is less than 50 percent of the original separation. | | f. | Same as class H. |
| | g. | Separation between any resistor and conductor combination that is less than 50 percent of the original separation. | | g. | Same as class H. |
| | h. | Increase in resistor width greater than 25 percent of the original design width. | | h. | Same as class H. |
| | i. | Resistor that is closer than 1.0 mil to the edge of the substrate. | | i. | Same as class H. |

Class H

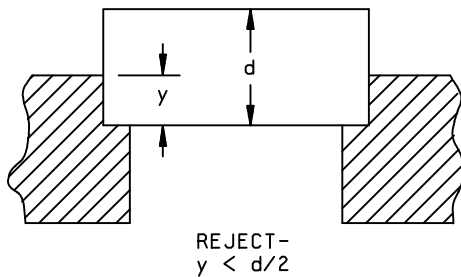
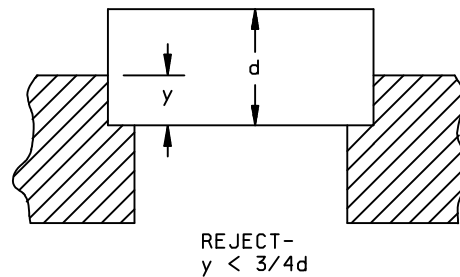
- 3.2.3 j. Reduction of resistor width resulting from voids, scratches, or chipouts, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-48h).
 PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.

FIGURE 2032-48h. Class H resistor width reduction criteria.Class K

- 3.2.3 j. Same as class H.

- k. Contact overlap between the metallization and the resistor in which the actual width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-49h).

- k. Less than 75 percent (see figure 2032-49k).

FIGURE 2032-49h. Class H resistor overlap criterion.FIGURE 2032-49k. Class K resistor overlap criterion.

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Class H

Class K

- | | | | | | |
|-------|----|---|-------|----|------------------|
| 3.2.3 | I. | Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 3.0 mils (see figure 2032-50h). | 3.2.3 | I. | Same as class H. |
|-------|----|---|-------|----|------------------|

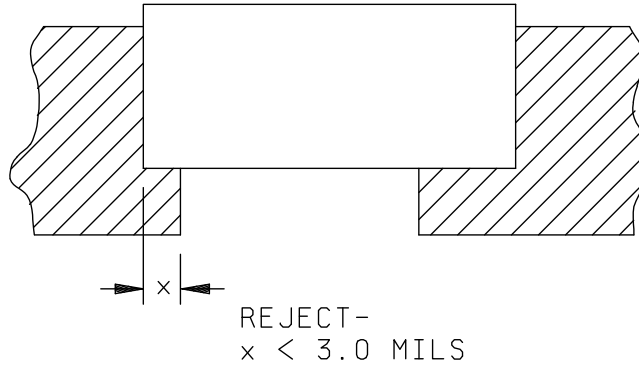


FIGURE 2032-50h. Resistor overlap criterion.

- | | | | |
|----|---|----|------------------|
| m. | Voids or misalignment of glassivation that results in less than 90 percent coverage of the resistor area, unless by design. | m. | Same as class H. |
| n. | Crazing of glassivation over a resistor. | n. | Same as class H. |
| o. | Glassivation scratches, lifting, or peeling that expose any portion of a resistor. | o. | Same as class H. |

Class HClass K

3.2.4 Trimmed thick film resistor defects, "low magnification". No element shall be acceptable that exhibits:

NOTE: The trim defect criteria contained in this section apply to active resistor areas only.

- a. A kerf width less than 0.5 mil (see figure 2032-51h).

- a. Same as class H.

NOTE: This does not apply to edge trimming.

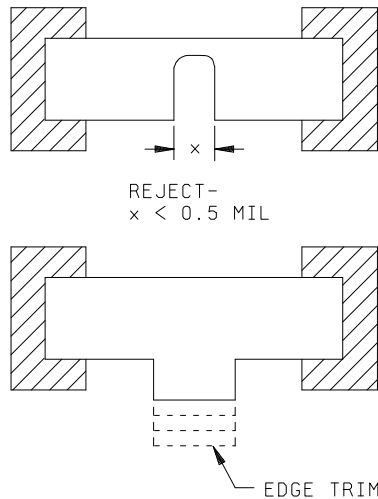


FIGURE 2032-51h. Class H kerf width criteria.

- b. A kerf containing detritus.

- b. Same as class H.

- c. A kerf which extends into metallization and leave less than 75 percent of the metallization width undisturbed (see figure 2032-52h).

- c. Same as class H.

NOTE: Opening a metallization link by design is acceptable.

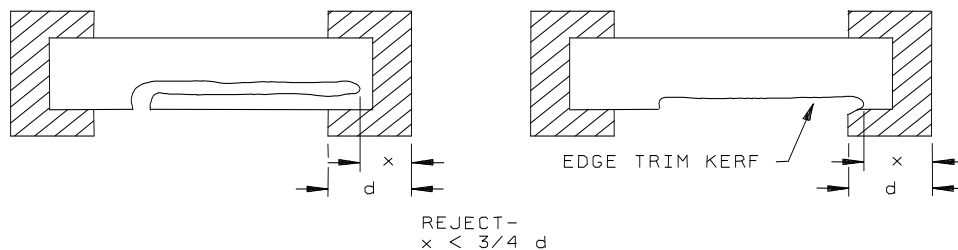


FIGURE 2032-52h. Class H laser trim kerf extension into metallization criteria.

Class H

- 3.2.4 d. A kerf that leaves less than 50 percent of the original width of a resistor, unless by design (see figure 2032-52Ah).
 PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.

Class K

- 3.2.4 d. Same as class H.

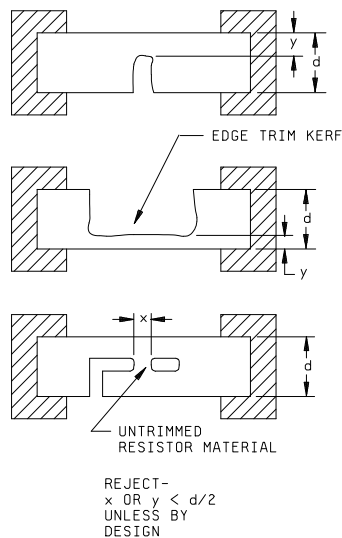


FIGURE 2032-52Ah. Class H resistor width reduction and untrimmed resistor material criteria.

- e. A trim that does not originate from the edge of the resistor. e. Same as class H.
- 3.2.5 Multilevel thick film defects, "low magnification". No element shall be acceptable that exhibits:
- a. Any insulating material that does not extend beyond the width of the upper and lower metallization by 3.0 mils minimum (see figure 2032-53h). a. Same as class H.

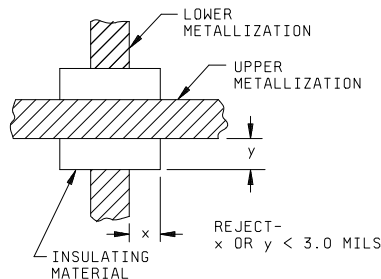


FIGURE 2032-53h. Class H dielectric extension criteria.

Class H

- 3.2.5 b. Voids in the insulating material that expose underlying metallization.
- c. Vias that are less than 50 percent of the original design area.
- d. Scratch that completely crosses the metallization and damages the insulating material surface on either side.

Class K

- 3.2.5 b. Same as class H.
- c. Same as class H.
- d. Same as class H.

3.2.6 All thick film capacitors and those overlay capacitors used in GaAs microwave devices,"low magnification". No element shall be acceptable that exhibits:

- a. Scratches that expose an underlying material.
- b. Any peeling or lifting of the metallization.
- c. Excess top metal which extend beyond the capacitor bottom metal.
- d. Voids in the capacitor bottom metal which extend under the capacitor top metal.
- e. Voids in the top metallization which leaves less than 75% of the metallization area undisturbed.

3.3 Nonplanar element inspection. Inspection for visual defects described in this section shall be conducted on each nonplanar passive element. The "low magnification" inspection shall be within the range of 10X to 60X.

Class HClass K

3.3.1 General nonplanar element defects,"low magnification". No element shall be acceptable that exhibits:

- a. Peeling or lifting of any metallization.
- b. Protrusion between metallization terminals that leaves less than 5.0 mils separation (see figure 2032-54h).
- a. Same as class H.
- b. Same as class H.

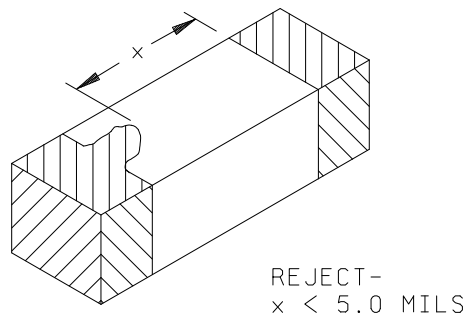


FIGURE 2032-54h. Class H metallization protrusion criterion.

<u>Class H</u>		<u>Class K</u>	
3.3.1	<ul style="list-style-type: none"> c. Lifting, blistering, or peeling of insulation. d. Voids in metallized terminals that expose underlying material over greater than 25 percent of any side of the metallized terminal area. 	3.3.1	<ul style="list-style-type: none"> c. Same as class H. d. Same as class H.
3.3.2	<p><u>Foreign material defects "low magnification".</u> No element shall be acceptable that exhibits:</p> <ul style="list-style-type: none"> a. For mounted elements, unattached, conductive foreign material on the surface of the element. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization path, active circuitry, or any combination of these. NOTE: If an element has an insulating layer (such as glassivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of unattached conductive foreign material that is large enough to bridge these features is acceptable since the features are protected by the insulating layer. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.) by a suitable cleaning process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material. NOTE: Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above. b. Attached, conductive foreign material that bridges metallization paths, active circuitry, or any combination of these. c. Liquid droplets, inkdrops, or any chemical stain that appear to bridge any unglassivated active circuit areas. d. Attached foreign material that covers more than 25 percent of a bonding pad area. 		
			<ul style="list-style-type: none"> a. Same as class H. b. Same as class H. c. Same as class H. d. Same as class H.

Class HClass K

3.3.3 Ceramic chip capacitor defects "low magnification". No element shall be acceptable that exhibits:

- a. Crack, chip or void in the body that exposes metal plates, (see figure 2032-55h).

- a. Same as class H.

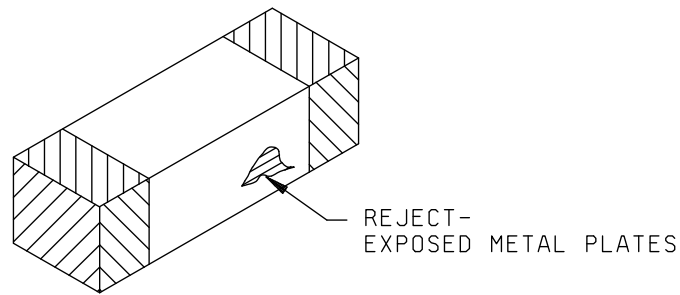


FIGURE 2032-55h. Class H metal plate exposure criteria.

- b. Crack that is greater than 50 percent of the width of the unmetallized sides, top, or bottom, or that extends around a corner (see figure 2032-56h).

- b. Crack.
NOTE: No cracks are allowed.

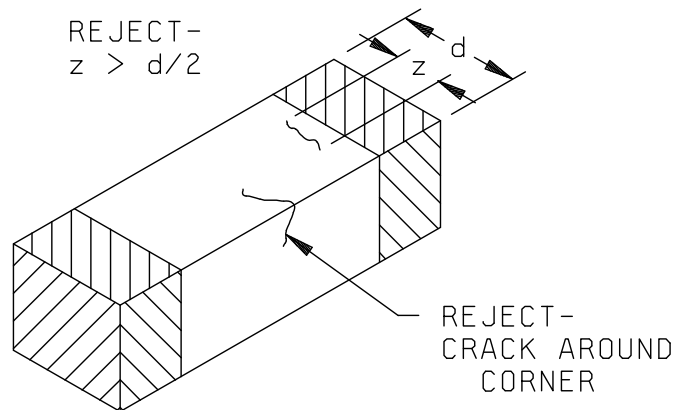


FIGURE 2032-56h. Class H crack criteria.

Class H

- 3.3.3 c. Evidence of separation (delamination) of metal plates or cracks along the plane of the metal plates (see figure 2032-57h).
NOTE: Narrow grooves or channel less than 1.0 mil wide that exhibit a glass-like appearance and do not expose metal plates are acceptable.

Class K

- 3.2.3 c. Delamination.

NOTE: No delamination is allowed.

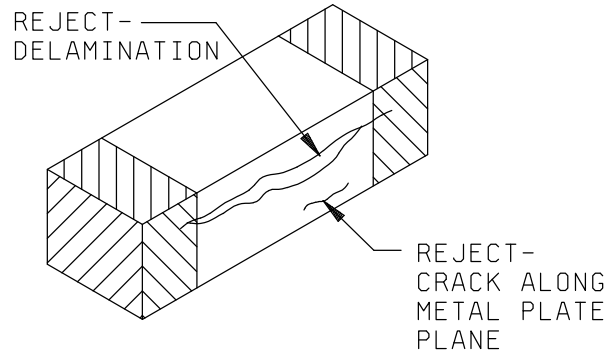


FIGURE 2032-57h. Class H delamination criteria.

- d. Crack or void in the metallization that exposes metal plates, or voids that are greater than 25 percent of the area of the metallized terminal (see figure 2032-58h).

- d. Same as class H.

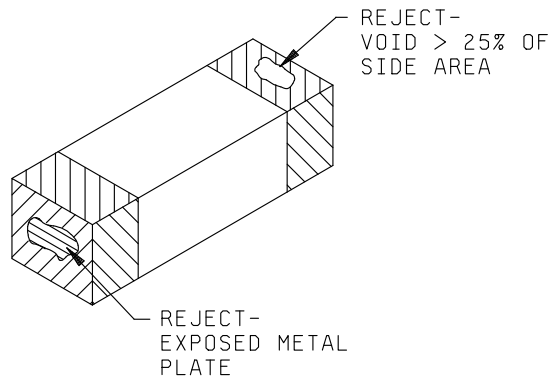


FIGURE 2032-58h. Class H termination defect criteria.

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- | | <u>Class H</u> | | <u>Class K</u> |
|-------|---|-------|---------------------|
| 3.3.3 | <p>e. Void in the metallized edges of the element that are greater than 10 percent of the metallized edge dimension, or bare corners of metallized terminals (see figure 2032-59h).
NOTE: This criteria ia applicable to solder attached elements only.</p> | 3.3.3 | e. Same as class H. |

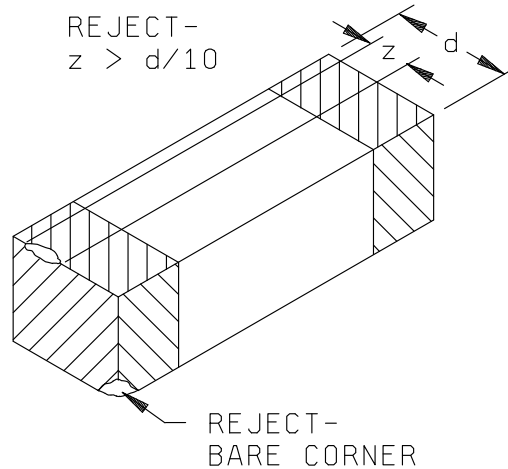
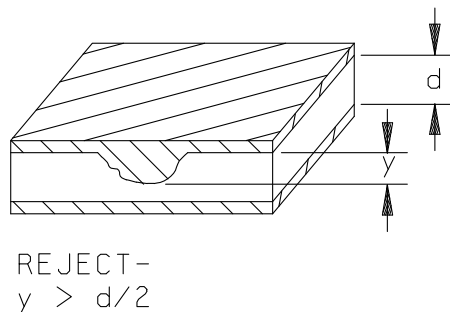


FIGURE 2032-59h. Class H metallized edge defect criteria.

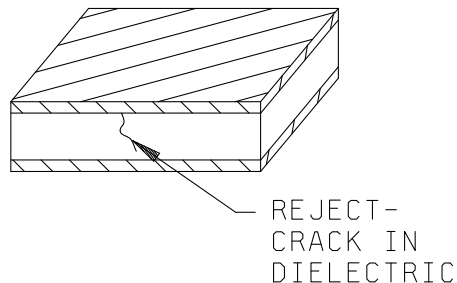
- | | |
|--|---------------------|
| f. Attached foreign material on the body that covers an area greater than 5.0 mils square on any side. | f. Same as class H. |
|--|---------------------|
- 3.3.4 Tantalum chip capacitor defects, "low magnification." No element shall be acceptable that exhibits:
- | | |
|---|---------------------|
| a. Flaking or peeling of the encapsulant that exposes any underlying material. | a. Same as class H. |
| b. A metallized terminal that is less than 90 percent free of encapsulant material. | b. Same as class H. |
| c. Less than 50 percent continuous metallized terminal weld area without cracks. For capacitors with riser wires, a riser wire connection with less than 25 percent continuous weld area. | c. Same as class H. |
| d. Metallized terminal containing residue from the welding operation that is not firmly attached metallurgically to the anode cap. | d. Same as class H. |

- | | <u>Class H</u> | | <u>Class K</u> |
|-------|--|-------|---------------------|
| 3.3.4 | e. Metallized terminal not aligned as shown in the applicable drawing. | 3.3.4 | e. Same as class H. |
| | f. Encapsulant preventing the metallized terminal from resting on the substrate bonding pads when the capacitor is in the bonding position except where the metallized terminal electrical contact is made by alternate means. | | f. Same as class H. |
| | g. Lifting, blistering or peeling of metallized terminal encapsulant. | | g. Same as class H. |
- 3.3.5 Parallel plate chip capacitor defects.
"low magnification". No element shall be acceptable that exhibits:

- | | | | |
|----|--|----|------------------|
| a. | Metallization that extends greater than 50 percent around the edge of the capacitor (see figure 2032-60h). | a. | Same as class H. |
|----|--|----|------------------|

FIGURE 2032-60h. Class H metallization extension criterion.

- | | | | |
|-------|---|-------|---------------------|
| 3.3.5 | b. Evidence of cracks in the dielectric body (see figure 2032-61h). | 3.3.5 | b. Same as class H. |
|-------|---|-------|---------------------|

FIGURE 2032-61h. Class H crack in dielectric criterion.

Class HClass K

3.3.6 Inductor and transformer defects, "low magnification". No element shall be acceptable that exhibits:

- | | |
|---|---------------------|
| a. Peeling, lifting or blistering of winding metallization or insulation. | a. Same as class H. |
| b. Evidence of shorts between adjacent turns or windings. | b. Same as class H. |
| c. Cracks or exposure of bare magnetic core material. Exposed bare magnetic core material is acceptable if by design. | c. Same as class H. |
| d. Pits or voids in the core insulation greater than 5.0 mils area that expose the magnetic core material. | d. Same as class H. |
| e. Separation less than 5.0 mils between wire termination points of the same or adjacent windings. | e. Same as class H. |
| f. Missing polarity identification unless by design. | f. Same as class H. |
| g. Operating metallization and multilevel thick film defects as described in 3.2.1 and 3.2.5 herein. | g. Same as class H. |

3.3.7 Chip resistor defects, "low magnification". No element shall be acceptable that exhibits:

- | | |
|---|---------------------|
| a. Reduction of the resistor width resulting from voids, bubbles, nicks, or scratches, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-62h). | a. Same as class H. |
|---|---------------------|

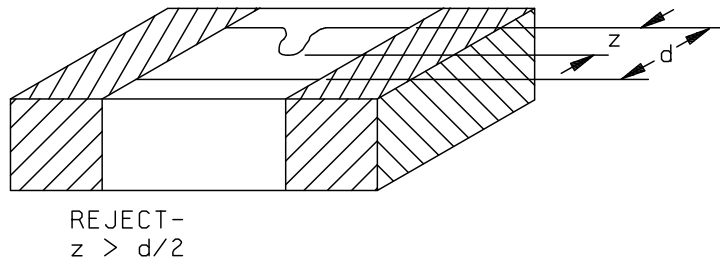


FIGURE 2032-62h. Class H resistor width reduction criterion.

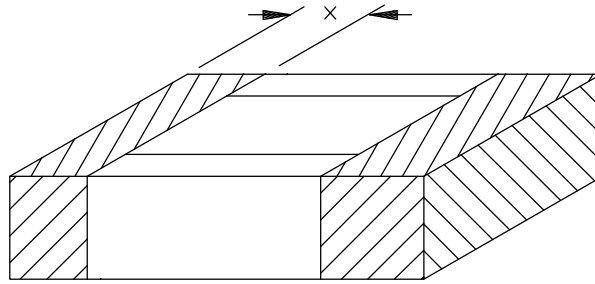
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Class H

- 3.3.7 b. A kerf that leaves less than 50 percent of the original width of the resistor unless by design.
- c. Metallized termination width less than 10.0 mils unless by design (see figure 2032-63h).

Class K

- 3.3.7 b. Same as class H.
- c. Same as class H.

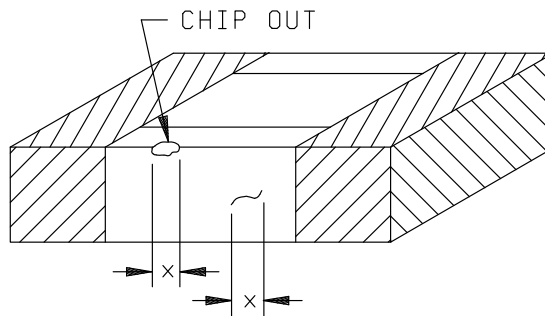


REJECT -
 $x < 10.0$ MILS
 UNLESS BY DESIGN

FIGURE 2032-63h. Class H termination width criterion.

- d. A crack, chipout or void in the substrate greater than 3.0 mils in any direction (see figure 2032-64h).

- d. Same as class H.



REJECT -
 $x > 3.0$ MILS

FIGURE 2032-64h. Class H substrate defect criteria.

Class H

- 3.3.7 e. Build-up of termination material on metallized termination areas greater than 3.0 mils high for weldable metallized terminations or 8.0 mils high for solderable metallized terminations (see figure 2032-65h).

Class K

- 3.3.7 e. Same as class H.



REJECT -
 $y > 3.0 \text{ MILS}$
 OR 8.0 MILS

FIGURE 2032-65h. Class H termination material buildup criteria.

Class H

- f. Termination material splattered throughout the resistor (see figure 2032-66h).

Class K

- f. Same as class H.

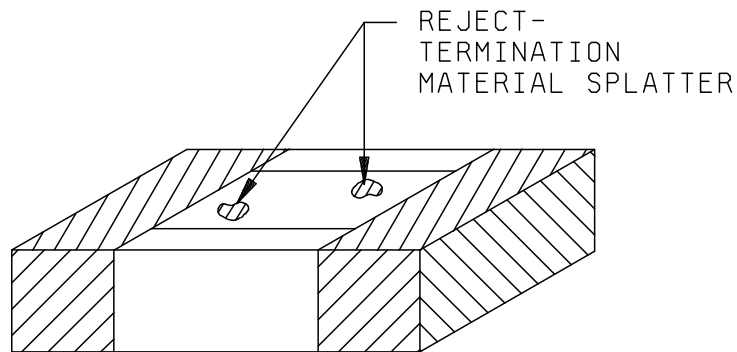


FIGURE 2032-66h. Class H termination material splatter criteria.

3.4 Surface acoustic wave (SAW) element inspection. Inspection for visual defects described in this section shall be conducted on each SAW element. When inspection is performed prior to mounting, then SAW elements may be inspected using backlighting. All inspection shall be performed at "low magnification" within the range of 10X to 60X for both class H and class K.

3.4.1 Defect control. The manufacturer shall perform an audit on a weekly basis for the presence of process related defects which impact SAW device performance (e.g., metallization voids, metallization scratches, metallization bridging, or crystal material pits/scratches/chipouts). This audit may be satisfied during routine internal visual inspection. If the presence of process related defects are discovered, the manufacturer shall monitor for a defect pattern to be used for the improvement of process controls. The manufacturer shall document the results of his investigation and corrective action to eliminate trends. The intent of this procedure is to require monitoring of process related defects which affect SAW device performance but do not cause reliability degradation leading to eventual failure of device function.

Class H

Class K

3.4.2 Operating metallization defects "low magnification." No element shall be acceptable that exhibits:

3.4.2.1 Metallization corrosion.

a. Any metallization corrosion.

a. Same as class H.

3.4.2.2 Metallization adherence.

a. Any metallization lifting, peeling or blistering.

a. Same as class H.

3.4.3 Substrate material defects "low magnification."
No element shall be acceptable that exhibits:

a. Any crack that exceeds 5.0 mils in length.

a. Same as class H.

b. Any crack that is within 0.1 mil of any active circuit area or operating metallization.

b. Same as class H.

c. Any crack exceeding 1.0 mil in length extending from the element edge directly toward the active circuit area or operating metallization.

c. Same as class H.

Class HClass K3.4.4 Foreign material defects "low magnification".

No element shall be acceptable that exhibits:

- | | |
|--|----------------------------|
| <p>a. For mounted and unmounted elements, unattached conductive foreign material on the surface of the element that is large enough to bridge operating metallization paths.</p> | <p>a. Same as class H.</p> |
| <p>NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with a mechanical device (i.e., needle, probe, pick, etc.) or by a suitable cleaning process approved by the acquiring activity, or by a nominal gas blow (approximately 20 psig). Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.</p> | |
| <p>b. Liquid droplets, ink drops, or chemical stains that appear to bridge unglassivated metallization.</p> | <p>b. Same as class H.</p> |
| <p>c. Attached foreign material that covers greater than 25 percent of a bonding pad area.</p> | <p>c. Same as class H.</p> |

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

- a. Class H or class K visual requirements.
- b. Where applicable, any conflicts with element design, topology or construction (see 3).
- c. Where applicable, gauges, drawings and photographs that are to be used as standards for operator comparison (see 2).
- d. Where applicable, magnifications other than those specified (see 3).

ULTRASONIC INSPECTION OF TAB BONDS

1. Purpose. The purpose of this method is to detect unbonded and insufficiently bonded sites in TAB (Tape automated bonding) devices in the open package condition, through the measurement of bond area by means of Scanning Laser Acoustic Microscope (SLAM) techniques. It establishes methods and criteria for ultrasonic inspection of these TAB semiconductor devices.

NOTES:

1. For various metallurgical constitutions, absolute strengths expressed as pull strengths per unit area of bond differ. A scalar equivalency must be established for each alloy and process, to relate bond area to anticipated bond strength.
 2. The term TAB bond in this document refers to one of the multiplicity of bonds, inner lead (ILB) or outer lead (OLB) formed by a tape automated bonding (TAB) process. In the case of ILB, it refers to that area of the device defined by the intersection of the beam lead, the semiconductor bonding pad area, and the contact outline of the thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the semiconductor die surface and the beam lead. In the case of OLB, it refers to that area of the device defined by the intersection of the beam lead, the substrate bonding pad area, and contact outline of thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the substrate surface and the beam lead.
 3. The terms ultrasonic inspection and SLAM as used in this document refer to the process and instrument performing high frequency ultrasonic inspection and produce grey-scale images of the internal features of devices by means of scanning laser acoustic microscopy, and by which bond area measurement may be performed.
2. Apparatus. The apparatus and materials for this evaluation shall include:
- a. Ultrasonic imaging equipment of the scanning laser acoustic microscope type, of frequency and resolution sufficient to penetrate the bond area and render an image which discloses the size and shape of the bond area with a linear dimensional allowance no greater than 20 percent of a bond dimension. Frequency is dictated by consideration of the wavelength of sound in the materials and the limit of resolution. Whereas lower frequencies have been used for inspection of larger scale device types, the present size of TAB sites requires frequencies of from one hundred to several hundred megahertz.
 - b. A visual output/storage device. A method of producing, displaying, and storing a scale image of adequate grey-scale range (minimum of 64 levels) shall be used. Such device may include a grey-scale printer/plotter, or preferably CRT display with an image digitizer capable of rendering images in digital code for bulk media storage and retrieval, and algorithmic processing and evaluation. The images so stored shall be suitable for manual, or preferably, automated analysis. The output devices shall be capable of producing and storing the images to a spatial and grey-scale resolution at least equal to the resolution of their acquisition by the ultrasonic imaging equipment. The output/storage device must be capable of presenting, storing, and retrieving image label information.
3. Procedure. The equipment used shall be adjusted as necessary to obtain satisfactory images of good contrast to achieve maximum image detail within the sensitivity requirements of the bond type being examined. The appropriate operator methodology will be used to insure adequate positioning and insonification (irradiation by ultrasound) of the device for purposes of producing its image. Additional protocols will be followed as required. The normal intrinsic strength of the bond metallurgy shall be known and established, and the metallurgy of the devices to be tested should be qualified as in agreement with that strength.

3.1 Calibration of the instrument. When specified, at least one device of the type and construction to be tested shall be available to set up the ultrasonic inspection equipment and peripherals. The device may be a scape non-operational device with TAB bonded leads which will be used to identify device landmarks and ensure the equipment is properly functional.

3.2 Labeling and identifying. The devices tested and the image records made of them shall be labeled in a standard format to include the following information:

- a. Device manufacturer's name or code identification number.
- b. Device type or part number.
- c. Production lot number and/or inspection date code lot number.
- d. Ultrasonic image view number and date; to include description or code for the region or bond number (s) viewed.
- e. Device serial/cross reference number if applicable.
- f. Ultrasonic operator identification.

3.3 Serialized devices. When device serialization is required, each device shall be readily identifiable by a serial number, and this serial number must be included in a form readable in the stored image. In the event of a skipped piece in the serialization, a blank space representing the skipped piece, and labeled with its serial number should appear in the storage medium. In the event of a large contiguous range of skipped pieces, a similar blank space advising of the range of pieces skipped should appear in the storage medium in place of the large physical space of the many skips.

3.4 Data back-up. When required, data back-up shall be specified from a choice of multiple floppy disk, multiple track data tape, or a video format tape, or other options having sufficient volume, resolution, speed, and reliability to suit the requirements for storage and labeling.

3.5 Mounting. The devices shall be mounted for ultrasonic inspection in a fixture which insures correct positioning in all dimensions, and adequately safeguards the potentially fragile bonds from mechanical contact with any substance other than the coupling fluid. Positioning thereafter must continue in a fashion which continues the above condition, and furthermore exposes each inspected bond area to the correct acoustic environment and portion of the instrumental field.

3.6 Angle of insonification. The angle of insonification must be specified by prior analysis, and if the mounting fixture is goniometrically agile it must be set to the correct angle by adjustment or selection.

3.7 Conditions of operation. Adjustments, selections, options, and settings used in the performance of the ultrasonic inspection must be recorded if they are of a nature critical to the proper operation of equipment; not to be recorded are those casual adjustments which are done as an obvious matter of course, and the performance of which are guided by such rules as trimming for maximum, minimum, or optimum, and which are not controlled by calibrated interfaces.

3.8 Operating personnel. Operating personnel shall have a basic familiarity of the nature of sound and the use of ultrasonic instruments in the inspection of devices. They shall be specifically trained and certified in the operation of the ultrasound and peripheral equipment used so that defects revealed by the method can be validly interpreted and compared with applicable standards.

3.9 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results from the ultrasonic inspection, and list the purchase order number, or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of the test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

3.10 Acoustic micrograph and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report, for the period specified.

3.11 Examination and acceptance criteria. Once the manufacturer has established the total bond area to be sought, based upon studies of the device to be bonded, and the inclusion of a prudent excess margin, then the following shall be considered the minimum bond area percentage:

- a. In the case of solder bonds of lead-tin alloys a bond area percentage of 75 percent of the total bond area shall be considered minimum.
- b. In the case of gold-tin eutectic and gold-gold thermocompression, a bond area percentage of 50 percent of the total bond area shall be considered minimum, except in the case of lead misalignment; when lead misalignment is a contributing factor a bond area percentage of 75 percent shall be considered minimum.

In the examination of devices, the following aspects shall be considered unacceptable bonding, and devices which exhibit any of the following defects shall be rejected:

- a. A bond having a total bond area less than the minimum bond area. The failure may be caused by any reason, including lateral or longitudinal misalignment.
- b. A bond meeting the minimum bond area, but with this area being discontinuous so that no single bonded area meets or exceeds the minimum bond area.

4. Summary. The following details shall be specified in the applicable acquisition document:

- a. Number of views to be taken by SLAM inspection of each piece or bonding site, in accordance with 3.10, if other than one view.
- b. Markings of devices, or labeling of images, if other than in accordance with 3.2, or special markings of devices to indicate that they have been ultrasonically imaged, if required.
- c. Defects to be sought in the devices, and criteria for acceptance or rejection, if other than in 3.11.
- d. Image and report retention when applicable (see 3.10).

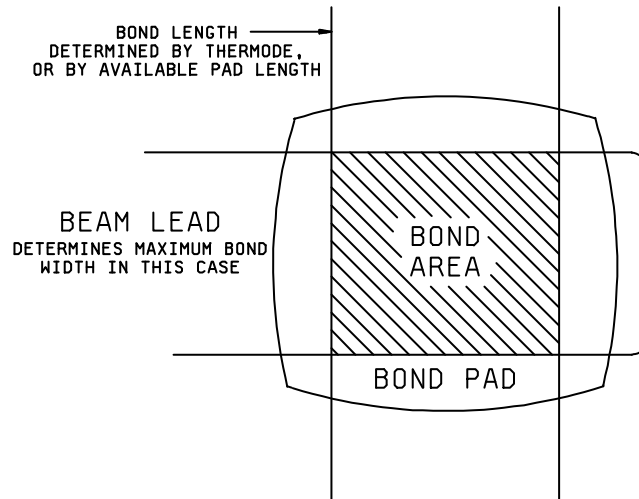


FIGURE 2035-1. Bond area.

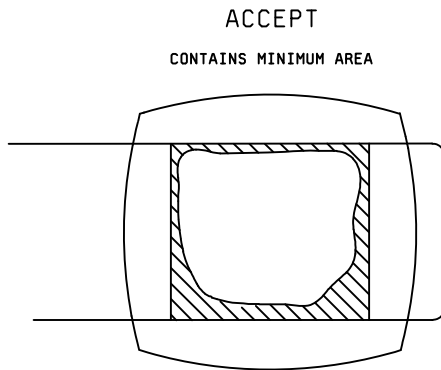


FIGURE 2035-2. Acceptable bond area.

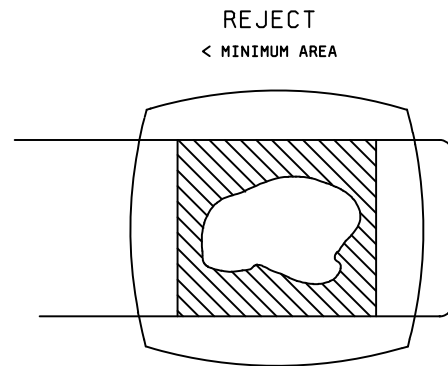


FIGURE 2035-3. Rejectable bond area.

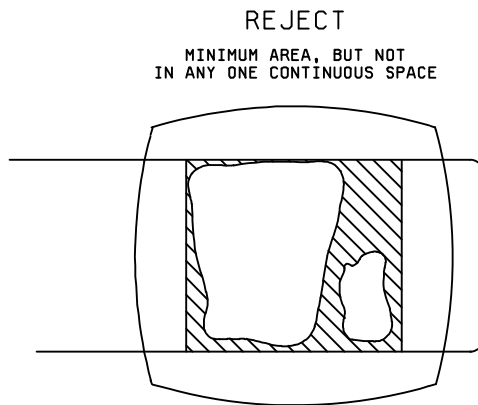


FIGURE 2035-4. Rejectable discontinuous bond area.

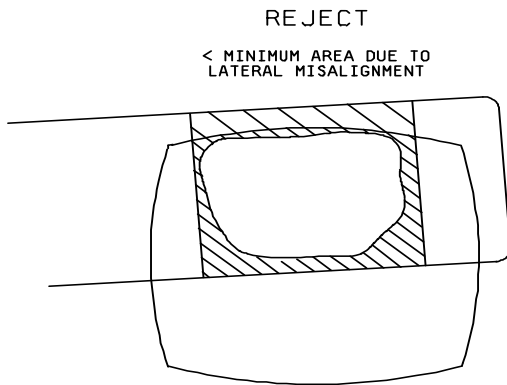


FIGURE 2035-5. Lateral misaligned bond area.

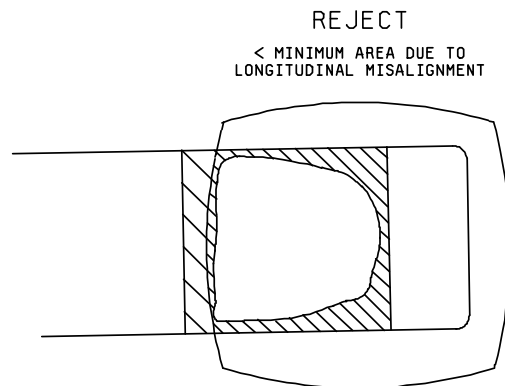


FIGURE 2035-6. Longitudinal misaligned bond area.

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RESISTANCE TO SOLDERING HEAT

1 PURPOSE. This test method is performed to determine whether termination leads and other component parts can withstand the effects of the heat to which they will be subjected during the soldering process (solder iron, solder dip, solder wave, or solder reflow). The heat can be either conducted heat through the termination into the component part, or radiant heat from the solder bath when in close proximity to the body of the component part, or both. The solder dip method is used as a reasonably close simulation of the conditions encountered in wave soldering, in regard to radiated and conducted heat. This test also is intended to evaluate the impact of reflow techniques to which components may be exposed. The heat of soldering can cause solder reflow which may affect the electrical characteristics of the component part and may cause mechanical damage to the materials making up the part, such as loosening of terminations or windings, softening of insulation, opening of solder seals, and weakening of mechanical joints.

2. APPARATUS.

2.1 Solder pot. A static solder pot, of sufficient size to accommodate the mounting board and the immersion of its terminations to the depth specified for the solder dip (without touching the bottom of the pot), shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified. The solder bath temperature shall be measured in the center of the pot at a depth of at least 0.500 inch (12.7 mm), but no deeper than 1 inch (25.4 mm) below the surface of the solder.

2.2 Heat sinks or shielding. The use of heat sinks or shielding is prohibited except when it is a part of the component. When applicable, heat sinks or shielding shall be specified in the individual specification, including all of the details, such as materials, dimensions, method of attachment, and location of the necessary protection.

2.3 Fixtures. Fixtures, when required, shall be made of a non-solderable material designed so that they will make minimum contact (i.e., minimum heat sink) with the component. Further, they shall not place undue stress on the component when fixtured.

2.4 Mounting board. A mounting board, in accordance with NEMA grade FR-4 of IPC-4101 (e.g. glass epoxy material, IPC-4101/21, IPC-4101/26, IPC-4101/82, IPC-4101/83, IPC-4101/92, IPC-4101/93, IPC-4101/95, IPC-4101/97 and IPC-4101/98), 9 square inches (e.g. 3 x 3, 1 x 9, etc.), minimum area, 0.062 inch \pm 0.0075 inch (1.57 mm \pm 0.191 mm) thick, shall be used, unless otherwise specified. Component lead holes shall be drilled such that the diametrical clearance between the hole and component terminals shall not exceed 0.015 inch (0.38 mm). Metal eyelets or feed-throughs shall not be used. Surface mount boards, when specified in the individual specification, shall have pads of sufficient size and number to accommodate the component being tested.

2.5 Solder iron. A solder iron, capable of maintaining a temperature of 350 °C \pm 10 °C, under thermal load, shall be used.

2.6 Reflow chambers. The reflow chambers or equivalent (Vapor Phase Reflow (VPR) chamber, Infrared Reflow (IRR) oven, air circulating oven, etc.) shall be of sufficient size to accommodate the mounting board and components to be tested. The chamber shall be capable of generating the specified heating rate, temperatures and environments.

2.7 Temperature measurement. Low mass thermocouples that do not affect the heating rate of the sample shall be used. A temperature recording device is recommended. The equipment shall be capable of maintaining an accuracy of \pm 1 °C at the temperature range of interest.

3. MATERIALS.

3.1 Solder. The solder or solder paste shall be tin-lead alloy with a nominal tin content of 50 percent to 70 percent in accordance with ANSI/J-STD-006, "Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications" or ANSI/J-STD-005, "Requirements for Soldering Pastes". When specified in the individual specification, other solders can be used provided they are molten at the specified temperature.

3.2 Flux. When flux is used, it shall conform to type A of ANSI/J-STD-004, "Requirements for Soldering Fluxes", or as specified in the individual specification.

3.3 VPR fluid. A perfluorocarbon fluid that has a boiling point of 215 °C shall be used.

4. **PROCEDURE.** The procedures described below in paragraph 4.4.1 through 4.4.6 are the default tests procedures. At the manufacturer's option, other test setups/procedures may be used provided it can be shown that they provide an equivalent stress. In the absence of equivalent procedures, the specified procedures shall be followed.

4.1 Special preparation of specimens. Any special preparation of specimens prior to testing shall be as specified in the individual specification. This could include specific instructions such as bending or any other relocation of terminations, cleaning, application of flux, pre-tinning, or attachment of heat sinks or protective shielding, prior to test.

4.2 Preparation of solder bath. The molten solder shall be agitated to assure that the temperature is uniform. The surface of the solder shall be kept clean and bright.

4.3 Application of flux. When flux is used, the terminations to be tested shall be immersed in the flux, which is at room ambient temperature, to the depth specified for the solder dip. The duration of the immersion shall be from 5 seconds (s) to 10 seconds.

4.4 Test conditions. Unless otherwise specified in the individual specification, the test shall be performed on all solder terminations attached to the component part (see FIGURE 2036-1 for examples). There are six types of soldering techniques covered by these test conditions. The test conditions are outlined below and in TABLE 2036-I.

Test condition A: Solder iron - Hand soldering of solder cups, through hole components, tab and post terminations, and solder eyelet terminations.

Test condition B: Solder dip - Simulates hot solder dipping (tinning) of leaded components.

Test condition C: Wave solder - Simulates wave solder of topside board mount product.

Test condition D: Wave solder - Simulates wave solder of bottom-side board mount product.

Test condition H: VPR – VPR environment without preheat.

Test conditions I, J, K: Infrared/Convection reflow - Simulates IRR, natural convection, and forced air convection reflow environments (see TABLE 2036-1 for temperature requirements).

4.4.1 Test condition A: Solder iron.

- a. When testing a solder cup, tab and post termination, or solder eyelet termination, the applicable wire size, properly prepared for the solder termination, shall be attached in the appropriate manner.
- b. When testing a board mount component, the component shall be placed on a mounting board (See 2.4).
- c. When specified, the components shall be fluxed (See 4.3).
- d. Unless otherwise specified, a solder iron in accordance with 2.5 shall be used.
- e. The solder iron shall be heated to $350\text{ }^{\circ}\text{C} \pm 10\text{ }^{\circ}\text{C}$ and applied to the termination for a duration of 4 seconds to 5 seconds as specified in TABLE 2036-I. The solder and iron shall be applied to the area of the assembly closest to the component body that the product is likely to experience. For surface mount components, the iron shall be placed on the pad only.
- f. Remove the iron and allow the component to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.2 Test condition B: Solder dip.

- a. Place the component in an appropriate fixture (See 2.3).
- b. When specified, the leads shall be fluxed (See 4.3).
- c. Unless otherwise specified, terminations shall be immersed to within 0.050 inch (1.27 mm) of the component body in accordance with TABLE 2036-1. Terminations shall be immersed simultaneously, if the geometry of the component permits.
- d. After the solder dip, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.3 Test condition C: Wave solder - topside board mount component.

- a. The component under test shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board (see FIGURE 2036-1 for mounting examples).
- b. When specified, the leads shall be fluxed (See 4.3).
- c. The components, mounted on the board, shall be preheated and immersed in the solder pot so that the bottom of the board floats on the molten solder in accordance with TABLE 2036-1.
- d. After the float, the components shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the components shall be cleaned using an appropriate cleaning solution.

4.4.4 Test condition D: Wave solder – bottom side board mount product.

- a. Place the component in an appropriate fixture (See 2.3).
- b. When specified, the terminations shall be fluxed (See 4.3).
- c. The component shall be preheated and fully immersed in the solder bath in accordance with TABLE 2036-I.
- d. After the immersion, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.5 Test condition H: Vapor phase reflow soldering.

- a. Components shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.
- b. A test chamber shall be used which is large enough to suspend the mounting board or fixture without touching the sides or solution (See 2.6). The VPR fluid shall be placed in the test chamber and shall be heated until it is boiling. The solution shall be allowed to boil for 5 minutes prior to suspending the mounting board or fixture.
- c. The specific combination of temperature, duration of exposure, and number of heats shall be as specified in TABLE 2036-I.
- d. After chamber equalization, the mounting board or fixture shall be suspended into the vapor in a horizontal plane. The mounting board or fixture shall not touch the solution.
- e. After the heat, the component shall be allowed to cool and stabilize at room ambient conditions. If a solder paste was used, the component shall be cleaned using an appropriate solution.

4.4.6 Test conditions I, J, K: Infrared / convection reflow soldering.

- a. Components shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.
- b. A test chamber as specified in 2.6 shall be used.
- c. A low mass thermocouple shall be attached tightly to the component at an appropriate position away from the edges.
- d. The mounting board or fixture shall be placed into the test chamber and the temperature of the component ramped at a rate of 1 °C/s to 4 °C/s, as measured by the thermocouple. The mounting board or fixture shall be above 183 °C for 90 seconds to 120 seconds and held at the final temperature and time designated by the test condition. The mounting board or fixture shall then be allowed to cool to room ambient temperature. This constitutes one heat cycle in accordance with TABLE 2036-1.

5 EXAMINATIONS AND MEASUREMENTS. Examinations and measurements are to be made before and after the test, as specified in the individual specification.

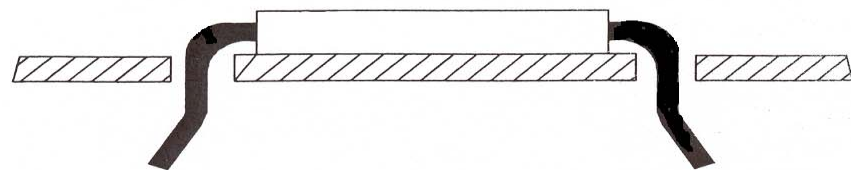
6. SUMMARY. The following details are to be specified in the individual specification:

- a. The use of heat sinks or shielding is prohibited except when they are part of the component (see 2.2).
- b. Mounting board, if different from that specified (see 2.4).
- c. Solder, if different from that specified (see 3.1).
- d. Flux, if applicable and if different from that specified (see 3.2, 4.1, and 4.3).
- e. Solder terminations that are not to be tested, if applicable (see 4.4).
- f. Special preparation of specimens if applicable (see 4.1).
- g. Depth of immersion in the molten solder, if different from that specified (see 4.4.2).
- h. Test condition letter (see 4.4).
- i. Cooling time prior to final examinations and measurements (see 4.4 and 5).
- j. Examinations and measurements before and after test, as applicable (see 5).
- k. Method of internal inspection, if required (see 5).

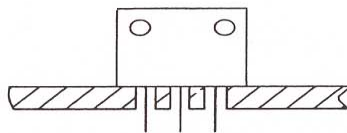
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TABLE 2036-1: Test conditions.

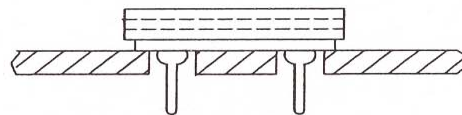
Test Condition	Solder Technique simulation	Temperature (°C)	Time (s) (at temp.)	Temperature ramp / immersion and / emersion rate	Number of heat cycles
A	Solder iron	350 ± 10 (solder iron temp)	4 - 5		1
B	Dip	260 ± 5 (solder temp)	10 ± 1	25 ± 6 mm/s	1
C	Wave: Topside	260 ± 5 (solder temp)	20 ± 1	Preheat 1 °C/s-4 °C/s to within 100 °C of solder temp. 25 mm/s ± 6 mm/s	1
D	Wave: Bottom-side	260 ± 5 (solder temp)	10 ± 1	Preheat 1 °C/s-4 °C/s to within 100 °C of solder temp. 25 mm/s ± 6 mm/s	1
H	Vapor phase reflow	215 ± 5 (vapor temp)	60 ± 5		1
I	IR/convection reflow	215 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3
J	IR/convection reflow	235 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3
K	IR/convection reflow	250 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3



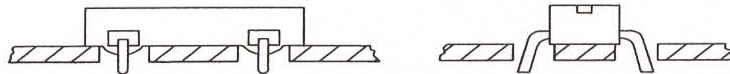
AXIAL LEADS - WIRE LEADS



PIN LEADS



RADIAL LEADS - PIN LEADS



DUAL IN-LINE PACKAGE - RIBBON LEADS

FIGURE 2036-1 Component lead and mounting examples.