The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 May 1997.

INCH - POUND

MIL-STD-883E
31 DECEMBER 1996
SUPERSEDING
MIL-STD-883D
15 NOVEMBER 1991

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

MICROCIRCUITS

AMSC N/A

FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

FOREWORD

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

* 2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center Columbus, P.O. Box 3990, Columbus, OH 43216-5000, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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TEST METHODS

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TEST METHODS

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5013	Wafer fabrication control and wafer acceptance procedures for processed GaAs wafers.

1. SCOPE

1.1 Purpose. This standard establishes uniform methods, controls, and procedures for testing microelectronic devices suitable for use within Military and Aerospace electronic systems including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations; mechanical and electrical tests; workmanship and training procedures; and such other controls and constraints as have been deemed necessary to ensure a uniform level of quality and reliability suitable to the intended applications of those devices. For the purpose of this standard, the term "devices" includes such items as monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices. The test methods, controls, and procedures described herein have been prepared to serve several purposes:

a. To specify suitable conditions obtainable in the laboratory and at the device level which give test results equivalent to the actual service conditions existing in the field, and to obtain reproducibility of the results of tests. The tests described herein are not to be interpreted as an exact and conclusive representation of actual service operation in any one geographic or outer space location, since it is known that the only true test for operation in a specific application and location is an actual service test under the same conditions.

b. To describe in one standard all of the test methods of a similar character which now appear in the various joint-services and NASA microelectronic device specifications, so that these methods may be kept uniform and thus result in conservation of equipment, manhours, and testing facilities. In achieving this objective, it is necessary to make each of the general tests adaptable to a broad range of devices.

c. To provide for a level of uniformity of physical, electrical and environmental testing; manufacturing controls and workmanship; and materials to ensure consistent quality and reliability among all devices screened in accordance with this standard.

1.2 Intended use of or reference to MIL-STD-883. When this document is referenced or used in conjunction with the processing and testing of JAN devices in conformance with the requirements of appendix A of MIL-PRF-38535, QML devices in conformance with MIL-PRF-38535 or non-JAN devices in accordance with 1.2.1 or 1.2.2 herein, such processing and testing shall be in full conformance with all the applicable general requirements and those of the specifically referenced test methods and procedures.

For contracts negotiated prior to 31 December 1984, device types that have been classified as manufacturer's 883 (B or S) product prior to 31 December 1984 shall not have to meet 1.2.1 or 1.2.2.

Existing contracts as of the 31 December 1984, previously negotiated add-ons to these contracts, and future spares for these contracts may continue to use device types which were classified as manufacturer's 883 (B or S) prior to 31 December 1984.

New contracts, and any device types classified as compliant to MIL-STD-883 after 31 December 1984 shall comply with 1.2.1. Any devices meeting only the provisions of 1.2.2 are noncompliant to MIL-STD-883.

1.2.1 Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices. When any manufacturer, contractor, subcontractor, or original equipment manufacturer requires or claims a non-JAN part compliant with MIL-STD-883, all provisions of Appendix A of MIL-PRF-38535 shall be met. In addition, manufacturers that have produced or are producing products in accordance with 1.2.1a are subject to a Government compliance validation audit on a drop-in basis with a minimum of notice. Such processing and testing shall be in compliance with all of the applicable general controls and requirements defined herein and those of the specifically referenced test methods and procedures with no reinterpretations, deviations or omissions except as specifically allowed in the device specification or standard microcircuit drawing covering the same generic device. Deviations specifically granted in the device specification or standard microcircuit drawing may also be applied to devices manufactured in the same process, to the same design criteria, and using elements of the same microcircuit group as those used for devices covered by the device specification or standard microcircuit drawing. Such reference include the following:

Manufacturers who use MIL-STD-883 in device marking, or make statements in applicable certificates of conformance that parts are compliant with MIL-STD-883, or make statements in advertisements or in published brochures or other marketing documents that parts provided are compliant with MIL-STD-883.

* Contractors, sub-contractors, or original equipment manufacturers who prepare vendor item drawings, (previously called Specification Control drawings), or Selected Item drawings which require compliance with MIL-STD-883, or invoke it in its entirety as the applicable standard (see 1.2.2 for noncompliant devices).

a. Custom monolithic, non-JAN multichip and all other non-JAN microcircuits except non-JAN hybrids described or implied to be compliant with methods 5004 and 5005 or 5010 of MIL-STD-883 shall meet all of the non-JAN requirements of Appendix A of MIL-PRF-38535.

b. Hybrid microcircuits described as compliant or multichip microcircuits described as compliant to MIL-PRF-38534 shall meet all the requirements of MIL-PRF-38534 (or equivalent procedures/ requirements of reciprocal listing provisions for product of other nations based on existing international agreements):

* 1.2.2 Provisions for the use of MIL-STD-883 in conjunction with non-compliant non -JAN devices. Any device that is processed with deviations and which is not processed in compliance with the provisions of 1.2.1 defined herein shall not be claimed to be compliant and shall not be marked "/883", "/883B", "/883S", or any variant thereof. All applicable documentation (including device specifications or manufacturer's data sheets and responses to RFQ's invoking MIL-STD-883) shall clearly and specifically define any and all areas of nonconformance and identify them as deviations in language that is not subject to misinterpretation by the acquiring authority.

If the contract or order specifically requires compliance with, equivalence to, or a product that is equal to or better than MIL-STD-883 class B or class S, any exceptions taken to the requirements of the referenced quality level (i.e., 1.2.1 above) shall prohibit the manufacturer from claiming or implying equivalence to that level.

Specific reference to one or more MIL-STD-883 method(s) on a stand-alone basis requires compliance to only the specifically referenced method(s). Such devices are not considered compliant in accordance with 1.2.1 above. However, compliance with only the test procedures contained in test methods 5004, 5005, and 5010 on a stand-alone basis (without specifying compliance or noncompliance to 1.2.1) does not satisfy the form, fit, and function requirements of MIL-STD-973 for configuration items, and any reference to these methods on a stand alone basis requires compliance to all the provisions of 1.2.1.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, and 5 of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, and 5 of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification For.
MIL-PRF-38534 - Hybrid Microcircuits, General Specification For.
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

STANDARDS

FEDERAL

FED-STD-209 - Clean Room and Work Station Requirements, Controlled Environment.

DEPARTMENT OF DEFENSE

MIL-STD-280 - Definitions of Item Levels, Item Exchangeability, Models, and Related Terms.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-217 - Reliability Prediction of Electronic Equipment.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Standardization Documents Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS

ANSI/IUPC-T-50 - Terms and Definitions.

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 7380 N. Lincoln Avenue, Lincolnwood, IL 60616.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540-1	-	Calibration Laboratories and Measuring and Test Equipment, General Requirements
ANSI/J-STD-004	-	Requirements for Soldering Fluxes
ANSI/J-STD-006	-	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications

(Application for copies should be addressed to the American National Standards Institute, Incorporated, 1430 Broadway, New York, NY 10018)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

C177	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Guarded Hot-Plate Apparatus.
C518	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Heat Flow Meter Apparatus.
D150	-	Standard Test Methods for A-C Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulating Materials.
D257	-	Standard Test Methods for D-C Resistance or Conductance of Insulating Materials.
D1002	-	Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal).
D3386	-	Coefficient of Linear Thermal Expansion of Electrical Insulating Materials, Test Method for.
D3850	-	Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermogravimetric Method, Test Method for.
E263	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Iron.
E264	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Nickel.
E265	-	Standard Test Method for Measuring Fast-Neutron Fluences by Radioactivation of Sulfur.
E666	-	Standard Practice for Calculating Absorbed Dose from Gamma or X Radiation.
E668	-	Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
E720	-	Standard Guide for Selection of a Set of Neutron- Activation Foils for Determining Neutron Spectra used in Radiation-Hardness Testing of Electronics.
E721	-	Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.

(Application for copies should be addressed to the American National Standards Institute, Incorporated, 1430 Broadway, New York, NY 10018.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purpose of this standard, the abbreviations, symbols, and definitions specified in ,MIL-PRF-19500, MIL-PRF-38535, or MIL-STD-280 shall apply. The following definitions shall also apply:

3.1.1 Microelectronic device. A microcircuit, microcircuit module, or an element of a microcircuit as defined in appendix A of MIL-PRF-38535. For the purposes of this document, each type of microelectronic device shall be identified by a unique type, or drawing number.

3.1.2 Mode of failure. The cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet (i.e., no failure analysis is required to identify the mode of failure, which should be obvious from the rejection criteria of the test method).

3.1.3 Mechanism of failure. The original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness and, where applicable, the nature of externally applied stresses which led to failure.

3.1.4 Absolute maximum ratings. The values specified for ratings, maximum ratings, or absolute maximum ratings are based on the "absolute system" and are not to be exceeded under any measurable or known service or conditions. In testing microelectronic devices, limits may be exceeded in determining device performance or lot quality, provided the test has been determined to be nondestructive and precautions are taken to limit device breakdown and avoid conditions that could cause permanent degradation. These ratings are limiting values beyond which the serviceability of any individual microelectronic integrated circuit may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings are permissible only if no single maximum rating is exceeded under any service condition. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of 25°C ±3°C. For pulsed or other conditions of operation of a similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variations, load variations, or manufacturing variations in the equipment itself.

The values specified for "Testing Ratings" (methods 1005, 1008, 1015, 5004, and 5005) are intended to apply only to short-term, stress-accelerated storage, burn-in, and life tests and shall not be used as basis for equipment design.

3.1.5 Worst case condition. Worst case condition(s) consists of the simultaneous application of the most adverse (in terms of required function of the device) values (within the stated operating ranges) of bias(es), signal input(s), loading and environment to the device under test. Worst cases for different parameters may be different. If all the applied test conditions are not established at the most adverse values, the term "partial worst case condition" shall be used to differentiate and shall be accompanied by identification of the departure from worst case. For example, the lowest values of supply voltages, signal input levels, and ambient temperature and the highest value of loading may constitute "worst case conditions" for measurement of the output voltage of a gate. Use of the most adverse values of applied electrical conditions, at room temperature, would then constitute "partial worst case conditions" and shall be so identified using a postscript "at room temperature."

3.1.5.1 Accelerated test condition. Accelerated test conditions are defined as test conditions using one or more applied stress levels which exceed the maximum rated operating or storage stress levels but are less than or equal to the "Testing Rating" values.

3.1.6 Static parameters. Static parameters are defined as dc voltages, dc currents, or ratios of dc voltages or dc currents, or both.

3.1.7 Dynamic parameters. Dynamic parameters are defined as those which are rms or time-varying values of voltages or currents, or ratios of rms or time-varying values of voltages or currents, or both.

3.1.8 Switching parameters. Switching parameters are defined as those which are associated with the transition of the output from one level to another or the response to a step input.

3.1.9 Functional tests. Functional tests are defined as those go, no-go tests which sequentially exercise a function (truth) table or in which the device is operated as part of an external circuit and total circuit operation is tested.

3.1.10 Acquiring activity. The acquiring activity is the organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity shall not have the authority to grant waivers, deviations, or exceptions unless specific written authorization to do so has also been given by the Government organization.

3.1.11 Accuracy. The quality of freedom from error. Accuracy is determined or assured by calibration, or reliance upon calibrated items.

3.1.12 Calibration. Comparison of measurement standard or instrument of known accuracy with another standard, instrument or device to detect, correlate, report or eliminate by adjustment, any variation in the accuracy of the item being compared. Use of calibrated items provide the basis for value traceability of product technical specifications to national standard values. Calibration is an activity related to measurement and test equipment performed in accordance with ANSI/NCSL Z540-1 or equivalent.

3.1.13 Precision. The degree to which an instrument, device, assemblage, test, measurement or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC). Term is used interchangeably with "repeatability".

3.1.14 Resolution. The smallest unit of readability or indication of known value in an instrument, device or assemblage thereof.

3.1.15 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRM's used in product testing provide traceability for technical specifications. SRM's do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

3.1.16 Tolerance. A documented range over which a specified value may vary.

3.1.17 Test accuracy ratio (TAR). A ratio of the tolerance of the device under test to the accuracy of the related measuring or test instrument or to the accuracy of the correlation device/SRM.

3.1.18 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

3.1.19 Susceptibility. The point at which a device fails to meet the postirradiation end-point electrical parameter limits or fails functionally during radiation exposure (e.g., neutron irradiation).

3.1.20 Class M. Class M is defined as 1.2.1 compliant product or product built in compliance to Appendix A of MIL-PRF-38535 documented on a Standard Microcircuit Drawing where configuration control is provided by the Government preparing activity. Class M devices shall use the conditions specified in the test methods herein for class level B product.

• 3.1.21 Class level B and class level S. 2 class levels are used in this document to define requirements for high reliability military applications (Class level B) and space applications (Class level S). Class level B requirements contained in this document are intended for use for Class Q, Class H, and Class M products, as well as Class B M38510 JAN slash sheet product. Class level B requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for high reliability military applications. Class level S requirements contained in this document are intended for use for Class V, Class K, as well as M38510 Class S JAN slash sheet product. Class level S requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for space level applications.

4. GENERAL REQUIREMENTS

4.1 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

4.1.1 Classification of tests. The tests are divided into four classes:

1001 to 1999	Environmental tests
2001 to 2999	Mechanical tests
3001 to 4999	Electrical tests
5001 to 5999	Test procedures

4.1.2 Revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 4001.1 is the first revision of test method 4001.

4.1.3 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification by specifying this standard, the method number, and the details required in the summary paragraph of the applicable method. To avoid the necessity for changing specifications which refer to this standard, the revision number should not be used when referencing test methods. For example, use 4001, not 4001.1.

4.2 Test results. The data resulting from application of any test method or procedure shall be reported in terms of the actual test conditions and results. "Equivalent" results (e.g., equivalent 25°C device hours or failure rate derived from 125°C test conditions) may be reported in addition to the actual results but shall not be acceptable as an alternative to actual results. Results of any test method or procedure shall be accompanied by information on the total quantity of devices in each lot being tested on a 100 percent or sampling basis, the associated quantity of devices in the sample for tests on a sampling basis, and the number of failures or devices rejected by test method and observed mode of failure. In cases where more than a single device type (part number) is involved in the makeup of a lot for inspection or delivery, the data shall be reported as above but with a further breakdown by part number.

4.3 Test sample disposition. Test sample disposition shall be in accordance with 40.3.2.1 of Appendix A of MIL-PRF-38535.

4.4 Orientation.

4.4.1 Identification of orientation and direction of forces applied. For those test methods which involve observation or the application of external forces which must be related to the orientation of the device, such orientation and direction of forces applied shall be identified in accordance with figures 1 and 2.

4.4.2 Orientation for other case configurations. For case configurations other than those shown in figures 1 and 2, the orientation of the device shall be as specified in the applicable acquisition document.

4.4.3 Orientation for packages with different size lateral dimensions. In flat packages where radial leads emanate from three or more sides, the X-direction shall be assigned to the larger and the Z-direction to the smaller of the two lateral dimensions.

FIGURE 1a. Orientation of microelectronic device to direction of applied force.

FIGURE 1b. Radial lead flat packages.

FIGURE 1c. Dual-in-line package.

FIGURE 1d. Flat package with radial leads from one side only.

FIGURE 1. Orientation noncylindrical microelectronic devices to direction of applied forces.

FIGURE 1e. Leadless chip carrier (top view).

NOTE: The Y1 force application is such that it will tend to lift the die off the substrate or the wires off the die. The reference to applied force actually refers to the force which operates on the device itself an may be the resultant of the primary forces applied in a different manner or direction to achieve the desired stress at the device (e.g., constant acceleration).

FIGURE 1. Orientation of noncylindrical microelectronic devices to direction of applied forces - Continued.

NOTE: The Y1 force application is such that it will tend to lift the die off the substrate or the wires off the die. The reference to applied force actually refers to the force which operates on the device itself and may be the resultant of the primary forces applied in a different manner or direction to achieve the desired stress at the device (e.g., constant acceleration).

FIGURE 2. Orientation of cylindrical microelectronic device to direction of applied forces.

4.5 Test conditions. All newly designed device types shall meet the test conditions specified in 4.5.1 through 4.5.3.2.

4.5.1 Calibration requirements. Calibration shall be applied to those items of measuring and test equipment used to assure product delivery specifications or critical manufacturing elements. Calibration shall be performed in accordance with the requirements of ANSI/NCSL Z540-1 or equivalent. Calibrated items shall be controlled, used and stored in a manner suitable to protect calibration integrity. Test equipment requiring calibration (single items or assemblages) shall be identified and labeled in accordance with ANSI/NCSL Z540-1 or equivalent.

4.5.2 Electrical test equipment accuracy. Unless otherwise specified in the acquisition document, test conditions such as: voltage, resistive loads, capacitive loads, input switching parameters, input static parameters, currents and others shall be set to nominal values as defined in the acquisition document, with tolerances suitable for the test in which they are used.

4.5.3 Electrical test equipment capability. Using any or all of the following techniques, the manufacturer shall determine that the test set/system is suitable to ensure product conformance with the acquisition document. Alternate suitable techniques may be used when approved by the qualifying activity. The manufacturer shall define and document methods used. The test equipment accuracy should be better than the allowable device tolerance in accordance with the following ratios:

a. Greater than or equal to 10:1 for routine processes.

b. Greater than or equal to 4:1 for special processes (commercial equipment not readily available).

NOTE: State of the art requirements in which 4:1 can not be effectively achieved due to a lack of national standards shall be justified and documented.

4.5.3.1 Control based on uncertainty. Test processes that have complex characteristics are best performed and controlled by the application of uncertainty analysis. The overall uncertainty in a test or measurement process shall be determined and the impact of said uncertainty on the product parameter tolerance shall be taken into account. The methods used for determining uncertainty shall be defined and documented. The method selected may use any (or combinations) of the following forms:

a. Arithmetic addition (linear), normally produces an overly conservative estimate and reflects a highly improbable situation in which contributing errors are at their maximum limit at the same time and same direction.

b. Root Sum Square (RSS), normally applied where the errors tend to fit a normal distribution (gaussian) and are from independent sources.

c. Partial Derivatives, used where complex relationships exist.

d. Monte Carlo Simulation, used in very complex situations where other methods are not easily applied or do not fit.

e. SRM (or controlled correlation device) testing providing observable data.

NOTE: Observable data, from a controlled device, may be relied upon to provide feedback that confirms process performance is within statistical limits.

f. Analysis of systematic and random errors, applying corrections as applicable.

g. Any other recognized method of combining errors into an expression of uncertainty substantiated by an engineering analysis.

4.5.3.2 Use and control of correlation devices/SRM's. When a manufacturer elects to use correlation devices or SRM's, methods of use and control shall be in place and documented including parameters, type, quantity, description, identification, storage, handling and periodic verification requirements.

4.5.4 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be the specified operating frequency. Where a frequency range is specified, major functional parameters shall be tested at the maximum and minimum frequencies of the range in addition to those tests conducted at any specified frequency within the range. Whenever electrical tests are conducted on microelectronic devices for which a range of frequencies or more than a single operating frequency is specified, the frequency at which tests are conducted shall be recorded along with the parameters measured at those frequencies.

4.5.5 Testing of multiple input/output devices. Where any input or output parameter is specified for devices having more than a single input or output, the specified parameter shall be tested at all input or output terminations of the device.

4.5.6 Testing of complex devices. Where microelectronic devices being tested contain multiple circuits or functions, whether independently connected to the external device leads or whether internally connected in some arrangement to minimize the number of external leads, suitable test circuits and procedures shall be applied so as to test all circuits or functions contained in the device with all the applicable test methods specified in the applicable acquisition document. For example, if a device contains a pair of logic gates it shall not be acceptable to test only one of the gates for the specified parameters. Furthermore, multiple circuit devices should be tested to assure that no significant interaction exists between individual circuits (e.g., application of signal to one gate of a dual gate device should not cause a change in output of the other gate). The intent of this requirement is to assure that all circuit elements in a microelectronic device are exercised to the fullest extent allowed by their construction and connection provisions. For circuit arrays containing complex signal paths which vary depending on the nature of incoming signals or internal functions performed on the incoming signals, this requirement shall be met by programming the operation of the device to assure that all circuit elements are caused to function and thus provide the opportunity to observe or measure the levels of their performance in accordance with the specified test methods.

4.5.7 Test environment. Unless otherwise specified herein, or in the applicable acquisition documentation, all measurements and tests shall be made at ambient temperature of 25°C +3°C, -5°C and at ambient atmospheric pressure from 580 to 800 millimeters mercury.

4.5.8 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

a. Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within ±2°C or ±4 percent, whichever is greater.

b. Space variation within working area: Chambers shall be so constructed that at any given time, the temperature of any point within the working area shall not deviate more than ±3°C or ±3 percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.

c. Chambers with specified minimum temperatures (e.g., burn-in, life test, etc.): When test requirements involve a specified minimum test temperature, the controls and chamber construction shall be such that the temperature of any point within the working area shall not deviate more than +8°C, -0°C; or +8, -0 percent, whichever is greater, from the specified minimum temperature.

4.5.9 Control of test temperature during electrical measurements. Unless otherwise specified, the specified test temperature, case (T_C), ambient (T_A), or junction (T_J) shall be controlled by the applicable procedure(s) specified herein. These are exclusively for the control of chambers, handlers, etc., used in electrical measurements of devices at specified temperatures and the provisions of 4.5.8 do not apply. Testing shall be conducted using either power-off condition followed by low duty cycle pulse testing or power stable temperature condition.

4.5.9.1 Temperature control during testing for T_C, T_A, or T_J above 25°C. Unless otherwise specified, the device shall be stabilized in the power-off condition until the device temperature is within ±3°C of the specified T_C, T_A, or T_J, as applicable. The temperature during test shall not fall more than 3°C below the specified T_C, T_A, or T_J. The temperature during test may exceed 3°C of the specified T_C, T_A, or T_J provided the manufacturer assures that the devices under test are not being degraded. The electrical test parameters shall be measured using low duty cycle pulse testing or, if specified, power stable conditions (see 4.5.9.4).

4.5.9.2 Temperature control during testing for T_C, T_A, or T_J below 25°C. Unless otherwise specified, the device shall be stabilized in the power-off condition until the device temperature is within ±3°C of the set temperature (see note below). The device shall not exceed +5°C of the specified temperature throughout the test duration. (This temperature shall be identified as the cold-start temperature.) The electrical test parameters shall be measured using low duty cycle pulse testing or, if specified, power stable conditions (see 4.5.9.4). When applicable, the detail specification shall specify those parameters or sequence of tests most sensitive to the cold-start temperature. These parameters, when specified, shall be measured at the start of the test sequence and shall be completed as soon as possible or within a specified time.

NOTE: Unless otherwise specified in the applicable detail specification, the set temperature shall be -55°C (T_C, T_A, or T_J, as applicable) or colder if the device temperature (T_C, T_A, or T_J, as applicable) increases by more than +5°C during the test duration.

4.5.9.3 Temperature control during testing for T_C, T_A, or T_J at 25°C. Unless otherwise specified, the device shall be stabilized in the power-off condition until the temperature is 25°C +3°C, -5°C. The electrical test parameters shall be measured using low duty pulse testing or, if specified, power stable conditions (see 4.5.9.4).

4.5.9.4 Power stable temperature condition. When specified, the device shall be stabilized in the specified steady-state power-on condition at the specified test temperature, T_A, T_C, or T_J as applicable, for temperatures at, above, or below 25°C for a minimum time period of 5 minutes or a specified time. The electrical parameters measurements shall be completed as soon as possible or within a specified period of time after temperature/power stabilization has occurred. Alternatively, when specified, the device temperature T_C or T_A may be stabilized within ±3°C of the junction temperature typically predicted for the specified steady-state power-on condition of 5 minutes or more and the testing conducted with low duty pulse techniques.

4.6 General precautions. The following precautions shall be observed in the testing of devices:

4.6.1 Transients. Devices shall not be subjected to conditions in which voltage or current transients cause the ratings to be exceeded.

4.6.2 Order of connection of leads. Care should be taken when connecting a microelectronic device to a power source. For MOS devices or other microelectronic circuits or devices where the order of connection of leads may be important, precautions cited in the applicable acquisition document shall be observed.

4.6.3 Soldering and welding. Adequate precautions shall be taken to avoid damage to the device during soldering or welding required for tests.

4.6.4 Radiation precautions. Due precautions shall be used in storing or testing microelectronic devices in substantial fields of x-rays, neutrons, or other energy particles.

4.6.5 Handling precautions for microelectronic devices.

a. Ground all equipment prior to insertion of the device for electrical test.

b. Where applicable, keep devices in metal shields until they are inserted in the equipment or until necessary to remove for test.

c. Where applicable, keep devices in carriers or other protective packages during test.

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

6.1 Chemical listing. The following is a listing of chemicals identified for use in MIL-STD-883 test methods:

Material	CAS listing	Test method
Acetic Acid	64-19-7	2021
3.5-Dimethyl-1-hexyn-3-o1	4209-91-0	1002
Ethylbenzene	100-41-4	2015
Fluorescein	2321-07-5	1014
Freon-113 1/	76-13-1	2015,1014
Hydrochloric Acid	7647-01-0	1009
Isopropyl Alcohol	67-63-0	2015,2003
Kerosene	8008-20-6	2015
Morpholine	110-91-8	1002
Methanol	67-56-1	1002
Methylene Chloride 1/	75-09-2	2015
Mineral Spirits	8032-32-4	2015
Monoethanolamine	141-43-5	2015
Nitric Acid	7697-37-2	2021
Phosphoric Acid	7664-38-2	2021
Propylene Glycol Monomethyl Ether	107-98-2	2015
Rhodamine B	81-88-9	1014
Sodium Chloride	7647-14-5	1009,1002
Sodium Hydroxide	1310-73-2	1009
Stannous Chloride	7772-99-8	1002
1,1,1-Trichloroethane 1/	71-55-6	2015
Zyglo Dye	8002-05-9	1014

In the event of a chemical emergency (example: spill, leak, fire, or exposure) obtain additional help or information by calling the telephone number listed below and identify the chemical by the CAS number provided above.

Chem Trec: 1-800-424-9300

6.2 Subject term (key word) listing.

Intended use
Provisions for the use of MIL-STD-883
Abbreviations
Classification of tests
Orientation
Electrical test equipment accuracy
Test environment
General precautions
Chemical listing

1/ These chemicals are no longer required to be used in MIL-STD-883 test methods.

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI, SM
Navy - AS, CG, MC, OS, SH, TD
Air Force - 19, 85, 99

Preparing activity:
DLA - ES

(Project 5962-1617)

METHOD 1001

BAROMETRIC PRESSURE, REDUCED (ALTITUDE OPERATION)

1. PURPOSE. The barometric-pressure test is performed under conditions simulating the low atmospheric pressure encountered in the nonpressurized portions of aircraft and other vehicles in high-altitude flight. This test is intended primarily to determine the ability of component parts and materials to avoid voltage breakdown failures due to the reduced dielectric strength of air and other insulating materials at reduced pressures. Even when low pressures do not produce complete electrical breakdown, corona and its undesirable effects, including losses and ionization are intensified. The simulated high-altitude conditions of this test can also be employed to investigate the influence on components' operating characteristics, of other effects of reduced pressure, including changes in dielectric constants of materials, and decreased ability of thinner air to transfer heat away from heat-producing components.

2. APPARATUS. The apparatus used for the barometric-pressure test shall consist of a vacuum pump and a suitable sealed chamber having means for visual observation of the specimen under test when necessary, a suitable pressure indicator to measure the simulated altitude in feet in the sealed chamber, and a microammeter or oscilloscope capable of detecting current over the range from dc to 30 megahertz.

3. PROCEDURE. The specimens shall be mounted in the test chamber as specified and the pressure reduced to the value indicated in one of the following test conditions, as specified. While the specimens are maintained at the specified pressure, the specimens shall be subjected to the specified tests. During this test and for a period of 20 minutes before, the test temperature shall be 25°C ±10°C. The device shall have the specified voltage applied and shall be monitored over the range from atmospheric pressure to the specified minimum pressure and return for any device malfunctions. A device which exhibits arc-overs, harmful coronas, or any other defect or deterioration which may interfere with the operation of the device shall be considered a failure.

Test condition	Pressure, maximum		Altitude	
	Inches of mercury	mm of mercury	Feet	Meters
A	17.3	439.00	15,000	4,572
B	8.88	226.00	30,000	9,144
C	3.44	87.00	50,000	15,240
D	1.31	33.00	70,000	21,336
E	0.315	8.00	100,000	30,480
F	0.043	1.09	150,000	45,720
G	9.436×10^{-6}	2.40×10^{-6}	656,000	200,000

3.1 Measurement. The device shall be connected for measurement and have the specified voltages applied during the entire pump-down cycle. The terminals to which the maximum voltage (see 4c.) is applied shall be monitored with a microammeter or oscilloscope for corona currents in the range from dc to 30 megahertz. Provision shall be made for calibrating the current flow in the test circuit minus the device under the applicable test condition to insure that test readings are characteristic of the device under test.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

   a. Method of mounting (see 3).

   b. Test condition letter (see 3). Unless otherwise specified, condition E shall be used.

   c. Tests during subjection to reduced pressure (see 3). Unless otherwise specified, the device shall be subjected to the maximum voltage it would be subjected to under rated operating conditions.

   d. Tests after subjection to reduced pressure, if applicable (see 3). Unless otherwise specified, the device shall be subjected to full electrical tests of specified device characteristics or parameters.

   e. Exposure time prior to measurement, if applicable (see 3).

METHOD 1002

IMMERSION

1. PURPOSE. This test is performed to determine the effectiveness of the seal of microelectronic devices. The immersion of the part under evaluation into liquid at widely different temperatures subjects it to thermal and mechanical stresses which will readily detect a defective terminal assembly, or a partially closed seam or molded enclosure. Defects of these types can result from faulty construction or from mechanical damage such as might be produced during physical or environmental tests. The immersion test is generally performed immediately following such tests because it will tend to aggravate any incipient defects in seals, seams, and bushings which might otherwise escape notice. This test is essentially a laboratory test condition, and the procedure is intended only as a measurement of the effectiveness of the seal following this test. The choice of fresh or salt water as a test liquid is dependent on the nature of the component part under test. When electrical measurements are made after immersion cycling to obtain evidence of leakage through seals, the use of a salt solution instead of fresh water will facilitate detection of moisture penetration. This test provides a simple and ready means of detection of the migration of liquids. Effects noted can include lowered insulation resistance, corrosion of internal parts, and appearance of salt crystals. The test described is not intended as a thermal- shock or corrosion test, although it may incidentally reveal inadequacies in these respects. This is a destructive test and shall not be used as a 100 percent test or screen.

2. APPARATUS. The apparatus used for the immersion test shall consist of controlled temperature baths capable of maintaining the temperatures indicated for the hot bath and the cold bath test condition selected. A suitable temperature indicator shall be used to measure bath temperature.

3. PROCEDURE. This test consists of successive cycles of immersions, each cycle consisting of immersion in a hot bath of fresh (tap) water at a temperature of 65°C +5°C, -0°C followed by immersion in a cold bath. The number of cycles, duration of each immersion, and the nature and temperature of the cold bath shall be as indicated in the applicable test condition listed below, as specified. The transfer of specimens from one bath to another shall be accomplished as rapidly as practicable and in no case shall transfer time exceed 15 seconds. After completion of the final cycle, specimens shall be thoroughly and quickly washed in fresh (tap) water or distilled water and all surfaces wiped or air-blasted clean and dry. Unless otherwise specified, measurements shall be made at least 4 hours, but not more than 48 hours, after completion of the final cycle. When specified in the applicable acquisition document, upon completion of the electrical measurements and external visual examination, the device shall be delidded or dissected and examined in accordance with method 2013 for evidence of corrosion of internal elements or the appearance of salt crystals. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Number of cycles	Duration of each immersion (minutes)	Immersion bath (cold)	Temperature of cold bath °C
A	2	15	Fresh (tap) water	25 +10 -5
B	2	15	Saturated solution of sodium chloride and water	25 +10 -5
C	5	60	Saturated solution of sodium chloride and water	0 ±3
D	5	60	(Parts by volume) Water -48 parts Methanol 1/ -50 parts Morpholine -1 part 3.5-dimethyl-1-hexyn-3-o1-1 part Stannous chloride - 5 grams	0 ±3

1/ Synonyms are tetrahydro-1, 4-oxazine and diethylenimide oxide.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Test condition letter (see 3). Unless otherwise specified, condition C shall be used.

b. Time after final cycle allowed for measurements, if other than that specified (see 3).

c. Measurements after final cycle (see 3). Unless otherwise specified, measurements shall include pin-to-pin resistance, pin-to-case resistance and full electrical test of all device characteristics or parameters listed in the applicable acquisition document. Final evaluation shall include external visual examination for legibility of device markings and for evidence of discoloration or corrosion of package and leads.

d. Dissection and internal examination, where applicable (see 3).

METHOD 1003

INSULATION RESISTANCE

1. PURPOSE. This test is to measure the resistance offered by the insulating members of a component part to an impressed direct voltage tending to produce a leakage of current through or on the surface of these members. Insulation-resistance measurements should not be considered the equivalent of dielectric withstanding voltage or electric breakdown tests. A clean, dry insulation may have a high insulation resistance, and yet possess a mechanical fault that would cause failure in the dielectric withstanding voltage test. Since insulating members composed of different materials or combinations of materials may have inherently different insulation resistances, the numerical value of measured insulation resistance cannot properly be taken as a direct measure of the degree of cleanliness or absence of deterioration.

1.1 Factors affecting use. Factors affecting insulation-resistance measurements include temperature, humidity, residual charges, charging currents or time constant of instrument and measured circuit, test voltage, previous conditioning, and duration of uninterrupted test voltage application (electrification time). In connection with this last-named factor, it is characteristic of certain components (for example, capacitors and cables) for the current to usually fall from an instantaneous high value to a steady lower value at a rate of decay which depends on such factors as test voltage, temperature, insulating materials, capacitance, and external circuit resistance. Consequently, the measured insulation resistance will increase for an appreciable time as test voltage is applied uninterruptedly. Because of this phenomenon, it may take many minutes to approach maximum insulation-resistance readings, but specifications usually require that readings be made after a specified time. This shortens the testing time considerably while still permitting significant test results, provided the insulation resistance is reasonably close to steady-state value, the current versus time curve is known, or suitable correction factors are applied to these measurements. For certain components, a steady instrument reading may be obtained in a matter of seconds. When insulation-resistance measurements are made before and after a test, both measurements should be made under the same conditions.

2. APPARATUS. Insulation-resistance measurements shall be made on an apparatus suitable for the characteristics of the component to be measured such as a megohm bridge, megohmmeter, insulation-resistance test set, or other suitable apparatus.

3. PROCEDURE. When special preparations or conditions such as special test fixtures, reconnections, grounding, isolation, low atmospheric pressure, humidity, or immersion in water are required, they shall be specified. Insulation-resistance measurements shall be made between the mutually insulated points or between insulated points and ground, as specified. When electrification time is a factor, the insulation-resistance measurements shall be made immediately after the specified time (see 4) of uninterrupted test voltage application, unless otherwise specified. However, if the instrument-reading indicates that an insulation resistance meets the specified limit, and is steady or increasing, the test may be terminated before the end of the specified period. When more than one measurement is specified, subsequent measurements of insulation resistance shall be made using the same polarity as the initial measurements. Unless otherwise specified, the direct potential applied to the specimen shall be that indicated by one of the test condition letters, as specified below, and insulation resistance measurements shall be made with both polarities of the applied voltage:

Test condition	Test potential
A	10 volts ±10%
B	25 volts ±10%
C	50 volts ±10%
D	100 volts ±10%
E	500 volts ±10%
F	1,000 volts ±10%

For inplant quality conformance testing, any voltage may be used provided it is equal to or greater than the minimum potential allowed by the applicable test condition. Unless otherwise specified, the measurement error at the insulation-resistance value shall not exceed 10 percent. Proper guarding techniques shall be used to prevent erroneous readings due to leakage along undesired paths.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

   a. Test condition letter, or other test potential, if specified (see 3).

   b. Special preparations or conditions, if required (see 3).

   c. Points of measurement (see 3). Unless otherwise specified, insulation resistance shall be measured between the device leads (all leads electrically connected to each other or to a common point) and the device case, and the measured resistance shall be no less than 15 megohms.

   d. Electrification time, if critical (see 1.1).

   e. Insulation resistance in terms of maximum leakage current at a specified test voltage. Unless otherwise specified, the maximum leakage between any adjacent disconnected leads shall not exceed 100 nanoampere at 100 volts dc.

METHOD 1004.7

MOISTURE RESISTANCE

1. PURPOSE. The moisture resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of component parts and constituent materials to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals; constituents of materials; and detrimental changes in electrical properties. This test differs from the steady-state humidity test and derives its added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes and, in addition, produces a "breathing" action of moisture into partially sealed containers. Increased effectiveness is also obtained by use of a higher temperature, which intensifies the effects of humidity. The test includes a low-temperature subcycle that acts as an accelerant to reveal otherwise indiscernible evidences of deterioration since stresses caused by freezing moisture tend to widen cracks and fissures. As a result, the deterioration can be detected by the measurement of electrical characteristics (including such tests as voltage breakdown and insulation resistance) or by performance of a test for sealing. Provision is made for the application of a polarizing voltage across insulation to investigate the possibility of electrolysis, which can promote eventual dielectric breakdown. This test also provides for electrical loading of certain components, if desired, in order to determine the resistance of current-carrying components, especially fine wires and contacts, to electrochemical corrosion. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. This test has proved reliable for indicating those parts which are unsuited for tropical field use.

2. APPARATUS. The apparatus used for the moisture resistance test shall include temperature-humidity chambers capable of maintaining the cycles and tolerance described on figure 1004-1 and electrical test equipment capable of performing the measurements in 3.6 and 4.

3. PROCEDURE. Specimens shall be tested in accordance with 3.2 through 3.7 inclusive, and figure 1004-1. Specimens shall be mounted in a manner that will expose them to the test environment.

3.1 Initial conditioning. Unless otherwise specified, prior to mounting specimens for the moisture resistance test, the device leads shall be subjected to a bending stress, initial conditioning in accordance with test condition B_1 of method 2004. Where the specific sample devices being subjected to the moisture resistance test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

3.2 Initial measurements. Prior to step 1 of the first cycle, the specified initial measurements shall be made at room ambient conditions, or as specified. When specified, the initial conditioning in a dry oven (see figure 1004-1) shall precede initial measurements and the initial measurements shall be completed within 8 hours after removal from the drying oven.

3.3 Number of cycles. Specimens shall be subjected to 10 continuous cycles, each as shown on figure 1004-1. In the event of no more than one unintentional test interruption (power interruption or equipment failure) prior to the completion of the specified number of cycles (except for the last cycle) the cycle shall be repeated and the test may continue. Unintentional interruptions occurring during the last cycle require a repeat of the cycle plus an additional uninterrupted cycle. Any intentional interruption, or any unintentional interruption of greater than 24 hours requires a complete retest.

3.4 Subcycle of step 7. During at least 5 of the 10 cycles a low temperature subcycle shall be performed. At least 1 hour but not more than 4 hours after step 7 begins, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced, for performance of the subcycle. Specimens during the subcycle shall be conditioned at -10°C +2°C, -5°C, with humidity not controlled, for 3 hours minimum as indicated on figure 1004-1. When a separate cold chamber is not used, care should be taken to assure that the specimens are held at -10°C +2°C, -5°C, for the full period. After the subcycle, the specimens shall be returned to 25°C at 80 percent relative humidity (RH) minimum and kept there until the next cycle begins.

3.5 Applied voltage. During the moisture resistance test as specified on figure 1004-1, when specified (see 4), the device shall be biased in accordance with the specified bias configuration which should be chosen to maximize the voltage differential between chip metallization runs or external terminals, minimize power dissipation and to utilize as many terminals as possible to enhance test results.

3.6 Conditions (see figure 1004-1). The rate of change of temperature in the chamber is unspecified; however, specimens shall not be subject to the radiant heat from the chamber conditioning processes. The circulation of air in the chamber shall be at a minimum cubic rate per minute equivalent to five times the volume of the chamber unless otherwise specified. The steady-state temperature tolerance is ±2°C of the specified temperature at all points within the immediate vicinity of the specimens and at the chamber surfaces. Specimens weighing 25 pounds or less shall be transferred between temperature chambers in less than 2 minutes.

3.7 Final measurements. Following step 6 of the final cycle (or step 7 if the subcycle of 3.3 is performed during the tenth cycle), devices shall be conditioned for 24 hours at room ambient conditions after which either an insulation resistance test in accordance with method 1003, test condition A, or the specified 25°C electrical end-point measurements shall be performed. Electrical measurements may be made during the 24 hour conditioning period. However, any failures resulting from this testing shall be counted, and any retesting of these failures later in the 24 hour period for the purpose of obtaining an acceptable result is prohibited. No other test (e.g., seal) shall be performed during the 24 hour conditioning period. The insulation resistance test or the alternative 25°C electrical end-point measurements shall be completed within 48 hours after removing the devices from the chamber. When the insulation resistance test is performed, the measured resistance shall be no less than 10 megohms and the test shall be recorded and data submitted as part of the end-point data. If the package case is electrically connected to the die substrate by design, the insulation resistance test shall be omitted and the specified 25°C electrical end-point measurements shall be completed within 48 hours after removal of the device from the chamber. A visual examination and any other specified end-point electrical parameter measurements (see 4.c) shall also be performed.

3.8 Failure criteria. No device shall be acceptable that exhibits:

a. Specified markings which are missing in whole or in part, faded, smeared, blurred, shifted, or dislodged to the extent that they are not legible. This examination shall be conducted with normal room lighting and with a magnification of 1X to 3X.

b. Evidence of corrosion over more than 5 percent of the area of the finish or base metal of any package element (i.e., lid, lead, or cap) or any corrosion that completely crosses the element when viewed with a magnification of 10X to 20X.

c. Leads missing, broken, or partially separated.

d. Corrosion formations which bridge between leads or between leads and metal case.

e. Electrical end-point or insulation resistance test failures.

NOTE: The finish shall include the package and entire exposed lead area from meniscus to the lead tip (excluding the sheared off tip itself) and all other exposed metal surfaces.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

* a. Initial measurements and conditions, if other than room ambient (see 3.1 and 3.2).

b. Applied voltage, when applicable (see 3.5), and bias configuration, when required. This bias configuration shall be chosen in accordance with the following guidelines:

(1) Only one supply voltage (V) either positive or negative is required, and an electrical ground (GND) or common terminal. The magnitude of V will be the maximum such that the specified absolute maximum ratings are not exceeded and test conditions are optimized.

(2) All normally specified voltage terminals and ground leads shall be connected to GND, unless otherwise specified.

(3) All data inputs, unless otherwise specified, shall be connected to V. The polarity and magnitude of V is chosen to minimize internal power dissipation and current flow into the device. All extender inputs shall be connected to GND, unless otherwise specified.

(4) All additional leads, e.g., clock, set, reset, outputs, etc., considered individually, shall be connected to V or GND whichever minimizes current flow.

(5) Leads with no internal connection shall be biased to V or GND whichever is opposite to an adjacent lead.

c. Final measurements (see 3.7). Final measurements shall include all electrical characteristics and parameters which are specified as end-point electrical parameters.

d. Number of cycles, if other than 10 (see 3.3).

e. Conditioning in dry oven before initial measurements, if required (see 3.2).

FIGURE 1004-1. Graphical representation of moisture-resistance test.

METHOD 1005.8

STEADY-STATE LIFE

1. PURPOSE. The steady-state life test is performed for the purpose of demonstrating the quality or reliability of devices subjected to the specified conditions over an extended time period. Life tests conducted within rated operating conditions should be conducted for a sufficiently long test period to assure that results are not characteristic of early failures or "infant mortality," and periodic observations of results should be made prior to the end of the life test to provide an indication of any significant variation of failure rate with time. Valid results at shorter intervals or at lower stresses require accelerated test conditions or a sufficiently large sample size to provide a reasonable probability of detection of failures in the sample corresponding to the distribution of potential failures in the lot(s) from which the sample was drawn. The test conditions provided in 3 below are intended to reflect these considerations.

When this test is employed for the purpose of assessing the general capability of a device or for device qualification tests in support of future device applications requiring high reliability, the test conditions should be selected so as to represent the maximum operating or testing (see test condition F) ratings of the device in terms of electrical input(s), load and bias and the corresponding maximum operating or testing temperature or other specified environment.

2. APPARATUS. Suitable sockets or other mounting means shall be provided to make firm electrical contact to the terminals of devices under test in the specified circuit configuration. Except as authorized by the acquiring or qualifying activity, the mounting means shall be so designated that they will not remove internally-dissipated heat from the device by conduction, other than that removed through the device terminals, the necessary electrical contacts and the gas or liquid chamber medium. The apparatus shall provide for maintaining the specified biases at the terminals of the device under test and, when specified, monitoring of the input excitation or output response. Power supplies and current-setting resistors shall be capable of maintaining the specified operating conditions as minimal throughout the testing period, despite normal variations in source voltages, ambient temperatures, etc. When test conditions result in significant power dissipation, the test apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. The test circuits need not compensate for normal variations in individual device characteristics, but shall be so arranged that the existence of failed or abnormal (i.e., open, short, etc.) devices in a group does not negate the effect of the test for other devices in the group.

3. PROCEDURE. The microelectronic devices shall be subjected to the specified test condition (see 3.5) for the specified duration at the specified test temperature, and the required measurements shall be made at the specified intermediate points and end points. QML manufactures who are certified and qualified to MIL-PRF-38535 may modify the time or the condition independently from the regression conditions contained in table I or the test condition/circuit specified in the device specification or standard microcircuit drawing provided the modification is contained in the manufacturer's QM plan and the "Q" certification identifier is marked on the devices. Lead-, stud-, or case-mounted devices shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified ambient temperature. The test condition, duration, sample size, and temperature selected prior to test shall be recorded and shall govern for the entire test. Test boards shall not employ load resistors which are common to more than one device, or to more than one output pin on the same device.

3.1 Test duration.

3.1.1 Test duration - standard life. The life test duration shall be 1,000 hours minimum at 125°C , unless otherwise specified or allowed (see 3.2.1). After the specified duration of the test, the device shall be removed from the test conditions and allowed to reach standard test conditions. Where the purpose of this test is to demonstrate compliance with a specified lambda (8), the test may be terminated at the specified duration or at the point of rejection if this occurs prior to the specified test duration.

3.1.2 Accelerated life test duration. For class level B, the life test duration, when accelerated, shall be the time equivalent to 1,000 hours at 125°C for the ambient temperature selected or specified (see table I). Within 72 hours after the specified duration of the test, the device shall be removed from the specified test conditions and allowed to reach standard test conditions without removal of bias. The interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed shall not be considered removal of bias.

3.2 Test temperature. The specified test temperature is the minimum ambient temperature to which all devices in the working area of the chamber shall be exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other suitable gas or liquid chamber medium. Therefore, calibration shall be accomplished in the chamber in a fully loaded, (boards need not be loaded with devices) unpowered configuration, and the indicator sensor located at, or adjusted to reflect, the coldest point in the working area.

3.2.1 Test temperature - standard life. Unless otherwise specified, the ambient life test temperature shall be 125°C minimum for test conditions A through E (see 3.5), except that for hybrid microcircuits, the conditions may be modified in accordance with table I. At the supplier's option, the ambient temperature for conditions A through E may be increased and the test duration reduced in accordance with table I using the specified test circuit and bias conditions. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that maximum rated case or junction temperatures for test or operation shall not exceed 200°C for class level B or 175°C for class level S (see 3.2.1.1).

3.2.1.1 Test temperature for high power devices. Regardless of power level, devices shall be able to be burned in or life-tested at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C, and where the ambient temperature would cause T_J to exceed +200°C (+175°C for class level S), the ambient operating temperature may be reduced during burn-in and life test from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

3.2.1.2 Test temperature for hybrid devices. The ambient or case life test temperature shall be as specified in table I, except case temperature life test shall be performed, as a minimum, at the maximum operating case temperature (T_C) specified for the device. Life test shall be for 1,000 hours minimum for class level S hybrid (class K). The device should be life tested at the maximum specified operating temperature, voltage, and loading conditions as specified in the detail specification. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that the maximum rated junction temperature as specified in the device specification or drawing and the cure temperature of polymeric materials as specified in the baseline documentation shall not be exceeded. If no maximum junction temperature is specified, a maximum of 175°C is assumed. Accelerated life test (condition F) shall not be permitted. The specified test temperature shall be the minimum actual ambient or case temperature that must be maintained for all devices in the chamber. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments and the flow of air or other suitable gas or liquid chamber medium.

3.2.2 Test temperature - accelerated life. When condition F is specified or is utilized as an option (when allowed by the applicable acquisition documents), the minimum ambient test temperature shall be +175°C , unless otherwise specified. Since accelerated testing will normally be performed at temperatures higher than the maximum rated operating junction temperature of the device(s) tested, care shall be taken to ensure that the device(s) does not go into thermal runaway.

3.2.3 Special considerations for devices with internal thermal limitation using test conditions A through E. For devices with internal thermal shutdown, extended exposure at a temperature in excess of the shut-down temperature will not provide a realistic indicator of long-term operating reliability. For devices equipped with thermal shutdown, operating life test shall be performed at an ambient temperature where the worst case junction temperature is at least 5°C below the worst case thermal shutdown threshold. Data supporting the defined thermal shutdown threshold shall be available to the preparing or acquiring activity upon request.

3.3 Measurements.

3.3.1 Measurements for test temperatures less than or equal to 150°C. Unless otherwise specified, all specified intermediate and end-point measurements shall be completed within 96 hours after removal of the device from the specified test conditions (i.e., either removal of temperature or bias). If these measurements cannot be completed within 96 hours, the devices shall be subjected to the same test condition (see 3.5) and temperature previously used for a minimum of 24 additional hours before intermediate or end-point measurements are made. When specified (or at the manufacturer's discretion, if not specified), intermediate measurements shall be made at 168 (+72, -0) hours and at 504 (+168, -0) hours. For tests in excess of 1,000 hours duration, additional intermediate measurement points, when specified, shall be 1000 (+168, -24) hours, 2,000 (+168, -24) hours, and each succeeding 1,000 (+168, -24) hour interval. These intermediate measurements shall consist of the parameters and conditions specified, including major functional characteristics of the device under test, sufficient to reveal both catastrophic and degradation failures to specified limits. Devices shall be cooled to less than 10°C of their power stable condition at room temperature prior to the removal of bias.

The interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed shall not be considered removal of bias. Alternatively, except for linear or MOS (CMOS, NMOS, PMOS, etc.) devices or unless otherwise specified, the bias may be removed during cooling, provided the case temperature of the devices under test is reduced to a maximum of 35°C within 30 minutes after removal of the test conditions and provided the devices under test are removed from the heated chamber within five minutes following removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the device(s).

3.3.2 Measurements for test temperatures greater than or equal to 175°C. Unless otherwise specified, all specified intermediate and end-point measurements shall be completed within 24 hours after removal of the device from the specified test conditions (i.e., either removal of temperature or bias). If these measurements cannot be completed within 24 hours, the steady-state life test shall be repeated using the same test condition, temperature and time. Devices shall be cooled to less than 10°C of their power stable condition at room temperature prior to the removal of bias, except that the interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions shall not be considered removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the device(s).

3.3.3 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, (once every 6 months or just prior to use if not used during the 6 month period) each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Board capacitance or resistance required to ensure stability of devices under test shall be checked during these initial and periodic verification tests to ensure they will perform their proper function (i.e., that they are not open or shorted). Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the devices under test.

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the oven, and brought up to at least 125°C or the specified test temperature, whichever is less, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. This may be performed by opening the oven for a maximum of 10 minutes. When the test conditions are checked at a test socket, contact points on the instrument used to make this continuity check shall be equal to or smaller dimensions than the leads (contacts) of the devices to be tested and shall be constructed such that the socket contacts are not disfigured or damaged.

c. At the conclusion of the test period, prior to removal of devices from temperature and test conditions, the voltage and signal condition verification of b. above shall be repeated.

d. For class level S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified test conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s). An approved alternate procedure may be used.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration (see 3.1), the test time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration whether or not the chamber is at temperature during the final 24 hours of life test shall require extension of the test duration for an uninterrupted 24 hours minimum, after the last bias interruption.

3.4 Test sample. The test sample shall be as specified (see 4). When this test method is employed as an add-on life test for a series or family of device types, lesser quantities of any single device type may be introduced in any single addition to the total sample quantity, but the results shall not be considered valid until the minimum sample size for each device has been accumulated. Where all or part of the samples previously under test are extracted upon addition of new samples, the minimum sample size for each type shall be maintained once that level is initially reached and no sample shall be extracted until it has accumulated the specified minimum test hours (see 3.1).

3.5 Test conditions.

3.5.1 Test condition A, steady-state, reverse bias. This condition is illustrated on figure 1005-1 and is suitable for use on all types of circuits, both linear and digital. In this test, as many junctions as possible will be reverse biased to the specified voltage.

3.5.2 Test condition B, steady-state, forward bias. This test condition is illustrated on figure 1005-1 and can be used on all digital type circuits and some linear types. In this test, as many junctions as possible will be forward biased as specified.

3.5.3 Test condition C, steady-state, power and reverse bias. This condition is illustrated on figure 1005-1 and can be used on all digital type circuits and some linear types where the inputs can be reverse biased and the output can be biased for maximum power dissipation or vice versa.

3.5.4 Test condition D, parallel excitation. This test condition is typically illustrated on figure 1005-2 and is suitable for use on all circuit types. All circuits must be driven with an appropriate signal to simulate, as closely as possible, circuit application and all circuits shall have maximum load applied. The excitation frequency shall not be less than 60 Hz.

3.5.5 Test condition E, ring oscillator. This test condition is illustrated on figure 1005-3, with the output of the last circuit normally connected to the input of the first circuit. The series will be free running at a frequency established by the propagation delay of each circuit and associated wiring and the frequency shall not be less than 60 Hz. In the case of circuits which cause phase inversion, an odd number of circuits shall be used. Each circuit in the ring shall be loaded to its rated maximum. While this condition affords the opportunity to continuously monitor the test for catastrophic failures (i.e., ring stoppage), this shall not be considered acceptable as a substitute for the intermediate measurements (see 3.3).

• 3.5.6 Test condition F, (class level B only) temperature-accelerated test. In this test condition, microcircuits are subjected to bias(es) at an ambient test temperature (175°C to 300°C) which considerably exceeds their maximum rated temperature. At higher temperatures, it is generally found that microcircuits will not operate normally, and it is therefore necessary that special attention be given to the choice of bias circuits and conditions to assure that important circuit areas are adequately biased without damaging overstresses to other areas of the circuit. To properly select the actual biasing conditions to be used, it is recommended that an adequate sample of devices be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the specified circuit and the applied electrical stresses do not induce damaging overstresses.

At the manufacturer's option, alternate time and temperature values may be established from table I. Any time-temperature combination which is contained in table I within the time limit of 30 to 1,000 hours may be used. The life test ground rules of 3.5 of method 1016 shall apply to life tests conducted using test condition F. The applied voltage at any or all terminals shall be equal to the voltage specified for the 125°C operating life in the applicable acquisition document, unless otherwise specified.

If necessary, with the specific approval of the qualifying activity, the applied voltage at any or all terminal(s) may be reduced to not less than 50 percent of the specified value(s) when it is demonstrated that excessive current flow or power dissipation would result from operation at the specified voltage(s). If the voltage(s) is so reduced, the life test duration shall be determined by the following formula:

$$T_a = \frac{t_o\,(100\%)}{100\% - V\%}$$

Where T_a is the adjusted total test duration in hours, t_o is the original test duration in hours, and V percent is the largest percentage of voltage reduction made in any specified voltage.

* 3.5.6.1 Special considerations for devices with internal thermal limitation. For devices with internal thermal shutdown, extended exposure at a temperature in excess of the shut-down temperature will not provide a realistic indicator of long-term operating reliability. For such devices, measurement of the case temperature should be made at the specified bias voltages at several different ambient temperatures. From these measurements, junction temperatures should be computed, and the operating life shall be performed at that ambient temperature which, with the voltage biases specified, will result in a worst case junction temperature at least 5°C but no more than 10°C below the minimum junction temperature at which the device would go into thermal shutdown, and the test time shall be determined from table I for the applicable device class level.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Special preconditioning, when applicable.

b. Test temperature, and whether ambient, junction, or case, if other than as specified in 3.2.

c. Test duration, if other than as specified in 3.1.

d. Test mounting, if other than normal (see 3).

e. Test condition letter.

f. End-point measurements and intermediate measurements (see 3.3).

g. Criteria for device failure for intermediate and end-point measurements (see 3.3), if other than device specification limits, and criteria for lot acceptance.

h. Test sample (see 3.4).

i. Time to complete end-point measurements, if other than as specified (see 3.3).

j. Authorization for use of condition F and special maximum test rating for condition F, when applicable (see 4.b).

k. Time temperature conditions for condition F, if other than as specified in 3.5.6.

TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	—	"
135	800	496	—	"
140	700	352	—	"
145	600	256	—	"
150	500	184	—	"
175		40	—	F
180		32	—	"
185		31	—	"
190		30	—	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

FIGURE 1005-1. Steady-state.

FIGURE 1005-2. Typical parallel, series excitation.

NOTE: For free running counter, N is an odd number and the output of N is connect to the input of 1.

FIGURE 1005-3. Ring oscillator.

METHOD 1006

INTERMITTENT LIFE

1. PURPOSE. The intermittent life test is performed for the purpose of determining a representative failure rate for microelectronic devices or demonstrating quality or reliability of devices subjected to the specified conditions. It is intended for applications where the devices are exposed to cyclic variations in electrical stresses between the "on" and "off" condition and resultant cyclic variations in device and case temperatures.

2. APPARATUS. See method 1005 of this standard.

3. PROCEDURE. The device shall be tested in accordance with all the requirements of method 1005 except that all electrical stresses shall be alternately applied and removed. The "on" and "off" periods shall be initiated by sudden, not gradual, application or removal of the specified electrical inputs (including signal and bias).

4. SUMMARY. In addition to the requirements of method 1005 of this standard, the following detail shall be specified in the applicable acquisition document:

Frequency and duration of "on" and "off" cycles.

METHOD 1007

AGREE LIFE

1. PURPOSE. The purpose of this test is to determine a representative failure rate for microelectronic devices or to demonstrate quality or reliability of devices subjected to the specified conditions where test conditions include a combination of temperature cycling, on-off electrical stressing and vibration to simulate as closely as possible actual system applications and environments.

2. APPARATUS. The apparatus required shall be described in method 1005 of this standard except that the temperature chambers shall be capable of following the specified test profile of figures 1 or 2 of MIL-STD-781 and suitable equipment shall be provided to satisfy the requirements for vibration as specified.

3. PROCEDURE. This test shall be conducted in accordance with all the requirements of method 1005 of this standard with the exceptions that temperature shall be cycled, periodic vibration shall be applied, and electrical stresses shall be applied in on-off cycles where and as required in the specified test level of MIL-STD-781. Only test levels E, F, G, H and J of MIL-STD-781 shall be considered acceptable as test conditions. Selection of the temperature range should take into account the temperature rise associated with the devices under test.

Test conditions for method 1007	Test level in accordance with MIL-STD-781	Temperature range °C
A	E	-54 to +55
B	F	-54 to +71
C	G	-54 to +95
D	H	-65 to +71
E	J	-54 to +125
F	Test level F with modified low temperature	0 to +70

4. SUMMARY. In addition to the requirements of method 1005 of this standard, the following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Test profile, specify figure 1 or 2 MIL-STD-781 and specify on-time and transfer-times, as applicable.

c. Total on-time.

METHOD 1008.2

STABILIZATION BAKE

1. PURPOSE. The purpose of this test is to determine the effect on microelectronic devices of storage at elevated temperatures without electrical stress applied. This method may also be used in a screening sequence or as a preconditioning treatment prior to the conduct of other tests. This test shall not be used to determine device failure rates for other than storage conditions. It may be desirable to make end point and, where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanisms with time and temperature.

2. APPARATUS. The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature and suitable electrical equipment to make the specified end point measurements.

3. PROCEDURE. The device shall be stored at the specified ambient conditions for the specified time. The time at high temperature shall be sufficient to allow the total mass of each device under test to reach the specified temperature before the specified time duration begins. Within the time interval of 24 hours before (0 hours before test durations less than 250 hours) to 72 hours after the specified duration of the test, the device shall be removed from the specified ambient test condition and allowed to reach standard test conditions. When specified, end-point measurements shall be completed within 96 hours after removal of device from the specified ambient test condition. When specified (or at the manufacturer's discretion, if not specified) intermediate measurements shall be made at intermediate points.

3.1 Test condition. The ambient test temperature shall be indicated by specifying a test condition letter from the following table. The specified test temperature is the minimum actual ambient temperature to which all devices in the working area of the chamber are exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other chamber atmosphere. Therefore, calibration, shall be accomplished on the chamber in a fully, loaded, unpowered configuration, and the indicator sensor located at, or adjusted to reflect, the coldest point in the working area. Unless otherwise specified, test condition C minimum, with a minimum time duration and temperature as specified in table I, shall apply. Unless otherwise specified, the test duration for all other test conditions shall be 24 hours minimum.

Test condition	Temperature (minimum)
A	75°C
B	125°C
C	See table I
D	200°C
E	250°C
F	300°C
G	350°C
H	400°C

TABLE I. Stabilization bake time temperature regression.

Minimum temperature	Minimum time (hours)
°C	Equivalent test condition C duration 1/
100 2/	1,000
125 2/	168
150	24
155	20
160	16
165	12
170	8
175	6
200	6

1/ The only allowed conditions are as stated above.
2/ These time-temperature combinations may be used for hybrid microcircuits only.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter if other than test condition C (see 3.1).

b. Test duration if other than 24 hours (see 3.1).

c. End point measurements, if applicable (see 3).

d. Intermediate measurements, if applicable (see 3).

e. Maximum test temperature rating, if applicable.

METHOD 1009.8

SALT ATMOSPHERE (CORROSION)

1. PURPOSE. This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmosphere on devices and package elements.

1.1 Terms and definitions.

1.1.1 Corrosion. Corrosion is the deterioration of coating or base metal or both by chemical or electrochemical action.

1.1.2 Corrosion site. A corrosion site is the site at which the coating or base metal or both is corroded. The location of corrosion.

1.1.3 Corrosion product (deposit). The effect of corrosion (i.e., rust or iron oxide, nickel oxide, tin oxide, etc.). The product of corrosion may be at the corrosion site, or may flow or run (due to action of liquid carrier of salt) so as to cover noncorroded areas.

1.1.4 Corrosion stain. Corrosion stain is a semitransparent deposit due to corrosion products.

1.1.5 Blister. A blister is a localized swelling and separation between the coating(s) and base metal.

1.1.6 Pinhole. A pinhole is a small hole occurring in the coating as an imperfection which penetrates entirely through the coating.

1.1.7 Pitting. Pitting is the localized corrosion of coating or base metal or both, confined to a point or small area, that takes the form of cavities.

1.1.8 Flaking. Flaking is the separation of small pieces of coating that exposes the base metal.

2. APPARATUS. Apparatus used in the salt-atmosphere test shall include the following:

a. Exposure chamber with fixtures for supporting devices. The chamber and all accessories shall be made of material (glass, plastic, etc.) which will not affect the corrosiveness of the salt atmosphere. All parts within the test chamber which come in contact with test specimens shall be of materials that will not cause electrolytic corrosion. The chamber shall be properly vented to prevent pressure build-up and allow uniform distribution of salt fog.

b. Salt solution reservoir adequately protected from the surrounding ambient. If necessary, auxiliary reservoirs may be used for long duration tests in accordance with test conditions C and D (see 3.2).

c. Means for atomizing the salt solution, including suitable nozzles and compressed air or a 20 percent oxygen, 80 percent nitrogen mixture (the gas entering the atomizers shall be free from all impurities such as oil and dirt).

d. Chamber-heating means and controls.

e. Means for humidifying the air at temperature above the chamber temperature.

f. Air or inert gas dryer.

g. Magnifier(s) 1X to 3X, 10X to 20X and 30X to 60X.

3. PROCEDURE.

3.1 Maintenance and conditioning of test chamber. The purpose of the cleaning cycle is to assure that all materials which could adversely affect the results of the subsequent tests are removed from the chamber. The chamber shall be cleaned by operating it at 95°F ±5°F (35°C ±3°C) with deionized or distilled water as long as necessary. The chamber shall be cleaned each time the salt solution in the reservoir has been used up. Several test runs therefore could be run before cleaning, depending on the size of the reservoir and the specified test condition (see 3.2). When long duration conditions (test conditions C and D, see 3.2) are required, the reservoir may be refilled via auxiliary reservoirs so that the test cycle shall not be interrupted. After the cleaning cycle, on restarting the chamber, the reservoir shall be filled with salt solution and the chamber shall be stabilized by operating it until the temperature comes to equilibrium, see 3.1.4. If operation of the chamber is discontinued for more than one week, the remaining salt solution, if any, shall be discarded. Cleaning shall then be performed prior to restarting the test chamber. Intermittent operation of the chamber is acceptable provided the pH and concentration of the salt solution are kept within limits defined in 3.1.1.

3.1.1 Salt solution. The salt concentration shall be 0.5 to 3.0 percent by weight in deionized or distilled water as required to achieve the deposition rates required by 3.1.4. The salt used shall be sodium chloride containing on the dry basis not more than 0.1 percent by weight of sodium iodide and not more than 0.3 percent by weight total impurities. The pH of the salt solution shall be maintained between 6.5 and 7.2 when measured at 95°F ±5°F (35°C ±3°C). Only CP grade (dilute solution) hydrochloric acid or sodium hydroxide shall be used to adjust the pH.

3.1.2 Preconditioning of leads. Unless otherwise specified, the test specimens shall not be preconditioned. If required (see 4.c.), prior to mounting specimens for the salt atmosphere test, the device leads shall be subjected to the bending stress initial conditioning in accordance with test condition B1 of method 2004. Where the specific sample devices being subjected to the salt atmosphere test have already been subjected to the required initial conditioning, as part of another test employing the same sample devices, the lead bend need not be repeated.

3.1.3 Mounting of test specimens. The test specimens shall be mounted on the holding fixtures (plexiglass rods, nylon or fiberglass screens, nylon cords, etc.) in accordance with the applicable orientation(s) below. Specimens shall also be positioned so that they do not contact each other, so that they do not shield each other from the freely settling fog, and so that corrosion products and condensate from one specimen does not fall on another.

a. Dual-in-line packages with leads attached to, or exiting from, package sides (such as side-brazed packages and ceramic dual-in-line packages): Lid upward 15° to 45° from vertical. One of the package sides on which the leads are located shall be oriented upward at an angle greater than or equal to 15° from vertical (see figure 1009-1a).

b. Packages with leads attached to, or exiting from the opposite side of the lid (such as TO cans, solid sidewall packages, and metal platform packages): Lid 15° to 45° from vertical. One-half of the samples shall be tested with the lid upward; the remaining samples shall be tested with the leads upward (see figure 1009-1b). For packages with leads attached to, or exiting from the same side as the lid, only one orientation (lid and leads upward) is required.

c. Packages with leads attached to, or exiting from package sides, parallel to the lid (such as flatpacks): Lid 15° to 45° from vertical. One of the package sides on which the leads are located shall be oriented upward at an angle greater than or equal to 15° from vertical. For packages with a metal case, one-half of the samples shall be tested with the lid upward; the remaining samples shall be tested with the case upward. All other packages shall be tested with the lid upward (see figure 1009-1c).

d. Leadless and leaded chip carriers: Lid 15° to 45° from vertical. One-half of the samples shall be tested with the lid upward; the remaining samples shall be tested with the lid downward (see figure 1009-1d).

e. Flat specimens (e.g., lids only and lead frames only): 15° to 45° from vertical.

NOTE: In cases where two orientations are required for testing, the specified sample size shall be divided in half (or as close to one-half as possible). In all cases, inspections following the test in accordance with 3.4 shall be performed on all package surfaces.

NOTE: Precautions may be used to prevent light induced photovoltaic electrolytic effects when testing windowed UV erasable devices.

3.1.4 Chamber operation. After conditioning of test chamber in accordance with 3, a salt fog having a temperature of 95°F minimum (35°C minimum) shall be passed through the chamber for the specified test duration (see 3.2). The exposure zone of the chamber shall be maintained at a temperature of 95°F ±5°F (35°C ±3°C). The fog concentration and velocity shall be so adjusted that the rate of salt deposit in the test area is between 20,000 and 50,000 mg/m²/24 hours. Rate of salt deposit may be determined by either volumetric, gravimetric, or other techniques at the user's option. The salt solution collecting at the bottom of the chamber shall be discarded.

3.2 Length of test. The minimum duration of exposure of the salt atmosphere test shall be specified by indicating a test condition letter from the following table. Unless otherwise specified, test condition A shall apply:

Test condition	Length of test
A	24 hours
B	48 hours
C	96 hours
D	240 hours

3.3 Preparation of specimens for examination. Upon completion of the salt exposure test, the test specimens shall be immediately washed with free flowing deionized water (not warmer than 100°F (38°C) for at least 5 minutes to remove salt deposits from their surface after which they shall be dried with air or inert gas, and subjected to the inspections below.

3.4 Failure criteria. All inspections shall be performed at a magnification of 10X to 20X, unless otherwise specified in this procedure (see 3.4.1b and 3.4.1c).

NOTES:

1. Corrosion stains shall not be considered as part of the defective area of 3.4.1a.

2. Corrosion products resulting from lead corrosion that deposit onto areas other than the lead shall not be considered as part of the defective area of 3.4.1a.

3. Corrosion at the tips of the leads and corrosion products resulting from such corrosion shall be disregarded.

4. Portions of leads which cannot be further tested in accordance with 3.4.1b, due to geometry or design (such as standoffs on pin grid arrays or the brazed portion of leads on side-brazed packages), shall be subject to the failure criteria of 3.4.1a.

3.4.1 Finished product. No device is acceptable that exhibits:

a. Corrosion defects over more than 5 percent of the area of the finish or base metal of any package element other than leads such as lid, cap, or case. Corrosion defects to be included in this measurement are: Pitting, blistering, flaking, and corrosion products. The defective area may be determined by: Comparison with charts or photographs of known defective areas (see figure 1009-2), direct measurement using a grid or similar measuring device, or image analysis.

b. Leads missing, broken, or partially separated. In addition, any lead which exhibits pinholes, pitting, blistering, flaking, corrosion product that completely crosses the lead, or any evidence of pinholes, pitting, blistering, flaking, corrosion product, or corrosion stain at the glass seal shall be further tested as follows:

Bend the lead through 90° at the point of degradation in such a manner that tensile stress is applied to the defect region. Any lead which breaks or shows fracture of the base metal through greater than 50 percent of the cross-sectional area of the lead shall be considered a reject. In the case of multiple defects the bend shall be made at the site exhibiting the worst case corrosion. On packages exhibiting defects on more than ten leads, bends shall be made on a maximum of ten leads exhibiting the worst case corrosion. The examination of the fracture shall be performed with a magnification of 30X to 60X.

c. Specified markings, which are missing in whole or in part, faded, smeared, blurred, shifted, or dislodged to the extent that they are not legible. This examination shall be conducted with normal room lighting and with a magnification of 1X to 3X.

3.4.2 Package elements. When this test is performed on package elements or partially assembled packages during incoming inspection or any time prior to completion of package assembly as an optional quality control gate or as a required test (see 4.d), no part is acceptable that exhibits:

a. Corrosion defects over more than 1.0 percent of the area of the finish or base metal of lids or over more than 2.5 percent of the area of the finish or base metal of any other package element other than leads (such as case). Corrosion on areas of the finish or base metal that will not be exposed to surrounding ambient after device fabrication shall be disregarded. This inspection shall be performed according to the procedure in 3.4.1a.

b. Leads with final lead finish that are rejectable in accordance with 3.4.1b.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test duration, if other than test condition A (see 3.2).

b. Measurements and examinations after test, when applicable for other than visual (see 3.4).

c. Requirement for preconditioning, if applicable, and procedure if other than in 3.1.2.

d. Requirement for incoming inspection of package elements or partially assembled packages (see 3.4.2), when applicable.

FIGURE 1009-1a. Dual-in-line packages with leads attached to, or exiting from package sides (such as side-brazed packages and ceramic dual-in-line packages):

FIGURE 1009-1b. Packages with leads attached to, or exiting from opposite sides of lids (such as TO cans, solid sidewall packages, metal platform packages, and pin grid arrays):

1. TO cans:

a. Expose one-half of samples with caps upward:

b. Expose other one-half of samples with leads upward:

FIGURE 1009-1. Example sample orientations.

2. Solid sidewall packages, metal platform packages, and pin grid arrays:

   a. Expose one-half of samples with lids upward:

   b. Expose other one-half of samples with leads upward:

FIGURE 1009-1c. Packages with leads attached to, or exiting from package sides, parallel to lid (such as flatpacks):

NOTE: If the case is metal, one-half of the samples shall be tested with the lids exposed upward, the other one-half with the cases exposed upward.

FIGURE 1009-1. Example sample orientations - Continued.

FIGURE 1d. Leadless or leaded chip carriers:

1. Expose one-half of samples with lids upward:

2. Expose other one-half of samples with lids downward:

FIGURE 1009-1. Example sample orientations - Continued.

FIGURE 1009.2. Corrosion area charts.

METHOD 1010.7

TEMPERATURE CYCLING

1. PURPOSE. This test is conducted to determine the resistance of a part to extremes of high and low temperatures, and to the effect of alternate exposures to these extremes.

1.1 Terms and definitions.

1.1.1 Load. The specimens under test and the fixtures holding those specimens during the test. Maximum load shall be determined by using the worst case load temperature with specific specimen loading. Monolithic loads used to simulate loading may not be appropriate when air circulation is reduced by load configuration. The maximum loading must meet the specified conditions.

1.1.2 Monitoring sensor. The temperature sensor that is located and calibrated so as to indicate the same temperature as at the worst case indicator specimen location. The worst case indicator specimen location is identified during the periodic characterization of the worst case load temperature.

1.1.3 Worst case load temperature. The temperature of specific specimens as indicated by thermocouples imbedded in their bodies. These indictor specimens shall be located at the center and at each corner of the load. The worst case load temperature is determined at periodic intervals.

1.1.4 Working zone. The volume in the chamber(s) in which the temperature of the load is controlled within the limits specified in table I.

1.1.5 Specimen. The device or individual piece being tested.

1.1.6 Transfer time. The elapsed time between specimen removal from one temperature extreme and introduction into the other.

1.1.7 Maximum load. The largest load for which the worst case load temperature meets the timing requirements (see 3.1).

1.1.8 Dwell time. The time from introduction of the load into the chamber until the load is transferred out of the chamber.

2. APPARATUS. The chamber(s) used shall be capable of providing and controlling the specified temperatures in the working zone(s) when the chamber is loaded with a maximum load. The thermal capacity and air circulation must enable the working zone and loads to meet the specified conditions and timing (see 3.1). Worst case load temperature shall be continually monitored during test by indicators or recorders reading the monitoring sensor(s). Direct heat conduction to specimens shall be minimized.

3. PROCEDURE. Specimens shall be placed in such a position with respect to the airstream that there is substantially no obstruction to the flow of air across and around the specimen. When special mounting is required, it shall be specified. The specimen shall then be subjected to the specified condition for the specified number of cycles performed continuously. This test shall be conducted for a minimum of 10 cycles using test condition C. One cycle consists of steps 1 and 2 or the applicable test condition and must be completed without interruption to be counted as a cycle. Completion of the total number of cycles specified for the test may be interrupted for the purpose of test chamber loading or unloading of device lots or as the result of power or equipment failure. However, if the number of interruptions for any reason exceeds 10 percent of the total number of cycles specified, the test must be restarted from the beginning.

3.1 Timing. The total transfer time from hot to cold or from cold to hot shall not exceed one minute. The load may be transferred when the worst case load temperature is within the limits specified in table I. However, the dwell time shall not be less than 10 minutes and the load shall reach the specified temperature within 15 minutes.

TABLE I. Temperature-cycling test conditions.

		Test condition temperature (°C)					
Step	Minutes	A	B	C	D	E	F
1 Cold	≥10	-55 +0 -10	-55 +0 -10	-65 +0 -10	-65 +0 -10	-65 +0 -10	-65 +0 -10
2 Hot	≥10	85 +10 -0	125 +15 -0	150 +15 -0	200 +15 -0	300 +15 -0	175 +15 -0

NOTE: Steps 1 and 2 may be interchanged. The load temperature may exceed the + or - zero (0) tolerance during the recovery time. Other tolerances shall not be exceeded.

3.2 Examination. After completion of the final cycle, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X. A visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X (except the magnification for examination shall be 1.5X minimum when this method is used for 100 percent screening). This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.3 Failure criteria. After subjection to the test, failure of one or more specified end-point measurements or examinations (see 4.d.), evidence of defects or damage to the case, leads, or seals or illegible markings shall be considered a failure. Damage to the marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Special mounting, if applicable (see 3).

b. Test condition letter, if other than test condition C (see 3).

c. Number of test cycles, if other than 10 cycles (see 3).

d. End-point measurements and examinations (see 3.1) (e.g., end-point electrical measurements, seal test (method 1014), or other acceptance criteria).

METHOD 1011.9

THERMAL SHOCK

1. PURPOSE. The purpose of this test is to determine the resistance of the part to sudden exposure to extreme changes in temperature and the effect of alternate exposures to these extremes.

1.1 Terms and definitions.

1.1.1 Cycle. A cycle consists of starting at ambient room temperature, proceeding to step 1, then to step 2, or alternately proceeding to step 2, then to step 1, and then back to ambient room temperature without interruption.

1.1.2 Dwell time. The total time the load is immersed in the bath.

1.1.3 Load. The devices under test and the fixture holding these devices.

1.1.4 Maximum load. The maximum mass of devices and fixtures that can be placed in the bath while maintaining specified temperatures and times.

1.1.5 Specimen. The device or individual piece being tested.

1.1.6 Transfer time. The elapsed time measured from removal of the load from one bath until insertion in the other bath.

1.1.7 Worst case load temperature. The body temperature of a specific device located at the center of the load.

1.1.8 Monitoring sensor. The temperature sensor that is located and calibrated so as to indicate the same temperature as at the worst case indicator specimen location. The worst case indicator specimen location is identified during the periodic characterization of the worst case load temperature.

2. APPARATUS. The baths used shall be capable of providing and controlling the specified temperatures in the working zone(s) when the bath is loaded with a maximum load. The thermal capacity and liquid circulation must enable the working zone and loads to meet the specified conditions and timing (see 3.1). Worst case load temperature shall be continually monitored during test by indicators or recorders reading the monitoring sensor(s). The worst case load temperature under maximum load conditions and configuration shall be verified as needed to validate bath performance. Perfluorocarbons that meet the physical property requirements of table II shall be used for conditions B and C.

3. PROCEDURE. Specimens shall be placed in the bath in a position so that the flow of liquid across and around them is substantially unobstructed. The load shall then be subjected to condition B or as otherwise specified (see 4b) of table I for a duration of 15 cycles. Completion of the total number of cycles specified for the test may be interrupted for the purpose of loading or unloading of device lots or as the result of power or equipment failure. However, if the number of interruptions for any given test exceeds 10 percent of the total number of cycles specified, the test must be restarted from the beginning.

3.1 Timing. The total transfer time from hot to cold or from cold to hot shall not exceed 10 seconds. The load may be transferred when the worst case load temperature is within the limits specified in table I. However, the dwell time shall be not less than 2 minutes and the load shall reach the specified temperature within 5 minutes.

3.2 Examination. After completion of the final cycle, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X except the magnification for examination shall be 1.5X minimum when this method is used for 100 percent screening. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of group, sequence, or subgroup of tests which include this test.

3.3 Failure criteria. After subjection to the test, failure of any specified end-point measurements or examinations (see 4d), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

TABLE I. Thermal shock temperature tolerances and suggested fluids. 1/

Test conditions		A	B	C
		Temperature	Temperature	Temperature
Step 1	Temperature tolerance, °C	100 +10 -2	125 +10 -0	150 +10 -0
	Recommended fluid	Water 2/	Perfluorocarbon 3/	Perfluorocarbon 3/
Step 2	Temperature tolerance, °C	-0 +2 -10	-55 +0 -10	-65 +0 -10
	Recommended fluid	Water 2/	Perfluorocarbon 3/	Perfluorocarbon 3/

1/ Ethylene glycol shall- not be used as a thermal shock test fluid.

2/ Water is indicated as an acceptable fluid for this temperature range. Its suitability chemically shall be established prior to use. When water is used as the fluid for condition A and the specified temperature tolerances are insufficient due to altitude considerations, the following alternate test conditions may be used:

a. Temperature: 100°C -6°C, 0°C +6°C.

b. Cycles shall be increased to 20.

3/ Perfluorocarbons contain no chlorine or hydrogen.

TABLE II. Physical property requirements of perfluorocarbon fluids. 1/

Test condition		B	C	ASTM test method
Step 1	Boiling point, °C	>125	>150	D1120
	Density at 25°C gm/ml	>1.6		D941
	Dielectric strength volts/mil	>300		D877
	Residue, microgram/gram	<50		D2109
	Appearance	Clear, colorless liquid		Not applicable
Step 2	Density at 25°C gm/ml	>1.6		D941
	Dielectric strength volts/mil	>300		D877
	Residue, micrograms/gram	<50		D2109
	Appearance	Clear, colorless liquid		Not applicable

1/ The perfluorocarbon used shall have a viscosity less than or equal to the thermal shock equipment manufacturer's recommended viscosity at the minimum temperature.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Special mounting, if applicable.

b. Test condition, if other than test condition B (see 3).

c. Number of test cycles, if other than 15 cycles (see 3).

d. End-point measurements and examinations (e.g., end-point electrical measurements, seal test (method 1014), or other acceptance criteria).

METHOD 1012.1

THERMAL CHARACTERISTICS

1. PURPOSE. The purpose of this test is to determine the thermal characteristics of microelectronic devices. This includes junction temperature, thermal resistance, case and mounting temperature and thermal response time of the microelectronic devices.

1.1 Definitions. The following definitions and symbols shall apply for the purpose of this test:

a. Case temperature, T_C, in °C. The case temperature is the temperature at a specified accessible reference point on the package in which the microelectronic chip is mounted.

b. Mounting surface temperature, T_M, in °C. The mounting surface temperature is the temperature of a specified point at the device-heat sink mounting interface (or primary heat removal surface).

c. Junction temperature, T_J, in °C. The term is used to denote the temperature of the semiconductor junction in the microcircuit in which the major part of the heat is generated. With respect to junction temperature measurements, $T_{J(Peak)}$ is the peak temperature of an operating junction element in which the current distribution is nonuniform, $T_{J(Avg)}$ is the average temperature of an operating junction element in which the current distribution is nonuniform, and $T_{J(Region)}$ is the temperature in the immediate vicinity within six equivalent radii (an equivalent radius is the radius of a circle having the same area as contained in a junction interface area) of an operating junction. In general $T_{J(Region)} \leq T_{J(Avg)} \leq T_{J(Peak)}$. If the current distribution in an operating junction element is uniform then $T_{J(Avg)} \leq T_{J(Peak)}$.

d. Thermal resistance, junction to specified reference point, $R_{\theta JR}$, in °C/W. The thermal resistance of the microcircuit is the temperature difference from the junction to some reference point on the package divided by the power dissipation P_D.

e. Power dissipation, P_D, in watts, is the power dissipated in a single semiconductor test junction or in the total package, $P_{D(Package)}$.

f. Thermal response time, t_{JR}, in seconds, is the time required to reach 90 percent of the final value of junction temperature change caused by the application of a step function in power dissipation when the device reference point temperature is held constant. The thermal response time is specified as $t_{JR(Peak)}$, $t_{JR(Avg)}$, or $t_{JR(Region)}$ to conform to the particular approach used to measure the junction temperature.

g. Temperature sensitive parameter, TSP, is the temperature dependent electrical characteristic of the junction-under test which can be calibrated with respect to temperature and subsequently used to detect the junction temperature of interest.

2. APPARATUS. The apparatus required for these tests shall include the following as applicable to the specified test procedures.

a. Thermocouple material shall be copper-constantan (type T) or equivalent, for the temperature range -180°C to +370°C. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and associated measuring system shall be ±0.5°C.

b. Controlled temperature chamber or heat sink capable of maintaining the specified reference point temperature to within ±0.5°C of the preset (measured) value.

c. Suitable electrical equipment as required to provide controlled levels of conditioning power and to make the specified measurements. The instrument used to electrically measure the temperature-sensitive parameter shall be capable of resolving a voltage change of 0.5 mV. An appropriate sample-and-hold unit or a cathode ray oscilloscope shall be used for this purpose.

d. Infrared microradiometer capable of measuring radiation in the 1 to 6 micrometer range and having the ability to detect radiation emitted from an area having a spatial resolution of less than 40 micrometers (1.6 mils) diameter at its half power points and a temperature resolution (detectable temperature change) of 0.5°C at 60°C.

NOTE: May be a scanning IR microradiometer.

e. A typical heat sink assembly for mounting the microelectronic device-under test is shown on figure 1012-1. The primary heat sink is water cooled and has a thermocouple sensor for inlet and outlet water temperature as shown in figure 1012-1a.

An adapter heat sink, as shown on figure 1012-1b is fastened to the top surface of the primary heat sink, and has a special geometry to handle specific size packages, e.g., flat packs, dual-in-line packages (small and large size) and TO-5 cans. This adapter provides a fairly repeatable and efficient interface between the package and the heat sink; the heat sink temperature is determined from a thermocouple peened into the underside of the adapter-near the package.

The adapter also contains the socket or other electrical interconnection scheme. In the case of the flat pack adapter heat sink, the package is dropped into a special slotted printed circuit board (PCB) to register the leads with runs on the PCB; toggle clamps then provide a pressure contact between the package leads and the PCB runs. Dual-in-line and axial lead packages plug into a regular socket.

The thermal probe assembly is shown on figure 1012-1b. In practice, the pressure adjustment cap is adjusted so the disk at the probe tip contacts the bottom surface of the package (chip carrier) with a predetermined force. A silicone grease (about 25-50 mm thick) is used at this interface to provide a reliable thermal contact.

3. PROCEDURE.

3.1 Direct measurement of reference point temperature, T_C or T_M. For the purpose of measuring a microelectronic device thermal resistance or thermal response time, the reference point temperature shall be measured at the package location of highest temperature which is accessible from outside the package. In general, that temperature shall be measured on the surface of the chip carrier directly below the chip. The location selected shall be as near the chip as possible and representative of a temperature in the major path of heat flow from the chip to the heat sink. The surface may be altered to facilitate this measurement provided that such alteration does not affect the original heat transfer paths and, hence, the thermal resistance, within the package by more than a few percent.

3.1.1 Case temperature, T_C. The microelectronic device under test shall be mounted on a temperature controlled heat sink so that the case temperature can be held at the specified value. A thermocouple shall be attached as near as possible to the center of the bottom of the device case directly under the chip or substrate. A conducting epoxy may be used for this purpose. In general, for ambient cooled devices, the case temperature should be measured at the spot with the highest temperature. The thermocouple leads should be electrically insulated up to the welded thermocouple bead. The thermocouple bead should be in direct mechanical contact with the case of the microelectronic device under test.

3.1.2 Mounting surface temperature, T_M. The mounting surface temperature is measured directly below the primary heat removal surface of the case. It is measured with a thermocouple at or near the mounting surface of the heat sink. A typical mounting arrangement is shown on figure 1012-2. The surface of the copper mounting base shall be nickel plated and free of oxides.

The thermocouple hole shall be drilled into the mounting base such that the thermocouple lead is directly below the area on the case of interest. It is recommended that the thermocouple be secured into the mounting base with a thermal conducting adhesive (or solder) and that particular attention be paid to minimizing air voids around the ball of the thermocouple. A thermal conducting compound (or adhesive) should be used at the interface of the mounting base and the device under test.

3.2 Thermal resistance, junction to specified reference point, $R_{\theta JR}$.

3.2.1 General considerations. The thermal resistance of a semiconductor device is a measure of the ability of its carrier or package and mounting technique to provide for heat removal from the semiconductor junction.

The thermal resistance of a microelectronic device can be calculated when the case temperature and power dissipation in the device, and a measurement of the junction temperature are known. The junction with the greatest power dissipation density (watts/mm^2) shall be selected for measurement since that junction will generally have the highest temperature on the chip. If the leads to that junction are not accessible and another junction is measured then it cannot be assured that the highest temperature on the chip will be measured. Direct measurement should be used in this case.

When making the test measurements indicated below, the package shall be considered to have achieved thermal equilibrium when the measured temperature difference, junction to case, reaches approximately 99 percent of its final value. The temperature difference at that time will change at a rate less than

$$\frac{d(T_J - T_C)}{dt} \leq \frac{0.03\,(T_J - T_C)}{t}$$

where t is the time after application of a power dissipation increment. The total time required for stabilization will typically be less than a minute.

3.2.2 Direct measurement of junction temperature for determination of $R_{\theta JR}$. The junction temperature of the thermally limiting element within the semiconductor chip can be measured directly using an infrared microradiometer. The cap or lid shall first be removed from the package to expose the active chip or device. The cavity shall not be covered with any IR transparent material unless the chip is extremely large and has an extremely poor heat conduction path to the chip carrier. The location of the junction to be measured should be referenced to a coordinate system on the chip so it can be relocated after coating the chip. The active area of the chip shall be coated uniformly with a thin layer (25-50 μm thick) of a known high emissivity ($\epsilon > 0.8$), low thermal conductivity material such as black pigmented lacquer. The package shall then be placed on a temperature controlled heat sink and the case or mounting surface temperature stabilized at the specified value. The microelectronic device under test shall then be operated at its rated power dissipation, the infrared microscope crosshairs focused on the junction and scanned back and forth slightly at that location to maximize the radiance measurement. That radiance measurement and the chip carrier temperature shall then be recorded. The power to the test package shall then be turned off and the chip carrier allowed to return to the specified case or mounting surface temperature. The emissivity of the coating over the junction region shall then be measured and the radiance from the operating junction region shall be converted to temperature using this emissivity value. (Note that this method assumes the emissivity of the coating material does not change appreciably with temperature. This assumption shall be valid if the results are to be accurate and repeatable.)

If the junction to be measured is not specified then the test shall proceed as above except that the IR microscope crosshairs shall be scanned over the whole active area of the chip to find and maximize the radiance measurement at the highest temperature junction region.
The minimum width or length of the junction area shall be greater than 5 times the half power diameter of the objective lens and greater than 5 times the thickness of the coating on the chip surface if this method is used to measure $T_{J(Peak)}$. For junction element diameters between 5 and 1 times the half power diameter of the IR microscope objective lens, some average junction temperature $T_{J(Avg)}$, where $T_{J(Region)} < T_{J(Avg)} < T_{J(Peak)}$, will be measured.

The following data shall be recorded for this test condition:

a. Peak or average junction temperature, $T_{J(Peak)}$ or $T_{J(Avg)}$.

b. Case or mounting surface temperature (usually 60°C ±0.5°C T_C, T_M).

c. Power dissipation, $P_{D(Package)}$, in the package.

d. Reference temperature measuring point.

e. Mounting arrangement.

f. Half power "spot" size of the IR microscope.

g. Thickness of the emissivity control coating (for $T_{J(Avg)}$ measurements only).

h. Minimum width or length of the junction measured (for $T_{J(Avg)}$ measurements only).

3.2.3 Indirect measurements of junction temperature for the determination of $R_{\theta JR}$. The purpose of the test is to measure the thermal resistance of integrated circuits by using particular semiconductor elements on the chip to indicate the device junction temperature.

In order to obtain a realistic estimate of the operating average junction temperature, $T_{J(Avg)}$, the whole chip or chips in the package should be powered in order to provide the proper internal temperature distribution. For other purposes though (see section 3.2.1), the junction element being sensed need only be powered. During measurement of the junction temperature the chip heating current shall be switched off while the junction calibration current remains stable. It is assumed that the calibration current will not affect the circuit operation; if so, then the calibration current must be switched on as the power is switched off.

The temperature sensitive device parameter is used as an indicator of an average junction temperature of the semiconductor element for calculations of thermal resistance. The measured junction temperature is indicative of the temperature only in the immediate vicinity of the element used to sense the temperature. Thus, if the junction element being sensed is also dissipating power with a uniform heating current distribution, then $T_{J(Avg)} \approx T_{J(Peak)}$ for that particular junction element. If the current distribution is not uniform then $T_{J(Avg)}$ is measured. If the junction element being sensed is in the immediate vicinity of the element dissipating power then $T_{J(Region)}$ will be measured. The heating power does not have to be switched off when $T_{J(Region)}$ is measured.

The temperature sensitive electrical parameters generally used to indirectly measure the junction temperature are the forward voltage of diodes, and the emitter-base and the collector-base voltages of bipolar transistors. Other appropriate temperature sensitive parameters may be used for indirectly measuring junction temperature for fabrication technologies that do not lend themselves to sensing the active junction voltages. For example, the substrate diode(s) in junction-isolated monolithic integrated circuits can be used as the temperature sensitive parameter for measurements of $T_{J(Region)}$. In this particular case though, the heating power has to be switched off at the same time that the substrate diode is forward biased.

3.2.3.1 Switching techniques for measuring $T_{J(Avg)}$. The following symbols shall apply for the purpose of these measurements:

I_M ----------	Measuring current in milliamperes.
V_{MD} ----------	Value of temperature-sensitive parameter in millivolts, measured at I_M, and corresponding to the temperature of the junction heated by P_D.
T_{MC} ----------	Calibration temperature in °C, measured at the reference point.
V_{MC} ----------	Value of temperature-sensitive parameter in millivolts, measured at I_M and specific value of T_{MC}.

The measurement of $T_{J(Avg)}$ using junction forward voltage as the TSP is made in the following manner:

Step 1 - Measurement of the temperature coefficient of the TSP (calibration).

The coefficient of the temperature sensitive parameter is generated by measuring the TSP as a function of the reference point temperature, for a specified constant measuring current, I_M, and collector voltage, by externally heating the device under test in an oven or on a temperature controlled heat sink. The reference point temperature range used during calibration shall encompass the temperature range encountered in the power application test (see step 2). The measuring current is generally chosen such that the TSP decreases linearly with increasing temperature over the range of interest and that negligible internal heating occurs during the measuring interval. A measuring current ranging from 0.05 to 5 mA is generally used, depending on the rating and operating conditions of the device under test, for measuring the TSP. The value of the TSP temperature coefficient, V_{MC}/T_{MC}, for the particular measuring current and collector voltage used in the test, is calculated from the calibration curve, V_{MC} versus T_{MC}.

Step 2 - Power application test.

The power application test is performed in two parts. For both portions of the test, the reference point temperature is held constant at a preset value. The first measurement to be made is that of the temperature sensitive parameter, i.e., V_{MC}, under operating conditions with the measuring current, I_M, and the collector voltage used during the calibration procedure. The microelectronic device under test shall then be operated with heating power (P_D) intermittently applied at greater than or equal to 99 percent duty factor. The temperature- sensitive parameter V_{MD} shall be measured during the interval between heating pulses ($\leq$100 µs) with constant measuring current, I_M, and the collector voltage that was applied during the calibration procedure (see step 1).

Because some semiconductor element cooling occurs between the time that the heating power is removed and the time that the temperature-sensitive parameter is measured, V_{MD} may have to be extrapolated back to the time where the heating power was terminated by using the following mathematical expression which is valid for the first 100 µs of cooling:

$$V_{MD}\ (t = 0) = V_{MD1} + \left[\frac{V_{MD2} - V_{MD1}}{t_1^{1/2} - t_2^{1/2}}\right] t_1^{1/2}$$

Where:

$V_{MD}(t = 0)$ = TSP, in millivolts, extrapolated to the time at which the heating power is terminated,
t = Delay time, in microseconds, after heating power is terminated,
V_{MD1} = TSP, in millivolts, at time $t = t_1$, and
V_{MD2} = TSP, in millivolts, at time $t = t_2 < t_1$.

If $V_{MD}(t)$ versus $t^{1/2}$ is plotted on linear graph paper for the first 100 µs of cooling, the generated curve will be a straight line except during the initial portion where nonthermal switching transients dominate. The time t_2 is the minimum time at which the TSP can be measured as determined from the linear portion of the $V_{MD}(t)$ versus $t^{1/2}$ cooling curve. Time t_1 should be at least equal to t_2 + 25 µs but less than 100 µs. The delay time before the TSP can be measured ranges from 1 to 50 µs for most microelectronic devices. This extrapolation procedure is valid for semiconductor (junction) sensing elements ≥0.2 mm (8 mils) in diameter over the delay time range of interest (1 to 50 µs).

When the error in the calculated thermal resistance caused by using V_{MD2} instead of the extrapolated value $V_{MD}(t = 0)$ exceeds 5 percent, the extrapolated value of V_{MD} shall be used for calculating the average junction temperature.

The heating power, P_D, shall be chosen such that the calculated junction-to- reference point temperature difference as measured at V_{MD2} is greater than or equal to 20°C. The values of V_{MD}, V_{MC}, and P_D are recorded during the power application test.

The following data shall be recorded for these test conditions:

a. Temperature sensitive electrical parameters (V_F, V_{EB} (emitter-only switching), V_{EB} (emitter and collector switching), V_{CB}, $V_{F(subst)}$, or other appropriate TSP).

b. Average junction temperature, $T_{J(Avg)}$, is calculated from the equation:

$$T_{J(AVG)} = T_R + (V_{MD} - V_{MC}) \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}$$

where: $T_R = T_C$ or T_M

c. Case or mounting surface temperature, T_C or T_M, (usually 60° ±0.5°C).

d. Power dissipation, P_D where $P_D = P_{D(Package)}$ or $P_{D(Element)}$.

e. Mounting arrangement.

3.2.3.2 Typical test circuits for indirect measurements of $T_{J(Avg)}$. The circuit on figure 1012-3 can be used to sense V_F, V_{EB}(emitter-only switches), V_{EB}(emitter and collector switching), and V_{CB}. The circuit is configured for heating power to be applied only to the junction element being sensed $P_{D(Element)}$ for illustration purposes only.

The circuit on figure 1012-3 is controlled by a clock pulse with a pulse width less than or equal to 100 µs and repetition rate less than or equal to 66.7 Hz. When the voltage level of the clock pulse is zero, the transistor Q1 is off and transistor Q2 is on, and the emitter current through the device under test (DUT) is the sum of the constant heating current and the constant measuring current. Biasing transistor Q1 on, shunts the heating current to ground and effectively reverse biases the diode D1. The sample-and-hold unit is triggered when the heating current is removed and is used to monitor the TSP of the device under test. During calibration, switch S4 is open.

The circuit on figure 1012-4 can be used to sense the forward voltage of the substrate diode of a junction isolated integrated circuit. In this test circuit the microelectronic device under test is represented by a single transistor operated in a common-emitter configuration. The substrate diode D_{SUBST} is shown connected between the collector (most positive terminal) and the emitter (most negative terminal) of the integrated circuit under test. The type of circuitry needed to interrupt the heating power will depend on the complexity of the integrated circuit being tested.
The circuit on figure 1012-4 is controlled by a clock pulse with a pulse width less than or equal to 100 µs and repetition rate less than or equal to 66.7 Hz. When the voltage level of the clock pulse is zero, transistor Q1 being off and transistor Q2 on, the device under test is dissipating heating power. Biasing transistor Q1 on and Q2 off, interrupts the heating power and forward biases the substrate diode. The sample-and-hold unit is triggered when the heating current is removed and is used to monitor the substrate diode forward voltage. During calibration, switch S1 is open.

3.3 Thermal response time, junction to specified reference point, t_{JR}.

3.3.1 General considerations. When a step function of power dissipation is applied to a semiconductor device, the junction temperature does not rise as a step function, but rather as a complex exponential curve. An infrared microradiometer or the electrical technique, in which a precalibrated temperature sensitive device parameter is used to sense the junction temperature, shall be used to generate the microelectronic device thermal response time.

When using electrical techniques, in which the device heating power is removed before the TSP is sensed for measuring the thermal response time, the cooling curve technique shall be used. The measurement of the cooling curve is performed by heating the device to steady state, switching the power off, and monitoring the junction temperature as the device cools. The cooling curve technique is based upon the assumption that the cooling response of a device is the conjugate of the heating response.

3.3.2 Measurement of junction temperature as a function of time for the determination of t_{JR}. The change in junction temperature as a function of time resulting from the application or removal of a step function of heating power dissipation in the junction(s) shall be observed using an infrared microradiometer with a response time of less than 100 µs, or electrical equipment with a response time of less than 100 µs and sufficient sensitivity to read a precalibrated temperature sensitive electrical parameter of the junction. During this test the device reference point temperature, as specified, shall be held constant, the step function of power dissipation shall be applied or removed, and the waveform of the junction temperature response versus time shall be recorded from the time of power application or removal to the time when the junction temperature reaches a stable value.

The following data shall be recorded for this test condition:

a. Temperature sensitive electrical parameter (see section 3.2.3).

b. Infrared microscope spatial resolution (see section 3.2.2).

c. Peak, average, or region junction temperature as a function of time (see section 3.2.2 or 3.2.3 for details).

d. Case or mounting surface temperature T_C or T_M (usually 60°C ±0.5°C).

e. Power dissipation, $P_{D(Package)}$ or $P_{D(Element)}$m in the package.

f. Reference temperature measuring point.

g. Mounting arrangement.

3.3.3 Typical test circuits for measurement of junction temperature as a function of time. The circuits depicted in section 3.2.3 are also used for the measurement of junction temperature as a function of time. The clock pulse is varied to give the required step of heating power and the TSP is monitored on a cathode ray oscilloscope. When an infrared microradiometer is used, the measuring current and TSP sensing circuitry is disconnected.

3.4 Calculations of $R_{\theta JR}$ and t_{JR}.

3.4.1 Calculations of package thermal resistance. The thermal resistance of a microelectronic device can be calculated when the peak junction, average junction, or region junction temperature, $T_{J(Peak)}$, $T_{J(Avg)}$, or $T_{J(Region)}$, respectively, has been measured in accordance with procedures outlined in sections 3.1 and 3.2. If the total package capability is to be assessed, then rated power $P_{D(Packages)}$ should be applied to the device under test. For quality control purposes the power dissipation in the single test junction $P_{H(Element)}$ can be used in the calculation of thermal resistance.

With the data recorded from each test, the thermal resistance shall be determined from:

$$R_{\theta JC(PEAK)} = \frac{T_{J(PEAK)} - T_C}{P_{D(Package)}}, \text{ junction peak-to-case;}$$

$$R_{\theta JC(Avg)} = \frac{T_{J(Avg)} - T_C}{P_{D(Package)}}, \text{ junction average-to-case; or}$$

$$R_{\theta JC(Region)} = \frac{T_{J(Region)} - T_C}{P_{D(Package)}}, \text{ junction region-to-case;}$$

For calculations of the junction element thermal resistance, $P_{D(Element)}$ should be used in the previous equations. Note that these thermal resistance values are independent of the heat sinking technique for the package. This is possible because the case or chip carrier (reference) temperature is measured on the package itself in an accessible location which provides a representative temperature in the major path of heat flow from the chip to the heat sink via the package.

3.4.2 Calculation of package thermal response time. The thermal response time of a microelectronic device can be calculated when the peak junction, average junction, or region junction temperature, $T_{J(Peak)}$, $T_{J(Avg)}$, or $T_{J(Region)}$, respectively, has been measured as a function of time in accordance with procedures outlined in section 3.3. If the total package capability is to be assessed, then rated power $P_{D(Package)}$ should be applied to the device under test. For quality control purposes the power dissipation in the single test junction $P_{D(Element)}$ can be used in the calculation of thermal response time.

With the data recorded from each test, the thermal response time shall be determined from a curve of junction temperature versus time from the time of application or removal of the heating power to the time when the junction temperature reaches a stable value. The thermal response time is 0.9 of this difference.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Description of package; including number of chips, location of case or chip carrier temperature measurement(s), and heat sinking arrangement.

   b. Test condition(s), as applicable (see section 3).

   c. Test voltage(s), current(s) and power dissipation of each chip.

   d. Recorded data for each test condition, as applicable.

   e. Symbol(s) with subscript designation(s) of the thermal characteristics determined to verify specified values of these characteristics, as applicable.

   f. Accept or reject criteria.

FIGURE 1012-1. Temperature controlled heat sink.

FIGURE 1012-1. Temperature controlled heat sink - Continued.

FIGURE 1012-2. Temperature arrangement for mounting surface temperature measurements.

TSP: Diode V_F - Switch S1 in position 2
Switch S2 in position 1

Transistor V_{EB} (Emitter-only switching) - Switch S1 in position 2
Switch S2 in position 2
Switch S3 in position 2

Transistor V_{EB} (Emitter and collector switching) - Switch S1 in position 2
Switch S2 in position 2
Switch S1 in position 1

Transistor V_{CB} - Switch S1 in position 1
Switch S2 in position 2
Switch S3 in position 1

FIGURE 1012-3. Typical test circuit for indirect measurement of $T_{J(Avg)}$ using p-n junction voltages of active devices.

FIGURE 1012-4. Typical test circuit for indirect measurement of $T_{J(Region)}$ using the substrate diode of junction isolated integrated circuit.

METHOD 1013

DEW POINT

1. PURPOSE. The purpose of this test is to detect the presence of moisture trapped inside the microelectronic device package in sufficient quantity to adversely affect device parameters. The most sensitive indicator of moisture is device leakage current. This test specifies a lower temperature of -65°C for the normal dew point test. It may be desirable in some cases, where the presence of moisture in concentrations lower than that would be revealed at this lower temperature, to extend the lower temperature downward.

2. APPARATUS. The apparatus used in this test shall be capable of varying the temperature from the specified high temperature to -65°C while the parameter is being measured.

3. PROCEDURE. The voltage and current specified in the applicable acquisition document shall be applied to the terminals and the device leakage current or other specified parameter(s) continuously monitored from the specified high temperature to -65°C and back to the high temperature. The dew point temperature is indicated by a sharp discontinuity in the parameter being measured with respect to temperature. If no discontinuity is observed, it shall be assumed that the dew point is at a temperature lower than -65°C and the device being tested is acceptable. Devices which demonstrate instability of the measured parameter at any point during this test shall be rejected even though a true dew point is not identified. If a high temperature is not specified in the applicable acquisition document, the device shall be taken to a temperature at least 10°C above ambient temperature to initiate this test and enable detection of dew point in devices which may already be at saturation. The rate of change of temperature for this test shall be no greater than 10°C per minute. The test voltage shall be at least equal to the rated breakdown voltage of the device since it is necessary to apply sufficient voltage to achieve ionization.

4. SUMMARY. The following details shall be specified on the applicable acquisition document:

   a. Test temperature, high (see 3) and low if other than -65°C (see 1).

   b. Test voltage and current (see 3).

   c. Test parameter (see 1 and 3).

METHOD 1014.10

SEAL

1. PURPOSE. The purpose of this test is to determine the effectiveness (hermeticity) of the seal of microelectronic and semiconductor devices with designed internal cavities.

1.1 Definitions.

a. Standard leak rate. Standard leak rate is defined as that quantity of dry air at 25°C in atmosphere cubic centimeters flowing through a leak or multiple leak paths per second when the high-pressure side is at 1 atmosphere (760 mm Hg absolute) and the low-pressure side is at a pressure of not greater than 1 mm Hg absolute. Standard leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/s).

b. Measured leak rate. Measured leak rate (R_1) is defined as the leak rate of a given package as measured under specified conditions and employing a specified test medium. Measured leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/s). For the purpose of comparison with rates determined by other methods of testing, the measured leak rates must be converted to equivalent standard leak rates.

c. Equivalent standard leak rate. The equivalent standard leak (L) of a given package, with a measured leak rate (R_1), is defined as the leak rate of the same package with the same leak geometry, that would exist under the standard conditions of 1.1a. The formula (does not apply to test condition B) in 3.1.1.2 represents the L/R ratio and gives the equivalent standard leak rate (L) of the package with a measured leak rate (R_1) where the package volume and leak test conditioning parameters influence the measured value of (R_1). The equivalent standard leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm cc/s).

2. APPARATUS. The apparatus required for the seal test shall be as follows for the applicable test condition:

2.1 Test conditions A_1, A_2, and A_4, 1/ tracer gas helium (He) fine leak. Apparatus required shall consist of suitable pressure and vacuum chambers and a mass spectrometer-type leak detector preset and properly calibrated for a helium leak rate sensitivity sufficient to read measured helium leak rates of 10^{-9} atm cc/s and greater. The volume of the chamber used for leak rate measurement should be held to the minimum practical, since this chamber volume has an adverse effect on sensitivity limits. The leak detector indicator shall be calibrated using a diffusion-type calibrated standard leak at least once during every working shift. In addition for test condition A_4, the following apparatus is required:

a. Fixture and fittings to mate the package to be tested to the leak detector.

b. Surgical rubber gasket.

c. Apeizon grease (type M or N), perfluorocarbon fluid 2/, or equivalent, if required to obtain seal.

1/ A_3 was intentionally omitted.
2/ Perfluorocarbons contain no chlorine or hydrogen.

2.2 Test condition B, radioisotope fine leak. Apparatus for this test shall consist of:

a. Radioactive tracer gas activation console.

b. Counting equipment consisting of a scintillation crystal, photomultiplier tube, preamplifier, ratemeter, and krypton-85 reference standards. The counting station shall be of sufficient sensitivity to determine through the device wall the radiation level of any krypton-85 tracer gas present within the device. The counting station shall have a minimum sensitivity corresponding to a leak rate of 10^{-9} atm cc/s of krypton-85 and shall be calibrated at least once every working shift using krypton-85 reference standards and following the equipment manufacturer's instruction.

c. A tracer gas consisting of a mixture of krypton-85 and dry nitrogen. The concentration of krypton-85 in dry nitrogen shall be no less than 100 microcuries per atmospheric cubic centimeter. This value shall be determined at least once each 30 days and recorded in accordance with the calibration requirements of this standard (see 4.5.1 of MIL-STD-883).

2.3 Test condition C, perfluorocarbon gross leak. Apparatus for this test shall consist of:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 105 psia up to 23.5 hours.

b. A suitable observation container with provisions to maintain the indicator fluid at a temperature of 125°C and a filtration system capable of removing particles greater than 1 micrometer in size from the fluid (condition C1 only).

c. A magnifier with a magnification in the range between 1.5X to 30X for observation of bubbles emanating from devices when immersed in the indicator fluid (condition C1 only).

d. Sources of type I detector fluids, and type II indicator fluids as specified in table I.

e. A lighting source capable of producing at least 15 thousand foot candles in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration but the light level at the point of observation (i.e., where the device under test is located during observation for bubbles), shall be verified (condition C1 only).

f. Suitable calibrated instruments to indicate that test temperatures, pressures, and times are as specified.

g. Suitable fixtures to hold the device(s) in the indicator fluid (condition C1 only).

h. A perfluorocarbon vapor detection system capable of detecting vapor quantities equivalent to 0.167 or 1/6 microliter of type I fluid (condition C3 only).

i. The vapor detector used for condition C3 shall be calibrated at least once each working shift using a type I fluid calibration source, and following the manufacturer's instructions.

2.4 Test condition D, penetrant dye gross leak. The following apparatus shall be used for this test:

a. Ultraviolet light source with peak radiation at approximately the frequency causing maximum reflection of the dye (3650 Å for Zyglo; 4935 Å for Fluorescein; 5560 Å for Rhodamine B, etc.).

b. Pressure chamber capable of maintaining 105 psia.

c. Solution of fluorescent dye (such as Rhodamine B, Fluorescein, Dye-check, Zyglo, FL-50, or equivalent) mixed in accordance with the manufacturer's specification.

d. A magnifier with a magnification in the range between 1.5X to 30X for dye observation.

2.5 Test condition E, weight gain gross leak. Apparatus for this test shall consist of:

a. A vacuum/pressure chamber for the evacuation and subsequent pressure bombing of devices up to 90 psia up to 10 hours.

b. An analytical balance capable of weighing the devices accurately to 0.1 milligram.

c. A source of type III detector fluid as specified in table I.

d. A filtration system capable of removing particles greater than 1 micrometer in size from the perfluorocarbon fluid.

e. Suitable calibrated instruments to measure test pressures and times.

TABLE I. Physical property requirements of perfluorocarbon fluids. 1/

Property	Type I	Type II	Type III	ASTM test method
Boiling point (°C)	50-95	140-200	50-110	D-1120
Surface tension (Dynes/cm) at 25°C		< 20		D-971 D-1331
Density at 25°C (gm/ml)	> 1.6	> 1.6	> 1.6	D-941
Density at 125°C (gm/ml)		> 1.5		D-941
Dielectric strength (volts/mil)	> 300	> 300	> 300	877
Residue (:gm/gm)	< 50	< 50	< 50	D-2109
Appearance	Clear colorless			NA

1/ Perfluorocarbons contain no chlorine or hydrogen.

2.6 Test conditions C_4 and C_5 - optical gross/fine leak. Apparatus required shall consist of suitable vacuum or vacuum/pressure chamber with an integral interferometry leak detector. The optical leak detector shall be preset and properly calibrated for an equivalent standard leak rate sensitivity of 10^{-5} atm-cc/s and greater for gross leak detection (C_4), or 1 X 10^{-7} atm-cc/s and greater for fine leak detection (C_5). The leak detection system shall be tested with a known good specimen at the beginning and end of each work shift.

3. PROCEDURE. Fine and gross leak tests shall be conducted in accordance with the requirements and procedures of the specified test condition. Testing order shall be fine leak (condition A or B or C_5) followed by gross leak (condition C_1, C_3, C_4, D, or E) except when C_4 is used together with A, B, or C_5. When specified (see 4), measurements after test shall be conducted following the leak test procedures. Where bomb pressure specified exceeds the microcircuit package capability, alternate pressure, exposure time, and dwell time conditions may be used provided they satisfy the leak rate, pressure, time relationships which apply, and provided a minimum of 30 psia (2 atmospheres absolute) bomb pressure is applied in any case or for condition C_4, a minimum of 10 psi differential test pressure is applied in any case. When test condition A_4 is used, gross leak testing is not required. However A_4 shall not be used in lieu of the required seal testing of lidded packages. When batch testing (more than one device in the leak detector at one time) is used in performing test condition A or B and a reject condition occurs it shall be noted as a batch failure. Each device may then be tested individually one time for acceptance if all devices in the batch are retested within one hour after removal from the tracer gas pressurization chamber. For condition B only, devices may be batch retested for acceptance providing all retesting is completed within one hour after removal from the tracer gas pressurization chamber. For condition C_3 only, devices that are batch tested, and indicate a reject condition, may be retested individually one time using the procedure of 3.3.3.1 herein, except that repressurization is not required if the devices are immersed in detector fluid within 20 seconds after completion of the first test, and they remain in the bath until retest. For conditions C_4 and C_5 only, the package must meet lid stiffness requirements defined in 3.6.

3.1 Test condition A_1, A_2, or A_4 tracer gas (He) fine leak. Test condition A_1 is a "fixed" method with specified conditions in accordance with table II that will ensure the test sensitivity necessary to detect the required measured leak rate (R_1) . Test condition A_2 is a "flexible" method that allows the variance of test conditions in accordance with the formula of 3.1.1.2 to detect the specified equivalent standard leak rate (L) at a predetermined leak rate (R_1). Test condition A_4 is a method that will detect the required measured leak rate (R_1) of an unsealed package.

3.1.1 Test conditions A_1 and A_2, procedure applicable to "fixed" and "flexible" methods. The completed device(s), shall be placed in a sealed chamber which is then pressurized with a tracer gas of 100 +0, -5 percent helium for the required time and pressure. The pressure shall then be relieved and each specimen transferred to another chamber or chambers which are connected to the evacuating system and a mass-spectrometer-type leak detector. When the chamber(s) is evacuated, any tracer gas which was previously forced into the specimen will thus be drawn out and indicated by the leak detector as a measured leak rate (R_1). (The number of devices removed from pressurization for leak testing shall be limited such that the test of the last device can be completed within 60 minutes for test condition A_1 or within the chosen value of dwell time t_2 for test condition A_2.)

3.1.1.1 Test condition A_1, fixed method. The devices(s) shall be tested using the appropriate conditions specified in table II for the internal cavity volume of the package under test. The time t_1 is the time under pressure and time t_2 is the maximum time allowed after release of pressure before the device shall be read. The fixed method shall not be used if the maximum equivalent standard leak rate limit given in the acquisition document is less than the limits specified herein for the flexible method.

TABLE II. Fixed conditions for test condition A_1.

Volume of package (V) in cm^3	Bomb condition			R_1 Reject limit (atm cc/s He)
	Psia ±2	Minimum exposure time hours (t_1)	Maximum dwell hours (t_2)	
<0.05	75	2	1	5×10^{-8}
≥0.05 - <0.5	75	4	1	5×10^{-8}
≥0.5 - <1.0	45	2	1	1×10^{-7}
≥1.0 - <10.0	45	5	1	5×10^{-8}
≥10.0 - <20.0	45	10	1	5×10^{-8}

3.1.1.2 Test condition A_2, flexible method. Values for bomb pressure exposure time, and dwell time shall be chosen such that actual measured tracer gas leak rate (R_1) readings obtained for the devices under test (if defective) will be greater than the minimum detection sensitivity capability of the mass spectrometer. The devices shall be subjected to a minimum of 2 atmospheres absolute of helium atmosphere. If the chosen dwell time (t_2) is greater than 60 minutes, graphs shall be plotted to determine an R_1 value which will assure overlap with the selected gross leak test condition. The chosen values, in conjunction with the value of the internal volume of the device package to be tested and the maximum equivalent standard leak rate (L) limit (as shown below or as specified in the applicable acquisition document), shall be used to calculate the measured leak rate (R_1) limit using the following formula:

$$R_1 = \frac{LP_E}{P_O}\left(\frac{M_A}{M}\right)^{\frac{1}{2}} \left\{ 1 - e^{-\left[\frac{LT_1}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]} \right\} e^{-\left[\frac{LT_2}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]}$$

Where:

R_1 = The measured leak rate of tracer gas (He) through the leak in atm cc/s He.
L = The equivalent standard leak rate in atm cc/s air.
P_E = The pressure of exposure in atmospheres absolute.
P_O = The atmospheric pressure in atmospheres absolute. (1)
M_A = The molecular weight of air in grams. (28.7)
M = The molecular weight of the tracer gas (Helium) in grams. (4)
t_1 = The time of exposure to P_E in seconds.
t_2 = The dwell time between release of pressure and leak detection, in seconds.
V = The internal volume of the device package cavity in cubic centimeters.

3.1.1.2.1 Failure criteria. Unless otherwise specified, devices with an internal cavity volume of 0.01 cc or less shall be rejected if the equivalent standard leak rate (L) exceeds 5×10^{-8} atm cc/s air. Devices with an internal cavity volume greater than 0.01 cc and equal to or less than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-7} atm cc/s air. Devices with an internal cavity volume greater than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-6} atm cc/s air.

3.1.2 Test condition A_4, procedure applicable to the unsealed package method. The fixture and fittings of 2.1a. shall be mounted to the evacuation port of the leak detector. Proof of fixturing integrity shall be verified by sealing a flat surfaced metal plate utilizing the gasket of 2.1 (and grease or fluid of 2.1 if required to obtain seal) and measuring the response of the leak test system. Testing shall be performed by sealing the package(s) to the evacuation port and the package cavity evacuated to 0.1 torr or less. Care shall be taken to prevent contact of grease with package (seal ring not included) to avoid masking leaks. The external portion of the package shall be flooded with Helium gas either by the use of an envelope or a spray gun, at a pressure of 45 psia.

3.1.2.1 Failure criteria. Unless otherwise specified, devices shall be rejected if the measured leak rate (R_1) exceeds 1 x 10^{-8} atm cc/s He.

3.2 Test condition B, radioisotope fine leak test.

3.2.1 Activation parameters. The activation pressure and soak time shall be determined in accordance with the following equation:

$$Q_S = \frac{R}{skTPt} \qquad (1)$$

The parameters of equation (1) are defined as follows:

Q_s = The maximum leak rate allowable, in atm cc/s Kr, for the devices to be tested.

R = Counts per minute above the ambient background after activation if the device leak rate were exactly equal to Q_s. This is the reject count above the background of both the counting equipment and the component, if it has been through prior radioactive leak tests.

s = The specific activity, in microcuries per atmosphere cubic centimeter, of the krypton-85 tracer gas in the activation system.

k = The overall counting efficiency of the scintillation crystal in counts per minute per microcurie of krypton-85 in the internal void of the specific component being evaluated. This factor depends upon component configuration and dimensions of the scintillation crystal. The counting efficiency shall be determined in accordance with 3.2.2.

T = Soak time, in hours, that the devices are to be activated.

$\bar{P}$ = $P_e^2 - P_i^2$, where P_e is the activation pressure in atmospheres absolute and P_i is the original internal pressure of the devices in atmospheres absolute. The activation pressure (P_e) may be established by specification or if a convenient soak time (T) has been established, the activation pressure (P_e) can be adjusted to satisfy equation (1).

t = Conversion of hours to seconds and is equal to 3,600 seconds per hour.

NOTE: The complete version of equation (1) contains a factor ($P_o^2 - (\Delta P)^2$) in the numerator which is a correction factor for elevation above sea level. P_o is sea level pressure in atmospheres absolute and ΔP is the difference in pressure, in atmospheres between the actual pressure at the test station and sea level pressure. For the purpose of this test method, this factor has been dropped.

3.2.2 Determination of counting efficiency (k). The counting efficiency (k) of equation (1) shall be determined as follows:

a. Five representative units of the device type being tested shall be tubulated and the internal void of the device shall be backfilled through the tubulation with a known volume and known specific activity of krypton-85 tracer gas and the tubulation shall be sealed off.

b. The counts per minute shall be directly read in the shielded scintillation crystal of the counting station in which the devices are read. From this value, the counting efficiency, in counts per minute per microcurie, shall be calculated.

3.2.3 Evaluation of surface sorption. All device encapsulations consisting of glass, metal, and ceramic or combinations thereof, including coatings and external sealants, shall be evaluated for surface sorption of krypton-85 before establishing the leak test parameters. Representative samples of the questionable material shall be subjected to the predetermined pressure and time conditions established for the device configuration as specified by 3.2.1. The samples shall then be counted every 10 minutes, with count rates noted, until the count rate becomes asymptotic with time. (This is the point in time at which surface sorption is no longer a problem.) This time lapse shall be noted and shall determine the "wait time" specified in 3.2.4.

3.2.4 Procedure. The devices shall be placed in radioactive tracer gas activation tank. The activation chamber may be partially filled with inert material to reduce pumpdown time. The tank shall be evacuated to 0.5 torr. The devices shall be subjected to a minimum of 2 atmospheres absolute pressure of krypton-85/dry nitrogen mixture for a minimum of 12 minutes. Actual pressure and soak time shall be determined in accordance with 3.2.1. The R value in counts per minute shall not be less than 600 above background. The krypton-85/dry nitrogen gas mixture shall be evacuated to storage until 0.5 to 2.0 torr pressure exists in the activation tank. The storage cycle shall be completed in 3 minutes maximum as measured from the end of the activation cycle or from the time the activation tank pressure reaches 60 psia if a higher bombing pressure is used. The activation tank shall then immediately be backfilled with air (air wash). The devices shall then be removed from the activation tank and leak tested within 1 hour after gas exposure with a scintillation-crystal-equipped counting station. Device encapsulations that come under the requirements of 3.2.3 shall be exposed to ambient air for a time not less than the "wait time" determined by 3.2.3. In no case will the time between removal from the activation chamber and test exceed 1 hour. This exposure shall be performed after gas exposure but before determining leak rate with the counting station. Device encapsulations that do not come under the requirements of 3.2.3 may be tested without a "wait time." (The number of devices removed from pressurization for leak testing shall be limited such that the test of the last device can be completed within 1 hour.) The actual leak rate of the component shall be calculated with the following equation:

$$Q = \frac{(\text{ACTUAL READOUT IN NET COUNTS PER MINUTE}) \times Q_s}{R}$$

Where Q = Actual leak rate in atm cc/s, and QS and R are defined in 3.2.1.

NOTE: CAUTION. Discharge of krypton 85 into the atmosphere must not exceed limits imposed by local and Federal regulations.

3.2.5 Failure criteria. Unless otherwise specified, devices that exhibit a leak rate equal or greater than the test limits of table III shall be considered as failures.

NOTE: CAUTION. Devices which do not exhibit a leak rate sufficient to fail seal test, may retain radioactive tracer gas in sufficient concentration to cause soft errors in complex, small geometry devices.

TABLE III. Test limits for radioisotope fine leak method.

Volume of package cc	Q_s
< 0.01	1×10^{-8}
> 0.01, ≤ 0.4	5×10^{-8}
> 0.4	5×10^{-7}

3.2.6 Personnel precautions. Federal, some state and local governmental regulations require a license for the possession and use of krypton-85 leak test equipment. In the use of radioactive gas, these regulations and their maximum permissible exposure and tolerance levels prescribed by law should be observed.

3.3 Test condition C_1 or C_3, perfluorocarbon gross leak. Test condition C_1 is a fixed method with specified conditions that will ensure the test sensitivity necessary. Test condition C_2 has been replaced by C_1. Test condition C3 is a fixed method that uses a vapor detection system instead of an indicator bath.

* 3.3.1 Procedure applicable to fixed (C_1) method. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr or less and maintained for 30 minutes minimum. The vacuum cycle may be omitted for packages with an internal volume ≥ 0.1 cm^3. A sufficient amount of type I detector fluid shall be admitted to cover the devices. When the vacuum cycle is performed, the fluid will be admitted after the minimum 30 minute period but before breaking the vacuum. The devices shall then be pressurized in accordance with table IV. When the pressurization period is complete the pressure shall be released and the devices removed from the chamber without being removed from a bath of detector fluid for greater than 20 seconds. A holding bath may be another vessel or storage tank. When the devices are removed from the bath they shall be dried for 2 ±1 minutes in air prior to immersion in type II indicator fluid, which shall be maintained at 125°C ±5°C. The devices shall be immersed with the uppermost portion at a minimum depth of 2 inches below the surface of the indicator fluid, one at a time or in such a configuration that a single bubble from a single device out of a group under observation may be clearly observed as to its occurrence and source. The device shall be observed against a dull, nonreflective black background though the magnifier, while illuminated by the lighting source, from the instant of immersion until, expiration of a 30-second minimum observation period, unless rejected earlier.

For packages greater than 5 grams, the effects of package thermal mass shall be determined by evaluating each package family with known leakers and measuring the time for bubbles to be observed. If the evaluation time exceeds the 30 seconds required for the observation time, then the observation time shall be extended to take into account the package thermal mass effect. Alternate methods may be used to meet this intent provided the method is documented and made available to the preparing or acquiring activity upon request.

3.3.1.1 Test condition C_1, fixed method. Allowable fixed method conditions shall be as shown in table IV, herein.

TABLE IV. Condition C pressurization conditions.

Pressure psia (min)	Minimum pressurization time (hour)	
	C_1	C_3
30	23.5	12
45	8	4
60	4	2
75	2	1
90	1	0.5
105	0.5	N/A

3.3.2 Failure criteria. A definite stream of bubbles or two or more large bubbles originating from the same point shall be cause for rejection.

* CAUTION: When the leak is large, the operator may notice a stream of liquid exiting the package without the release of bubbles. *This condition shall result in the package being rejected.*

3.3.3 Test condition C_3, perfluorocarbon vapor detection.

3.3.3.1 Procedure. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr and maintained for 30 minutes minimum. A sufficient amount of type I detector fluid shall be admitted to the pressure chamber to cover the devices. The fluid shall be admitted after the 30 minute minimum vacuum period but before breaking the vacuum. The devices shall then be pressurized in accordance with table IV. The pressure shall be maintained for a period of 30 minutes minimum. Upon completion of the pressurization period, the pressure shall be released, the devices removed from the pressure chamber without being removed from a bath of detector fluid for more than 20 seconds and then retained in a bath of perfluorocarbon fluid. When the devices are removed from the fluid they shall be air dried for a minimum of 20 seconds and a maximum of 5 minutes prior to the test cycle. If the type I detector fluid has a boiling point of less than 80°C, the maximum drying time shall be 3 minutes.

The devices shall then be tested with a perfluorocarbon vapor detector that is calibrated in accordance with 2.3h and 2.3i. "Purge" time shall be in accordance with table V. Test time shall be a minimum of 3.5 seconds (unless the device is rejected earlier) with the perfluorocarbon vapor detector purge and test chambers at a temperature of 125 ±5°C, or 2.5 seconds minimum with the purge and test chambers at a temperature of 150 ±5°C.

NOTE: Air dry, purge and test limits for each device shall be complied with in all cases, including stick to stick handling.

NOTE: Test temperature shall be measured at the chamber surface that is in contact with the device(s) being tested. Device orientation within the test cell should maximize heat transfer from the heated chamber surface to the cavity of the device within the capability of the equipment.

3.3.3.2 Failure criteria. A device shall be rejected if the detector instrumentation indicates more than the equivalent of 0.167 or 1/6 microliter of type I detector fluid in accordance with table I.

TABLE V. Purge time for condition C_3.

Package with internal free volume (CM^3)	Purge time (seconds)
≤0.01	≤ 5
>0.01 ≤0.10	≤ 9
>0.10	≤ 13

NOTE: Maximum purge time can be determined by cycling a device with a 0.02 to 0.05 inch hole and measuring the maximum purge time that can be used without permitting the device to escape detection during the test cycle.

3.3.4 Precautions. The following precautions shall be observed in conducting the perfluorocarbon gross leak test:

a. Perfluorocarbon fluids shall be filtered through a filter system capable of removing particles greater than 1 micrometer prior to use. Bulk filtering and storage is permissible. Liquid which has accumulated observable quantities of particulate matter during use shall be discarded or reclaimed by filtration for re-use. Precaution should be taken to prevent contamination.

b. Observation container shall be filled to assure coverage of the device to a minimum of 2 inches.

c. Devices to be tested should be free from foreign materials on the surface, including conformal coatings and any markings which may contribute to erroneous test results.

d. A lighting source capable of producing at least 15 thousand foot candles in air at a distance equal to that which the most distant device in the bath will be from the source. The lighting source shall not require calibration but the light level at the point of observation (i.e., where the device under test is located during observation for bubbles) shall be verified.

e. Precaution should be taken to prevent operator injury due to package rupture or violent evolution of bomb fluid when testing large packages.

* 3.4 Test condition D, penetrant dye gross leak. This test shall be permitted only for destructive verification of devices (see 3.7). The pressure chamber shall be filled with the dye solution to a depth sufficient to completely cover all the devices. The devices shall be placed in the solution and the chamber pressurized at 105 psia minimum for 3 hours minimum. For device packages which will not withstand 105 psia, 60 psia minimum for 10 hours may be used. The devices shall then be removed and carefully washed, using a suitable solvent for the dye used, followed by an air-jet dry. The devices shall then be immediately examined under the magnifier using an ultraviolet light source of appropriate frequency.

3.4.1 Failure criteria. Any evidence of dye penetration into the device cavity shall constitute a failure.

3.5 Test condition E, weight gain gross leak.

3.5.1 Procedure. The devices shall be placed in an oven at 125°C for 1 hour minimum, after which they shall be allowed to cool to room ambient temperature. Each device shall be weighed and the initial weight recorded or the devices may be categorized into cells as follows. Devices having a volume of <0.01 cc shall be categorized in cells of 0.5 milligram increments and devices with volume ≥0.01 cc shall be categorized in cells of 1.0 milligram increments. The devices shall be placed in a vacuum/pressure chamber and the pressure reduced to 5 torr and maintained for 1 hour except that for devices with an internal cavity volume ≥0.1 cc, this vacuum cycle may be omitted. A sufficient amount of type III detector fluid shall be admitted to the pressure chamber to cover the devices. When the vacuum cycle is performed, the fluid shall be admitted after the 1-hour period but before breaking the vacuum. The devices shall then be pressurized to 75 psia minimum except that 90 minimum psia shall be used when the vacuum cycle has been omitted. The pressure shall be maintained for 2 hours minimum. If the devices will not withstand the 75 psia test pressure, the pressure may be lowered to 45 psia minimum with the vacuum cycle and the pressure maintained for 10 hours minimum.

Upon completion of the pressurization period, the pressure shall be released and the devices removed from the pressure chamber and retained in a bath of the perfluorocarbon fluid. When the devices are removed from the fluid they shall be air dried for 2 ±1 minutes prior to weighing. Transfer the devices singly to the balance and determine the weight or weight category of each device. All devices shall be tested within 4 minutes following removal from the fluid. The delta weight shall be calculated from the record of the initial weight and the post weight of the device. Devices which were categorized shall be separated into two groups, one group which shall be devices which shifted one cell or less and the other group which shall be devices which shifted more than one cell.

3.5.2 Failure criteria. A device shall be rejected if it gains 1.0 milligram or more and has an internal volume of ≤ 0.01 cm^3 and 2.0 milligrams or more if the volume is > 0.01 cm^3. If the devices are categorized, any device which gains enough weight to cause it to shift by more than one cell shall be considered a reject. A device which loses weight of an amount which if gained would cause the device to be rejected may be retested after it is baked at 125°C for a period of 8 hours.

3.6 Test condition C_4 or C_5 - optical gross or gross/fine leak. Test conditions C_4 and C_5 are specific to packages with thin lids (thickness < 0.025, typically metallic). Sensitivity is related to the extent of deflection of the lid due to a specific pressure change. For a specific lid material and size the following formula must be met:

For condition C_4: $R^4 / E\,T^3 > 1.0 \times 10^{-4}$

For condition C_5: $R^4 / E\,T^3 > 1.0 \times 10^{-3}$

Where:
R = The minimum width of free lid (inside braze or cavity dimension in inches
E = The modulus of elasticity of the lid material
T = The thickness of the lid (inches)

3.6.1 Test condition C_4 - optical gross leak. The completed device(s) shall be placed in the sealed test chamber. An optical interferometer is set to observe the package lid(s). The chamber is then evacuated while the deflection of the lid(s) is being observed with the optical interferometer. The deflection of the lid(s) with the pressure change, and the lack of continued deflection of the lid(s) with the reduced pressure held constant for time t_1 (or equivalent procedure), will be observed for each package in the field of view simultaneously.

3.6.1.1 Failure criteria. A device shall be rejected for any of the following criteria:

a. If the optical interferometer did not detect deflection of the lid as the chamber pressure was initially changed.

b. If the interferometer detects the lid deflecting as the chamber pressure is held constant (or equivalent procedure.

3.6.2 Test condition C_5 - optical gross/fine leak. The completed device(s) shall be placed in the sealed test chamber. An optical interferometer is set to observe the package lid(s). The chamber is then evacuated while the deflection of the lid(s) is being observed with the optical interferometer. The deflection on the lid(s) with the pressure change and the lack of continued deflection of the lid(s) with the reduced pressure held constant for time t_1 (or equivalent procedure), will be observed for each package in the field of view simultaneously.

The sealed test chamber is then pressurized wuth Helium gas to 30 psig. The lack of deflection of the lid(s) is then observed with an optical interferometer for time t_2 (or equivalent procedure).

3.6.2.1 Failure criteria. A device shall be rejected for any of the three following criteria:

a. If the interferometer did not detect deflection of the lid as the chamber pressure was initially charged.

b. If the interferometer detects the lid deflecting from the package leaking its entrapped internal pressure during time t_1 as the pressure is held constant (or equivalent procedure).

c. If the interferometer detects the lid deflecting from the package leaking in the pressurized Helium gas during time t_2 as the pressure is held constant (or equivalent procedure).

3.7 Retest. Devices which fail gross leak (test conditions C or E) may be retested destructively. If the retest shows a device to pass, that was originally thought to be a failure, then the device need not be counted as a failure in the accept number of sample size number calculations. Devices which fail fine leak (test conditions A_1, A_2, A_4, or B) shall not be retested for acceptance unless specifically permitted by the applicable acquisition document. Where fine leak retest is permitted, the entire leak test procedure for the specified test condition shall be repeated. That is, retest consisting of a second observation on leak detection without a re-exposure to the tracer fluid or gas under the specified test condition shall not be permissible under any circumstances. Preliminary measurement to detect residual tracer gas is advisable before any retest.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter when a specific test is to be applied (see 3).

b. Accept or reject leak rate for test condition A or B or C_5 when other than the accept or reject leak rate specified herein applies (see 3.1.1.1, 3.1.1.2, 3.1.2, 3.2.5, and 3.6.2.1).

c. Where applicable, measurements after test (see 3).

d. Retest acceptability for test conditions A and B (see 3.7).

e. Order of performance of fine and gross if other than fine followed by gross except when using C_4 (see 3).

f. Where applicable, the device package pressure rating shall be specified if that rating is less than 75 psia.

g. Fine leak testing with condition C_5 is only applicable for use where conditions A or B are not applicable. These conditions include package inspection on completed assemblies (PC boards), packages with external absorbing materials (connectors), or other special conditions.

METHOD 1015.9

BURN-IN TEST

1. PURPOSE. The burn-in test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which cause time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at or above maximum rated operating conditions or to apply equivalent screening conditions which will reveal time and stress dependent failure modes with equal or greater sensitivity.

2. APPARATUS. Details for the required apparatus shall be as described in method 1005.

* 3. PROCEDURE. The microelectronic device shall be subjected to the specified burn-in screen test condition (see 3.1) for the time and temperature specified (see method 5004 for the appropriate device class level) or, unless otherwise specified, for an equivalent time and temperature combination as determined from table I (see 3.1.1 and 3.1.2). QML manufacturers who are certified and qualified to MIL-I-38535 may modify the time or the temperature condition independently from the regression conditions contained in table I or the test condition/circuit specified in the device specification or standard microcircuit drawing provided the modification is contained in the manufacturers Quality Management Plan and the "Q" certification identifier is marked on the devices. Any time-temperature combination which is contained in table I for the appropriate class level may be used for the applicable test condition. The test conditions (duration and temperature) selected prior to test shall be recorded and shall govern for the entire test. Lead-, stud-, or case-mounted devices shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified ambient temperature. Pre and post burn-in measurements shall be made as specified. Burn-in boards shall not employ load resistors which are common to more than one device, or to more than one output pin on the same device.

* 3.1 Test conditions. Basic test conditions are as shown below. Unless otherwise specified, test condition F shall not be applied to class level S devices. Details of each of these conditions, except where noted, shall be as described in method 1005.

a. Test condition A: Steady-state, reverse bias.

b. Test condition B: Steady-state, forward bias.

c. Test condition C: Steady-state, power and reverse bias.

d. Test condition D: Parallel excitation.

e. Test condition E: Ring oscillator.

f. Test condition F: Temperature-accelerated test.

* 3.1.1 Test temperature. The ambient burn-in test temperature shall be 125°C minimum for conditions A through E (except for hybrids see table I). At the supplier's option, the test temperature for conditions A through E may be increased and the test time reduced in accordance with table I. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit employed should be so structured that maximum rated junction temperature for test or operation shall not exceed 200°C for class level B or 175°C for class level S (see 3.1.1.1). Devices with internal thermal shut-down circuitry shall be handled in accordance with 3.2.3 of method 1005. The specified test temperature is the minimum actual ambient temperature to which all devices in the working area of the chamber shall be exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other suitable gas or liquid chamber medium. Therefore, calibration shall be accomplished on the chamber in a fully loaded (boards need not be loaded with devices), unpowered configuration, and the indicator sensor located at, or adjusted to reflect the coldest point in the working area.

* 3.1.1.1 Test temperature for high power devices. Regardless of power level, devices shall be able to be burned in or life-tested at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C and where the ambient temperature would cause T_J to exceed +200°C (+175°C for class level S), the ambient operating temperature may be reduced during burn-in and life test from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

* 3.1.1.2 Test temperature for hybrid devices. The ambient or case burn-in test temperature shall be as specified in table I, except case temperature burn-in shall be performed, as a minimum, at the maximum operating case temperature (T_C) specified for the device. Burn-in shall be 320 hours minimum for class level S hybrids (class K). The device should be burned in at the maximum specified operating temperature, voltage, and loading conditions as specified in the device specification or drawing. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that the maximum rated junction temperature as specified in the device specification or drawing, and the cure temperature of polymeric materials as specified in the baseline documentation shall not be exceeded. If no maximum junction temperature is specified, a maximum of 175°C is assumed. Accelerated burn-in (condition F) shall not be permitted. The specified test temperature shall be the minimum actual ambient or case temperature that must be maintained for all devices in the chamber. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments and the flow of air or other suitable gas or liquid chamber medium.

3.1.2 Temperature accelerated test details. In test condition F, microcircuits are subjected to bias(es) at a temperature (175°C to 250°C) which considerably exceeds the maximum rated junction temperature. At these elevated temperatures, it is generally found that microcircuits will not operate normally as specified in their applicable acquisition documents, and it is therefore necessary that special attention be given to the choice of bias circuits and conditions to assure that important circuit areas are adequately biased without subjecting other areas of the circuit to damaging overstress(es). To properly select the accelerated test conditions, it is recommended that an adequate sample of devices be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the applied electrical stresses do not induce damaging overstress. Unless otherwise specified in the device specifications or drawings, the minimum time-temperature combination shall be as delineated by table I. The minimum test time shall be 12 hours. The applied voltage at any or all terminals shall be equal to the recommended operating voltage(s) at 125°C. When excessive current flow or power dissipation would result from operation at the specified voltage(s), the applied voltage(s) at any or all terminals may be reduced to a minimum of 50 percent of the specified voltage(s) and the testing time shall be determined in accordance with the formula given in 3.5.6 of method 1005. Devices with internal thermal shut-down circuitry shall be handled in accordance with 3.5.6.1 of method 1005. Thermal runaway conditions must be avoided at all times.

3.2 Measurements. Pre burn-in measurements, when specified, or at the manufacturer's discretion when not specified, shall be conducted prior to applying burn-in test conditions. Post burn-in measurements shall be completed within 96 hours after removal of the devices from the specified burn-in test condition (i.e., either removal of temperature or bias) and shall consist of all 25°C dc parameter measurements) (subgroup A-1 of method 5005, or subgroups tested in lieu of A-1 as allowed in the most similar military device specification or standard microcircuit drawing) and all parameters for which delta limits have been specified as part of interim (post-burn-in) electrical measurements. Delta limit acceptance, when applicable, shall be based upon these measurements. If these measurements cannot be completed within 96 hours, for either the standard or accelerated burn-in, the devices shall be subjected to the same test condition (see 3.1) and temperature previously used for a minimum additional reburn-in time as specified in table I before post burn-in measurements are made.

3.2.1 Cooldown after standard burn-in. All devices shall be cooled to within 10°C of their power stable condition at room temperature prior to the removal of bias. The interruption of bias for up to 1 minute for the purpose of moving the devices to cooldown positions separate from the chamber within which burn-in testing was performed shall not be considered removal of bias, (bias at cooldown position shall be same as that used during burn-in). Alternatively, except for linear or MOS (CMOS, NMOS, PMOS, etc.) devices or unless otherwise specified, the bias may be removed during cooling provided the case temperature of devices under test is reduced to a maximum of 35°C within 30 minutes after the removal of the test conditions and provided the devices under test are removed from the heated chamber within 5 minutes following removal of bias. All 25°C dc measurements or alternate subgroups (see 3.2) shall be completed prior to any reheating of the device(s).

3.2.2 Cooldown after accelerated burn-in. All devices subjected to the accelerated testing of condition F shall be cooled to within 10°C of power stable at room temperature prior to the removal of bias. Interruption of bias for a period of up to 1 minute for the purpose of moving devices to cooldown positions separate from the chamber within which burn-in was conducted shall not be considered removal of bias, (bias at cooldown position shall be same as that used during burn-in). All specified 25°C dc electrical measurements shall be completed prior to any reheating of the devices.

3.2.3 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, (once every 6 months or just prior to use if not used during the 6 month period) each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Board capacitance or resistance required to ensure stability of devices under test shall be checked during these initial and periodic verification tests to ensure they will perform their proper function (i.e., that they are not open or shorted). Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the devices under test.

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the oven, and brought up to at least 125°C (or the specified test temperature, if less than 125°C) each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. This shall be performed by opening the oven for a maximum of 10 minutes.

c. At the conclusion of the test period, prior to removal of devices from temperature and test conditions, the voltage and signal condition verification of b above shall be repeated.

* d. For class level S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified test conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s). An approved alternate procedure may be used.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration (see 3.1), the test time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration while the chamber is at temperature during the final 8 hours of burn-in shall require extension of the test duration for an uninterrupted 8 hours minimum, after the last bias interruption.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

* a. Test duration if other than as defined for the applicable class level in method 5004, or time-temperature combination shown in table I.

b. Test condition letter.

c. Burn-in test temperature, and whether ambient, junction, or case (see 3), if other than as specified in 3.1.1.

d. Test mounting, if other than normal (see 3).

e. Pre and post burn-in measurements and drift limits, as applicable (see 3.2).

f. Authorization for use of condition F and special maximum test rating for condition F (see 3.1 and 3.1.2), when applicable.

g. Time within which post burn-in measurements must be completed if other than specified (see 3.2).

TABLE I. Burn-in time-temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.1)	Minimum reburn-in time (hours)
	Class level S	Class level B	Class level S hybrids (Class K)		
100	—	352	700	Hybrids only	24
105	—	300	600	"	24
110	—	260	520	"	24
115	—	220	440	"	24
120	—	190	380	"	24
125	240	160	320	A - E	24
130	208	138	—	"	21
135	180	120	—	"	18
140	160	105	—	"	16
145	140	92	—	"	14
150	120	80	—	"	12
175	—	48	—	F	12
200	—	28	—	"	12
225	—	16	—	"	12
250	—	12	—	"	12

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

METHOD 1016

LIFE/RELIABILITY CHARACTERIZATION TESTS

1. PURPOSE. The purpose of the life characterization tests is to determine: (1) the life distributions, (2) the life acceleration characteristics, and (3) the failure rate (λ) potential of the devices. For a discussion of failure rates and life test considerations, see MIL-HDBK-217. Failure rates are ordinarily determined either for general qualification of devices or the production lines from which they are obtained or for the purpose of predicting the failure rates (or Mean Time Between Failure (MTBF)) of equipments in which the devices are to be employed.

NOTE: A detailed dissertation on the life test result analysis techniques, with application examples, is presented by D.S. Peck in the Proceedings of the 9th Annual Reliability Physics Symposium (1971), pages 60 through 78. Further improvements to the methods of test result analysis are possible by using computer aided techniques such as regression analysis and iterative curve fitting.

2. APPARATUS. Suitable sockets or other mounting means shall be provided to make firm electrical contact to the terminals of devices under test in the specified circuit configuration. The mounting means shall be so designed that they will not remove internally dissipated heat from the device by conduction, other than that removed through the device terminals and the necessary electrical contacts, which shall be maintained at or above the specified ambient temperature. The apparatus shall provide for maintaining the specified biases at the terminal(s) of the device under test and, when specified, monitoring of the input excitation. Power supplies and current-setting resistors shall be capable of maintaining the specified operating conditions, as minima, throughout the testing period with normal variations in their source voltages, ambient temperatures, etc. The test equipment shall preferably be so arranged that only natural-convection cooling of the devices occurs. When test conditions result in significant power dissipation, the test apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. The test circuits need not compensate for normal variations in individual device characteristics but shall be arranged so that the existence of failed or abnormal (i.e., open, short, etc.) devices in a group does not negate the effect of the test for other devices in the group.

3. PROCEDURE. The microelectronic devices shall be subjected to the specified test condition (see 3.4) for the specified duration and test temperature, and the required measurements shall be made at the specified intermediate points and endpoints. Lead-, stud-, or case-mounted devices shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified temperature. The test condition, duration, sample size, and temperature selected prior to test shall be recorded and shall govern for the entire test.

3.1 Test duration. The life test duration shall be as follows:

Initial qualification:	4,000 (+72, -240) hours or 75 percent failures, whichever comes first
All other tests:	1,000 (+72, -24) hours or 50 percent failures, whichever comes first

Within the time interval of 24 hours before to 72 hours after the specified duration of the test, the devices shall be removed from the specified test conditions and allowed to reach standard test conditions prior to the removal of bias.

3.2 Measurements. Measurements shall be grouped into two categories as follows:

Type A: Initial and final measurement.

Type B: Interim measurements.

Unless otherwise specified, all measurements shall be completed within 8 hours after removal of the device from the specified test conditions and shall consist of the following:

Type A: All specified endpoint measurement.

Type B: Selected critical parameters (see 4).

The type A measurements shall be made at the zero hour and final measurement time. The type B interim measurements shall be made at the 4, 8, 16, 32, 64, 128, 256, 512 hour times for the 1000 hour test and additionally, at 1000, and 2000 hour times for the 4000 hour test.

3.2.1 Measurements following life test. When devices are measured following application of life test conditions, they shall be cooled to room temperature prior to the removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the devices.

3.2.2 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the devices under test.

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the oven, and brought up to at least 125°C or the specified test temperature, whichever is less, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. This may be performed by opening the oven for a maximum of 10 minutes.

c. At the conclusion of the test period, prior to removal of devices from temperature and test conditions, the voltage and signal condition verification of b above shall be repeated.

* d. For class level S devices when loading boards or trays the continuity between each device and a bias supply shall be verified.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration, the test time shall be extended to assure actual exposure for the total minimum specified test duration.

3.3 Test sample. The test sample shall be as specified (see 4). No fewer than 40 devices shall be specified for a given test temperature.

3.4 Test conditions. In this condition microcircuits are subjected to bias(es) at temperatures (200°C to 300°C) which considerably exceed the maximum rated operating temperature. At these elevated temperatures, it is generally found that microcircuits will not operate normally as specified in their applicable acquisition document and it is therefore necessary that special attention be given to the choice of bias circuits and conditions to assure that important circuit areas are adequately biased, without damaging overstress of other areas of the circuit.

3.4.1 Test temperatures. Unless otherwise specified, test temperatures shall be selected in the range of 200°C to 300°C. The specified test temperature is the minimum actual ambient temperature to which all devices in the working area of the chamber shall be exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other chamber atmosphere. Therefore, calibration shall be accomplished on the chamber in a fully loaded, unpowered configuration, and the indicator sensor located at, or adjusted to reflect the coldest point in the working area. For the initial failure rate determination test, three temperatures shall be selected. A minimum of 25°C separation shall be maintained between the adjacent test temperatures selected. All other periodic life tests shall be conducted with two temperatures and a minimum of 50°C separation.

3.4.2 Bias circuit selection. To properly select the accelerated test conditions, it is recommended that an adequate sample of devices be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the applied electrical stresses do not induce damage. Therefore, prior to performing microcircuit life tests, test circuit, thermal resistance (where significant), and step-stress evaluations should be performed over the test ranges, usually 200°C to 300°C. Steps of 25°C for 24 hours minimum duration (all steps of equal duration with a tolerance of no greater than ±5 percent), each followed by proper electrical measurements, shall be used for step-stress tests.

Optimum test conditions are those that provide maximum voltage at high thermal stress to the most failure-prone junctions or sites, but maintain the device current at a controlled low level. Excessive device current may lead to thermal runaway (and ultimately device destruction). Current-limiting resistors shall be employed.

The applied voltage at any or all terminal(s) shall be equal to the maximum rated voltage at 125°C. If necessary, only with the specific approval of the qualifying activity, the applied voltage at any or all terminals(s) may be reduced to not less than 50 percent of the specified value(s) when it is demonstrated that excessive current flow or power dissipation would result from operation at the specified voltage(s). If the voltage(s) is so reduced, the life testing time shall be determined in accordance with the formula given in 3.5.6 of method 1005.

3.5 Life test ground rules. As an aid to selecting the proper test conditions for an effective microcircuit accelerated life or screening test, the following rules have been formulated:

a. Apply maximum rated voltage (except as provided in 3.4.2) to the most failure prone microcircuit sites or junctions identified during step-stress evaluation.

b. Apply electrical bias to the maximum number of junctions.

c. In each MOS or CMOS device, apply bias to different gate oxides so that both positive and negative voltages are present.

d. Control device currents to avoid thermal runaway and excessive electromigration failures.

e. Employ current-limiting resistors in series with each device to ensure the application of electrical stress to all nonfailed devices on test.

f. Select a value of each current-limiting resistor large enough to prevent massive device damage in the event of failure, but small enough to minimize variations in applied voltage due to current fluctuations.

g. Avoid conditions that exceed design or material limitations such as solder melting points.

h. Avoid conditions that unduly accelerate nontypical field condition failure-mechanisms.

i. Employ overvoltage protection circuitry.

The determination of test conditions that conform to the established ground rules involves three basic steps: (1) evaluation of candidate bias circuits at accelerated test temperatures, (2) device thermal characterization, and (3) the performance of step-stress tests.

3.6 Test results analysis. Failure analysis of the accelerated test results is necessary to separate the failures into temperature and nontemperature dependent categories. The nontemperature dependent failures should be removed from the test data prior to life distribution analysis. All failures shall be reported together with the analysis results and rationale for deletion of those identified as nontemperature dependent.

3.6.1 Life distribution analysis. The effectiveness of the test result analysis can be enhanced by diligent failure analysis of each test failure. Failures should be grouped by similarity of failure mechanisms, that is, surface related, metal migration, intermetallic formation, etc. The time-to-failure history of each failure in a group should be recorded. This includes the individual failure times and the associated calculated cumulative percent failures. To facilitate estimating the distribution parameters from small-sample life tests, the data is plotted as a cumulative distribution. Since semiconductor life distributions have been shown to follow a lognormal distribution, graph paper similar to figure 1016-1 is required for data analysis. The lognormal distribution will appear as a straight line on this paper. The expected bimodal distribution of "freak" and "main" populations in a combined form normally appears as an s-shaped plot. The distribution parameters necessary for data analysis, median life and sigma (σ) can be calculated as:

$$\sigma \approx \ln \frac{time\ of\ 50\%\ failure}{time\ of\ 16\%\ failure}$$

Separate analysis of the individual "freak" and "main" populations should be performed and "goodness of fit" tests applied to test the apparent distribution(s).

3.6.2 Life acceleration analysis. Life/reliability characterization requires the establishing of failure distributions for several temperature stress levels at the same rated voltage condition. These failure distributions must represent a common failure mechanism. Using a specially prepared graph paper for Arrhenius Reaction Rate Analysis as shown in figure 1016-2, the median life times for the "freak" and "main" populations can be plotted to determine equivalent life-times at the desired use temperatures.

3.6.3 Failure rate calculations. Semiconductor failures are lognormally distributed. Therefore, the failure rate will vary with time. Semiconductor failure rates at any given time can be calculated using figure 1016-3 which is a normalized presentation of the mathematical calculations for the instantaneous failure rate from a lognormal distribution.

4. SUMMARY. The following details shall be as specified in the applicable acquisition document:

a. Test temperature(s) and whether ambient or case.

b. Test mounting if other than normal (see 3).

c. Endpoint measurements (see 3.2).

d. Intermediate measurements (see 3.2).

e. Criteria for failure for endpoint and intermediate measurements (see 3.2), if other than device specification limits.

f. Test sample (see 3.3).

g. Requirements for inputs, outputs, biases, test circuit, and power dissipation, as applicable (see 3.4).

h. Requirements for data analysis, including:

(1) Failure analysis results.

(2) Data calculations:

(a) Log normal by temperature.

(b) Reaction rate relationships

(c) Failure rate versus time.

FIGURE 1016-1. Cumulative failure distribution plot.

FIGURE 1016-2. Arrhenius plot - high temperature operating test - accelerated life.

FIGURE 1016-3. Lognormal failure rates.

METHOD 1017.2

NEUTRON IRRADIATION

1. PURPOSE. The neutron irradiation test is performed to determine the susceptibility of semiconductor devices to degradation in the neutron environment. The tests described herein are applicable to integrated circuits, transistors, and diodes. This is a destructive test. Objectives of the test are: (1) to detect and measure the degradation of critical semiconductor device parameters as a function of neutron fluence, and (2) to determine if specified semiconductor device parameters are within specified limits after exposure to a specified level of neutron fluence (see section 4).

2. APPARATUS.

2.1 Test instruments. Test instrumentation to be used in the radiation test shall be standard laboratory electronic test instruments such as power supplies, digital voltmeters, and picoammeters, etc., capable of measuring the electrical parameters required. Parameter test methods and calibration shall be in accordance with MIL-STD-883 or MIL-STD-750, whichever is applicable.

2.2 Radiation source. The radiation source used in the test shall be in a TRIGA Reactor or a Fast Burst Reactor. Operation may be in either pulse or steady-state mode as appropriate. The source shall be one that is acceptable to the acquiring activity.

2.3 Dosimetry equipment.

a. Fast-neutron threshold activation foils such as ^{32}S, ^{54}Fe, and ^{58}Ni.

b. CaF_2 thermoluminescence dosimeters (TLDs).

c. Appropriate activation foil counting and TLD readout equipment.

2.4 Dosimetry measurements.

2.4.1 Neutron fluences. The neutron fluence used for device irradiation shall be obtained by measuring the amount of radioactivity induced in a fast-neutron threshold activation foil such as ^{32}S, ^{54}Fe, or ^{58}Ni, irradiated simultaneously with the device.

A standard method for converting the measured radioactivity in the specific activation foil employed into a neutron fluence is given in the following Department of Defense adopted ASTM standards:

E263	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Iron.
E264	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Nickel.
E265	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Sulfur.

The conversion of the foil radioactivity into a neutron fluence requires a knowledge of the neutron spectrum incident on the foil. If the spectrum is not known, it shall be determined by use of the following DoD adopted ASTM standards, or their equivalent:

E720	-	Standard Guide for Selection of a Set of Neutron-Activation Foils for Determining Neutron Spectra used in Radiation-Hardness Testing of Electronics.
E721	-	Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.
E722	-	Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an Equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.

Once the neutron energy spectrum has been determined and the equivalent monoenergetic fluence calculated, then an appropriate monitor foil (such as ^{32}S, ^{54}Fe, or ^{58}Ni) should be used in subsequent irradiations to determine the neutron fluence as discussed in E722. Thus, the neutron fluence is described in terms of the equivalent monoenergetic neutron fluence per unit monitor response. Use of a monitor foil to predict the equivalent monoenergetic neutron fluence is valid only if the energy spectrum remains constant.

2.4.2 Dose measurements. If absorbed, dose measurements of the gamma-ray component during the device test irradiations are required, then such measurements shall be made with CaF_2 thermoluminescence dosimeters (TLDs), or their equivalent. These TLDs shall be used in accordance with the recommendations of the following DoD adopted ASTM standard:

E668	-	Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

3. PROCEDURE.

3.1 Safety requirements. Neutron irradiated parts may be radioactive. Handling and storage of test specimens or equipment subjected to radiation environments shall be governed by the procedures established by the local Radiation Safety Officer or Health Physicist.

NOTE: The receipt, acquisition, possession, use, and transfer of this material after irradiation is subject to the regulations of the U.S. Nuclear Regulatory Commission, Radioisotope License Branch, Washington, DC 20555. A by-product license is required before an irradiation facility will expose any test devices. (U.S. Code, see 10 CFR 30-33.)

3.2 Test samples. A test sample shall be randomly selected and consist of a minimum of 10 parts, unless otherwise specified. All sample parts shall have met all the requirements of the governing specification for that part. Each part shall be serialized to enable pre and post test identification and comparison.

3.3 Pre-exposure.

3.3.1 Electrical tests. Pre-exposure electrical tests shall be performed on each part as required. Where delta parameter limits are specified, the pre-exposure data shall be recorded.

3.3.2 Exposure set-up. Each device shall be mounted unbiased and have its terminal leads either all shorted or all open. For MOS devices or any microcircuit containing an MOS element, all leads shall be shorted. An appropriate mounting fixture which will accommodate both the sample and the required dosimeters (at least one actuation foil and one CaF_2 TLD) shall be used. The configuration of the mounting fixture will depend on the type of reactor facility used and should be discussed with reactor facility personnel. Test devices shall be mounted such that the total variation of fluence over the entire sample does not exceed 20 percent. Reactor facility personnel shall determine both the position of the fixture and the appropriate pulse level or power time product required to achieve the specified neutron fluence level.

3.4 Exposure. The test devices and dosimeters shall be exposed to the neutron fluence as specified. The exposure level may be obtained by operating the reactor in either the pulsed or power mode. If multiple exposures are required, the post-radiation electrical tests shall be performed (see 3.5.1) after each exposure. A new set of dosimeters are required for each exposure level. Since the effects of neutrons are cumulative, each additional exposure will have to be determined to give the specified total accumulated fluence. All exposures shall be made at 20°C ±10°C and shall be correlated to a 1 MeV equivalent fluence.

3.5 Post-exposure.

3.5.1 Electrical tests. Test items shall be removed only after clearance has been obtained from the Health Physicist at the test facility. The temperature of the sample devices must be maintained at 20°C±10°C from the time of the exposure until the post-electrical tests are made. The post-exposure electrical tests as specified shall be made within 24 hours after the completion of the exposure. If the residual radioactivity level is too high for safe handling, this level to be determined by the local Radiation Safety Officer, the elapsed time before post- test electrical measurements are made may be extended to 1 week. Alternatively, provisions may be made for remote testing. All required data must be recorded for each device after each exposure.

3.5.2 Anomaly investigation. Parts which exhibit previously defined anomalous behavior (e.g., nonlinear degradation of .125) shall be subjected to failure analysis in accordance with method 5003, MIL-STD-883.

3.6 Reporting. As a minimum, the report shall include the part type number, serial number, manufacturer, controlling specification, the date code and other identifying numbers given by the manufacturer. Each data sheet shall include radiation test date, electrical test conditions, radiation exposure levels, ambient conditions as well as the test data. Where other than specified electrical test circuits are employed, the parameter measurement circuits shall accompany the data. Any anomalous incidents during the test shall be fully explained in footnotes to the data.

4. SUMMARY. The following details shall be specified in the request for test or, when applicable, the acquisition document:

a. Part types.

b. Quantities of each part type to be tested, if other than specified in 3.2.

c. Electrical parameters to be measured in pre and post exposure tests.

d. Criteria for pass, fail, record actions on tested parts.

e. Criteria for anomalous behavior designation.

f. Radiation exposure levels.

g. Test instrument requirements.

h. Radiation dosimetry requirements, if other than 2.3.

i. Ambient temperature, if other than specified herein.

j. Requirements for data reporting and submission, where applicable (see 3.6).

METHOD 1018.2

INTERNAL WATER-VAPOR CONTENT

1. PURPOSE. The purpose of this test is to measure the water-vapor content of the atmosphere inside a metal or ceramic hermetically-sealed device. It can be destructive (procedures 1 and 2) or nondestructive (procedure 3).

2. APPARATUS. The apparatus for the internal water-vapor content test shall be as follows for the chosen procedure:

2.1 Procedure 1. (Procedure 1 measures the water-vapor content of the device atmosphere by mass spectrometry.) The apparatus for procedure 1 shall consist of:

a. A mass spectrometer capable of reproducibly detecting the specified moisture content for a given volume package with a factor of ten sensitivity safety margin (i.e., for a specified limit of 5,000 ppmv, .01 cc, the mass spectrometer shall demonstrate a 500 ppmv or less absolute sensitivity to moisture for a package volume of .01 cc). The smallest volume shall be considered the worst case. The calibration of the mass spectrometer shall be accomplished at the specified moisture limit (±20 percent) using a package simulator which has the capability of generating at least three known volumes of gas ±10 percent on a repetitive basis by means of a continuous sample volume purge of known moisture content ±10 percent. Moisture content shall be established by the standard generation techniques (i.e., 2 pressure, divided flow, or cryogenic method). The absolute moisture shall be measured by an NIST calibrated moisture dew point analyzer at least once every 2 years. The NIST calibrated dew pointer shall be returned to the National Institute of Standards and Technology at least once each year for recalibration. Calibration records shall be kept on a daily basis and made available to DCMA personnel. Gas analysis results obtained by this method shall be considered valid only in the moisture range or limit bracketed by at least two (volume or concentration) calibration points (i.e., 5,000 ppmv between .01 - .1 cc or 1,000 - 5,000 ppmv between .01 - .1 cc). A best fit curve shall be used between volume calibration points. Corrections of sensitivity factors deviating greater than 10 percent from the mean between calibration points shall be required.

b. A vacuum opening chamber which can contain the device and a vacuum transfer passage connecting the device to the mass spectrometer of 2.1a. The transfer passage shall be maintained at 125°C ±5°C. The fixturing in the vacuum opening chamber shall position the specimen as required by the piercing arrangement of 2.1c, and maintain the device at 100°C ±5°C for a minimum of 10 minutes prior to piercing.

c. A piercing arrangement functioning within the opening chamber or transfer passage of 2.1b, which can pierce the specimen housing (without breaking the mass spectrometer chamber vacuum and without disturbing the package sealing medium), thus allowing the specimen's internal gases to escape into the chamber and mass spectrometer.

NOTE: A sharp-pointed piercing tool, actuated from outside the chamber wall via a bellows to permit movement, should be used to pierce both metal and ceramic packages. For ceramic packages, the package lid or cover should be locally thinned by abrasion to facilitate localized piercing.

2.2 Procedure 2. (Procedure 2 measures the water-vapor content of the device atmosphere by integrating moisture picked up by a dry carrier gas at 50°C.) The apparatus for procedure 2 shall consist of:

a. An integrating electronic detector and moisture sensor capable of reproducibly detecting a water-vapor content of 300 ±50 ppmv moisture for the package volume being tested. This shall be determined by dividing the absolute sensitivity in micrograms H_2O by the computed weight of the gas in the device under test, and then correcting to ppmv.

b. A piercing chamber or enclosure, connected to the integrating detector of 2.2a, which will contain the device specimen and maintain its temperature at 100°C ±5°C during measurements. The chamber shall position the specimen as required by the piercing arrangement. The piercing mechanism shall open the package in a manner which will allow the contained gas to be purged out by the carrier gas or removed by evacuation. The sensor and connection to the piercing chamber will be maintained at a temperature of 50°C ±2°C.

2.3 Procedure 3. (Procedure 3 measures the water-vapor content of the device atmosphere by measuring the response of a calibrated moisture sensor or an IC chip which is sealed within the device housing, with its electrical terminals available at the package exterior.) The apparatus for procedure 3 shall consist of one of the following:

a. A moisture sensor element and readout instrument capable of detecting a water-vapor content of 300 ±50 ppmv while sensor is mounted inside a sealed device.

b. Metallization runs on the device being tested isolated by back-biased diodes which when connected as part of a bridge network can detect 2,000 ppmv within the cavity. The chip shall be cooled in a manner such that the chip surface is the coolest surface in the cavity. The device shall be cooled below dew point and then heated to room temperature as one complete test cycle.

NOTE: Suitable types of sensors may include (among others) parallel or interdigitated metal stripes on an oxidized silicon chip, and porous anodized-aluminum structures with gold-surface electrodes.

Surface conductivity sensors may not be used in metal packages without external package wall insulation. When used, the sensor shall be the coolest surface in the cavity. It should be noted that some surface conductivity sensors require a higher ionic content than available in ultraclean CERDIP packages. In any case, correlation with mass spectrometer procedure 1 shall be established by clearly showing that the sensor reading can determine whether the cavity atmosphere has more or less than the specified moisture limit at 100°C.

3. PROCEDURE. The internal water-vapor content test shall be conducted in accordance with the requirement of procedure 1, procedure 2, or procedure 3. Devices containing desiccants or organics shall be prebaked for 12 to 24 hours at 100°C ±5°C prior to hot insertion into apparatus.

3.1 Procedure 1. The device shall be hermetic in accordance with test method 1014, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion, the device and chamber shall be pumped down and baked out at a temperature of 100°C ±5°C until the background pressure level will not prevent achieving the specified measurement accuracy and sensitivity. After pumpdown, the device case or lid shall be punctured and the following properties of the released gases shall be measured, using the mass spectrometer:

a. The increase in chamber pressure as the gases are released by piercing the device package. A pressure rise of less than 50 percent of normal for that package volume and pressurization may indicate that (1) the puncture was not fully accomplished, (2) the device package was not sealed hermetically, or (3) does not contain the normal internal pressure.

b. The water-vapor content of the released gases, as a proportion (by volume) of the total gas content.

c. The proportions (by volume) of the other following gases: N_2, He, Mass 69 (fluorocarbons), O_2, Ar, H_2, CO_2, CH_4, and other solvents, if available. Calculations shall be made and reported on all gases present greater than 1 percent by volume. Data reduction shall be performed in a manner which will preclude the cracking pattern interference from other gas specie in the calculations of moisture content. Data shall be corrected for any system dependent matrix effects such as the presence of hydrogen in the internal ambient.

3.1.1 Failure criteria.

a. A device which has a water-vapor content greater than the specified maximum value shall constitute a failure.

b. A device which exhibits an abnormally low total gas content, as defined in 3.1a, shall constitute a failure, if it is not replaced. Such a device may be replaced by another device from the same population; if the replacement device exhibits normal total gas content for its type, neither it nor the original device shall constitute a failure for this cause.

c. Data analysis on devices containing desiccants or organics shall be terminated after 95 percent of the gas has been analyzed in a dynamic measurement system or data shall be taken after pressure has stabilized for a period of 2 minutes in a static system or in any manner which approaches the true measurement of ambient moisture in equilibrium at 100°C within the cavity.

3.2 Procedure 2. The device shall be hermetic in accordance with test method 1014, and free from any surface contaminants which may interfere with accurate water-vapor content measurement.

After device insertion into the piercing chamber, gas shall be flowed through the system until a stable base-line value of the detector output is attained. With the gas flow continuing, the device package shall then be pierced so that a portion of the purge gas flows through the package under test and the evolved moisture integrated until the base-line detector reading is again reached. An alternative allows the package gas to be transferred to a holding chamber which contains a moisture sensor and a pressure indicator. System is calibrated by injecting a known quantity of moisture or opening a package of known moisture content.

3.2.1 Failure criteria.

a. A device which has a water-vapor content (by volume) greater than the specified maximum value shall constitute a failure.

b. After removal from the piercing chamber, the device shall be inspected to ascertain that the package has been fully opened. A device package which was not pierced shall constitute a failure, if the test is not performed on another device from the same population; if this retest sample or replacement is demonstrated to be pierced and meets the specified water-vapor content criteria, the specimen shall be considered to have passed the test.

c. A package which is a leaker in the purge case will be wet and counted as a failure. In the case of evacuation, a normal pressure rise shall be measured as in 3.1a.

3.3 Procedure 3. The moisture sensor shall be calibrated in an atmosphere of known water-vapor content, such as that established by a saturated solution of an appropriate salt or dilution flow stream. It shall be demonstrated that the sensor calibration can be verified after package seal or that post seal calibration of the sensor by lid removal is an acceptable procedure.

The moisture sensor shall be sealed in the device package or, when specified, in a dummy package of the same type. This sealing shall be done under the same processes, with the same die attach materials and in the same facilities during the same time period as the device population being tested.

The water-vapor content measurement shall be made, at 100°C or below, by measuring the moisture sensor response. Correlation with procedure 1 shall be accomplished before suitability of the sensor for procedure 3 is granted. It shall be shown the package ambient and sensor surface are free from any contaminating materials such as organic solvents which might result in a lower than usual moisture reading.

3.3.1 Failure criteria. A specimen which has a water-vapor content greater than the specified maximum value shall constitute a failure.

* 4. IMPLEMENTATION. Suitability for performing method 1018 analysis is granted by the qualifying activity for specific limits and volumes. Method 1018 calibration procedures and the suitability survey are designed to guarantee ±20 percent lab-to-lab correlation in making a determination whether the sample passes or fails the specified limit. Water vapor contents reported either above or below the (water vapor content - volume) range of suitability are not certified as correlatable values. This out of specification data has meaning only in a relative sense and only when one laboratory's results are being compared. Suitability status has been granted for a specification limit of 5,000 ppmv and package volumes falling between .01 cc and .85 cc. The range of suitability for each laboratory will be extended by the qualifying activity when the analytical laboratories demonstrate an expanded capability. Information on current analytical laboratory suitability status can be obtained by writing DSCC-VQC, 3990 East Broad Street, Columbus, OH 43216-5000 or by calling 614-692-0601.

5. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The procedure (1, 2, or 3) when a specific procedure is to be used (see 3).

b. The maximum allowable water-vapor content falling within the range of suitability as specified in test method 5005, 5008, or 5010.

METHOD 1019.4

IONIZING RADIATION (TOTAL DOSE) TEST PROCEDURE

1. PURPOSE. This test procedure defines the requirements for testing packaged semiconductor integrated circuits for ionizing radiation (total dose) effects from a cobalt-60 (^{60}Co) gamma ray source. In addition this procedure provides an accelerated aging test for estimating low dose rate ionizing radiation effects on devices. This aging test is important for low dose-rate or certain other applications in which devices may exhibit significant time-dependent effects. This procedure addresses only steady state irradiations, and is not applicable to pulse type irradiations. This test may produce severe degradation of the electrical properties of irradiated devices and thus should be considered a destructive test.

1.1 Definitions. Definitions of terms used in this procedure are given below:

a. Ionizing radiation effects. The changes in the electrical parameters of a device or integrated circuit resulting from radiation-induced charge. It is also referred to as total dose effects.

b. In-flux test. Electrical measurements made on devices during irradiation exposure.

c. Not in-flux test. Electrical measurements made on devices at any time other than during irradiation.

d. Remote tests. Electrical measurements made on devices which are physically removed from the radiation location.

e. Time dependent effects. Significant degradation in electrical parameters caused by the growth or annealing or both of radiation-induced trapped charge after irradiation. Similar effects also take place during irradiation.

f. Accelerated aging test. A procedure utilizing elevated temperature to accelerate time-dependent effects.

2. APPARATUS. The apparatus shall consist of the radiation source, electrical test instrumentation, test circuit board(s), cabling, interconnect board or switching system, an appropriate dosimetry measurement system, and an environmental chamber (if required for time-dependent effects measurements). Adequate precautions shall be observed to obtain an electrical measurement system with sufficient insulation, ample shielding, satisfactory grounding, and suitable low noise characteristics.

2.1 Radiation source. The radiation source used in the test shall be the uniform field of a ^{60}Co gamma ray source. Uniformity of the radiation field in the volume where devices are irradiated shall be within ±10 percent as measured by the dosimetry system, unless otherwise specified. The intensity of the gamma ray field of the ^{60}Co source shall be known with an uncertainty of no more than ±5 percent. Field uniformity and intensity can be affected by changes in the location of the device with respect to the radiation source and the presence of radiation absorption and scattering materials.

2.2 Dosimetry system. An appropriate dosimetry system shall be provided which is capable of carrying out the measurements called for in 3.2. The following American Society for Testing and Materials (ASTM) standards or other appropriate standards shall be used:

ASTM E 666 - Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.

ASTM E 668 - Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

ASTM E 1249 - Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.

ASTM E 1250 - Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.

ASTM E 1275 - Standard Practice for Use of a Radiochromic Film Dosimetry System.

These industry standards address the conversion of absorbed dose from one material to another, and the proper use of various dosimetry systems. 1/

2.3 Electrical test instruments. All instrumentation used for electrical measurements shall have the stability, accuracy, and resolution required for accurate measurement of the electrical parameters. Any instrumentation required to operate in a radiation environment shall be appropriately shielded.

2.4 Test circuit board(s). Devices to be irradiated shall either be mounted on or connected to circuit boards together with any associated circuitry necessary for device biasing during irradiation or for in-situ measurements. Unless otherwise specified, all device input terminals and any others which may affect the radiation response shall be electrically connected during irradiation, i.e., not left floating. The geometry and materials of the completed board shall allow uniform irradiation of the devices under test. Good design and construction practices shall be used to prevent oscillations, minimize leakage currents, prevent electrical damage, and obtain accurate measurements. Only sockets which are radiation resistant and do not exhibit significant leakages (relative to the devices under test) shall be used to mount devices and associated circuitry to the test board(s). All apparatus used repeatedly in radiation fields shall be checked periodically for physical or electrical degradation. Components which are placed on the test circuit board, other than devices under test, shall be insensitive to the accumulated radiation or they shall be shielded from the radiation. Test fixtures shall be made such that materials will not perturb the uniformity of the radiation field intensity at the devices under test. Leakage current shall be measured out of the radiation field. With no devices installed in the sockets, the test circuit board shall be connected to the test system such that all expected sources of noise and interference are operative. With the maximum specified bias for the test device applied, the leakage current between any two terminals shall not exceed ten percent of the lowest current limit value in the pre-irradiation device specification. Test circuit boards used to bias devices during accelerated aging must be capable of withstanding the temperature requirements of the accelerated aging test and shall be checked before and after testing for physical and electrical degradation.

2.5 Cabling. Cables connecting the test circuit boards in the radiation field to the test instrumentation shall be as short as possible. If long cables are necessary, line drivers may be required. The cables shall have low capacitance and low leakage to ground, and low leakage between wires.

2.6 Interconnect or switching system. This system shall be located external to the radiation environment location, and provides the interface between the test instrumentation and the devices under test. It is part of the entire test system and subject to the limitation specified in 2.4 for leakage between terminals.

2.7 The environmental chamber. The environmental chamber for time-dependent effects testing, if required, shall be capable of maintaining the selected accelerated aging temperature within ±5°C.

1/ Copies may be obtained from the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.

3. PROCEDURE. The test devices shall be irradiated and subjected to accelerated aging testing (if required for time-dependent effects testing) as specified by a test plan. This plan shall specify the device description, irradiation conditions, device bias conditions, dosimetry system, operating conditions, measurement parameters and conditions, and accelerated aging test conditions (if required).

3.1 Sample selection and handling. Only devices which have passed the electrical specifications as defined in the test plan shall be submitted to radiation testing. Unless otherwise specified, the test samples shall be randomly selected from the parent population and identically packaged. Each part shall be individually identifiable to enable pre- and post-irradiation comparison. For device types which are ESD-sensitive, proper handling techniques shall be used to prevent damage to the devices.

* 3.2 Burn-in. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within postirradiation specified electrical limits) on the total dose radiation response, then one of the following must be done:

* 3.2.1 The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing or

* 3.2.2 The manufacturer shall develop a correction factor, (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

* 3.3 Dosimetry measurements. The radiation field intensity at the location of the device under test shall be determined prior to testing by dosimetry or by source decay correction calculations, as appropriate, to assure conformance to test level and uniformity requirements. The dose to the device under test shall be determined one of two ways: (1) by measurement during the irradiation with an appropriate dosimeter, or (2) by correcting a previous dosimetry value for the decay of the ^{60}Co source intensity in the intervening time. Appropriate correction shall be made to convert from the measured or calculated dose in the dosimeter material to the dose in the device under test.

* 3.4 Lead/Aluminum (Pb/Al) container. Test specimens shall be enclosed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. A minimum of 1.5 mm Pb, surrounding an inner shield of at least 0.7 mm Al, is required. This Pb/Al container produces an approximate charged particle equilibrium for Si and for TLDs such as CaF_2 The radiation field intensity shall be measured inside the Pb/Al container (1) initially, (2) when the source is changed, or (3) when the orientation or configuration of the source, container, or test-fixture is changed. This measurement shall be performed by placing a dosimeter (e.g., a TLD) in the device-irradiation container at the approximate test-device position. If it can be demonstrated that low energy scattered radiation is small enough that it will not cause dosimetry errors due to dose enhancement, the Pb/Al container may be omitted.

* 3.5 Radiation level(s). The test devices shall be irradiated to the dose level(s) specified in the test plan within ±10 percent. If multiple irradiations are required for a set of test devices, then the post-irradiation electrical parameter measurements shall be performed after each irradiation.

* 3.6 Radiation dose rate.

CAUTION: For the application of some bipolar and biCMOS devices to space-level dose rates, testing at condition A dose rates may not provide worst case results. These are devices that fail due to reduced transistor gain. For such devices, the excess base current has been observed to increase at decreasing dose rates. For these devices, testing shall be accomplished at the lowest dose rate of interest in accordance with conditions B or C in order to obtain a conservative estimate of the device performance.

* 3.6.1 Condition A. For condition A (standard condition) the dose rate shall be between 50 and 300 rads(Si)/s [0.5 and 3 Gy(Si)/s] ^{60}Co 2/ The dose rates may be different for each radiation dose level in a series; however, the dose rate shall not vary by more than ±10 percent during each irradiation.

2/ The SI unit for the quantity absorbed dose is the gray, symbol GY. 100 rads = 1 Gy.

* 3.6.2 Condition B. For condition B, if the maximum dose rate is < 50 rads(Si)/s in the intended application, the parties to the test may agree to perform the test at a dose rate ≥ the maximum dose rate of the intended application. Unless the exclusions in 3.11.1b are met, the accelerated aging test of 3.11.2 shall be performed.

* 3.6.3 Condition C. For condition C, (as an alternative) the test may be performed at the dose rate of the intended application if this is agreed to by the parties to the test.

3.7 Temperature requirements. Since radiation effects are temperature dependent, devices under test shall be irradiated in an ambient temperature of 24°C ±6°C as measured at a point in the test chamber in close proximity to the test fixture. The electrical measurements shall be performed in an ambient temperature of 25°C ±5°C. If devices are transported to and from a remote electrical measurement site, the temperature of the test devices shall not be allowed to increase by more than 10°C from the irradiation environment. If any other temperature range is required, it shall be specified.

* 3.8 Electrical performance measurements. The electrical parameters to be measured and functional tests to be performed shall be specified in the test plan. As a check on the validity of the measurement system and pre- and post-irradiation data, at least one control sample shall be measured using the operating conditions provided in the governing device specifications. For automatic test equipment, there is no restriction on the test sequence provided that the rise in the device junction temperature is minimized. For manual measurements, the sequence of parameter measurements shall be chosen to allow the shortest possible measurement period. When a series of measurements is made, the tests shall be arranged so that the lowest power dissipation in the device occurs in the earliest measurements and the power dissipation increases with subsequent measurements in the sequence.

The pre- and post-irradiation electrical measurements shall be done on the same measurement system and the same sequence of measurements shall be maintained for each series of electrical measurements of devices in a test sample. Pulse-type measurements of electrical parameters should be used as appropriate to minimize heating and subsequent annealing effects. Devices which will be subjected to the accelerated aging testing (see 3.11) may be given a preirradiation burn-in to eliminate burn-in related failures.

* 3.9 Test conditions. The use of in-flux or not in-flux testing shall be specified in the test plan. (This may depend on the intended application for which the data is being obtained.) The use of in-flux testing may help to avoid variations introduced by post-irradiation time dependent effects. However, errors may be incurred for the situation where a device is irradiated in-flux with static bias, but where the electrical testing conditions require the use of dynamic bias for a significant fraction of the total irradiation period. Not-in-flux testing generally allows for more comprehensive electrical testing, but can be misleading if significant post-irradiation time dependent effects occur.

* 3.9.1 In-flux testing. Each test device shall be checked for operation within specifications prior to being irradiated. After the entire system is in place for the in-flux radiation test, it shall be checked for proper interconnections, leakage (see 2.4), and noise level. To assure the proper operation and stability of the test setup, a control device with known parameter values shall be measured at all operational conditions called for in the test plan. This measurement shall be done either before the insertion of test devices or upon completion of the irradiation after removal of the test devices or both.

* 3.9.2 Remote testing. Unless otherwise specified, the bias shall be removed and the device leads placed in conductive foam (or similarly shorted) during transfer from the irradiation source to a remote tester and back again for further irradiation. This minimizes post-irradiation time dependent effects.

* 3.9.3 Bias and loading conditions. Bias conditions for test devices during irradiation or accelerated aging shall be within ±10 percent of those specified by the test plan. The bias applied to the test devices shall be selected to produce the greatest radiation induced damage or the worst-case damage for the intended application, if known. The specified bias shall be maintained on each device in accordance with the test plan. Bias shall be checked immediately before and after irradiation. Care shall be taken in selecting the loading such that the rise in the junction temperature is minimized.

* 3.10 Post-irradiation procedure. *Unless otherwise specified, the following time intervals shall be observed:*

a. The time from the end of an irradiation to the start of electrical measurements shall be a maximum of 1 hour.

b. The time to perform the electrical measurements and to return the device for a subsequent irradiation, if any, shall *be within two hours of the end of the prior irradiation.*

To minimize time dependent effects, these intervals shall be as short as possible. The sequence of parameter measurements shall be maintained constant throughout the tests series.

* 3.11 MOS accelerated aging test. The accelerated aging test provides an estimate of worst-case degradation of MOS microcircuits in low dose rate environments. The procedure involves heating the device following irradiation at specified temperature, time and bias conditions. An accelerated aging test (see 3.11.2) shall be performed for cases where time dependent effects (TDE) can cause a device to degrade significantly or fail. Only standard testing shall be performed as specified in 3.1 through 3.10 for cases where TDE are known not to cause significant device degradation or failure (see 3.11.1) or where they do not need to be considered, as specified in 3.11.1.

* 3.11.1 Need to perform accelerated aging test. The parties to the test shall take appropriate steps to determine whether accelerated aging testing is required. The following criteria shall be used:

a. The tests called out in 3.11.2 shall be performed for any device or circuit type that contains MOS circuit elements (i.e., transistors or capacitors).

b. TDE tests may be omitted if:

1. circuits are known not to contain MOS elements by design, or

2. the ionizing dose in the application, if known, is below 5 krads(Si), or

3. the lifetime of the device from the onset of the irradiation in the intended application, if known, is short compared with TDE times, or

4. the test is carried out at the dose rate of the intended application.

5. the device type or IC technology has been demonstrated via characterization testing not to exhibit TDE changes in device parameters greater than experimental error (or greater than an otherwise specified upper *limit) and the variables that affect* TDE response are demonstrated to be under control for the specific vendor processes, or

At a minimum, the characterization testing in (5) shall include an assessment of TDE on propagation delay, output drive, and minimum operating voltage parameters. Continuing process control of variables affecting TDE may be demonstrated through lot sample tests of the radiation hardness of MOS test structures.

c. This document provides no guidance on the need to perform accelerated aging tests on technologies that do not include MOS circuit elements.

* 3.11.2 Accelerated aging test procedure. If the device passes the tests in 3.1 through 3.10 to the total ionizing dose level specified in the test plan or device specification or drawing and the exclusions of 3.11.1 do not apply, the accelerated aging test shall be conducted as follows:

a. Overtest.

1. Irradiate each test device to an additional 0.5-times the specified dose using the standard test conditions (3.1 through 3.10). Note that no electrical testing is required at this time.

2. The additional 0.5-times irradiation in 3.11.2.a.1 may be omitted if it has been demonstrated via characterization testing that:

a. none of the circuit propagation delay, output drive, and minimum operating voltage parameters recover toward their pre-irradiation value greater than experimental accelerated aging test of 3.11.2.b, and

b. the irradiation biases chosen for irradiation and accelerated aging tests are worst-case for the response of these parameters during accelerated aging.

The characterization testing to establish worst-case irradiation and aging biases shall be performed at the specified level. The testing shall at a minimum include separate exposures under static and dynamic irradiation bias, each followed by worst-case static bias during accelerated aging according to 3.11.2.b.

b. Accelerated aging. Heat each device under worst-case static bias conditions in an environmental chamber according to one of the following conditions:

1. At 100°C ±5°C for 168 ±12 hours, or

2. At an alternate temperature and time that has been demonstrated via characterization testing to cause equal or greater change in the parameter(s) of interest, e.g., propagation delay, output drive, and minimum operating voltage, in each test device as that caused by 3.11.2.b.1, or

3. At an alternate temperature and time which will cause trapped hole annealing of >60% and interface state annealing of <10% as determined via characterization testing of NMOS test transistors from the same process. It shall be demonstrated that the radiation response of test transistors represent that of the device under test.

c. Electrical testing. Following the accelerated aging, the electrical test measurements shall be performed as specified in 3.8 and 3.9.

* 3.12 Test report. As a minimum, the report shall include the device type number, serial number, the manufacturer, package type, controlling specification, date code, and any other identifying numbers given by the manufacturer. The bias circuit, parameter measurement circuits, the layout of the test apparatus with details of distances and materials used, and electrical noise and current leakage of the electrical measurement system for in-flux testing shall be reported using drawings or diagrams as appropriate. Each data sheet shall include the test date, the radiation source used, the bias conditions during irradiation, the ambient temperature around the devices during irradiation and electrical testing, the duration of each irradiation, the time between irradiation and the start of the electrical measurements, the duration of the electrical measurements and the time to the next irradiation when step irradiations are used, the irradiation dose rate, electrical test conditions, dosimetry system and procedures and the radiation test levels. The pre- and post-irradiation data shall be recorded for each part and retained with the parent population data in accordance with the requirements of MIL-PRF-38535 or MIL-PRF-38534. Any anomalous incidents during the test shall be fully documented and reported. The accelerated aging procedure, if used, shall be described. Any other radiation test procedures or test data required for the delivery shall be specified in the device specification, drawing or purchase order.

* 4. SUMMARY. The following details shall be specified in the applicable acquisition document as required:

a. Device-type number(s), quantity, and governing specifications (see 3.1).

b. Radiation dosimetry requirements (see 3.3).

c. Radiation test levels including dose and dose rate (see 3.5 and 3.6).

d. Irradiation, electrical test and transport temperatures if other than as specified in 3.7.

e. Electrical parameters to be measured and device operating conditions during measurement (see 3.8).

f. Test conditions, i.e., in-flux or not-in-flux type tests (see 3.9).

g. Bias conditions for devices during irradiation (see 3.9.3).

h. Time intervals of the post-irradiation measurements (see 3.10).

i. Requirement for accelerated aging test, if required (see 3.11).

j. Documentation required to be delivered with devices (see 3.12).

FIGURE 1019-1. Flow diagram for ionizing radiation test procedure.

METHOD 1020.1

DOSE RATE INDUCED LATCHUP TEST PROCEDURE

1. PURPOSE. This test procedure defines the detailed requirements for performing latchup testing of microcircuits to identify susceptibility to dose rate induced latchup.

1.1 Definitions. Definitions of terms used in this procedure are provided below:

a. Dose rate induced latchup. Dose rate induced latchup is regenerative device action in which a parasitic region (e.g., a four layer p-n-p-n or n-p-n-p path) is turned on by a photocurrent generated by a pulse of ionizing radiation, and remains on for an indefinite period of time after the photocurrent subsides. The device will remain latched as long as the power supply delivers voltage greater than the holding voltage and current greater than the holding current. Latchup disrupts normal circuit operation in some portion of the circuit, and may also cause catastrophic failure due to local heating of semiconductor regions, metallization or bond wires.

b. Latchup windows. A latchup window is the phenomenon in which a device exhibits latchup in a specific range of dose rates. Above and below this range, the device does not latchup. A device may exhibit more than one latchup window. This phenomenon has been observed for some CMOS logic devices, oxide sidewall logic and LSI memories, and may occur in other devices.

c. Combinational logic. Combinational (determined) logic devices are those whose output is solely determined by the logic signals at its inputs (except for switching delays). Combinational logic circuits contain no internal storage elements, and include multiplexers, decoders, and gates.

d. Sequential logic. Sequential (nondetermined) devices are those in which the output state at any given time depends on the sequence and time relationship of logic signals that were previously applied to its inputs. Sequential logic circuits contain internal storage elements. Examples of sequential logic devices are shift registers, memories, counters, and flip-flops.

e. Recovery period. The recovery period is the time interval in which the device supply current recovers from the radiation pulse.

f. Holding voltage and holding current: The voltage and current above which latchup is sustained.

1.2 Test plan. Prior to latchup testing, a latchup test plan shall be prepared which describes the radiation source, the dosimetry techniques, test equipment and conditions to be used. A detailed procedure for each device type to be tested shall be prepared, either as part of the test plan or in separate test procedure documents. The procedure shall include bias conditions, test sequence, and schematics of the test setup. The test plan shall be approved by the acquiring activity, and as a minimum, the items listed below shall be provided in the test plan or test procedure:

a. Device types, including package types, and quantities to be tested.

b. Traceability requirements, such as requirements for serialization, wafer or lot traceability, etc.

c. Requirements for data reporting and submission.

d. Temperature for test (see 2.3.6).

e. Block diagram or schematic representation of test set up.

f. Electrical parameters to be monitored and device operating conditions, including bias conditions and functional test requirements before, during, and after the radiation pulse.

g. Group A electrical test requirements for pre- and post-latchup testing, to include test limits and failure criteria.

h. Radiation pulse width(s), radiation dose(s) per pulse and dose rate range(s).

i. Total dose limit for each device type.

j. Failure criteria.

In addition to those items listed above, the test plan or procedure for production tests shall include the following:

k. Method(s) to detect latchup, e.g., monitoring of the supply current, functional testing (to include test vector set, etc.).

l. Recovery period and when to begin post-irradiation in-situ tests. The recovery period for SSI devices is typically 50 to 300 μs; however, other device types may require a longer recovery period, or there may be special program requirements which call for earlier recovery.

m. Functional test requirements. The functional tests shall demonstrate that the device responds properly to input commands and that the device is operating properly. Note that high speed functional tests may be incompatible with the long leads and unavoidable capacitance associated with most latchup test systems.

n. Exposure states or operating conditions. For digital devices, a specific state and its complement are usually used. However, for more complex devices, more than two exposure states may be required, and the specific states shall be as determined by the characterization testing (and analysis, if required) and specified in the test plan or procedure.

o. Bias and load conditions. Unless otherwise specified, the maximum rated operating supply voltage shall be used.

p. Outputs to be monitored.

q. The minimum dc current that must be available from the power supply, or the value of series current limiting resistor that has been approved by the acquiring activity. (Note that any current limiting resistor shall be less than or equal to that in the system application and shall be approved by the acquiring activity prior to latchup testing.)

2. APPARATUS. The apparatus shall consist of the radiation source, the dosimetry system, and the latchup test system which includes the device interface fixture, the test circuit, cabling, timing, and temperature control systems. Precautions shall be observed to obtain adequate electrical grounding to ensure low noise.

2.1 Radiation source. Either of two radiation sources shall be used for latchup testing: 1) a flash x-ray machine (FXR), or 2) an electron linear accelerator (LINAC). The FXR shall be used in the x-ray mode and the LINAC in the electron (e-beam) mode. The FXR peak (endpoint) energy shall be 2 MeV or greater, and the LINAC beam energy shall be 10 MeV or greater. The pulse width shall be from 20 to 100 ns, or as specified in the acquisition document, and the uniformity of the radiation field in the device irradiation volume shall be ±15 percent as measured by the dosimetry system. The dose per radiation exposure shall be as specified in the test plan or procedure. (See 3.5.1 for production test requirements.)

* 2.2 Dosimetry system. A dosimetry system shall be used which provides a measurement accuracy within ±15 percent. A calibrated PIN diode may be used to obtain both the shape of the radiation pulse and the dose, and the following DOD adopted American Society for Testing and Materials (ASTM) standards or their equivalent may be used:

ASTM E 666 - Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.
ASTM E 668 - Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation Hardness Testing of Electronic Devices.
ASTM E 1249 - Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.

2.3 Latchup test system. A block diagram of a typical latchup test system is presented on figure 1020-1. The instrumentation shall be capable of establishing the required test conditions and measuring and recording the required parameters. The test system shall be designed to maintain the instantaneous bias supply voltage within the limits specified in 2.3.2 below for both transient and dc conditions, including a latchup condition. The test system shall not limit the ac or dc bias supply current to values that prevent latchup from occurring or being detected. Components other than the device under test (DUT) shall be insensitive to the expected radiation levels, or they shall be shielded from the radiation. The system used for latchup testing shall contain the following elements:

2.3.1 Device interface fixture. The DUT shall be interfaced to the test circuitry with a fixture having good high frequency characteristics, and providing a low inductance connection to the power supply and bypass capacitor.

2.3.2 Bias and functional test circuit. The test circuit for each device type shall provide worst case bias and load conditions for the DUT, and shall perform in-situ functional testing of the DUT as specified in the test plan or procedure. Line drivers shall be used, when necessary, to isolate the DUT from significant extraneous loading by the cabling. The characteristics of the line drivers (e.g., linearity, dynamic range, input capacitance, transient response, and radiation response) shall be such that they do not reduce the accuracy of the test. The power supply shall have low source impedance and meet the following requirements:

a. The power supply voltage shall drop no more than 20 percent at the DUT during the rise time of the DUT during the rise time of the DUT supply current, and no more than 10 percent thereafter. These requirements can be achieved by selecting appropriate capacitance values and minimizing lead lengths of the stiffening capacitors. A high frequency, radiation resistant capacitor shall be placed at the DUT for each bias supply voltage, and larger capacitors may be placed a short distance from the fixture shielded from the radiation.

b. DC power supplies shall provide sufficient current for device operation and to maintain holding current if latchup occurs.

c. Power supplies connected in series with digital ammeters (current probes or current sensors) may be used only if the ammeter is physically located on the power supply side of the bypass capacitor. The ammeter should be selected to minimize the series dc voltage drop at the maximum expected load current. If necessary, the power supply voltage should be adjusted upwards slightly to ensure that the voltage measured at the DUT is within the specified limits for the test conditions.

d. Current limiting resistors shall not be used in series with the supply voltage unless approved by the acquiring activity prior to latchup testing, and the value of the resistance is less than or equal to that in the system application.

   CAUTION: Current limiting resistors can produce a relatively narrow latchup window which may reside entirely outside the standard testing range of 500 ±200 rads(Si). If current limiting is used, especially when used as a means of latchup prevention, characterization tests shall be performed to determine the dose rate appropriate for production testing.

   If current limiting resistors are used, they shall be placed sufficiently close to the DUT to ensure that the voltage drop at the DUT during the transient photocurrent rise time is governed by the resistance and not the inductance from the leads (i.e., voltage drop is approximately IR and not L di/dt). The requirements of paragraphs a-c apply with the reference point being the power supply side of the current limiting resistor, instead of the DUT supply pin(s). For applications using small value bypass capacitors directly at the power supply pin(s), the same, or larger, value of capacitance must be used in the test circuit when current limiting resistors are used. As noted above, leads shall be kept to the minimum practical lengths.

2.3.3 Cabling. Cabling shall be provided to connect the test circuit board to the test instrumentation. All cables shall be as short as possible. Coaxial cables, terminated in their characteristic impedance, should be used if high speed functional testing is to be performed and line drivers are used to isolate the monitoring equipment.

2.3.4 Monitoring and recording equipment. Equipment to monitor and record the parameters required in the test plan or procedure shall be integrated into the latchup test system. Oscilloscopes and transient digitizers may be used to monitor the transient response of the device. Additionally, the dose records from each pulse shall be correlated to the specific device(s) irradiated by that pulse.

2.3.5 Timing control. An adjustable timing control system shall be incorporated into the latchup test system such that post-irradiation in-situ functional testing is performed at the specified time, typically 50 µs to 300 µs, after the radiation pulse. Longer time periods, as long as several minutes, may be required to complete the functional tests for complex devices.

2.3.6 Temperature control. When testing at other than room temperature, a temperature control system shall control the temperature of the DUT to ±10°C of the specified temperature. Unless otherwise specified, latchup testing shall be performed at the highest device operating temperature in the system application or 15°C below the maximum rated temperature of the device, whichever is less. (See cautionary note below.) If an application temperature is not known, or is not available, the device shall be tested at 15°C below the maximum rated temperature. Heat sinking may be required to ensure that the device is not operated above the maximum rated temperature.

CAUTION: The thermal conduction through the latchup test sockets is often much less than that through the pins in soldered boards.

3. PROCEDURE.

3.1 Device identification. In all cases, devices shall be serialized, and the applicable recorded test data shall be traceable to the individual device.

3.2 Radiation safety. All personnel shall adhere to the health and safety requirements established by the local radiation safety officer or health physicist.

3.3 Total dose limit. Unless otherwise specified, any device exposed to more than 10 percent of its total dose limit shall be considered to have been destructively tested. The total dose limit shall be determined for each device type to be tested, and shall be specified in the test plan.

3.4 Characterization testing and analysis. Characterization tests should be performed on new or unfamiliar device types to determine their performance as a function of dose rate and to establish requirements for production testing. Because latchup is dependent on lot to lot variations, samples for characterization tests should be pulled from the production lot(s). The following are examples of information gained from characterization testing:

a. Latchup threshold as a function of radiation dose, dose rate, and pulse width.

b. Existence and dose rate range of latchup windows. To check for windows, latchup testing is performed over a wide range of dose rates in fine increments.

c. Worst case or unique conditions that cause the device to exhibit latchup, such as operating voltage, temperature, and bias conditions.

d. Method(s) to detect latchup, e.g., monitoring supply current, functional testing, or both. Note that in-situ functional tests must be thorough enough to determine if a small portion of a large circuit has latched without drawing enough additional current to significantly increase the device supply current.

e. Group A electrical parameter degradation subsequent to latchup testing.

f. Holding current and holding voltage.

Before testing LSI/VLSI circuits, an analysis is often required to determine likely latchup paths and requirements for bias conditions, exposure states, and functional testing. These large circuits often have too many outputs to be monitored individually, and through the analysis, monitored outputs can be limited to those most apt to show a change should latchup occur.

3.5 Production testing. Prior to production testing, characterization testing shall be performed at least once for new or unfamiliar device types (i.e., new design or process, unfamiliar or very complex devices with little or not latchup test history). The results of the characterization tests are used to develop the requirements for the production tests (see 3.4). These requirements are specified in the applicable test plan or procedure and include those items listed in 1.2.

3.5.1 General requirements for production tests. Unless otherwise specified, the dose per pulse shall be 500 ±200 rad(Si) with a pulse width between 20 and 100 ns, inclusive. Circuits shall be exposed to radiation pulses in at least two difference states (for digital devices) as specified in the test plan or procedure. Unless otherwise specified, determination of latchup shall be based on a combination of DUT supply current and output signal (voltage) recovery within the specified time limits and the results of post-irradiation in-situ functional tests. Power supplied to the DUT shall not be interrupted until after the post-irradiation in-situ tests are completed. The DUT supply current shall be measured immediately before and at the specified time after the radiation pulse to determine if the supply current has returned to within specified limits. A functional test shall be performed immediately after the recovery period to demonstrate that the device functions properly. Unless otherwise specified, tests shall be performed at the highest device operating temperature in the system application or 15°C below the maximum rated temperature of the device, whichever is less. Current limiting resistors are allowed only if prior approval is obtained from the acquiring activity and the value of the resistor is less than or equal to that in the system application. Unless otherwise specified, endpoint electrical tests (group A, subgroups 1 and 7, as a minimum) shall be performed pre- and post-latchup testing. These group A tests are generally not performed in-situ, and there is no time limit on performing the group A tests. If group A testing is performed as part of another test (e.g., post-burn in, final electrical acceptance), the group A tests need not be duplicated as long as the test sequence is: Group A tests - latchup testing - group A tests.

3.5.2 Production test sequence.

CAUTION: Exercise caution when handling devices, particularly with regard to pin alignment in the carriers and holding fixture and when attaching devices to the test circuit. Insure that bias voltage are off before attachment. Observe ESD handling procedures for the class of devices being tested.

The latchup test system, including test circuitry, cables, monitoring, and recording equipment, shall be assembled to provide the specified biasing and output monitoring. Place the DUT in position for the specified dose; ensure that the system is functioning as follows:

Step 1: Apply and verify the bias voltages at the interface fixture with the device removed.

Step 2: Adjust timing control system to provide the required time interval between radiation pulse and post-irradiation measurements.

Step 3: Remove bias voltages and install a control sample device (identical to devices to be tested).

Step 4: Turn on bias voltages and verify proper device function in accordance with performance requirements.

Step 5: Verify proper operation of all recording, monitoring, and timing control equipment.

Step 6: Remove bias voltages and control device, in that order.

Adjust the radiation source to operate in the specified mode to deliver the specified dose. Verify as follows:

Step 7: Put dosimetry in position and expose to radiation pulse. Verify that the dose recording equipment is working properly and that the appropriate dose was delivered.

When the latchup test system, radiation source, and dosimetry system have been verified to be working properly, continue as follows for each device type to be tested:

3.5.2.1 Combinational logic. Latchup tests for combinational logic circuits shall be performed as follows:

Step 8: Install the DUT in the proper position in front of the radiation source, and bring the device to test temperature.

Step 9: Bias the device in accordance with the test plan or procedure and verify proper device functional operation.

Step 10: Load the specified test pattern and verify correct output conditions.

Step 11: Irradiate the device (maintaining above input condition) and record the dose and parameters required by the test plan or procedure.

Step 12: To verify recovery time, measure the DUT supply current at the specified time after the radiation pulse. Verify that the supply current and output voltages have returned to within the specified limits.

Step 13: Perform another functional test and determine if the device passes.

Step 14: Put the device in complement state and repeat steps 10-13. (The number of states in which the device is to be tested shall be specified in the test plan or procedure.)

Step 15: Remove bias voltages and device, in that order.

A combinational device fails the latchup test if the output after the recovery time is not in the proper state, it fails the post-irradiation in-situ functional test, or if the supply current does not return to within specified limits within the specified time after irradiation.

3.5.2.2 Sequential logic. Latchup tests for sequential logic circuits shall be performed as follows:

Step 8: Install the DUT in the proper position in front of the radiation source, and bring the device to test temperature.

Step 9: Bias the device in accordance with the test plan or procedure and verify proper device functional operation.

Step 10: Load the specified test pattern and verify correct output conditions.

Step 11: Irradiate the device (maintaining above input condition) and record the dose and parameters required by the test plan or procedure.

Step 12: To verify recovery time, measure the DUT supply current at the specified time after the radiation pulse. Verify that the supply current and output voltages have returned to within the specified limits.

Step 13: Perform functional test to determine if the device passes.

Step 14: Change the conditions of the initial output to the complement state and repeat steps 10-13. (The number of states in which the device is to be tested shall be specified in the test plan or procedure.)

Step 15: Remove bias voltages and device, in that order.

In sequential logic devices, the radiation pulse can cause logic state changes at the output as well as within internal storage registers. Therefore, the post-radiation verification of recovery must be determined from a combination of device supply current and post-exposure functional test results. A sequential logic device fails the latchup test if the supply current does not return to within specified limits within the specified recovery period or if it fails the functional test requirements. The specified supply current limits must take into account changes in the supply current that may result from changes in the internal logic state and internal registers.

3.5.2.3 Linear devices. Latchup testing for linear devices is inherently device and application specific because of the large number of types of linear circuits and application conditions. Latchup in linear devices is detected through a combination of monitoring the device supply current, monitoring of the output waveform, and in-situ functional tests. The minimum number of monitored outputs shall be as specified in the test plan or procedure, but the in-situ functional test shall exercise all outputs. The transient response of the device output is monitored through the use of an oscilloscope with a camera, or a transient digitizer. An example is shown on figure 1020-2. Trace A shows a device output which operated properly after the radiation pulse, and trace B shows an output that failed. Note that the device will not respond properly to the oscillating input after the radiation exposure. Testing of linear devices is performed as follows:

Step 8: Install the DUT in the proper position in front of the radiation source, and bring the device up to test temperature.

Step 9: Bias the device in accordance with the test plan or procedure and verify proper device functional operation.

Step 10: Adjust input signal as specified in the test plan or procedure and verify correct output level.

Step 11: Irradiate the device and record the dose. Monitor the supply current and output voltages during and after the pulse, and measure the recovery times of the supply current and the output voltages. Monitor the waveform of the output.

Step 12: After the recovery period, determine if the device supply currents have returned to within the specified limits.

Step 13: Determine if the output voltages have returned to within specified limits in the specified recovery time. Ensure device responds properly to input commands, and compare pre-rad and post-rad waveforms.

Step 14: Change the conditions of the input as specified in the test plan or procedure and repeat steps 10-13. (The number of conditions in which the device is to be tested shall be specified in the test plan or procedure.)

Step 15: Remove the bias voltages and device, in that order.

A linear device fails the latchup test if the supply current or the output signals (or voltages) do not recover within the recovery period specified in the test plan, or if the outputs do not respond properly to an input signal.

3.5.2.4 Other device types. For other types of microcircuits, such as LSI/VLSI and greater complexity circuits and hybrid microcircuits, the worst case bias conditions, exposure states, outputs to be monitored, necessary post-irradiation testing, and failure criteria are determined through a combination of characterization testing and analysis. These requirements are specified in the test plan or procedure for each device. Depending on the circuit type, the device is tested as described in 3.5.2.1 to 3.5.2.3.

4. REPORT. A latchup test report shall be prepared in which the devices tested are identified by device type, manufacturer, date code, and lot/wafer identification. The report shall list by device serial number, pass/fail status of each device and the doses (or dose range) delivered to each device in each radiation pulse. The test plan and procedure shall either be appended to the test report or referenced in the test report.

5. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Device types and quantities to be tested.

b. Temperature of test (see 2.3.6).

c. Traceability (device number, wafer/lot number, etc.) requirements and requirements for data reporting and submission.

d. The maximum allowable recovery period.

e. Radiation pulse width and radiation dose per pulse.

f. Total dose limit for each device type.

g. Requirements for group A electrical testing pre- and post-latchup testing.

h. Test instrument requirements, if other than those indicated above.

i. Requirements for characterization, recharacterization, and analysis.

j. Minimum dc power supply current required, or value of current limiting resistor, if allowed.

FIGURE 1020-1. Latchup system.

FIGURE 1020-2. Linear device latchup screen test photograph (50 µs/div).

METHOD 1021.2

DOSE RATE UPSET TESTING OF DIGITAL MICROCIRCUITS

1. PURPOSE. This test procedure defines the requirements for testing the response of packaged digital integrated circuits to pulsed ionizing radiation. A flash x-ray or linear accelerator is used as a source of pulses of ionizing radiation. The response may include transient output signals, changes in the state of internal storage elements, and transient current surges at inputs, outputs, and power supply connections. The dose rate at which logic or change-of-state errors first occur is of particular interest in many applications.

1.1 Definitions. Definitions of terms used in this procedure are given below:

a. Dose rate threshold for upset. The dose rate which causes either:

(1) A transient output upset for which the change in output voltage of an operating digital integrated circuit goes either above or below (as appropriate) specified logic levels (see 3.2 on transient voltage criteria), and the circuit spontaneously recovers to its preirradiation condition after the radiation pulse subsides, or

(2) A stored data or logic state upset for which there is a change in the state of one or more internal memory or logic elements that does not recover spontaneously after the radiation pulse. However, the circuit can be restored to its preirradiation condition by applying the same sequence of logic signals to its inputs that were previously used to establish the preirradiation condition, or

(3) A dynamic upset which results in a change in the expected output or stored test pattern of a device that is functionally operating during the time it is irradiated. The upset response may depend on the precise time relationship between the radiation pulse and the operating cycle of the device. For operations requiring many clock signals, it may be necessary to use a wide radiation pulse.

b. Dose rate. Energy absorbed per unit time per unit mass by a given material from the radiation field to which it is exposed.

c. Combinational logic circuit. A digital logic circuit with the property that its output state is solely determined by the logic signals at its inputs. Combinational logic circuits contain no internal storage elements. Examples of combinational circuits include gates, multiplexers, and decoders.

d. Sequential logic circuit. A digital logic circuit with the property that its output state at a given time depends on the sequence and time relationship of logic signals that were previously applied to its inputs. Sequential logic circuits contain internal storage elements. Examples of sequential logic circuits include memories, shift registers, counters, and flip-flops.

e. State vector. A state vector completely specifies the logic condition of all elements within a logic circuit. For combinational circuits the state vector includes the logic signals that are applied to all inputs; for sequential circuits the state vector must also include the sequence and time relationship of all input signals (this may include many clock cycles).

1.2 Interferences. There are several interferences that need to be considered when this test procedure is applied. These include:

a. Total dose damage. Devices may be permanently damaged by total dose. This limits the number of radiation pulses that can be applied during transient upset testing. The total dose sensitivity depends on fabrication techniques and device technology. MOS devices are especially sensitive to total dose damage. Newer bipolar devices with oxide-isolated sidewalls may also be affected by low levels of total dose. The maximum total dose to which devices are exposed must not exceed 20 percent of the typical total dose failure level of the specific part type.

b. Steps between successive radiation levels. The size of the steps between successive radiation levels limits the accuracy with which the dose rate upset threshold is determined. Cost considerations and total dose damage limit the number of radiation levels that can be used to test a particular device.

c. Latchup. Some types of integrated circuits may be driven into a latchup condition by transient radiation. If latchup occurs, the device will not function properly until power is temporarily removed and reapplied. Permanent damage may also occur, primarily due to the large amount of localized heating that results. Although latchup is an important transient response mechanism, this procedure does not apply to devices in which latchup occurs. Functional testing after irradiation is required to detect internal changes of state, and this will also detect latchup. However, if latchup occurs it will usually not be possible to restore normal operation without first interrupting the power supply.

d. Limited number of state vectors. Cost, testing time, and total dose damage usually make it necessary to restrict upset testing to a small number of state vectors. These state vectors must include the most sensitive conditions in order to avoid misleading results. An analysis is required to select the state vectors used for radiation testing to make sure that circuit and geometrical factors that affect the upset response are taken into account (see 3.1).

2. APPARATUS. Before testing can be done, the state vectors must be selected for radiation testing. This requires a logic diagram of the test device. The apparatus used for testing shall consist of the radiation source, dosimetry equipment, a test circuit board, line drivers, cables, and electrical test instrumentation to measure the transient response, provide bias, and perform functional tests. Adequate precautions shall be observed to obtain an electrical measurement system with ample shielding, satisfactory grounding, and low noise from electrical interference or from the radiation environment.

2.1 Radiation source. The radiation source used in this test shall be either a flash x-ray machine (FXR) used in the photon mode or a linear accelerator (LINAC) used in the electron beam mode. The LINAC beam energy shall be greater than 10 MeV. The radiation source shall provide a uniform (within 20 percent) radiation level across the area where the device and the dosimeter will be placed. The radiation pulse width for narrow pulse measurements shall be between 10 and 50 ns. For narrow pulse measurements either a LINAC or FXR may be used. Wide pulse measurements (typically 1 - 10 μs) shall be performed with a LINAC. The pulse width for LINAC irradiations shall be specified. The dose rate at the location of the device under test shall be adjustable between 10^8 and 10^{12} rads(Si)/s (or as required) for narrow pulse measurements and between 10^5 and 10^{11} rads(Si)/s (or as required) for wide pulse measurements. Unless otherwise specified, a test device exposed to a total dose that exceeds 20 percent of the total dose failure level shall be considered as destructively tested and shall be removed from the lot (see 1.2a).

2.2 Dosimetry equipment. Dosimetry equipment must include a system for measuring total dose, such as a thermoluminescent dosimeter (TLD) or calorimeter, a pulse shape monitor, and an active dosimeter that allows the dose rate to be determined from electronic measurements, e.g., a p-i-n detector, Faraday cup, secondary emission monitor, or current transformer.

2.3 Test circuit. The test circuit shall contain the device under test, wiring, and auxiliary components as required. It shall allow for the application of power and bias voltages or pulses at the device inputs to establish the state vector. Power supply stiffening capacitors shall be included which keep the power supply voltage from changing more than 10 percent of its specified value during and after the radiation pulse. They should be placed as close to the device under test as possible, but should not be exposed to the direct radiation beam. Provision shall be made for monitoring specified outputs. Capacitive loading of the test circuit must be sufficiently low to avoid interference with the measurement of short-duration transient signals. Generally a line driver is required at device outputs to reduce capacitive loading. Line drivers must have sufficient risetime, linearity, and dynamic range to drive terminated cables with the full output logic level. The test circuit shall not affect the measured output response over the range of expected dose rates and shall not exhibit permanent changes in electrical characteristics at the expected accumulated doses. It must be shielded from the radiation to a sufficient level to meet these criteria.

Test circuit materials and components shall not cause attenuation or scattering which will perturb the uniformity of the beam at the test device position (see 2.1 for uniformity). The device under test shall be oriented so that its surface is perpendicular to the radiation beam.

2.4 Cabling. Cabling shall be provided to connect the test circuit board, located in the radiation field, to the test instrumentation located in the instrumentation area. Coaxial cables, terminated in their characteristic impedance, shall be used for all input and output signals. Double shielded cables, triax, zipper tubing or other additional shielding may be required to reduce noise to acceptable levels.

2.5 Transient signal measurement. Oscilloscopes or transient digitizers are required to measure transient output voltages, the power supply current and the dosimeter outputs. The risetime of the measuring instrumentation shall be less than 10 ns for pulse widths greater than 33 ns or less than 30 percent of the radiation pulse width for pulse widths less than 33 ns.

2.6 Functional testing. Equipment is also required for functional testing of devices immediately after the radiation pulse in the radiation test fixture. This equipment must contain sources to drive inputs with specified patterns, and comparison circuitry to determine that the correct output patterns result. This equipment may consist of logic analyzers, custom circuitry, or commercial integrated circuit test systems. However, it must be capable of functioning through long cables, and must also be compatible with the line drivers used at the outputs of the device in the test circuit.

• 2.7 General purpose test equipment. Power supplies, voltmeters, pulse generators, and other basic test equipment that is required for testing is general purpose test equipment. This equipment must be capable of meeting the test requirements and should be periodically calibrated in accordance with ANSI/NCSL Z540-1 or equivalent.

3. PROCEDURE. An outline of the procedure is as follows: a) determine the state vectors (or sequence of test vectors for a dynamic test) in which the device will be irradiated; b) following the test plan, set up the test fixture, functional test equipment, and transient measurement equipment; c) set up and calibrate the radiation source; d) perform a noise check on the instrumentation; and e) test devices at a sequence of radiation pulses, determining the transient response at specified dose rates. The dose rate upset level can be determined by measuring the transient response at several dose rates, using successive approximation to determine the radiation level for dose rate upset.

3.1 State vector selection. Two approaches can be used to select the state vectors in which a device is to be irradiated:

a. Multiple output logic states. Partition the circuit into functional blocks. Determine the logic path for each output, and identify similar internal functions. For example, a 4-bit counter can be separated into control, internal flip-flop, and output logic cells. Four identical logic paths exist, corresponding to each of the four bits. Determine the total number of unique output logic state combinations, and test the circuit in each of these states. For the counter example this results in 16 combinations so that the upset must be determined for each of these 16 state vectors.

b. Topological analysis approach. If a photomicrograph of the circuit is available, the number of required states can be reduced by examining the topology of the internal circuits. This allows one to eliminate the need to test paths with the same output state which have identical internal geometries. For the counter, this reduces the required number of states to two. This approach is recommended for more complex circuits where the multiple output logic approach results in too many required state vectors.

3.2 Transient output upset criteria. The transients that are permitted at logic outputs depend on the way that the system application allocates the noise margin of digital devices. Most systems use worst-case design criteria which are not directly applicable to sample testing because the samples represent typical, not worst-case parts, and have higher noise margins. For example, although the logic swing of TTL logic devices is typically greater than 2 volts, the worst-case noise margin is specified at 400 mV. In a typical system, much of this noise margin will be required for aberrations and electrical noise, leaving only part of it, 100 mV to 200 mV, for radiation-induced transients. Thus, the allowable voltage transient is far lower than the typical logic signal range. Loading conditions also have a large effect on output transients.

However, transient upset testing is usually done at a fixed temperature under conditions that are more typical than they are worst-case. Thus, the noise margin during testing is much greater. The recommended default condition if not specified by the system is a transient voltage exceeding 1 V for CMOS or TTL logic devices with 5 V (nominal) power supply voltage, and 30 percent of the room-temperature logic level swing for other technologies such as ECL, open collector devices, or applications with other power supply voltages. Default loading conditions are minimum supply voltage and maximum fanout (maximum loading).

The time duration of transient upset signals is also important. If the duration of the transient voltage change is less than the minimum value required for other circuits to respond to it, the transient signal shall not be considered an upset. The minimum time duration shall be one-half the minimum propagation delay time of basic gate circuits from the circuit technology that is being tested.

Testing criteria may also be established for other parameters, such as the power supply current surge. Output current is also important for tri-state or uncommitted ("open-collector") circuits. These criteria must be specified by the test plan, and are normally based on particular system requirements.

3.3 Test plan. The test plan must include the following:

a. Criteria for transient voltage upset, output current, and power supply current, as applicable.

b. Power supply and operating frequency requirements.

c. Loading conditions at the outputs.

d. Input voltage conditions and source impedance.

e. Functional test approach, including dynamic upset, if applicable.

f. Radiation pulse width(s).

g. Sequence used to adjust the dose rate in order to determine the upset threshold by successive approximation.

h. State vectors used for testing (determined from 3.1).

i. Radiation levels to be used for transient response measurements, if applicable.

j. A recommended radiation level at which to begin the test sequence for transient upset measurements, if applicable.

k. The temperature of the devices during testing (usually 25°C ±5°C).

3.4 Test circuit preparation. The test circuit shall be assembled including a test circuit board, line drivers, electrical instruments, functional test equipment, transient measurement equipment, and cables to provide the required input biasing, output monitoring, and loading.

3.5 Facility preparation. The radiation source shall be adjusted to operate in the specified mode and provide a radiation pulse width within the specified width range. The required dosimeters shall be installed as close as practical to the device under test. If special equipment is needed to control the temperature to the value specified in the test plan, this equipment must be assembled and adjusted to meet this requirement.

3.6 Safety requirements. The health and safety requirements established by the local Radiation Safety Officer or Health Physicist shall be observed.

3.7 Test circuit noise check. With all circuitry connected, a noise check shall be made. This may be done by inserting a resistor circuit in place of the test device. Resistor values chosen shall approximate the active resistance of the device under test. A typical radiation pulse shall be applied while the specified outputs are monitored. If any of the measured transient voltages are greater than 10 percent of the expected parameter response, the test circuit is unacceptable and shall not be used without modification to reduce noise.

3.8 Bias and load conditions. Unless otherwise specified, the power supply shall be at the minimum allowed value. Input bias levels shall be at worst-case logic levels. Outputs shall be loaded with the maximum load conditions in both logic states (usually equivalent to maximum circuit fanout).

3.9 Temperature. The temperature of the devices during test should be measured with an accuracy of ±5°C unless higher accuracy is required in the test plan.

3.10 Procedure for dose rate upset testing. The device to be tested shall be placed in the test socket. The required pulse sequence shall be applied so that the device is in the state specified by the first of the state vectors in 3.1.

a. Set the intensity of the radiation source to the first radiation test level specified in the test plan. Expose the device to a pulse of radiation, and measure the transient output responses and power supply current transient. For sequential logic circuits, perform a dynamic functional test to see if changes occurred in internal logic states.

b. Repeat 3.10a for all other state vectors and radiation levels specified in the test plan.

3.11 Radiation exposure and test sequence for upset threshold testing. The device to be tested shall be placed in the test socket. The required pulse sequence shall be applied so that the device is in the state specified by the first of the state vectors determined in 3.1, or is operating with the specified test vector sequence for dynamic upset.

a. Set the intensity of the radiation source to the initial level recommended in the test plan, and expose the device to a pulse of radiation. Determine whether a stored data upset, logic state upset, or dynamic upset occurs, as appropriate.

b. If no upset occurred, increase the radiation level according to the sequence specified in the test plan; if an upset is observed decrease the radiation level. After the radiation source is adjusted to the new intensity, reinitialize the part to the required state vector, expose it to an additional pulse, and determine whether or not upset occurred. Continue this sequence until the upset response threshold level is bracketed with the resolution required in the test plan.

c. The power supply peak transient current shall be monitored and recorded during radiation testing unless it is not required by the test plan.

d. Repeat test sequences 3.11a through 3.11c for all of the state vectors.

3.12 Report. As a minimum the report shall include the following:

a. Device identification.

b. Test date and test operator.

c. Test facility, radiation source specifications, and radiation pulse width.

d. Bias conditions, output loading, and test circuit.

e. Description of the way in which state vectors for testing were selected.

f. State vectors used for radiation testing and functional test conditions for each state vector.

g. Criteria for transient output upset.

h. Records of the upset threshold and power supply current for each state vector.

i. Equipment list.

j. Results of the noise test.

k. Temperature (see 3.9).

4. SUMMARY. The following details shall be specified.

a. Device type and quantity to be tested.

b. Test circuit to be used, including output loading impedance.

c. State vectors to be used in testing and device output pins to be monitored.

d. Functional test sequence.

e. Power supply voltage and bias conditions for all pins.

f. Pulse width of the radiation source (see 2.1).

g. The method of selecting steps between successive irradiation levels and the required resolution.

h. Restrictions on ionizing (total) dose if other than that specified in 3.1.

i. Temperature of the devices during testing.

j. Requirement for measuring and recording power supply peak transient current (see 3.11c).

k. Failure criteria for transient output voltage upset.

l. Failure criteria for power supply current and output current, if applicable.

METHOD 1022

MOSFET THRESHOLD VOLTAGE

1. PURPOSE. This method establishes the means for measuring MOSFET threshold voltage. This method applies to both enhancement-mode and depletion-mode MOSFETs, and for both silicon on sapphire (SOS) and bulk-silicon MOSFETs. It is for use primarily in evaluating the response of MOSFETs to ionizing radiation, and for this reason the test differs from conventional methods for measuring threshold voltage.

1.1 Definition.

MOSFET threshold voltage, V_{TH}. The gate-to-source voltage at which the drain current is reduced to the leakage current, as determined by this method.

2. APPARATUS. The apparatus shall consist of a suitable ammeter, voltmeters, and voltage sources. The apparatus may be manually adjusted or, alternatively, may be digitally programmed or controlled by a computer. Such alternative arrangements shall be capable of the same accuracy as specified below for manually adjusted apparatus.

2.1 Ammeter (A_1). The ammeter shall be capable of measuring current in the range specified with a full scale accuracy of ±0.5 percent or better.

2.2 Voltmeters (V_1 and V_2). The voltmeters shall have an input impedance of 10 MΩ or greater and have a capability of measuring 0 to 20 V with a full scale accuracy of ±0.5 percent or better.

2.3 Voltage sources (VS_1 and VS_2). The voltage sources shall be adjustable over a nominal range of 0 to 20 V, have a capability of supplying output currents at least equal to the maximum rated drain current of the device to be tested, and have noise and ripple outputs less than 0.5 percent of the output voltage.

3. PROCEDURE.

NOTE: The absolute maximum values of power dissipation, drain voltage, drain current, or gate voltage specified in either the applicable acquisition document or the manufacturer's specifications shall not be exceeded under any circumstances.

3.1 n-channel devices.

3.1.1 Test circuit. The test circuit shown on figure 1022-1 shall be assembled and the apparatus turned on. With the voltage sources VS_1 and VS_2 set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate polarity switch shall be set to the appropriate position, and voltage source VS_1 shall be set 1.0 V negative with respect to the anticipated value of threshold voltage V_{TH}. Voltage source VS_2 shall be adjusted until voltmeter V_2 indicates the specified drain voltage V_D. The current I_D, indicated by ammeter A_1, and the gate voltage V_G, indicated by voltmeter V_1, shall be measured and recorded.

3.1.2 Measurement of gate voltages. The measurement shall be repeated at gate voltages which are successively 0.25 volts more positive until either the maximum gate voltage or maximum drain current is reached. If the gate voltage reaches 0 volts before either of these limits has been reached, the gate polarity switch shall be changed as necessary and measurements shall continue to be made at gate voltages which are successively 0.25 volts more positive until one of these limits has been reached.

3.2 p-channel devices.

3.2.1 Test circuit. The test circuit shown on figure 1022-2 shall be assembled and the apparatus turned on. With the voltage sources VS_1 and VS_2 set to 0 volts, the MOSFET to be tested shall be inserted into the test circuit. The gate polarity switch shall be set to the appropriate position, and voltage source VS_1 shall be set 1.0 V positive with respect to the anticipated value of threshold voltage V_{TH}. Voltage source VS_2 shall be adjusted until voltmeter V_2 indicates the specified drain voltage V_D. The current I_D, indicated by ammeter A_1, and the gate voltage V_G, indicated by voltmeter V_1, shall be measured and recorded.

3.2.2 Measurement of gate voltages. The measurement shall be repeated at gate voltages which are successively 0.25 volts more negative until either the maximum gate voltage or maximum drain current is reached. If the gate voltage reaches 0 volts before either of these limits has been reached, the gate polarity switch shall be changed as necessary and measurements shall continue to be made at gate voltages which are successively 0.25 volts more negative until one of these limits has been reached.

3.3 Leakage current. The leakage current shall be measured.

3.3.1 Drain voltage. The drain voltage shall be the value specified in 4b.

3.3.2 Gate voltage. The gate voltage shall be five volts different from the anticipated threshold voltage in the direction of reduced drain current.

3.4 Plot of gate voltage. The gate voltage, V_G, shall be plotted versus the square-root of the drain current minus the leakage current, $\sqrt{I_D - I_L}$. At the point of maximum slope, a straight line shall be extrapolated downward. The threshold voltage V_{TH} is the intersection of this line with the gate voltage axis. Examples are shown on figure 1022-3.

3.5 Report. As a minimum, the report shall include the device identification, the test date, the test operator, the test temperature, the drain voltage, the range of gate voltage, the leakage current, and the threshold voltage.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test temperature. Unless otherwise specified, the test shall be performed at ambient.

b. Drain voltage.

c. Maximum drain current.

d. Range of gate voltage.

NOTES: Gate polarity switch set at A for enhancement mode, B for depletion mode.

FIGURE 1022-1. Test circuit for n-channel MOSFETs.

NOTE: Gate polarity switch set at A for enhancement mode, B for depletion mode.

FIGURE 1022-2. Test circuit for p-channel MOSFETs.

FIGURE 1022-3. Examples of curves.

METHOD 1023.2

Dose Rate Response and Threshold for Upset of Linear Microcircuits

1. PURPOSE. This test procedure defines the requirements for measuring the dose rate response and upset threshold of packaged devices containing analog functions when exposed to radiation from a flash X-ray source or from a linear accelerator. This procedure addresses the measurement of dose rate response characteristics of a linear circuit, excluding latchup which is addressed in MIL-STD-883 Test Method 1020.

1.1 Definitions. The following are the definitions of terms used in this method:

a. Dose rate response. The transient changes which occur in the operating parameters or in the output signal of an operating linear microcircuit when exposed to a pulse of ionizing radiation.

b. Dose rate. Energy absorbed per unit time and per unit mass by a given material from the radiation field to which it is exposed. Units are specified in Gray (Gy) per second (s) in the material of interest, e.g., Gy(Si)/s, Gy(SiO_2)/s, Gy(GaAs)/s, etc.

c. Dose rate induced upset. An upset has occurred when the radiation induced transient change in a specified parameter (e.g., in output voltage, supply current, output signal waveform) exceeds a predetermined level.

d. Upset threshold. The upset threshold is the minimum dose rate at which the device upsets. However, the reported measured upset threshold shall be the maximum dose rate at which the device does not upset and which the transient disturbance of the output waveform and/or supply current remains within the specified limits.

1.2 Test plan. Prior to dose rate testing, a test plan shall be prepared which describes the radiation source, the dosimetry techniques, test equipment, the device to be tested, test conditions, and any unique testing considerations. A detailed procedure for each device type to be tested shall be prepared, either as part of the test plan, or in separate test procedure documents. The procedure shall include bias conditions, test sequence, schematics of the test setup and specific functions to be tested. The test plan shall be approved by the acquiring activity, and as a minimum, the items listed below shall be provided in the test plan or procedure:

a. Device types, including package types, manufacturer, date codes, and quantities to be tested.

b. Traceability requirements, such as requirements for serialization, wafer or lot traceability, etc.

c. Requirements for data reporting and submission.

d. Block diagram or schematic representation of test set up.

e. List of equipment used in the testing and calibration compliance requirements as required.

f. Test conditions, e.g., bias voltage, temperature, etc.

g. Electrical parameters to be monitored and device operating conditions, including functional test requirements before, during and after the radiation pulse. Test patterns to be used for devices with storage elements, or devices with input pattern sensitivity shall also be specified.

h. Group A electrical test requirements for pre- and post-dose rate testing, when applicable, to include test limits and failure criteria.

i. Radiation test parameters such as pulse width(s), radiation dose(s) per pulse and dose rate range(s).

j. Total ionizing dose limit acceptable for each device type.

k. Upset and failure criteria, e.g., effective number of bits (ENOB) or missing codes in analog to digital converters (ADCs), delta VOH or Vref, time to recovery, output waveform distortion in shape or frequency, etc.

1.3 Formulation of the upset criteria. The upset criteria are usually generated from characterization data at the dose rate of interest. Upset criteria can sometimes be determined by analysis/simulation (SPICE or equivalent computer code) of the application circuit, if the code has been verified to agree with experimental data for similar circuits and exposure conditions.

1.4 Specification of the upset criteria. Once formulated, the upset criteria shall be specified in the detailed specification. The upset criteria may consist of the following (a waveform may be included denoting the acceptable boundaries):

a. Measurement circuit to which criteria apply.

b. Peak amplitude of tolerable transient change in output voltage.

c. Allowable duration of transient output change (recovery time).

d. Limiting value for the surge in power supply current and recovery characteristics.

e. Steady state (return to normalcy) level of the output voltage following recovery.

f. ENOB or missing codes for ADCs.

g. Delta parameters such as Vref or VOH.

h. Device saturation time.

2. APPARATUS. The apparatus shall consist of the radiation source, dosimetry equipment, remote test circuit to include signal recording devices, cabling, line drivers, interconnect fixture, and exposure board. Adequate precautions shall be observed to obtain an electrical measurement system with sufficient insulation, ample shielding, satisfactory grounding and low noise from electrical interference or from the radiation environment (see section 3.7.3).

2.1 Radiation Source. Either of two radiation sources shall be used for dose rate testing: 1) a flash x-ray machine (FXR), or 2) an electron linear accelerator (LINAC). The FXR shall be used in the x-ray mode and the LINAC in the electron (e-beam) mode. Unless otherwise specified, the FXR peak charging voltage shall be 2 MV or greater, and the LINAC beam energy shall be 10 MeV or greater. The uniformity of the radiation field in the device irradiation volume shall be ± 15% as measured by the dosimetry system. The dose per radiation exposure shall be as specified in the test plan or procedure.

2.2 Dosimetry System. A dosimetry system shall be used which provides a measurement accuracy within ± 15 percent. A calibrated PIN diode may be used to obtain both the shape of the radiation pulse and the dose. The following American Society for Testing and Materials (ASTM) standards or their equivalent may be used:

ASTM E 526 Standard Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests.

ASTM E 666 Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.

ASTM E 668 Standard Practice for the Application of Thermo-luminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation Hardness Testing of Electronic Devices.

These methods describe techniques to determine the absorbed dose in the material of interest. Device packaging material and thickness should be considered in determining the dose to the DUT. For FXR tests, dose enhancement effects of the package shall be considered. Dosimetry techniques shall be reported in the test report as well as device packaging material, thickness and dose enhancement effects, if applicable.

2.3 Dose Rate Test System. The instrumentation shall be capable of establishing the required test conditions and measuring and recording the required parameters in the specified time frame. Components other than the device under test (DUT) shall be insensitive to the expected radiation levels, or they shall be shielded from the radiation. The system used for dose rate testing shall contain the following elements:

2.3.1 Remote Test circuit. The remote portion of the test circuit includes power sources, input and control signal generators, instrumentation for detecting, measuring and recording transient and steady state response, and may also include automated test equipment (ATE). The remote portion of the test equipment is shielded from radiation and from radiation induced electromagnetic fields. Specified signals shall be measured and recorded during the radiation pulse, and the logic pattern shall be verified after the pulse (when applicable).

2.3.2 Interconnect fixture. The interconnecting fixture is located in the radiation exposure chamber and is connected to the remote portion of the test circuit via the cabling system. It serves as a power and signal distribution box and contains the line drivers that buffer the various DUT output signals. The characteristics of the line drivers (e.g., linearity, dynamic range, input capacitance, transient response and radiation response) shall be such that they accurately represent the response of the DUT output. The interconnect fixture shall be located as close as practical to the exposure fixture, and must be appropriately shielded against scattered radiation fields so that radiation induced effects do not adversely affect the fidelity of the output response being measured.

2.3.3 Test circuit. The test circuit for each device type shall provide worst case bias and load conditions for the DUT, and shall enable in-situ functional testing of the DUT as specified in the test plan or procedure. The test circuit accommodates the DUT, output loads, and the supply stiffening capacitors connected directly to the DUT supply pins or its socket (see 2.3.4). To avoid ground loops, there shall be only one ground plane (or ground rings connected to a single ground) on the test circuit. Test Circuit parasitic resistance shall be kept to a minimum.

2.3.4 Stiffening capacitors. A high frequency capacitor shall be placed at each bias supply pin of the DUT with lead lengths as short as practicable. These capacitors should be large enough such that the power supply voltage drop at the DUT is less than 10% during the radiation pulse (typical values are between 4.7 and 10 μF). In parallel with this capacitor should be a low inductance capacitor (e.g., 0.1 μF), again as close as possible to the supply pin and with lead lengths as short as practical. In addition, for each supply line into the DUT, a larger capacitor, $\geq$ 100 μF, may be placed a short distance away from the DUT and shielded from radiation.

2.3.5 Current Limiting Series resistor. A current limiting resistor in series with the power supply may only be used with prior approval of the acquiring activity. Note that a current limiting resistor may degrade the upset performance of the DUT.

2.3.6 Timing control. A timing control system shall be incorporated into the test system such that post-irradiation in-situ functional testing is performed at the specified time, and that recovery of the signal and supply current can be monitored.

2.4 Cabling. The remote test circuit shall be connected to the interconnect and exposure fixtures by means of shielded cables terminated in their characteristic impedance. Additional shielding provisions (e.g., doubly shielded cables, triax, zipper tubing, aluminum foil) may be required to reduce noise to acceptable levels.

2.5 Measuring and recording equipment. Oscilloscopes or transient waveform digitizers shall be used to measure and record the transient signal and the recovery period of the output voltage and supply current. The rise time of these instruments shall be such that they are capable of accurately responding to the expected pulse width(s).

3. PROCEDURE.

3.1 Device identification. In all cases, devices shall be serialized, and the applicable recorded test data shall be traceable to each individual device.

3.2 Radiation safety. All personnel shall adhere to the health and safety requirements established by the local radiation safety officer or health physicist.

3.3 Stress limits.

3.3.1 Total ionizing dose limit. Unless otherwise specified, any device exposed to more than 10% of its total ionizing dose limit shall be considered to have been destructively tested. The total dose limit shall be determined (or data obtained) for each device type to be tested. The total ionizing dose limit shall be specified in the test plan.

3.3.2 Burnout Limit. A device exposed to greater than 10% of the level at which photocurrent burnout occurs shall be considered destructively tested. The burnout level shall be specified in the test plan/procedure. The burnout level may be specified as the maximum dose rate level at which the device type has been tested and does not burnout. Note that dose rate testing causes surge currents ranging from 20 ns to 500 ns (typically) in duration, which may exceed the manufacturers' maximum ratings for current and power for that time period.

3.4 Characterization testing. Characterization tests shall be performed or data obtained to determine device performance as a function of dose rate and to establish requirements for production testing, if applicable. The following are examples of information gained from characterization testing:

a. Parameter behavior over dose rate and pulse width.

b. Upset threshold as a function of radiation dose rate and pulse width.

c. Determination of susceptible circuit conditions.

d. Identification of the most susceptible circuits of a device, and the appropriate outputs to monitor.

e. Effect of temperature on upset or failure.

* f. Upset, recovery time and failure criteria to be specified in the device specification or drawing.

g. Group A electrical parameter degradation subsequent to dose rate testing.

h. Worst case power supply voltage.

i. Maximum surge currents and duration, and photocurrent burnout level.

3.5 Production testing. Prior to production testing, characterization testing shall be performed or characterization data obtained for each device type. The results of the characterization tests (paragraph 3.4), or the existing data, will be used to develop the requirements for the production tests. These requirements are specified in the applicable test plan or procedure and include those items listed in paragraph 1.2.

3.5.1 General requirements for production tests. Production tests shall be performed at the specified dose rates (and pulse widths), with bias and load conditions as specified in the test plan or procedure. The measured response shall be compared to the upset criteria and determination of pass/fail shall be made. Devices having storage elements shall be loaded with the applicable test pattern prior to exposure and post-exposure functional test shall be performed to the extent necessary to verify the stored pattern.

3.6 Testing of Complex Linear Devices. Testing of complex linear devices, such as analog to digital and digital to analog converters, shall be performed using the necessary (as specified in the test plan or procedure) exposure conditions to ensure adequate coverage. Often, four or more exposure conditions are required. To the greatest extent practical, the most susceptible exposure conditions (i.e., most favorable for upset to occur) shall be used. For linear devices that have storage elements, each exposure state shall consist of a stored test pattern plus the external bias. Each test pattern shall be loaded prior to exposure, and following the application of the radiation pulse, functional testing of the device must be performed to the extent necessary to verify the pattern.

3.7 Dose Rate Test Sequence.

3.7.1 Facility Preparation. The radiation source shall be adjusted to operate in the specified mode and provide a radiation pulse within the specified pulse width range. The required dosimeters shall be installed as close as practical to the DUT.

3.7.2 Test Circuit preparation. The dose rate test system, including all test circuitry, cables, monitoring and recording equipment shall be assembled to provide the specified bias and load conditions and output monitoring. The test circuit shall be placed in position such that the DUT will receive the specified dose. Unless otherwise specified, dose rate testing shall be performed at 25° ± 5°C. (The test temperature shall be specified in the test plan/procedure.)

3.7.3 Test circuit noise check. With all circuitry connected, a noise check, including radiation induced noise, shall be made. Noise signals shall be kept as low as practicable. The circuitry and cabling system shall be modified until the noise signals are below an acceptable level (usually less than 10% of the expected response).

3.7.4 Test Procedure.

CAUTION: Exercise caution when handling devices, particularly with regard to pin alignment in the and holding fixture and when installing devices in the test circuit. Ensure that voltages are off before inserting the DUT. Observe ESD handling procedures for the class of devices being tested, as appropriate.

Step 1: Adjust timing control system to provide the required time interval between radiation pulse and post-irradiation measurements.

Step 2: Remove bias voltages and install a control sample device (same type as devices to be tested).

Step 3: Turn on bias voltages and verify proper device function in accordance with performance requirements.

Step 4. Verify proper operation of all recording, monitoring and timing control equipment. Monitor and record noise level and temperature.

Step 5. Remove bias voltages and control device, in that order.

Adjust the radiation source to operate in the specified mode to deliver the specified dose. Verify as follows:

Step 6: Put dosimetry in position and expose to radiation pulse. Verify that the dose recording equipment is working properly and that the appropriate dose was delivered.

When the dose rate test system, radiation source and dosimetry system have been verified to be working properly, continue as follows for each device type to be tested:

Step 7: Ensure bias is removed from the test circuit and install DUT.

Step 8: Bias the device and load the test patterns (if applicable) in accordance with the test plan or procedure. Verify proper device functional operation.

Step 9: Expose the DUT to the radiation pulse and measure the response of the specified outputs, as well as the recovery characteristics.

Step 10: Compare the DUT response to upset criteria, if applicable.

Repeat steps 8-10 for each exposure state and for each radiation dose rate.

Step 11: Remove bias and DUT in that order.

Note that the upset threshold shall be reported as the maximum dose rate at which the DUT does not upset.

4. Test Report. A dose rate test report shall be prepared and shall include the following (as a minimum):

* a. Device identification, including manufacturer, wafer lot and/or inspection lot traceability information, pre-radiation history (e.g., class level S, class level B, prototype, etc).

b. Radiation test facility, type of source, pulse width, dosimetry data including pulse waveform.

c. Test date, test operator's name and organization.

d. Results of the noise test.

e. Device response data, listed by device serial number, including output and supply recovery waveforms, and dose per pulse for each device.

f. Power supply droop during pulse.

g. Post-exposure functional test data if applicable.

h. All information included in the test plan/procedure (may be referenced or appended to test report), and any deviations from the approved test plan/procedure.

i. Package material and thickness, and effect of package material on dose to the device (see paragraph 2.2).

* 5. SUMMARY. The applicable device specification or drawing shall specify the following (as applicable):

a. Device types and quantities to be tested.

b. Traceability (device number, wafer/lot number, etc.) requirements and requirements for data reporting and submission.

c. Electrical configuration of the DUT during exposure (include schematic of exposure configuration).

d. Sequence of exposure conditions and logical test patterns.

e. Outputs to be monitored and recorded.

f. Dose rate level(s) and pulse width(s).

g. Criteria for upset and recovery, steady state value of recovered outputs and/or supply current. Include sample waveforms if necessary.

h. Upset threshold and failure level (if applicable).

i. Post exposure functional test necessary to verify the stored pattern, and maximum time interval between application of the radiation pulse and start of functional test.

j. Total ionizing dose limit and burnout level for each device type.

k. Maximum current limiting resistance in series with the power supply in the application (if applicable), and allowable resistance in the test circuit (paragraph 2.3.5).

l. Requirements for Group A electrical testing pre- and post-radiation testing, if applicable.

m. Test instrument requirements, if other than those indicated above.

n. Requirements for characterization, recharacterization and analysis.

APPENDIX A

A1. This appendix provides an example of the specification of test details for an operational amplifier. Because the test conditions depend both on the type of device and on the specific application, this example shall not be considered as suitable for use in any given case. It is provided only as an illustration of the use of this test method.

A2. Test specification, method 1023:

a. Type 741 operational amplifier, in 8-pin TO-5 package.

b. Test circuit as given on figure 1023-1. Leave pins 1, 5, and 8 unconnected.

c. V+=9.0 ± 0.2 V; V-=-9.0 ± 0.2 V; input signal 280 mV ±5% peak to peak, 2000 ±50 Hz.

d. Monitor pin 6 and the power supply current.

e. Standard noise limits apply.

f. Pulse width: 20 ns (Full width half maximum).

g. Total Ionizing dose shall not exceed 10 Gy(Si).

h. Test at a dose rate of 10^5 ±30% Gy(Si)/s.

i. Test temperature shall be ambient (25° ±5°C).

j. Pass/Fail Criteria: Power supply currents and the output signal shall return to within 10% of the pre-rad levels within 1 ms of the radiation pulse.

k. This test is considered a destructive test.

FIGURE 1023-1. Example of test circuit for OP-AMP.

APPENDIX B

B1. This appendix provides an example of the specification of test details for an analog to digital converter (ADC). Because the test conditions depend both on the type of device and on the specific application, this example shall not be considered as suitable for use in any given case. It is provided only as an illustration of the use of this test method.

B2. Test specification, method 1023:

a. Type ADC (n=# bits=12), 40 pin ceramic DIP.

b. The test circuit is given in Figure 1023-2, and an overview of the test setup is provided in Figure 1023-3.

The storage RAM must write at a speed (taa>tclk) exceeding the DUT clock frequency, and provide an interface to the controller, and be capable of storing a trigger pulse from the radiation source. Note that if the data ready line of the ADC is used, it must be monitored separately, as it may also upset.

c. A minimum of 3 input voltages shall be tested. Adjust input bias to center output code on:

1. Midscale ($2^n/2$)

2. Fullscale - 10% (2^n-0.1*2^n)

3. Zero + 10% (0+0.1*2^n)

d. As a minimum, perform tests at 10 MHz and 1 MHz (Fmax and 0.1*Fmax).

e. Upset Criteria: Determination of the upset threshold shall be determined by statistical analysis comparing the pre-shot ADC output codes with the data taken during and immediately after the shot. The time to recover (within 20%) shall also be determined by comparing the pre-rad data with the post-rad data.

f. Pulse width: 20 ns (Full width half maximum).

g. Test at dose rates ranging from 10^2 - 10^7 Gy(Si)/s to establish upset threshold.

h. Total ionizing dose shall not exceed 500 Gy(Si).

i. Test at ambient temperature (25° ±5°C).

j. After completion of the upset tests, test up to the machine maximum dose rate to determine if devices burn out. This test is a destructive test.

FIGURE 1023-2. Example of test circuit for ADC (C1 = 4.7 µF, C2 = 0.1 µF).

FIGURE 1023-3. Schematic of example test setup for ADC.

METHOD 1030.1

PRESEAL BURN-IN

1. PURPOSE. The purpose of preseal burn-in is to identify marginal devices or stabilize monolithic, hybrid, or multichip microcircuits prior to the sealing of packages so that rework or retrimmings can be performed. Standard or sealed-lid burn-in testing (see method 1015) is designed to screen or eliminate marginal devices by stressing microcircuits at or above maximum rated operating conditions or by applying equivalent screening conditions which will reveal time and stress failure modes with equal or greater sensitivity. Performance of a portion of the standard burn-in testing prior to sealing will identify marginal devices or those requiring retrimming at a point where rework or retrimming can readily be performed. Use of preseal burn-in is optional and should be a function of the complexity of the microcircuit in question coupled with, if available, actual sealed-lid burn-in failure rates.

2. APPARATUS. Details for the required apparatus and compensation for air velocity, when required, shall be as described in method 1005. In addition, the oven used for preseal burn-in shall be so equipped to provide a dry (less than 100 ppm moisture, at the supply point) nitrogen at class 100,000 maximum environment. Suitable equipment shall be provided to control the flow of dry nitrogen and to monitor the moisture content of the dry nitrogen flowing into the oven.

* 3. PROCEDURE. All microcircuits shall be subjected to the specified preseal burn-in test condition (see 3.1) for the time and temperature and in the environment specified after all assembly operations, with the exception of lid sealing, have been completed (see method 5004 herein, MIL-PRF-38534 or MIL-PRF-38535); internal visual inspection shall be performed prior to sealing. The microcircuits shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified ambient temperature. Measurements before and after preseal burn-in shall be made as specified.

3.1 Test conditions. Basic test conditions are as shown below. Details of each of these conditions shall be as described in method 1005.

a. Test condition C: Steady-state dc voltages.

b. Test condition D: Series or parallel excitation with ac conditions as applicable to exercise the device under test to normal operating conditions.

3.1.1 Test time. Unless otherwise specified, preseal burn-in shall be performed for a minimum of 48 hours. It shall be permissible to divide the total minimum burn-in time between preseal and postseal burn-in provided that the total burn-in time equals or exceeds the specified burn-in time of 160 hours and that the postseal burn-in time equals or exceeds 96 hours.

3.1.2 Test temperature. Unless otherwise specified, the preseal burn-in test temperature shall be 125°C. If a lower temperature is used, a corresponding increase in time is necessary as shown on figure 1015-1.

3.1.3 Test environment. Preseal burn-in shall be performed in a dry nitrogen (less than 100 ppm moisture, at the supply point), class 100,000 maximum environment. Prior to heat-up, the oven shall be purged with dry nitrogen and then the bias shall be applied. Testing shall not commence until the specified environment has been achieved.

3.2 Measurements. Measurements before preseal burn-in, shall be conducted prior to applying preseal burn-in test conditions. Unless otherwise specified, measurements after preseal burn-in shall be completed within 96 hours after removal of the microcircuits from the specified pre-seal burn-in test condition and shall consist of all 25°C dc parameter measurements (subgroup A-1 of method 5005) and all parameters for which delta limits have been specified as part of interim electrical measurements. Delta limit acceptance, when applicable, shall be based upon these measurements. If these measurements cannot be completed within 96 hours, the microcircuits shall be subjected to the same specified test conditions (see 3.1) previously used for a minimum of 24 additional hours before measurements after pre-seal burn-in are made.

3.2.1 Cooldown after preseal burn-in. All microcircuits shall be cooled to within 10°C of their power stable condition at room temperature prior to the removal of bias. The interruption of bias for up to 1 minute for the purpose of moving the microcircuits to cool-down positions separate from the chamber within which testing was performed shall not be considered removal of bias. Alternatively, except for linear or MOS devices (CMOS, NMOS, PMOS, etc.) the bias may be removed during cooling provided the case temperature of microcircuits under test is reduced to a maximum of 35°C within 30 minutes after the removal of the test conditions. All 25°C dc measurements shall be completed prior to any reheating of the microcircuits.

* 3.2.2 Failure verification and repair. Microcircuits which fail the 25°C dc measurements after preseal burn-in shall be submitted for failure verification in accordance with test condition A of method 5003. After verification and location of the defective or marginal device in the microcircuit, rework shall be performed as allowed in MIL-PRF-38535 or MIL-PRF-38534. Upon completion of rework, repaired microcircuits shall be remeasured and, if found satisfactory, shall be returned for additional preseal burn-in (see 3.1) if such rework involved device replacement.

3.2.3 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all microcircuits are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Except for this initial and periodic verification, each microcircuit socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the microcircuits under test.

b. Connectors to test boards or trays. After the test boards are loaded with microcircuits and are inserted into the oven, and prior to the nitrogen purge, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration.

c. At the conclusion of the test period, after cool-down, the voltage and signal condition verification of b above shall be repeated.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration (see 3.1), the test time shall be extended to assure actual exposure for the total minimum specified test duration.

3.3 Handling of unsealed microcircuits. It is recommended that unsealed microcircuits be covered at all times for protection from handling induced defects. Snap-on metal covers, or rigid plastic covers with a conductive coating, may be removed from the microcircuits after all microcircuits are in place in the burn-in racks. Covers, if removed shall be replaced immediately after bias removal and completion of burn-in and cool-down prior to removal of microcircuits from the burn-in racks. Regardless of the method of handling during the time period between the completion of internal visual inspection following preseal burn-in and sealing, the microcircuits shall be retained in a controlled environment (see method 2017).

* 3.4 Sealed-lid burn-in. After completion of preseal burn-in, internal visual, other preseal screens and sealing all microcircuits shall undergo the screening specified in method 5004 herein, MIL-PRF-38534 or MIL-PRF-38535 except that stabilization bake may be deleted. Sealed-lid burn-in shall be performed as specified in method 5004 herein , MIL-PRF-38534 or MIL-PRF-38535 (see method 1015 for test details).

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

   a. Test condition letter and burn-in circuit with requirements for inputs, outputs, applied voltages and power dissipation as applicable (see 3.1).

   b. Test mounting, if other than normal (see 3).

   c. Pre and post preseal burn-in measurement and shift limits, as applicable (see 3.2).

   d. Time within which post preseal burn-in measurements must be completed if other than specified (see 3.2).

   e. Type of covers used to protect microcircuits from handling induced defects (see 3.3).

   f. Test duration for preseal and sealed lid burn-in (see 3.1.1).

   g. Test temperature, if less than 125°C (see 3.1.2).

METHOD 1031

THIN FILM CORROSION TEST

1. PURPOSE. The thin film corrosion test is performed for the purpose of demonstrating the quality or reliability of devices subjected to the specified conditions over a specified time period. This sample test is to be applied as either a short term specialized quality assurance test or as a long term acceleration test to assure device reliability. It is particularly suited to devices containing thin film conductors, resistors, or fuses which are susceptible to corrosion as a result of cavity water vapor which is less than the limits specified in methods 5005 herein and MIL-PRF-38534. Because of the destructive nature of the test, it should not be used as a 100 percent screen. It is the intent of this test to reveal time and temperature, stress dependent, moisture related failure modes resulting from metallization corrosion.

2. APPARATUS. Suitable sockets or other mounting means shall be provided to make firm electrical contact to the terminals of devices under test in the specified circuit configuration. Power supplies and a temperature chamber shall be capable of maintaining the specified operating conditions as a minima throughout the testing period. The test chamber shall be conditioned with dry air to prevent the test ambient from reaching 100 percent relative humidity during temperature cycling.

3. PROCEDURE. The microcircuits shall be subjected to the specified conditions, duration, and temperature, and the required measurements shall be made at the conclusion of the test. The test conditions, duration, quantity, and temperature shall be recorded and shall govern for the entire test. All programmable devices processed by the manufacturer to an altered item drawing shall be programmed prior to the test.

3.1 Test conditions.

3.1.1 Device conditioning. All devices shall be conditioned, without bias at 125°C ±10°C for a minimum of 24 hours before proceeding with the test.

3.1.1.1 Short term testing. For short term quality assurance testing the time-temperature bias sequence of figure 1031-1 shall be followed for 16 cycles, 3 hours each, for a total of 48 hours. The following sequence shall be used for the short term test:

Initial conditioning drives out deeply trapped water into ambient

Step AB	125°C: Activate surface water from walls.
Step BC	Freeze out ambient water on walls and chip (temperature ramp 100°C/minute).
Step CD	Allow surface temperatures inside package to come to equilibrium (i.e., redistribute water).
Step DE	Transfer water from walls to chip (cold surface pump). At point E apply bias while chip is wet.
Step EF	Adjust temperature ramp so that chip is always the coldest temperature by minimizing heat dissipation and adjusting temperature ramp (maximum 100°C/minute).
Step FG	Maintain 2°C ambient to insure highest R.H. near chip while bias is still applied.
Step GH	Heat quickly to evaporate water from walls, possibly with explosive force to enhance contaminant transfer from the walls to the chip (maximum 100°C/minute).

Temperature test cycle at 25°C when bias is applied. Remove from test fixture.

3.1.1.2 Long term testing. For long term reliability assurance testing the following modifications shall be made:

Step AB	Increased to 12 hours.
Step CD	Increased to 1 hour.
Step DE	Remains the same one-half hour.
Step EG	Bias applied at pt E and then cycled 30 minutes on, 30 minutes off during FG. Total time 24 hours.
Step EF	May be extended to 4 hours if power dissipation can be minimized.
Step FG	Increased to 6.5 hours. Total test time 10 weeks or 70 cycles.

Terminate test cycle at 25°C when bias is applied.

Remove from test fixture.

3.2 Measurements. Unless otherwise specified, all electrical measurement shall be completed within 12 hours after removal from the specified test conditions. End point measurements shall consist of group A, subgroups 1 and 7 at 25°C.

NOTE: Method 1014 fine and gross leak test must be accomplished before 3.1.1 and after 3.2. Any circuit failing the leak test will be removed from the test lot.

4. SUMMARY. The following details shall be provided in the applicable device specification or drawing:

a. The electrical test configuration.

b. The number of devices to be tested and the acceptance criteria.

c. Requirements for data recording, when applicable.

FIGURE 1031-1. Graphical representation of corrosion test.

METHOD 1032.1

PACKAGE INDUCED SOFT ERROR TEST PROCEDURE (DUE TO ALPHA PARTICLES)

1. PURPOSE. This test method defines the procedure for testing integrated circuits under known test conditions for susceptibility to alpha induced errors. This test was specifically designed to measure the device's ability to withstand alpha particle impact. In addition, the procedure will determine the effectiveness of a "die-coating" shield. The test objective is to determine the rate that failures are induced due to alpha radiation sourced from the device package, die and die-coat material.

1.1 Definitions. The following definitions were created to be specific and relevant within the confines of this method.

1.1.1 DUT. Device under test.

1.1.2 Soft error. Any error induced by alpha particle impact resulting in either a transient error or an error in data storage witnessed at the DUT's output.

1.1.3 Source. A foil of Thorium-232. (Note: This foil generates particles which have an alpha energy spectrum of 0 through 10 MeV).

1.1.4 Soft error rate (SER). Failures per unit time under normal conditions of package environment.

1.1.5 Accelerated soft error rate (ASER). Failures per unit time induced by exposure to a known alpha particle source.

1.1.6 Failure in time (FIT). 1 FIT = 1 failure in 10^9 device-hours.

1.1.7 Package flux. The total number of alpha particles impinging on the die surface per unit of time and area, due to package material impurities (i.e., lid, die material, sealants, and optional alpha barrier material). Normal units of measurement: alpha/cm^2-hr.

1.1.8 Modified package flux. The total number of alpha particles impinging on the die surface per unit of time and area, when a die coat is in place. Normal units of measurement: alpha/cm^2-hr.

1.1.9 Source flux. The total number of alpha particles impinging on the die surface per unit of time and area, due to the calibrated source. Normal units of measurement: alpha/cm^2-s.

2. APPARATUS. The apparatus will consist of electrical test instrumentation, test circuit board(s), cabling, interconnect boards, or switching systems and a Thorium-232 foil (optional). Precautions will be observed to obtain an electrical measurement system with adequate shielding, low electrical noise induction, and proper grounding.

2.1 Radiation source. The radiation source used in this test shall be a Thorium-232 foil with dimensions large enough to cover the entire exposed die cavity. The plated source shall be within the range of 0.01 - 5.0 μCi and shall produce the same energy spectrum as the package impurities. Radiation sources must be controlled according to state and federal regulations. The sources shall be certified periodically and decay rates used to determine the actual flux values at the time of use. *This source must be processed at least one year before being used. Caution: These sources should not be* exposed to heat.

2.2 Electrical test instruments. Electrical test instruments will be standard test instruments normally used for testing the DUT. They must be capable of establishing the required test conditions and measuring the required electrical parameters. All instruments shall be periodically calibrated in accordance with the general requirements of this test method standard.

2.3 Test circuits. The test circuit shall contain the DUT, wiring, and auxiliary components as required. Connection will allow for the application of the specified test conditions to obtain the specified outputs. Provision will be made for monitoring and recording the specified outputs. Any loading of the output(s), such as resistors or capacitors, shall be specified. The test circuit must not exhibit permanent changes in electrical characteristics as a result of exposure to the radioactive source. Shielding will be incorporated to prevent such effects from occurring if necessary.

2.4 Cabling. Cabling, if required, shall be provided to connect the test circuit board containing the DUT to the test instrumentation. All cables will be as short as possible. Care will be exercised to reduce electrical noise induced by the cable by using shielded cable, triax, zipper tubing, or other shielding methods.

3. PROCEDURES. Two methods of testing are allowed by this procedure. The first is a long term test (sometimes referred to as a system test) which does not incorporate a source but which accumulates a statistically valid amount of test time to determine the SER directly. This method is self explanatory and must be accomplished using the same parameters outlined in 3.1 (test plan). To determine the SER from this method, the following formula should be used and the result converted to FIT's.

SER = Total number of errors/Total test time

The second method incorporates the use of the source outlined in 2.1 (radiation source). The procedure for testing with an accelerated flux provided by the source is given below. These steps will be followed for each test outlined in 3.1.

a. The flux that the surface of the die would receive without a die coat will be determined. This is designated as the package flux.

b. If the device has a die-coat it should be left in place for the next portion of the test. The DUT will be delidded and the source placed directly over the die cavity at the same distance as the package lid was from the die.

   NOTE: The distance between the foil and the die must be less than 50 mils and the foil must cover the entire die-cavity opening in order to assure all angles of incidence will be maintained.

   NOTE: If the DUT has an inverted die configuration (e.g., flip-chip) a test jig must be implemented which will expose the active surface of the die to the irradiating source.

c. The testing outlined in 3.1 will be performed at this time with the configuration in b. above, in order to determine the SER for each test performed.

d. Recorded for each test performed will be the following:

   (1) Total number of errors recorded during each test.

   (2) Time to accumulate the errors.

   (3) SER_1, calculated from the following formulas:

   $ASER_1$ = Total number of errors/test time

   SER_1 = $ASER_1$ x (Package flux/source flux)

e. If no die-coating has been applied, the SER_1 will be reported as the measured rate of failure. However, if a die coat exists, steps 3.f through 3.j will also be performed.

f. The flux at the surface of the die will be determined when the die coat is in place; this is designated as the modified package flux.

NOTE: The modified package flux should be the sum of the flux from the die and die-coat material only.

g. The die coat should be removed, assuring that no damage to the die has occurred and the source placed as described in step b.

h. The tests performed in step 3.c must be repeated with this configuration, and the new SER will be designated SER_2.

i. Recorded for each test performed will be the following:

(1) Total number of errors recorded during each test.

(2) Time to accumulate the errors.

(3) SER (SER_2), calculated from the following formulas:

$ASER_2$ = Total number of errors/test time

$SER_2 = ASER_2$ x (Modified package flux/source flux)

j. The SER for the corresponding tests will be summed and reported as the rate of failure for this DUT, using the following formula:

$$SER = SER_1 + SER_2$$

NOTE: The order of the steps above can be reversed to enable testing before the die coat is applied and then after it has been applied, if desired.

3.1 Test plan. A test plan will be devised which will include determination of the worst case operating environment of the DUT to determine the worst case SER, incorporating the steps outlined above. The data patterns used will ensure that each cell and path, or both, is tested for both the logic zero and logic one states. The device will be continuously monitored and refreshed and the data errors counted. *This test will be required for each new device type or design revisions. The source* value and exposure time will be sufficient to obtain a significant number of soft error failures.

NOTE: If a data-retention or a reduced supply mode is a valid operating point for the DUT, this condition must also be tested for its SER.

3.1.1 The test equipment program. The test equipment program will be devised to cycle and refresh the stored data or cycled pattern continually, recording the number of errors.

3.1.2 Test conditions. Testing shall be performed at three separate cycle rates and at minimum and maximum voltages. Unless otherwise specified, the following cycle timing will be used: The minimum and the maximum specified cycle timing and the midpoint between the minimum and maximum specified cycle timing.

NOTE: If the device is a static or dynamic random access memory device, the device will be tested under both read and write operations.

3.2 Report. As a minimum, the report will include device identification, test date, test operator, test facility (if applicable), radiation source, test cycle times and voltages, data analysis, and equipment used in the test.

4. SUMMARY. The following details shall be specified.

   a. Device type and quantity to be tested.

   b. Test circuit to be used.

   c. Device output pins to be monitored.

   d. Alpha source used if other than specified herein.

   e. Alpha source Curie level.

   f. Package flux measurement techniques.

   g. Test equipment to be used.

   h. Procedures for proper handling of radioactive materials.

METHOD 1033

ENDURANCE LIFE

1. PURPOSE. Endurance life is performed in order to demonstrate the quality and reliability of nonvolatile memory devices subjected to repeated write/erase cycles. This method may also be used in a screening sequence or as a preconditioning treatment prior to conducting other tests. It may be desirable to make end point, and where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanism with cycles, time, or temperature.

1.1 Terms and definitions.

1.1.1 Endurance. The number of write/erase cycles a device can tolerate before failing to perform to specification.

1.1.2 Write/erase cycle. The act of changing the data from original to opposite to original in all bits of a memory device. This may be done for all bits in parallel or serial, e.g., block, byte, or bit.

1.1.3 Data retention screen. The unbiased baking at high temperature to accelerate the loss of charge from the storage node.

2. APPARATUS. The apparatus required for this test shall consist of equipment capable of write/erase cycling the devices, a controlled temperature chamber for performing a data retention bake, and suitable electrical test equipment to make the specified interim and end point measurements.

3. PROCEDURE. The devices shall be write/erase cycled (all bits) for specified maximum number of cycles, followed by electrical test, the specified data retention bake and electrical test. Interim pull points shall use the same sequence of cycle, electrical test, data retention bake, and electrical test.

* 3.1 Test condition. The case temperature, cycle time, data retention bake, and electrical test temperatures and conditions will be specified in the applicable device specification or drawing (see 4).

3.2 Failure criteria. No device is acceptable that exhibits:

a. Inability to write or erase across the temperature range.

b. Inability to retain data.

c. Inability to read at specified timing conditions, across the temperature and supply voltage range.

d. Inability to be write/erase cycled a minimum number of times n.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Number of write/erase cycles, n.

   b. Data retention bake conditions, including duration and temperature.

   c. Electrical test case temperature and timing conditions.

   d. Requirements for preconditioning, if applicable, and procedure if different than in 3.

   e. *Cycle conditions including temperature, type (e.g., block, byte, or bit) and write/erase pulse duration and repetition rate.*

   f. The sample plan including number of devices to be cycled and acceptance number.

   g. End-point and interim electrical test criteria.

METHOD 1034

DYE PENETRANT TEST

1. PURPOSE. This method tests the capability of a Plastic Encapsulated Microcircuit (PEM) to withstand moisture ingress and to detect flaws in packaging materials.

2. APPARATUS. The apparatus for the Dye Penetrant test shall be as follows.

a. Protective absorbant mats (paper/plastic)

b. 2 2000 ml containers

c. 2 1000 ml beakers

d. 2 mixing magnets

e. 2 hot plates for mixing

f. Whatman 42 filters (0.005μ)

g. 500 ml funnel

h. Fisher bell jar with stopper

i. Filtration base with vacuum accessories (fisher allied filtrator #9-788 11 cm base)

j. Vacuum pump, hoses, and clamps

k. 15 ml beaker

l. 50 ml beaker

m. 2 250 ml beakers

n. Watchglass or evaporating dish

o. Petri dish

p. Drummond 0.1 ml pipettes and plunger

q. Graduated cylinder

r. Vacuum oven

s. Heating oven

t. B1 filter / polyvar (or olympus PMG3 inverted microscope)

u. 52 film - 400 ASA

v. 57 film - 3000 ASA

3. PROCEDURES. The following procedures shall be followed in performing the Dye Penetrant test. This technique utilizes a low viscosity, anaerobic liquid penetrant (Resinol) which is mixed with a fluorescent powder (Yellow Dye G) and a anaerobic accelerator (17724).

NOTE: These chemicals are skin, eye and nose irritants.

3.1 Dye penetration procedure outline.

a. Mix dye solution.

Loctite Resinol RTC 18018
Loctite Accelerator for PMS 17724
Morton Fluorescent Yellow G

b. Place the parts in a beaker of the dye solution.

c. Place the beaker in the vacuum oven.

d. Leave the beaker for 15 minutes at a vacuum of 1 to 0.3 torr.

e. Bring the vacuum oven back to atmospheric pressure, then wait 15 minutes.

f. Remove the parts from the dye solution.

g. Wipe off the parts to remove the excess dye.

h. Heat the parts in the oven at 100°C for 1 hour to harden the polymer mixture.

i. Mount the parts for crosssectioning.

j. Crosssection the parts.

k. View the parts under magnification.

l. Take an optical photo of the crosssection.

m. Take a photo of the crosssection under UV to document the depth of penetration.

NOTE: Lay down a double layer of protective mats before starting this procedure. The dye spreads and stains quite easily. Be sure to wear the appropriate protective apparel, which includes chemical gloves, goggles, and a lab coat.

3.1.1 PREMIX solution preparation. Prepare a stock solution (PREMIX solution) of the resinol and yellow dye.

3.1.1.1 Mixing the solution. A mixture of 100 parts resinol to 1 part yellow dye powder is required to make the PREMIX solution.

a. Measure and pour 2000 ml of resinol into a beaker.

b. Measure 20 g of yellow dye and pour it into the 2000 ml of resinol. Stir this mixture for 5 minutes, then separate the mixture into two 1000 ml beakers to make it easier to work with. Place a mixing magnet in each of the beakers, then place the beakers on mixing plates. Stir the mixtures for two to three hours.

3.1.1.2 Filtering the PREMIX. The PREMIX must be filtered to ensure that any undesolved particles are removed from the solution.

a. Take a WHATMAN 42 filter and place it in the 11 cm Buckner funnel. Place the funnel adapter on the stem of the funnel. Then place the funnel into the top of the bell jar. Place a 250 ml beaker on the bell jar base. Place the bell jar and funnel over the beaker on the bell jar base.

b. Turn on the vacuum pump.

c. Take one of the 1000 ml beakers of premix and pour about 200 ml of the premix into the funnel. When the solution has drained through the funnel, turn off the vacuum pump, and pour the filtered solution into an empty container marked "RESINOL AND YELLOW DYE G MIXTURE". Repeat this process until all of the solution is filtered.

d. Remove the filter and replace it with a new one.

e. Repeat step 3 with the second 1000 ml beaker of solution.

f. Wash the beakers in a soap and water solution.

3.1.2 Setup of PREMIX and accelerator. A mixture of 200,000 parts PREMIX to 1 part accelerator is required. Due to the small amount of accelerator required, the mixture of premix and accelerator is performed in two steps. First a 200:1 mixture is prepared, then a 1000:1 mixture is made utilizing the 200:1 solution in order to achieve a 200,000:1 mixture.

a. Measure out 10 ml of premix (resinol/yellow dye stock solution) with a graduated cylinder. Pour the 10 ml into a small beaker.

b. Insert the Drummond pipette and plunger into the accelerator solution. The glass pipette has two green markings. The first marking is 0.05 ml, and the second marking is 0.1 ml.

c. Draw up 0.05 ml (1st green mark) of accelerator, and mix it into the 10 ml of premix.

d. Place a mixing magnet into the solution, and place the beaker on the mixing plate. Stir the solution for 5 minutes. This completes the mixing of the 200:1 premix:accelerator solution.

e. Clean the pipette and plunger in a soap and water solution. They must be clean when they are used in step h.

f. Fill a graduated cylinder with the amount of premix (resinol/yellow dye solution) that is needed to submerse the devices requiring dye penetration. Most jobs will require 25 ml of solution. The amount will vary depending upon the number and size of the devices in the job.

g. Pour the 25 ml of premix (or the desired amount) into a small beaker.

h. Using a clean plunger and pipette, a small amount of the 200:1 premix:accelerator solution is added to the desired amount of premix. For 25 ml of premix, 0.025 ml of 200:1 premix/accelerator solution is used. Other typical mixtures are listed below.

10 ml premix : 0.010 ml 200:1 premix/accelerator solution
25 ml premix : 0.025 ml 200:1 premix/accelerator solution
50 ml premix : 0.050 ml 200:1 premix/accelerator solution
75 ml premix : 0.075 ml 200:1 premix/accelerator solution
100 ml premix : 0.100 ml 200:1 premix/accelerator solution

i. Place a mixing magnet into the solution and place on a mixing plate for 5 minutes. This creates the final 200,000:1 premix:accelerator solution.

j. The 200:1 solution can now be discarded by placing it in the bottle marked "RESINOL, YELLOW DYE G, and ACCELERATOR WASTE".

k. Clean all of the glassware and pipettes with a soap and water solution.

3.1.3 Vacuum setup.

a. Place the parts in the premix/accelerator mixture.

b. Place the beaker in a petri dish to catch any spill solution that spills over during the vacuum operation.

c. Place a larger beaker over the beaker with solution in it to prevent splattering all over the vacuum oven.

3.1.3.1 Vacuum. Many vacuum ovens can be used for this procedure as long as the oven is able to reach 1 to 0.3 torr. The oven should have a gauge that can accurately measure the pressure at this level. One method is given below.

a. Place the door of the vacuum chamber by unscrewing the handle counter clockwise.

b. Place the beaker set-up into the vacuum chamber.

c. Close the vacuum oven door. Close the door latch and turn it clockwise until tight.

d. Close the valves on both sides of the oven. The vacuum is monitored by the gauge on the top of the oven. The vacuum meter is connected to the outtake of the oven.

e. Turn on the vacuum pump.

f. Monitor the outgassing of the solution while its under vacuum. Violent outgassing will start at approximately 10 torr. The valves on either side of the oven (one on the left side and one on the right side of the oven) can be cracked open to lessen the vacuum on the inside of the oven. By doing this, the outgassing can be controlled, so that the mixture doesn't spill over.

g. Once the outgassing stops, close the valves on the vacuum oven and wait for the pressure to decrease to 1 torr. The working vacuum for the procedure is 1 to 0.3 torr.

h. Once the Granville-Phillips vacuum gauge reaches 1 torr, wait for 15 minutes.

3.1.3.2 Post vacuum procedure.

a. At the end of 15 minutes, turn off the vacuum pump.

b. Open both of the intake valves until the vacuum inside the chamber is equal to the outside pressure. Leave the devices in this state for 15 minutes.

c. At the end of the 15 minutes, open the door and remove the beakers from the vacuum chamber.

3.1.4 Cleaning the devices.

a. Remove the devices from the solution.

b. Pad off the excess solution with a paper towel and cotton swab.

c. The remaining mixture can now be discarded into the bottle marked "RESINOL, YELLOW DYE G, AND ACCELERATOR WASTE".

d. The beakers, pipettes, and glassware can all be cleaned in soap and water.

3.1.5 Baking the devices.

a. Place the devices in a petri dish, and place the dish into an oven preheated to 100 degrees C. Bake for 1 hour.

b. After the bake, the parts can be mounted for crosssectioning.

3.1.6 Crosssectioning.

a. Normal crosssectioning procedures can be performed on the samples.

b. Make sure that stray particles of dye do not smear or become embedded in the cross-sectioned surfaces. This will give you a false representation of the dye in the sample. (Smearing looks like little stars when viewed through the ultraviolet filtering.) Be sure to clean the samples thoroughly after grinding and polishing operations to avoid these complications.

3.1.7 Viewing crosssections on a microscope. The exposure time will vary from sample to sample and from microscope to microscope. The best scope for viewing dye penetration will have a bright light source (200 W mercury lamp).

a. View the crosssection under normal bright field conditions. To take a photo, use the green filter, set the proper exposure, then take the photo using Polaroid 52 film (ASA 400).

b. Slide out the bright field mirror cube.

c. For the Olympus PMG3, slide in the blue excitation fluorescence cube (BH2-UDMB). For the Polyvar, remove the B1 filter from the filter box and insert it into the left hand side of the Polyvar.

d. Remove the green viewing filter. The fluorescence of the dye will be difficult to see if the filter is in place.

e. Insert the Polaroid 57 film. Though the ASA for 57 film is 3200, leave the ASA at 400 to take the photo. This will give you a good approximation for the proper exposure. Make adjustments as necessary to obtain the desired exposure. The exposure time will vary depending upon the amount of fluorescent dye there is in frame.

3.2 Die penetrant evaluation criteria. The following cross sections or other relevant cross sections shall be evaluated.

a. One cross section on the long axis of the package (examine tie bar)

b. Three cross sections on the short axis (examine shortest lead, die or paddle edge, and one other).

As a minimum the following criteria shall be used for evaluation and any discrepancies shall be reported:

a. Any evidence of fracture or other packaging related defects.

b. Any evidence of delamination.

c. Any evidence of dye reaching the die attach or die surface.

d. Any evidence of dye penetration of more than 50 percent at a lead egress.

e. Any evidence of dye penetration of more than 50 percent of the length of any lead in the package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Any failure criteria different than that specified in 3.2.

b. Test sample if no sample is specified.

METHOD 2001.2

CONSTANT ACCELERATION

1. PURPOSE. This test is used to determine the effects of constant acceleration on microelectronic devices. It is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. It may be used as a high stress test to determine the mechanical limits of the package, internal metallization and lead system, die or substrate attachment, and other elements of the microelectronic device. By establishing proper stress levels, it may also be employed as an in-line 100 percent screen to detect and eliminate devices with lower than nominal mechanical strengths in any of the structural elements.

2. APPARATUS. Constant acceleration tests shall be made on an apparatus capable of applying the specified acceleration for the required time.

3. PROCEDURE. The device shall be restrained by its case, or by normal mountings, and the leads or cables secured. Unless otherwise specified, a constant acceleration of the value specified shall then be applied to the device for 1 minute in each of the orientations X_1, X_2, Y_2, Y_1, Z_1, and Z_2. For devices with internal elements mounted with the major seating plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount. Unless otherwise specified, test condition E shall apply.

Test condition	Stress level (g)
A	5,000
B	10,000
C	15,000
D	20,000
E	30,000
F	50,000
G	75,000
H	100,000
J	125,000

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Amount of acceleration to be applied, in gravity units (g) if other than test condition E (see 3).

b. When required, measurements to be made after test.

c. Any variations in duration or limitations to orientation (e.g., Y_1 only) (see 3).

d. Sequence of orientations, if other than as specified (see 3).

METHOD 2002.3

MECHANICAL SHOCK

1. PURPOSE. The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

2. APPARATUS. The shock-testing apparatus shall be capable of providing shock pulses of 500 to 30,000 g (peak) as specified with a pulse duration between 0.1 and 1.0 millisecond, to the body of the device. The acceleration pulse shall be a half-sine waveform with an allowable distortion not greater than ±20 percent of the specified peak acceleration, and shall be measured by a transducer and optional electronic filter with a cut-off frequency of at least 5 times the fundamental frequency of the shock pulse. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ±0.1 millisecond or ±30 percent of the specified duration.

3. PROCEDURE. The shock-testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Means may be provided to prevent the shock from being repeated due to "bounce" in the apparatus. Unless otherwise specified, the device shall be subject to 5 shock pulses of the peak (g) level specified in the selected test condition and for the pulse duration specified in each of the orientations X_1, X_2, Y_2, Y_1, Z_1, and Z_2. For devices with internal elements mounted with the major plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount. Unless otherwise specified, test condition B shall apply.

Test condition	g level (peak)	Duration of pulse (ms)
A	500	1.0
B	1,500	0.5
C	3,000	0.3
D	5,000	0.3
E	10,000	0.2
F	20,000	0.2
G	30,000	0.12

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurements or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition, if other than test condition B (see 3).

b. Number and direction of shock pulses, if other than specified (see 3).

c. Electrical-load conditions, if applicable (see 3).

d. When required, measurement made after test (see 3 and 3.1).

e. When required, measurement during test.

METHOD 2003.7

SOLDERABILITY

1. PURPOSE. The purpose of this test method is to evaluate the solderability of terminations (including leads up to 0.125 inch in diameter) that are normally joined by a soldering operation. This evaluation is made on the basis of the ability of these terminations to be wetted by a coating of solder, and to produce a suitable fillet when dip soldered. These procedures will test whether the treatment used in the manufacturing process to facilitate soldering is satisfactory and that it has been applied to the required portion of the part that is designed to accommodate a solder connection. An accelerated aging test is included in this test method that simulates natural aging under a combination of various storage conditions that have different deleterious effects.

1.1 Terms and definitions. The definition of terms shall be in accordance with the following:

1.1.1 Solderability. The property of a metal to be wetted by solder.

1.1.2 Wetting. The formation of a relatively uniform, smooth and unbroken film of solder, adherent to the surface tested.

1.1.3 Porosity. A condition of a solder coating with a spongy appearing, uneven surface that contains a concentration of small pinholes and pits. See figure 2003-1.

1.1.4 Nonwetting. A condition whereby a surface has contacted molten solder, but the solder has not adhered to all of the surface, and the surface tested remains exposed. See figure 2003-2.

1.1.5 Pinholes and voids. Holes occurring as imperfections that penetrate entirely through the solder layer. See figures 2003-3, 2003-4, and 2003-5.

1.1.6 Dewetting. A condition that results when molten solder has coated a surface and then receded leaving irregularly shaped mounds of solder separated by areas covered with a thin solder film, and where the base metal is not exposed. See figure 2003-6.

1.1.7 Foreign material. Particles of material located on, but different from, the lead material or coating. See figure 2003-7.

1.1.8 Solder and flux minimum application depth.

1.1.8.1 Dual-in-line packages. The location at which the termination widens to its maximum shoulder dimension, or to the package base plane, whichever is the further point from the seal.

1.1.8.2 Radial-lead packages (e.g., flatpacks, top brazed quads). A location on the lead, no greater than 0.05 inch from the package.

1.1.8.3 Axial-lead packages (e.g., TO cans, PGA, and platform packages). A location on the lead that is no greater than 0.05 inch from the body of the package, the seating plane, or the standoff, whichever is the furthest from the glass seal.

1.1.8.4 Leaded chip carriers (i.e., J bend, gull wing). A location on the leads equal to an extension of the base plane onto the leads, or the point at which the lead widens.

1.1.8.5 Leadless chip carriers. The location that provides for complete immersion of the termination.

2. APPARATUS.

2.1 Solder pot. A solder pot of sufficient size to contain at least two pounds of solder shall be used. The solder shall be static during the dipping procedure. The apparatus shall be capable of maintaining the solder at the temperature specified in 4.4.

2.2 Dipping mechanism. A dipping mechanism capable of controlling the rates of immersion and emersion of the terminations and providing a dwell time (total time at the required depth) in the solder bath as specified in 4.4 shall be used. The sample holder shall not come in contact with the solder bath and shall be designed to minimize the trapping of flux.

2.3 Optical equipment. A binocular optical system capable of providing a minimum magnification of 10X shall be used.

2.3.1 Lighting equipment. A lighting system shall be used that will provide a uniform, nonglare, nondirectional illumination of the specimen.

2.4 Steam aging equipment. A noncorrodible container and cover of sufficient size to allow the placement of specimens inside the vessel shall be used. The specimens shall be placed such that the lowest portion of the specimen is a minimum of 1.5 inches above the surface of the water (see 3.4). A suitable method of supporting the specimens shall be improvised using noncontaminating material. The apparatus shall be capable of having the specified temperature verified as required by 4.2.

2.4.1 Cleaning of the system. The apparatus shall be drained and cleaned at least once per month or prior to use. A more frequent cleaning cycle may be necessary as indicated by resistivity, visual, or general cleanliness of the water. No contaminating solvents shall be used.

3. MATERIALS

3.1 Flux. The flux shall conform to flux type symbol "A" (flux type "L0") of ANSI/J-STD-004, Requirements for Soldering Fluxes (previously designated as type "R" in MIL-F-14256) (25 percent by weight gum rosin in a 99 percent isopropyl alcohol solvent). The specific gravity of the flux shall be maintained within the range of 0.838 to 0.913 at 25°C. The customer/equipment manufacturer may, at their option, use flux type symbol "A" or "B" (flux type "L0" or "L1") flux (previously designated as "RMA" in MIL-F-14256).

3.2 Solder. The acquired solder shall conform to type Sn63A or Pb37A (previously designated as Sn63 in QQ-S-571) or Sn60A or Pb40A (previously designated as Sn60 in QQ-S-571) of ANSI/J-STD-006, Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications.

3.3 Isopropyl alcohol. Commercial grade isopropyl alcohol or better shall be used.

3.4 Water. The water to be used for steam aging purposes shall be either distilled or deionized.

WARNING: These materials may involve substances that are flammable, toxic to eyes, skin, or respiratory tract, or present a serious burn potential. Eye and skin protection should be used. Heat resistant gloves should be used when handling hot objects.

4. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the acquisition document. The test may be performed just prior to packaging for storage or shipment, immediately upon removal from the manufacturer's protective packaging, or as a qualification or quality conformance test. The sample shall be selected at random. During handling, special care shall be exercised to prevent the surfaces being tested from being abraded or contaminated by grease, perspiration, or abnormal atmospheres. The test procedure shall consist of the following operations:

a. Proper preparation of the specimens (see 4.1), if applicable.

b. Aging of all specimens (see 4.2).

c. Application of flux and immersion of the terminations into molten solder (see 4.3 and 4.4).

d. Examination and evaluation of the tested portions of the terminations upon completion of the solder-dip process (see 4.5).

4.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed prior to testing. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the acquisition document. The customer/equipment manufacturer, may, at their option, clean the terminations using a nonabrasive, nonactive solvent (e.g., isopropyl alcohol).

4.2 Steam aging. Prior to the application of the flux and subsequent solder dips, all specimens assigned to this test shall be subjected to aging by exposure of the surfaces to be tested to water vapor for 8 hours ±0.5 hour in the apparatus specified in 2.4. The water vapor temperature at the component lead level shall be in accordance with table I. Aging may be interrupted once for 10 minutes maximum. The devices shall be removed from the test apparatus upon completion of the specified test period.

4.2.1 Drying and storage procedures. Upon removing the test specimens from the apparatus, the parts may be dried using one of the following procedures:

a. Bake at 100°C maximum for no more than 1 hour in a dry atmosphere (dry nitrogen atmosphere is recommended).

b. Air dry at ambient temperature for a minimum of 15 minutes.

NOTE: Parts not solderability-tested within 2 hours after removal from the aging apparatus shall be stored in a desiccant jar or dry nitrogen cabinet for a maximum of 72 hours before testing. The parts shall not be used for testing if they have exceeded the storage requirements.

4.3 Application of flux. The terminations to be tested shall be immersed in flux maintained at room ambient temperature. The terminations, unless otherwise specified in the individual specification, shall be immersed according to 1.1.8. The terminations to be tested shall be immersed in the flux for 5 to 10 seconds, and shall be drained for 5 to 20 seconds prior to dipping in the solder pot. The flux shall be covered when not in use and discarded a minimum of once a day. Any obvious droplets of flux clinging to the termination may be removed by blotting.

4.4 Solder dip procedure. The dross and burned flux shall be skimmed from the surface of the molten solder prior to testing. A wave solder pot may be used for this purpose, but the solder shall be static during the dipping procedure. The molten solder shall be at a uniform temperature of 245°C ±5°C (473°F, ±9°F). (Skimming may not be required in wave or flow pots). The part shall be attached to a dipping mechanism (see 2.2) and the flux covered terminations immersed once (except for the possible duplicate immersion of corner terminations on leadless packages) in the molten solder to the depth specified in 1.1.8. NOTE: The test sample shall not be suspended above the hot solder pot for longer than 7 seconds. The immersion and emersion rates shall be 1.0 inch per second ±.25 inch per second. The dwell time in the solder shall be 5 seconds ±.5 second. The dwell time for terminations greater than or equal to 0.040 inch in diameter shall be 7 seconds ±.5 second. After the dipping process, the part shall be allowed to cool in air. Residual flux shall be removed from the terminations by dipping the parts in isopropyl alcohol or other suitable solvent. If necessary, a clean soft cloth, cotton swab, or equivalent, moistened with clean isopropyl alcohol or other suitable solvent, may be used to remove all remaining flux.

4.4.1 Solder dipping of gold plated terminations. Gold plated terminations shall be cycled twice in flux and solder using one or two solder pots. The first immersion is to scavenge the gold on the terminations. It is recommended that a separate solder pot be used for gold plated devices.

4.4.2 Immersion angle. Unless otherwise specified, the terminations shall be immersed perpendicular to the solder surface. For leaded or leadless chip carriers, the terminations shall be immersed at a 30° to 45° angle to the solder surface.

4.4.3 Solder bath contaminants. The manufacturer shall have a system to verify that the solder bath does not exceed the contaminant levels specified in table II.

TABLE I. Altitude versus steam temperature (see 4.2).

Altitude (feet)	Steam temperature (°C +3, -5)
0 - 2,000	93
2,001 - 4,000	91
4,001 - 6,000	89
Greater than 6,000	87

TABLE II. Maximum limits of solder bath contaminant (see 4.4.3).

Contaminant	Contaminant percentage limit
Copper	0.300
Gold	0.200
Cadmium	0.005
Zinc	0.005
Aluminum	0.006
Antimony	0.500
Iron	0.020
Arsenic	0.030
Bismuth	0.250
Silver	0.100
Nickel	0.010

NOTE: The total copper, gold, cadmium, zinc, and aluminum contaminants shall not exceed 0.4 percent.

4.5 Examination of terminations. The dipped portion of the terminations shall be examined using a magnification of 10-15X. Verification of failures may be accomplished with higher magnifications up to 60X. The customer/equipment manufacturer of the component may establish a critical portion of the termination within the dipped area. The customer/equipment manufacturer has the option to accept solderability defects outside their established critical area. The customer/equipment manufacturer has the option of cleaning parts to remove carbonate/sulfate deposits caused by exposure of the parts to the steam aging or cleaning process. The customer/equipment manufacturer shall assure that the cleaning process does not adversely affect the physical, mechanical, electrical, or reliability performance of the parts. This cleaning process shall be fully documented. For leaded devices only, the cut portions of the lead which expose lead ends shall not be used for examination and evaluation of the solder coverage of the termination.

4.5.1 Criteria for acceptance. The criteria for acceptable solderability (see figures 2003-1 through 2003-7) are:

a. The dipped portion of the terminations is at least 95 percent covered by a continuous new solder coating.

b. Pinholes, voids, porosity, nonwetting, or dewetting do not exceed 5 percent of the total area.

c. For leadless terminations and elements having solder attachment terminations, there shall be no solder bridging between any termination area and any other metallization not connected to it by design. In the event that the solder dipping causes bridging, the test shall not be considered a failure provided that a local application of heat (e.g., gas, soldering iron, or redipping) results in solder pullback and no wetting of the dielectric area as indicated by microscopic examination. The area of the surface to be tested shall be as specified in 1.1.8.

NOTE: The total area of the surface to be tested including all faces for rectangular leads) as specified in 4.5 shall be examined. In the case of a dispute, the percentage of coverage with pinholes or voids shall be determined by the actual measurement of those areas, compared to the total area(s).

5. SUMMARY. The following details are to be specified in the individual specifications unless otherwise noted:

a. The number of terminations of each part to be tested (see 4).

b. Special preparations of the terminations, if applicable (see 4.1).

c. Depth of immersion if other than in 1.1.8.

d. Magnification, if other than in 2.3.

e. Solder composition, flux, and temperature if other than those specified in this document.

f. Number of cycles, if other than one, or as noted in this test method. Where more than one cycle is specified to test the resistance of the device to heat as encountered in multiple solderings, the examinations and measurements required shall be made at the end of the first cycle and again at the end of the total number of cycles applied. Failure of the device on any examination and measurement at either the one-cycle or the end point shall constitute a failure to meet this requirement.

FIGURE 2003-1. Porosity.

FIGURE 2003-2. Nonwetting.

How to use this chart:

1. The chart is set-up for .5 inch long leads.
2. View the entire circumference of the lead.
3. Locate the lead diameter on the left side of the chart.
4. Locate the diameter of the void on the top of the chart.

	0.001	0.003	0.005	0.010	0.015	0.020	0.030	0.040
0.010	1000	111	40	10	4.4	2.5	1.10	0.62
0.015	1500	167	60	15	6.6	3.75	1.60	0.937
0.020	2000	222	80	20	8.8	5	2.22	1.25
0.030	3000	333	120	30	13.0	7.5	3.33	1.87
0.040	4000	444	160	40	17.7	10	4.44	2.50
0.050	5000	555	200	50	22.0	12.5	5.55	3.12
0.060	6000	666	240	60	26.6	15	6.66	3.75

Examples for less than .5 inch leads:

A. Lead length = 0.350.
B. 0.350/0.500 = 0.700.
C. To determine the number of acceptable voids, multiply the number of voids on the chart by 0.700.
D. For a 0.01 inch void on a 0.010 inch diameter lead = 700 voids.
E. For leads greater than 1.0 inch in length, see 4.5.

FIGURE 2003-3. Solderability evaluation guidelines.

FIGURE 2003-4. Solderability coverage of a 0.5 inch, .025 diameter lead at 10X magnification.

FIGURE 2003-5. Pinholes.

FIGURE 2003-6. Dewetting.

FIGURE 2003-7. Foreign material.

METHOD 2004.5

LEAD INTEGRITY

1. PURPOSE. This method provides various tests for determining the integrity of microelectronic device leads (terminals), welds, and seals. Test condition A provides for straight tensile loading. Test condition B_1 provides for application of bending stresses to determine integrity of leads, seals, and lead plating while B_2 employs multiple application of bending stresses primarily to determine the resistance of the leads to metal fatigue under repeated bending. Test conditions C_1 and C_2 provide for application of torque or twisting stresses to device leads or studs, respectively, to determine integrity of leads and seals. Test condition D provides for application of peel and tensile stresses to determine integrity of terminal adhesion and plating of leadless packages. It is recommended that this test be followed by a seal test in accordance with method 1014 to determine any effect of the stresses applied on the seal as well as on the leads (terminals).

2. APPARATUS. See applicable test condition.

3. GENERAL PROCEDURE APPLICABLE TO ALL TEST CONDITIONS. The device shall be subjected to the stresses described in the specified test condition and the specified end-point measurements and inspections shall be made except for initial conditioning or unless otherwise specified. Unless otherwise specified, the LTPD sampling shall apply to the leads, terminals, studs or pads chosen from a minimum of 3 devices.

4. SUMMARY. The following details and those required by the specific test condition shall be specified in the applicable acquisition document:

a. Test condition letter.

b. Number and selection of leads (terminals), if different from above.

TEST CONDITION A - TENSION

1. PURPOSE. This test is designed to check the capabilities of the device leads, welds, and seals to withstand a straight pull.

2. APPARATUS. The tension test requires suitable clamps and fixtures for securing the device and attaching the specified weight without lead restriction. Equivalent linear pull test equipment may be used.

3. PROCEDURE. A tension of 0.227 kg (8 ounces), unless otherwise specified, shall be applied, without shock, to each lead or terminal to be tested in a direction parallel to the axis of the lead or terminal and maintained for 30 seconds minimum. The tension shall be applied as close to the end of the lead (terminal) as practicable.

3.1 Failure criteria. When examined using 10X magnification after removal of the stress, any evidence of breakage, loosening, or relative motion between the lead (terminal) and the device body shall be considered a failure. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), meniscus cracks shall not be cause for rejection of devices which pass the seal test.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Weight to be attached to lead, if other than .227 kg (8 ounces) (see 3).

b. Length of time weight is to be attached, if other than 30 seconds (see 3).

TEST CONDITION B_1 - BENDING STRESS

1. PURPOSE. This test is designed to check the capability of the leads, lead finish, lead welds, and seals of the devices to withstand stresses to the leads and seals which might reasonably be expected to occur from actual handling and assembly of the devices in application, or to precondition the leads with a moderate bending stress prior to environmental testing.

2. APPARATUS. Attaching devices, clamps, supports, or other suitable hardware necessary to apply the bending stress through the specified bend angle.

3. PROCEDURE. Each lead or terminal to be tested shall be subjected to force sufficient to bend the lead as specified in 3.1 through 3.5, as applicable. Any number or all of the leads of the test device may be bent simultaneously. Rows of leads may be bent one row at a time. Each lead shall be bent through one cycle as follows: Bend through the specified arc in one direction and return to the original position. All arcs shall be made in the same plane without lead restriction.

3.1 Direction of bends. Test leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. No lead shall be bent so as to interfere with another lead. If interference is unavoidable, the test lead shall be bent in the opposite direction to the angle specified and returned to its normal position.

3.2 Procedure for initial conditioning of formed leads. When normally straight leads are supplied in a formed condition (including the staggered lead dual-in- line configuration), the lead forming operation shall be considered acceptable initial conditioning in place of that specified, provided the lead forming has been done after lead plating and the forming is at least as severe in permanent lead deformation as the specified bending.

3.3 Procedure for flexible and semi-flexible leads (e.g., flat packs and axial-lead metal-can devices).

3.3.1 Flexible leads. A lead shall be considered flexible if its section modulus (in the least rigid direction) is less than or equal to that of a rectangular lead with a cross section of 0.15 x 0.51 mm (.006 x .020 inch). Round leads less than or equal to 0.51 mm (.020 inch) in diameter shall be considered flexible. Flexible leads shall be bent through an arc of at least 45° measured at a distance 3.05 ±.76 mm (0.120 ±0.03 inch) along the lead from the seal unless otherwise specified.

3.3.2 Semi-flexible leads. Semi-flexible leads are those leads with a section modulus (in the least rigid direction) greater than that of a rectangular lead with a cross section of 0.15 x 0.51 mm (0.006 x 0.020 inch) which are intended to be bent during insertion or other application. Round leads greater than 0.51 mm (.020 inch) diameter shall be considered semi-flexible except as noted in 3.5. Semi-flexible leads shall be bent through an arc of at least 30° measured at the lead extremities unless otherwise specified.

3.4 Procedure for dual-in-line and pin grid array package leads. Dual-in-line package leads are leads with more than one section modulus, with leads normally aligned in parallel at a 90° angle from the bottom of the package during insertion. Dual-in-line package leads shall be bent inward through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. For configuration 1 and 2, the angle of bend shall be measured from the lead extremities to the first bend (see figure 2004-1), For configuration 3, the angle of bend shall be measured from the lead extremities to the seating plane (see figure 2004-1). Pin grid array packages shall have the leads required for testing from the outside row of leads on opposite sides bent through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. The angle of bend shall be 15° from normal and the bend shall be made at the approximate seating plane. At the completion of the initial bend, the leads shall be returned to their approximate original position.

3.5 Procedure for rigid leads or terminals. A lead or terminal shall be considered rigid if it is not intended to be flexed in mounting, and not covered in 3.3 or 3.4. Devices with terminals complying with this description shall be subjected to a normal mounting operation and removal, unless otherwise specified. When the normal mounting/removal operation is destructive to the terminals (e.g., terminal weld, wire wrap), the initial conditioning need not be performed.

3.6 Failure criteria. When examined using magnification between 10X and 20X after removal of the stress, any evidence of breakage, loosening, or relative motion between the terminal lead and the device body shall be considered a device failure. When specified, post-test measurements (see 4) shall be made after visual examination. When the above procedures are used as initial conditioning in conjunction with other tests, these measurements may be conducted at the conclusion of that test or sequence of tests.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Bending arc, if other than that specified.

b. Procedure, if other than that specified.

c. Number and selection of leads and procedure for identification, if other than that specified.

d. Post test measurements, if applicable (see 3.6)

TEST CONDITION B_2 - LEAD FATIGUE

1. PURPOSE. This test is designed to check the resistance of the leads to metal fatigue.

2. APPARATUS. Attaching devices, clamps, supports, or other suitable hardware necessary to apply a repeated bending stress through the specified bend angle.

3. PROCEDURE. The appropriate procedure of 3.1 or 3.2 for the device under test shall be used.

3.1 Procedure for dual-in-line packages. The leads to be tested shall be subjected to three cycles of test condition B_1 and shall be subjected to a force sufficient to bend the leads as specified in 3.4 of condition B_1.

3.2 Procedure for flat packages and can packages. A force of 0.229 ±0.014 kg (8 ±0.5 ounces), unless otherwise specified, shall be applied to each lead to be tested for three 90° ±5° arcs of the case. For leads with a preplated or prefinished section modulus equal to or less than that of a rectangular lead with a cross section of 0.16 x 0.51 mm (0.006 x 0.020 inches) or round leads with a cross section of 0.51 mm (0.020 inch) in diameter, the force shall be 0.085 ±0.009 kg (3 ±0.3 ounces). Section modulus is defined as $bc^2/6$ for rectangular leads, and $0.098\ (\phi b_1)^3$ for round leads (see MIL-STD-1835). An arc is defined as the movement of the case, without torsion, to a position perpendicular to the pull axis and return to normal. All arcs on a single lead shall be made in the same direction and in the same plane without lead restriction. A bending cycle shall be completed in from 2 to 5 seconds. For devices with rectangular or ribbon leads, the plane of the arcs shall be perpendicular to the flat plane of the lead. The test shall not be applied to end leads of packages where its application will apply primarily torsion forces at the lead seal.

3.2.1 Optional procedure for fine pitch/small leads. A force as determined by the following formula unless otherwise specified, shall be applied to each lead to be tested for 90 degrees ±5 degree arcs of the device. All other conditions of section 3.2 shall apply: Weight = (area in square inches) x 2.1 % x (K psi) x 453.6 grams/lb. Where K is based on the ultimate tensile strength (UTS) for a particular material. Typical value for kovar and alloy 42 are listed below. The UTS for other materials can be found in vendor data sheets. The result shall be rounded to the nearest whole number.

NOTE: A lead pitch of less than or equal to 25 mils is considered fine pitch.

Material	UTS in psi
Kovar	75000
Alloy 42	71000

3.3 Failure criteria. A broken lead on a device shall be considered a failure. When examined using magnification between 10X and 20X after removal of the stress, any device which exhibits any evidence of breakage, loosening, or relative motion between the terminal lead and the device body shall be considered a device failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Force to be applied to the lead, if other than above (see 3).

b. Number of cycles, if other than above (see 3).

c. Maximum bend angle, if other than above (see 3).

TEST CONDITION C_1 - LEAD TORQUE

1. PURPOSE. This test is designed to check device leads (or terminals) and seals for their resistance to twisting motions.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or other suitable method of applying the specified torque without lead restriction.

3. PROCEDURE. The appropriate procedure of 3.1 or 3.2 for the device under test shall be used.

3.1 Procedure for devices with circular cross-section terminals or leads. The device body shall be rigidly held and the specified torque shall be applied for 15 seconds minimum to the lead (terminal) to be tested, without shock, about the axis of the lead (terminal).

3.2 Procedure for devices with rectangular cross-section terminals or leads. The device body shall be rigidly held and a torque of 1.45 ±.145 kg-mm (2.0 ±0.2 ounce-inch) unless otherwise specified, shall be applied to the lead (terminal) at a distance of 3.05 ±0.76 mm (0.12 ±0.03 inch) from the device body or at the end of the lead if it is shorter than 3.05 mm (0.12 inch). The torque shall be applied about the axis of the lead once in each direction (clockwise and counterclockwise). When devices have leads which are formed close to the body, the torque may be applied 3.05 ±0.76 mm (0.12 ±0.03 inch) from the form. For device leads which twist noticeably when less than the specified torque is applied, the twist shall be continued until the twist angle reaches 30° ±10° or the specified torque is achieved, whichever condition occurs first. The lead shall then be restored to its original position.

3.3 Failure criteria. When examined using magnification between 10X and 20X after removal of the stress, any evidence of breakage, loosening, or relative motion between the terminal (lead) and the device body shall be considered a device failure. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), meniscus cracks shall not be cause for rejection of devices which pass the seal test.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Torque to be applied for circular cross-section leads (see 3.1).

b. Duration of torque application for circular cross-section leads, if other than 15 seconds minimum (see 3.1).

c. Torque to be applied for rectangular cross-section leads, if other than 1.45 ±0.145 kg-mm (2.0 ±0.2 ounce-inch) (see 3.2).

d. See general summary above.

TEST CONDITION C_2 - STUD TORQUE

1. PURPOSE. This test is designed to check the resistance of the device with threaded mounting stud to the stress caused by tightening the device when mounting.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or suitable method of applying the specified torque.

3. PROCEDURE. The device shall be clamped by its body or flange. A flat steel washer of a thickness equal to six thread pitches of the stud being tested and a new class 2 fit steel nut shall be assembled in that order on the stud, with all parts clean and dry. The specified torque shall be applied without shock to the nut for the specified period of time. The nut and washer shall then be disassembled from the device, and the device then examined for compliance with the requirements.

3.1 Failure criteria. The device shall be considered a failure if any of the following occurs:

a. The stud breaks or is elongated greater than one-half of the thread pitch.

b. It fails the specified post-test end point measurements.

c. There is evidence of thread stripping or deformation of the mounting seat.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The amount of torque to be applied (see 3).

b. Length of time torque is to be applied (see 3).

c. Measurements to be made after test (see 3).

TEST CONDITION D - SOLDER PAD ADHESION FOR LEADLESS CHIP CARRIER AND SIMILAR DEVICES

1. PURPOSE. This test is designed to check the capabilities of the device solder pads to withstand a delamination (peel) stress of specified tension and time.

2. APPARATUS. Equipment for 10X magnification, suitable clamps and fixtures for securing the device and applying the specified tension/time conditions to wires soldered to the device solder pads. Equivalent linear pull test equipment may be used.

• 3. PROCEDURE. Unless otherwise specified, a delamination (peel) stress test shall be applied to randomly selected solder pads from each device selected for test. Further, unless otherwise specified, the sampling shall be Sample Size Number = 15, c = 0 based on the number of solder pads tested, chosen from a minimum of three devices. Preparation and testing of devices shall be in accordance with figure 2004-2 of this method and as follows.

• a. Pretinned soft annealed solid copper wire of a gauge (diameter) nearest, but not exceeding that of the nominal solder pad width, shall be soldered using Sn60A or Pb40A or Sn63A or Pb37A of ANSI/J-STD-006 (previously known as Sn60 or Sn63 solder in accordance with QQ-S-571) to each solder pad to be tested in a manner such that the wire is bonded over the entire solder pad length and terminates at the package edge (see figure 2004-2). The unsoldered portion of the wire shall be bent perpendicular to the bond plane prior to attachment. Caution should be taken to assure that the solder pad metallization is not damaged during the soldering or the wire bending operation.

b. Unless otherwise specified, a minimum tension of 8 ounces (2.22 N) shall be applied, without shock, to each solder pad to be tested in a direction perpendicular to the solder pad surface and maintained for 30 seconds minimum.

3.1 Failure criteria. When examined, using 10X magnification, after removal of the tension stress, the appearance of any delamination involving constituent solder pad interfaces shall be considered an adhesion failure of the solder pad. Separation of the solder pad from the device is an obvious (without visual magnification) adhesion failure. Separation of the wire from the solder fillet (leaving the solder pad intact) or wire breakage is considered a test procedure failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Sampling criteria, if other than specified (see 3.1).

b. Failure criteria, if other than specified (see 3.1).

c. Tension to be applied in this test if other than 8 ounces (2.22 N).

d. Length of time tension is to be applied if other than 30 seconds.

FIGURE 2004-1 Angle of bend for dual-in-line package configurations.

MATERIALS

Flux: Flux type symbol "A" or "B" (flux type "L0" or "L1") in accordance with ANSI/J-STD-004 (previously designated as Type R or RMA only, in accordance with MIL-F-14256).

Solder: Sn60A or Pb40A or Sn63A or Pb37A in accordance with ANSI/J-STD-006 (previously designated as Sn 60 or Sn 63 in accordance with QQ-S-571).

Wire: Soft annealed solid copper.

FIGURE 2004-2 Solder pad adhesion.

METHOD 2005.2

VIBRATION FATIGUE

1. PURPOSE. The purpose of this test is to determine the effect on the device of vibration in the frequency range specified.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the sustained vibration within the specified levels and the necessary optical and electrical equipment to conduct post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with a constant amplitude simple harmonic motion having a peak acceleration corresponding to the specified test condition. For test condition A, constant amplitude harmonic motion in the range of 60 ±20 Hz having an amplitude of 0.06 inch double amplitude (total excursion) shall be acceptable as an alternative to the specified peak acceleration. The vibration shall be applied for 32 ±8 hours minimum, in each of the orientations X, Y, and Z for a total of 96 hours, minimum. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, g
A	20
B	50
C	70

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

3.3 Test frequency and amplitude. For test condition A, B, or C, the double amplitude and frequency used shall result in the application of the peak accelerations of 20, 50, or 70 g's. Peak acceleration may be computed using the following equation:

$$g = \frac{A\,(F)^2}{(2)\,(386)}$$

Where: A = double amplitude in inches.
F = frequency in radians/second.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Test frequency and test double amplitude (see 3 and 3.3), if other than specified.

c. Test time and specimen orientation, if other than specified (see 3).

d. Measurements after test (see 3 and 3.1).

METHOD 2006.1

VIBRATION NOISE

1. PURPOSE. The purpose of this test is to measure the amount of electrical noise produced by the device under vibration.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels, a calibrated high impedance voltmeter for noise measurement during test and the necessary optical and electronic equipment for post-test measurements.

3. PROCEDURE. The device and its leads shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion having either an amplitude of 0.06 inch double amplitude (maximum total excursion) or a constant peak acceleration of 20 g minimum. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range shall be traversed in not less than 4 minutes for each cycle. This cycle shall be performed once in each of the orientations X, Y, and Z (total of 3 times), so that the motion shall be applied for a total period of approximately 12 minutes. The specified voltages and currents shall be applied in the test circuit. The maximum noise-output voltage across the specified load resistance during traverse, shall be measured with an average-responding root-mean-square (rms) calibrated high impedance voltmeter. The meter shall measure, with an error of not more than 3 percent, the rms value of a sine-wave voltage at 2,000 Hz. The characteristic of the meter over a bandwidth of 20 to 2,000 Hz shall be ±1 decibel (dB) of the value at 2,000 Hz, with an attenuation rate below 20 and above 20,000 Hz of 6 ±2 dB per octave. The maximum inherent noise in the circuit shall be at least 10 dB below the specified noise-output voltage. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Test voltages and currents (see 3). Unless otherwise specified, these shall be the nominal operating voltages and currents for the device.

c. Load resistance (see 3). Unless otherwise specified, this shall be the maximum rated operating load of the device.

d. Measurements after test (see 3 and 3.1).

e. Noise-output voltage limit (see 3).

METHOD 2007.2

VIBRATION, VARIABLE FREQUENCY

1. PURPOSE. The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range. This is a destructive test.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels and the necessary optical and electrical equipment for post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion having either a peak to peak amplitude of 0.06 inch (±10 percent) or a peak acceleration of the specified test condition A, B, or C (+20 percent, -0 percent g). Test conditions shall be amplitude controlled below the crossover frequency and g level controlled above. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range of 20 to 2,000 Hz and return to 20 Hz shall be traversed in not less than 4 minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (total of 12 times), so that the motion shall be applied for a total period of not less than 48 minutes. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, g
A	20
B	50
C	70

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Measurements after test (see 3 and 3.1).

METHOD 2008.1

VISUAL AND MECHANICAL

Method 2008 is canceled effective 15 November 1974. It is superseded by methods 2014, 2015, and 2016. Test condition A of method 2008 is superseded by method 2016. Test condition B, except for 3.2.1 (Marking), is superseded by method 2014. Paragraph 3.2.1 is superseded by method 2015.

METHOD 2009.9

EXTERNAL VISUAL

1. PURPOSE. The purpose of this test method is to verify the workmanship of hermetically packaged devices. This test method shall also be utilized to inspect for damage due to handling, assembly, and/or test of the packaged device. This examination is normally employed at outgoing inspection within the device manufacturer's facility, or as an incoming inspection of the assembled device.

2. APPARATUS. Equipment used in this test shall be capable of demonstrating device conformance to the applicable requirements. Equipment shall include optical devices capable of magnification of at least 1.5X to 10X, with a relatively large and accessible field of view.

3. PROCEDURE

3.1 Magnification. Devices shall be examined at 1.5X to 10X magnification. Devices may be examined anywhere in the range of 1.5X to 10X, however, acceptable product must be capable of passing all criteria when examined at 10X magnification. Individual glass seals (see 3.3.8) shall be examined at 7X to 10X magnification.

3.2 Foreign material. When foreign material is present, and its adherence is in question, the device may be subjected to a clean filtered gas stream (vacuum or expulsion) of approximately 20 psig.

3.3 Failure criteria. Devices shall fail if they exhibit any of the following:

3.3.1 General

a. Illegible marking, or marking content or placement not in accordance with the applicable specification.

b. Presence of any secondary coating material that visually obscures a seal area(s) (i.e., any hermetic interface).

c. Evidence of any nonconformance with the detail drawing or applicable procurement document, or absence of any required feature.

3.3.2 Foreign/displaced material

a. Braze material flow, or other foreign material (i.e., contamination or corrosion) that reduces the isolation between leads or between braze pads to less than 50% of the lead separation (pad separation for brazed leads) but in no case less than the case outline minimum.

b. Leads or terminals that are not free of foreign material such as paint or other adherent deposits.

3.3.3 Construction defects

a. Protrusions on the bottom (mounting) surface of the package that extend beyond the seating plane.

b. Protrusions (excluding glass run-out) on any other package surface that exceed the lead thickness in height (leaded packages).

c. Protrusions on the lid or cover, or extending beyond the surface plane of solder pads, that exceed 25% of the terminal width in height (leadless packages).

d. Metallization not intended by design between solder pads, between elements of thermal patterns and/or between seal ring or lid to metallized castellations that reduce the isolation to less than 50% of pad separation (leadless packages).

3.3.4 Package Body/Lid Finish

a. Defective finish (peeling, flaking, pitting, blistering, or corrosion). Discoloration that does not exhibit these conditions is acceptable.

b. Scratches, mars, or indentations, either due to damage or processing, that expose base metal. Exposed underplate is acceptable.

3.3.5 Leads

a. Broken leads.

b. Leads or terminals that are not intact or aligned in their normal location, free of sharp or unspecified lead bends, or twisted more than 20° from the normal lead plane.

c. Leads with pits and/or depressions that exceed 25% of the width (diameter for round leads) and are greater than 50% of the lead thickness in depth.

d. Leads with burrs exceeding a height greater than 50% of the lead thickness.

e. Lead misalignment to the braze pad to the extent that less than 75% of the lead braze section is brazed to the pad.

f. Metallization (including solder lead finish) in which the isolation between leads or between lead and other package metallization is reduced to less than 50% of lead separation (pad separation for brazed leads) but in no case less than the case outline minimum.

g. Braze material that increases the lead dimensions to greater than 1.5 times the lead thickness above the design maximum between the seating plane and the ceramic body or that increases the lead dimensions to greater than the design maximum below the seating plane.

h. Scratches that expose base metal over more than 5% of the lead surface area. Exposed base metal on the cut lead ends is acceptable and does not count in the 5%.

3.3.6 Package body/lid - leaded devices

a. Broken packages or cracks in the packages. Surface scratches shall not be cause for failure except where they violate other criteria stated herein for marking, finish, etc.

b. Any chipout dimension that exceeds 0.060 inch in any direction on the surface and has a depth that exceeds 25% of the thickness of the affected package element (e.g., cover, base, or wall).

c. External lead metallization stripe forming a conductor to a brazed lead that exhibits voids greater than 25% of the conductor width.

d. Evidence of cracks, delamination, separation, or voiding on any multilayer ceramic package.

3.3.7 Package body/lid - leadless devices

a. Ceramic chip-outs that dimensionally exceed 50% of the distance between terminals in any direction on the affected surface (edge or corner), and exceed a depth of 25% of the thickness of the affected package element (e.g., cover, lid, base, or wall).

b. Evidence of cracks, delamination, separation, or voiding on any package element.

c. Castellation to solder pad misalignment. The metal in the castellation, exclusive of the angular ring, shall be within the visually extended boundaries of the solder pad (see figure 2009-1).

FIGURE 2009-1. Castellation to solder pad misalignment.

d. Castellation configuration not in accordance with the following (see figure 2009-2). The castellation shall be roughly concave, confined by a 3-dimensional space traversing all castellated ceramic layers at the package edge. The surface of the castellation may be irregular. The "3-dimensional space" has these dimensions:

1. Minimum width >1/3 package terminal pad width.

2. Minimum depth > 1/2 castellation minimum width.

3. Length = as designed (see figure 2009-2).

4. Maximum width ≤ package terminal pad width.

5. Maximum depth ≤ 1/2 castellation maximum width.

These dimensions are an attempt to ensure with some reasonableness that the castellations are not viewed, in the extreme sense, as virtual flat surfaces on the package edge and are not virtual closed vias (holes).

NOTE: Ceramic layers shift, edges are rough after punching, plating buildup is not smooth etc., all of these combine during package manufacture to make the castellation measurement difficult. Therefore, in the event of conflicts in determining castellation acceptance, direct contact measurement shall be made using the limits specified in MIL-STD-1835.

FIGURE 2009-2. Castellation requirements

3.3.8 Glass seals.

a. Crazing of the glass seal surface (see figure 2009-3).

FIGURE 2009-3. Crazed glass surface.

b. Any single circumferential crack (or overlapping crack) that does not lie completely within a single quadrant (i.e., extends beyond 90° arc or rotation about the lead), and extends beyond or is located in the region beyond the midpoint of distance from the lead to the case (see Figure 2009-4).

FIGURE 2009-4. Circumferential cracks.

c. Radial cracks that exhibit the following:

1. *Cracks that do not originate at the lead (see figures 2009-5a and 2009-5b).*

2. Three or more cracks that extend beyond the midpoints of distance from the lead to the case (see figure 2009-5c).

3. Two cracks that extend beyond the midpoint of the distance from the lead to the case and that lie within the same *quadrant (see figure 2009-5d).*

FIGURE 2009-5. Radial Cracks.

d. Any chip-out that penetrates the sealing glass deeper than the glass meniscus plane. The glass meniscus is defined as that area of glass that wicks up the lead or terminal. Exposed base metal as a result of meniscus chip outs is acceptable, provided that the exposed area is no deeper than 0.010 inch (see figure 2009-6).

FIGURE 2009-6. Chip-outs.

FIGURE 2009-7. Surface bubbles.

e. Surface bubbles that exceed the following:

1. Open bubbles in the glass seal that exceed 5 mils in diameter (see Figure 2009-7).

2. Open bubbles in strings or clusters that exceed 2/3 of the distance between the lead and the package wall.

f. Subsurface bubbles that exceed the following:

1. Large bubbles or voids that exceed 1/3 of the glass sealing area (see Figure 2009-8a).

2. Single bubble or void that is larger than 2/3 of the distance between the lead and the package wall at the site of inclusion (see Figure 2009-8b).

3. Two bubbles in a line totaling more than 2/3 distance from pin to case (see Figure 2009-8c).

4. Interconnecting bubbles greater than 2/3 the distance between pin and case (see Figure 2009-8d).

FIGURE 2009-8. Subsurface bubbles.

g. Reentrant seals that exhibit non-uniform wicking (i.e., negative meniscus) at the lead and/or body interface (see

Figure 2009-9).

FIGURE 2009-9. Reentrant seals.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Requirements for markings and the lead (terminal), or pin identification.

b. Any additional detailed requirements for materials, design, construction, and workmanship.

METHOD 2010.10

INTERNAL VISUAL (MONOLITHIC)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable acquisition document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in normal applications. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Furthermore, the criteria of this test method will be used during destructive physical analysis (DPA) following the procedures outlined in test method 5009, "Destructive Physical Analysis". Test condition A and B provide a rigorous and detailed procedure for internal visual inspection of high reliability microcircuits as specified in the screening requirements of test method 5004. For condition B product the alternate screening procedure (alternate 1) documented in test method 5004 may be used by the manufacturer as an option to internal visual inspection as specified. For condition A or B product, the alternate screening procedure (alternate 2) documented in test method 5004 may be used by the manufacture as an option to internal visual inspection as specified.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

2.1 GaAs device requirements. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table.

TABLE I. GaAs microwave device high magnification requirements.

Feature Dimensions	Magnification range
> 5 microns	75 - 150x
1 - 5 microns	150 - 400x
< 1 micron	400 - 1000x

2.2 Silicon-on-Sapphire (SOS) device requirements. SOS devices shall be inspected to all applicable criteria specified herein, except where noted. The sapphire portions of the die shall be considered "nonconductive and nonoperational material".

3. PROCEDURE.

a. General. The device shall be examined within the specified magnification range to determine compliance with the requirements of the applicable acquisition document and the criteria of the specified test condition.

The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated.

b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer.

When inverted die mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die. Devices which fail any test criteria herein are defective devices and shall be rejected and removed at the time of observation.

Visual criteria may be inspected as follows:

(1) Prior to die attachment without re-examination after die attachment; 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.4 e and f, 3.1.5, 3.1.6 a-f, 3.2.6.

(2) Prior to bonding without re-examination after bonding; 3.2.3.

(3) For condition B only; the following criteria may be inspected prior to die attachment at high power, plus low power after die attachment, provided a high magnification sample to sample size number = 45 accept number C = 0 is performed at precap inspection; 3.1.1.1, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.3, 3.1.4 a-d and g-o, 3.1.6 g and h, 3.1.7. If the sample fails the entire lot shall be reinspected at high magnification for the failed criteria.

* c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections in accordance with 3b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to condition A shall be inspected and prepared for sealing in class 100 environment and devices examined to condition B criteria shall be inspected and prepared for sealing in a class 100,000 environment, (see 40.8.1.1.7 of appendix A of MIL-PRF-38535), except that the maximum allowable relative humidity in either environment shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination perpendicular to the die surface. "Low magnification" inspection shall be performed with a metallurgical or stereomicroscope with the device under suitable illumination. Low magnification may be performed at an angle other than 90° to the die surface to facilitate the inspection. The inspection criteria of 3.2.1 may be examined at "high magnification" at the manufacturer's option.

* e. Reinspection. When inspection for product acceptance is conducted subsequent to the manufacturer's inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. When suspected defects or deficiencies are noted, additional inspection may be performed at magnifications needed to evaluate or resolve the suspect items.

f. Definitions:

(1) Active circuit area. All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.

(2) Coupling (air) bridge. A raised layer of metallization used for interconnection that is isolated from the surface of the element.

(3) Block resistor. A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

(4) Channel. An area lying between the drain and the source of FET structures.

(5) Controlled environment. Shall be class 1,000, (see 40.8.1.1.7 of appendix A of MIL-PRF-38535), except that the maximum allowable relative humidity shall not exceed 65 percent.

(6) Crazing. The presence of numerous minute cracks in the referenced material, (e.g., glassivation crazing).

(7) Detritus. Fragments of original or laser modified resistor material remaining in the kerf.

(8) Dielectric isolation. Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolating barrier such as semiconductor oxide.

(9) Diffusion tub. A volume (or region) formed in a semiconductor material by a diffusion process (n- or p- type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (*dielectric isolation, coplanar process*, SOS, SOI).

(10) Foreign material. Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.

(11) Functional circuit elements. Diodes, transistors, crossunders, capacitors, and resistors.

(12) Gate oxide. The oxide or other dielectric that separates gate metallization (or other material used for the gate electrode) from the channel of MOS structures (see figure 2010-1).

FIGURE 2010-1. P channel MOS transistor.

(13) Glassivation. The top layer(s) of transparent insulating material that covers the active circuit area, with the exception of bonding pad areas and beam leads.

(14) Glassivation cracks. Fissures in the glassivation layer.

(15) Junction line. The outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any P/N junction intended to conduct current during normal operation of the circuit element, (e.g., collector to base).

(16) Kerf. That portion of the component area from which material has been removed or modified by trimming or cutting.

(17) Line of separation. Visible distance or space between two features that are observed not to touch at the magnification in use.

(18) MESFET. (Metal semiconductor field-effect transistor). A field-effect transistor in which a metal semiconductor rectifying contact is used for the gate electrode. Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used. Both depletion-type and enhancement type devices have been manufactured. The acronyms are D-MESFET, and E-MESFET, respectively.

(19) Metallization nonadherence. Unintentional separation of material from an underlying substrate excluding air bridges and undercutting by design.

(20) Multilayered metallization (conductors). Two or more layers of metal or any other material used for interconnections that are not isolated from each other by insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal (see figure 2010-2).

FIGURE 2010-2. Multilayered metallization.

(21) Multilevel metallization (conductors). Two or more levels of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric) (see figure 2010-3).

FIGURE 2010-3. Multilevel metallization.

(22) Narrowest resistor width. The narrowest portion of a given resistor prior to trimming.

(23) Operating metallization (conductors). Metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

(24) Original width. The width dimension or distance that would have been present, in the absence of the observed abnormality (e.g., original metal width, original diffusion width, original beam width, etc.).

(25) Package post. A generic term used to describe the bonding location on the package.

(26) Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel devices.

(27) Passivation step. An abrupt change of elevation (level) of the passivation such as a contact window, or operating metallization crossover.

(28) Peripheral metal. All metal that lies immediately adjacent to or over the scribe grid.

(29) Shooting metal. Metal (e.g., aluminum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

(30) Substrate. The supporting structural material into or upon which or both the passivation, metallization and circuit elements are placed.

(31) Substrate via. A small hole formed through the wafer and metallized, causing electrical connection to be made from the frontside (the side on which the circuitry is formed) to the backside of the wafer.

(32) Thick film. That conductive/resistive/dielectric system that is a film having greater than 50,000Å thickness.

(33) Thin film. That conductive/resistive/dielectric system that is a film equal to or less than 50,000Å in thickness.

(34) Via metallization. That which connects the metallization of one level to another.

g. Interpretations. Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the acquiring activity. For inspections performed on the range of 75X to 100X, the criteria of 0.1 mil of passivation, separation or metal can be satisfied by a line of separation or a line of metal visible.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for (1) the presence of foreign material within incoming piece part lids and bases, and (2) the presence of foreign material on the die surface or within the package of assembled parts.

The audit of assembled parts may be satisfied during routine internal visual inspection. If the presence of foreign material is discovered, the manufacturer shall perform the necessary analysis on a sample of the foreign material on the suspect devices to determine the nature of the material. The manufacturer shall document the results of this investigation and corrective action to eliminate the foreign material and this information will be available to the Government QAR, and the acquiring activity or the qualifying activity, as applicable. A corrective action plan shall be obtained within a maximum of 10 working days of discovery.

The audit of incoming piece part lids and bases shall be performed before parts are assembled, or may be satisfied during routine incoming quality inspection. If the presence of foreign material of a size 1 mil or greater is discovered, the manufacturer will analyze the foreign material to determine its nature and document the results of the analysis. If applicable, these results shall be distributed to the vendor supplying the parts, with the request that the vendor document corrective actions to minimize or eliminate such foreign material. This information will be available to the manufacturer, Government QAR, and the acquiring activity or qualifying activity, as applicable.

NOTE: The piece part audit requirements can be replaced by a piece part cleaning process, approved by the qualifying activity, that is always performed either prior to or during the assembly process and these piece parts are stored in a controlled environment until they are used.

The intent of these procedures is to require investigation and resolution of foreign material problems that do not have an effective screening or detection methodology but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality Assurance to continue processing.

Condition A Class level S	Condition B Class level B

3.1 High power inspection. Internal visual examination as required in 3.1.1 through 3.1.3 shall be conducted on each microcircuit. In addition, the applicable criteria contained in 3.1.4 through 3.1.7 shall be used for the appropriate microcircuit area where glassivation, dielectric isolation or film resistors are used.

NOTE: Unless otherwise specified, for flip chip product the criteria of 3.1 shall apply only to top circuit side inspection. After die mounting, only criteria in 3.1.3i shall apply.

The high magnification inspection shall be within the range of 100X to 200X.	The high magnification inspection shall be within the range of 75X to 150X.

For high magnification inspection of GaAs microwave devices, see table I herein. Also, for < 1 micron features, the manufacturer may implement a sample inspection plan which shall be documented in the manufacturer's internal procedure and approved by the qualifying activity.

3.1.1 Metallization defects. No device shall be acceptable that exhibits the following defects in the operating metallization.

3.1.1.1 Metallization scratches:

a. Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-4).	a. Scratch in the metallization, excluding bonding pads and beam leads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2010-5).

NOTE: For GaAs microwave devices, scratches in the gate stripe or gate insertion metallization.

FIGURE 2010-4. Metallization scratch criteria for class level S.

* Condition A
Class level S

b. For condition A, see 3.1.1.1a above.

Condition B
Class level B

FIGURE 2010-5. Metallization scratch criteria for class level B.

b. For condition B only. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side (for MOS devices, the path shall be the (L) dimension) (see figure 2010-6).

NOTE: When standard metallization scratch criterion is applied to the gate area, the dimensions (W) and (L) shall be considered as the original channel width and length respectively.

FIGURE 2010-6. MOS scratch criteria.

Condition A Class level S	Condition B Class level B
c. Scratch in multilayered metallization, excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 percent of the original metal width undisturbed (see figure 2010-7).	c. Scratch in multilayered metallization, excluding bond pads and beam leads that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the original metal width undisturbed (see figure 2010-8).

FIGURE 2010-6. MOS scratch criteria - Continued.

FIGURE 2010-7. Scratch criteria for class level S.

Condition A
Class level S

Condition B
Class level B

FIGURE 2010-8 Scratch criteria for class level B.

NOTE: For condition B only. Criteria 3.1.1.1a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path.

d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria 3.1.1.1a, b, c, and d can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond, on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-9).

Condition A
Class level S

Condition B
Class level B

FIGURE 2010-9. Termination ends.

e. Scratch in the metallization, over the gate oxide (applicable to MOS structures only) (see figure 2010-10).

e. Scratch in the metallization, over the gate oxide, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (applicable to MOS structures only) (see figure 2010-11).

Condition A
Class level S

FIGURE 2010-10. MOS scratch criteria for class level S.

Condition B
Class level B

FIGURE 2010-11. MOS scratch criteria for class level B.

Condition A Class level S	Condition B Class level B
f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover. (Not applicable to air bridges.)	
g. Scratch in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.	g. Scratch in the bonding pad or fillet area that exposes underlying passivation or substrate and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

h. Scratch(es) (probe mark(s), etc.) in the bonding pad area that exposes underlying passivation or substrate and leaves less than 75 percent of the unglassivated metallization area undisturbed.

i. For GaAs devices only, any tears, peeling, gaps, and lateral displacement of metal.

3.1.1.2 Metallization voids;

a. Void(s) in the metallization that leaves less than 75 percent of the original metal width undisturbed (see figure 2010-12).	a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-13).

FIGURE 2010-12. Void criteria for class level S.

FIGURE 2010-13. Void criteria for class level B.

NOTE: For condition B only. Criteria can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path.

Condition A Class level S	Condition B Class level B

b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria of 3.1.1.2a and b can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-14).

FIGURE 2010-14. Termination ends.

c. Void(s) in the metallization over the gate oxide that leaves less than 75 percent of the metallization length (L) or width (W) between source and drain diffusions undisturbed (applicable to MOS structures only) (see figure 2010-15).

Condition A Class level S	Condition B Class level B
d. Void(s) that leave less than 75 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).	d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).

e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line undisturbed (applicable to MOS structures only) (see figure 2010-15).

FIGURE 2010-15. MOS void criteria.

f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed (see figure 2010-16).

g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. (see figure 2010-16).	g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately (see figure 2010-16).

FIGURE 2010-16. Bond pad terminology.

NOTE: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

h. Void(s) in the metallization area of a thin film capacitor that leave less than 75 percent of the designed metallization area.

i. For GaAs microwave devices only, voids in the gate stripe.

3.1.1.3 Metallization corrosion. Any metallization corrosion. Metallization having any localized discolored area shall be closely examined and rejected, unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

3.1.1.4 Metallization nonadherence. Any metallization lifting, peeling, or blistering.

3.1.1.5 Metallization probing. Criteria contained in 3.1.1.1 shall apply as limitations on probing damage.

* Condition A Class level S	Condition B Class level B

3.1.1.6 Metallization bridging.

NOTE: For SOS devices, exclude the insulator scribe lines.

a. Any metallization bridging where the separation between metallization paths is reduced to less than 50 percent of the original design.	a. Any metallization bridging where a line of separation is not visible between metallization paths. NOTE: For GaAs microwave devices, metallization bridging across spacings of less than 1 μm shall be inspected only in accordance with 3.2 and table I at 400X to 1,000X. If a clear line of separation is not discernible, device functional testing at the wafer level shall suffice.
b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad to less than 0.25 mils or 50 percent design separation, whichever is less.	b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad such that a line of separation is not visible.

3.1.1.7 Metallization alignment.

a. Contact window that has less than 75 percent of its area covered by metallization.	a. Contact window that has less than 50 percent of its area covered by metallization.
b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization.	b. Contact window that has less than 40 percent of its perimeter covered by metallization.

c. Contact window that has less than 75 percent of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures only).

NOTE: When, by design, metal is completely contained in a contact window or does not cover the entire contact perimeter, criteria 3.1.1.7a, b, or c can be deleted, provided the design criteria is satisfied.

d. A metallization path not intended to cover a contact window that is not separated from the contact window by a line of separation.

e. Any exposure of the gate oxide (i.e., oxide not covered by gate electrode in the area between source and drain diffusions, applicable to MOS structures only) (see figure 2010-17).

3.1.1.8 Via hole metallization. For GaAs devices only,

a. Overetched via hole or misaligned via visible around the pad.

b. Poor adhesion (lifting, peeling or blistering).

c. Any cracks originating at the via hole.

d. Evidence of bulging metal over a via hole.

e. Evidence of solder coming up through via hole pad, when die is mounted on a carrier.

Condition A Class level S	Condition B Class level B

3.1.1.9 Coupling (air) bridge defects "high magnification". For GaAs devices only. No element shall be acceptable that exhibits:

a. A void in the coupling (air) bridge metallization that leaves less than 75 percent of the original metallization width undisturbed. (see figure 2010-17A).

b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2010-17A)

c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2010-17A)

d. Attached, conductive foreign material that is greater, in any dimensions, than 50% of the original coupling (air) bridge metallization width.

e. No visible separation between the coupling (air) bridge and the underlying operating metallization.

NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2010-17A)

f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2010-17A)

g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.

NOTE: Air bridges which are depressed, over operating metallization, due to normal backside processing are not considered mechanically damaged. A visual line of separation still applies in accordance with 3.1.1.9e.

FIGURE 2010-17A. Class level S and Class level B coupling (air) bridge criteria.

FIGURE 2010-17. MOS gate alignment.

f. For MOS structures containing a diffused guard ring, gate metallization not coincident with or not extending over the diffused guard ring (see figure 2010-18).

FIGURE 2010-18. MOS gate alignment.

Condition A Class level S	Condition B Class level B

3.1.2 Diffusion and passivation layer faults. No devices shall be acceptable that exhibits the following:

3.1.2.1 Diffusion faults.

a. Diffusion fault that allows bridging between diffused areas (see figure 2010-19).

FIGURE 2010-19. Diffusion faults.

b. Any isolation diffusion that is discontinuous (except isolation walls around unused areas or unused bonding pads) or any other diffused area with less than 25 percent (50 percent for resistors) of the original diffusion width remaining (see figure 2010-20).

FIGURE 2010-20. Diffusion faults.

Condition A Class level S	Condition B Class level B

3.1.2.2 Passivation faults.

NOTE: For SOS devices, exclude defects between first-level conductive interconnect (metallization, polysilicon, ect.) and sapphire areas of the die, where no active circuit elements are present.

a. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization unless by design for GaAs devices. Multiple lines indicate that the fault can have sufficient depth to penetrate down to bare semiconductor material.

NOTE: The multiple line criteria can be excluded when a second passivation layer is applied in a separate operation prior to metallization deposition or for bond pads located in isolated tubs.

NOTE: For condition B only. Should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons respectively, then these techniques may be used (see figure 2010-21).

FIGURE 2010-21. Passivation faults.

b. Active junction line not covered by passivation, unless by design.

c. Contact window that extends across a junction line, unless by design.

Condition A Class level S	Condition B Class level B

3.1.3 Scribing and die defects. No device shall be acceptable that exhibits:

a. Less than 0.25 mil of passivation visible between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22).	a. No line of separation between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22).

NOTE: For GaAs devices only, less than 0.1 mil of substrate visible between operating metallization or bond periphery and edge of the die.

NOTE: Criteria can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the substrate.

NOTE: Does not apply to SOS devices.

b. A chipout or crack in the active circuit area (see figures 2010-22 and 2010-38). In addition for GaAs a chipout into or underneath the functional metallization, e.g., bond pads, capacitors, peripheral metallization, etc., but excluding test structures of the device.

NOTE: Criteria can be excluded for peripheral metallization that is at the same potential as the substrate. At least 50 percent undisturbed metallization width shall remain at the chipout.

c. A crack that exceeds 3.0 mils in length, or comes closer than 0.25 mils to any operating metallization (except for substrate potential peripheral metal) or functional circuit element (see figure 2010-22).	c. A crack that exceed 5.0 mils in length, or that does not exhibit a line of separation to any operating metallization (except for substrate potential peripheral metal) or function circuit element (see figure 2010-22).
d. For condition A only. Semicircular crack(s) terminating at the die edge, whose chord is long enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.) (see figure 2010-22).	d. No condition B.

e. Exposed semiconductor material extending over the passivation edge at the point of the beam lead exit from the die (applicable to beam lead structures only) (see figure 2010-38).

f. Die having attached portions of the active circuit area of another die.

g. A crack that exceeds 1.0 mil in length inside the scribe line (or semiconductor material edge for beam lead devices) that points toward operating metallization or functional circuit elements (see figure 2010-22).

h. A crack that comes closer than 0.5 mil to operating beam lead metallization (see figure 2010-38).

NOTE: Criteria of 3.1.3c and h can be excluded for beam lead devices where the chipout or crack does not extend into the semiconductor material.

NOTE: Criteria of 3.1.3e and h do not apply to GaAs devices.

FIGURE 2010-22 Scribing and die defects.

Condition A Class level S	Condition B Class level B

i. For flip chip, cracks, or chipouts in the substrate material that extends beyond 50 percent of substrate thickness or a crack greater than 5.0 mils in length in the substrate material (see figure 2010-23).

FIGURE 2010-23. Scribing and die defects.

j. Any blistering, peeling, delamination, corrosion, or other gross defects in glassivation, metal, interlevel dielectrics or other layers.

Condition A Class level S	Condition B Class level B

3.1.4 Glassivation defects. No device shall be acceptable that exhibits (see figure 2010-24):

NOTE: For condition B only. Criteria of 3.1.4 can be excluded when the defect(s) is due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation defects, equal to or greater than one half times the narrowest resistor width.

FIGURE 2010-24. Laser trimmed glassivation defects.

a. Glass crazing or glass damage that prohibits the detection of visual criteria contained herein.

b. Any lifting or peeling of the glassivation in the active areas or which extends more than 1.0 mil distance from the designed periphery of the glassivation.

c. A glassivation void that exposes two or more active metallization paths, except by design.

d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.

e. Unglassivated areas at the edge of bonding pad exposing bare semiconductor material, except by design.

f. Glassivation covering more than 25 percent of the designed open contact bonding area.

g. Crazing over a film resistor.

Condition A Class level S	Condition B Class level B

h. Scratch(es) in the glassivation that disturbs metal and bridges metallization paths.

i. Crack(s) (not crazing) in the glassivation that forms a closed loop over adjacent metallization paths.

j. Glassivation void(s) that exposes any portion of a thin film resistor or fusible link except where the glassivation is opened by design.

k. For GaAs devices, voids in the glassivation that extends over the gate channel of the FET.

l. For GaAs devices, scratches in the glassivation over the gate channel of the FET.

m. For GaAs devices, scratches in the glassivation over the gate insertion of the FET.

n. For GaAs devices, cracks in the glassivation which are more than 1.0 mil inside the scribe line, or are more than 50 percent of the distance between the scribe line and any functional or active element (e.g., capacitor, resistor, FET) and which point toward any functional or active element unless the crack terminates at a device feature (e.g., transmission line or dc line).

3.1.5 Dielectric isolation. No device shall be acceptable that exhibits:

a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see figure 2010-25).

b. Absence of a continuous isolation line between any adjacent tubs, containing functional circuit elements (see figure 2010-25).

FIGURE 2010-25. Dielectric isolation defects.

Condition A Class level S	Condition B Class level B

c. A diffused area which overlaps dielectric isolation material and does not exhibit a line of separation to an adjacent tub, or an overlap of more than one diffusion area into the dielectric isolation material (see figure 2010-25).

FIGURE 2010-26. Dielectric isolation defects.

d. A contact window that touches or overlaps dielectric material, except by design.

NOTE: Metallization scratch and void defects over a dielectric isolation step shall be rejected in accordance with criteria contained in 3.1.1.1d and 3.1.1.2b.

3.1.6 Film resistor. Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.1.1 shall apply as applicable. No device shall be acceptable that exhibits:

Condition A Class level S	Condition B Class level B

a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width.

FIGURE 2010-27. Film resistor contact area.

b. No visible line of contact overlap between the metallization and film resistor (see figure 2010-28).

FIGURE 2010-28. Film resistor contact area.

Condition A Class level S	Condition B Class level B

c. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal.

d. Inactive resistor inadvertently connected to two separate points on an active circuit.

e. Separation between any two resistors or a resistor and a metallization path that is less than 0.25 mil, or 50 percent of the design separation, whichever is less.

f. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.) (see figure 2010-26).

NOTE: This criteria does not apply to square isolated islands of single crystal silicon in the polysilicon area.

g. Any resistor width reduced to less than one half the narrowest resistor width, resulting from voids or scratches or a combination thereof (see figure 2010-29).

NOTE: Maximum allowable current density requirements shall not be exceeded.

FIGURE 2010-29. Scratch and void criteria for untrimmed resistors.

h. Any sharp change in color of resistor material within 0.1 mil of the resistor/connector termination.

3.1.7 Laser-trimmed thin-film resistors. Rejection shall be based on defects found within the actively used portions of the film resistor. No device shall be acceptable that exhibits:

a. A kerf less than 0.1 mil in width, unless by design.

NOTE: Criteria does not apply for edge trimming.

b. A kerf containing particles of detritus.

Condition A Class level S	Condition B Class level B

c. A kerf containing untrimmed resistor material, unless that material is continuous across the kerf, and is undisturbed for a width greater than one-half times the narrowest resistor width, unless by design (see figure 2010-30).

NOTE: Maximum allowable current density requirements shall not be exceeded.

Top hat trim

FIGURE 2010-30. Untrimmed resistor material criteria.

Condition A
Class level S

Condition B
Class level B

Rectangular L trim

FIGURE 2010-30. Untrimmed resistor material criteria - Continued.

d. Resistor width that has been reduced by trimming to less than one-half the narrowest resistor width, including voids, scratches, or a combination thereof, in the trim area (see figure 2010-31).

NOTE: Trimming of more than 50 percent of a given resistor shunt link is acceptable by design providing that the last shunt link of the resistor adder network is not trimmed greater than 50 percent. All trimmable resistor shunt links shall be defined on the design layout drawing.

FIGURE 2010-31. Scratch and void criteria for trimmed resistors.

*	Condition A Class level S	Condition B Class level B

e. Trim path into the metallization except block resistors.

NOTE: This criteria can be excluded for trim paths into terminator ends of metallization runs. Conductors or resistors may be trimmed open for link trims or by design.

f. Trim for block resistors which extends into the metallization (excluding bonding pads) more than 25 percent of the original metal width (see figure 2010-32).

TRIM INTO METAL

FIGURE 2010-32. Block resistor criteria.

g. Pits into the silicon dioxide in the kerf which do not exhibit a line of separation between the pit and the resistor material.

	Condition A Class level S	Condition B Class level B

3.2 Low power inspection. Internal visual examination as required in 3.2.1 through 3.2.3 shall be conducted on each microcircuit at low magnification range of 30X to 60X. In addition, the applicable criteria contained in 3.2.4 shall be applicable where beam lead assembly technology is used and 3.2.5 shall be inspected at both high and low power as indicated, high power magnification shall be same as 3.1, subject to conditions in 3b.

3.2.1 Lower power wire bond inspection. This inspection and criteria shall be required inspection for the bond type (s) and location(s) to which they are applicable when viewed from above (see figure 2010-33).

NOTE: The criteria applicable for bonds (called "wedgebonds" or "bonds") in this test method refers to the fully or partially deformed area including the tool impression shown as "L and W" in figure. The criteria applicable for "bond tails" (or "tails") in this test method refers to resulting length of bonding wire extending beyond the bond shown as "T" in figure 2010-33. Tail is not part of bond.

FIGURE 2010-33. Bond dimensions.

Condition A Class level S	Condition B Class level B

3.2.1.1 Gold ball bonds. No devices shall be acceptable that exhibits:

a. Gold ball bonds on the die or package post wherein the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the wire center exit is not within the boundaries of the unglassivated bonding pad area.

3.2.1.2 Wedge bonds. No device shall be acceptable that exhibits:

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or more than 3.0 times the wire diameter in width, or less than 1.5 times or more than 6.0 times the wire diameter in length.

b. Thermosonic wedge bonds on the die or package post that are less than 1.5 times or more than 3.0 times the wire diameter in width or are less than 1.5 times or more than 6.0 times the wire diameter in length.

c. Bond width less than 1.0 times the wire diameter for aluminum wires 2.0 mils or greater in diameter.

d. Wedge bonds where the tool impression does not cover the entire width of the wire.

3.2.1.3 Tailless bonds (crescent, terminating capillary bond). No device shall be acceptable that exhibits:

a. Tailless bonds on the die or package post that are less than 1.2 times or more than 5.0 times the wire diameter in width, or are less than 0.5 times or more than 3.0 times the wire diameter in length.

b. Tailless bonds where tool impression does not cover the entire width of the wire.

Condition A Class level S	Condition B Class level B

3.2.1.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable the exhibits (see figure 2010-16):

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area.	a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.

b. Bond tails that do not exhibit a line of separation between the tail and unglassivated metallization, another wire, wire bond, or wire bond tail, excluding common conductors and pads.

c. Bond tails extending over glassivated metallization where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.

d. Wire bond tails: Tails that exceed 2 wire diameters in length on die or on post.

e. Bonds that are not completely within the boundaries of the package post. For glass sealed packages, bonds not within 20 mils of the end of post.

f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond is less than .25 mils.	f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond does not exhibit a visible line of separation.

NOTE: When by design, there are multiple bonds on a common bonding pad or post they may not reduce the width of an adjacent bond by more than 25 percent.

NOTE: For SOS devices, exclude the insulator scribe lines.

g. Bonds (excluding tails) placed such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed to an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe (see figure 2010-34).

NOTE 1: When bond tails prevent visibility of the connecting path and the metallization immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.

NOTE 2: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

NOTE 3: This criteria is in addition to the bond placement criteria in 3.2.1.4a.

Condition A
Class level S

Condition B
Class level B

Reject: Bond (excluding tails) placed, such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.

Reject: When bond tails prevent visibility of the connecting path to the bond periphery and the metallization immediately adjacent to the bond tail is disturbed.

Accept: Bonds (excluding tails) placed, such that there is 2.0 mils or greater of bond periphery (on glassivated or unglassivated areas) exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.

Arrows demonstrate the connecting path to the bond periphery.

FIGURE 2010-34. Bonds at entering/exiting metallization stripe.

Condition A Class level S	Condition B Class level B

h. Bonds where more than 25 percent of the bond is located on die mounting material.

i. Any evidence of repair of conductors by bridging with additional material.

j. Bonds on foreign material.

k. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of that portion of the gold bond located on metal.

3.2.1.5 Rebonding of monolithic devices. Rebonding of monolithic microcircuits, may be done with the following limitations. No device shall be acceptable that exhibits:

a. Rebond over exposed passivation or over metal which shows evidence of peeling. More than one rebond attempt at any design bond location. Rebonds that touch an area of exposed oxide caused by lifted metal.

b. A bond on top of, or partially on top of, another bond, bond wire tail, or residual segment of wire.

b. Bond along side or partially on top of another bond, bond wire tail or residual segment of wire, when the overlap width is greater than 25 percent.

c. Rebond attempts that exceed 10 percent of the total number of bonds in the microcircuit. (e.g., for a 28 lead wire bonded package there are 56 bonds. A bond of one end of a wire shall count as a single attempt. A replacement of a wire bonded at both ends, counts as two rebond attempts.)

NOTE: For class level B only. Bond-offs required to clear the bonder after an unsuccessful first bond attempt are not considered as rebonds provided they can be identified as bond-offs.

d. Missing or extra wires.

Condition A Class level S	Condition B Class level B

3.2.2 Internal wires. When the requirements of 3.2.2 are not easily determined vertically, the device may be tilted about the x and y axis to allow an alternate view of the wires such that the vertical separation can be verified. No device shall be acceptable that exhibits:

a. Any wire with a separation of less than two wire diameters to unglassivated operating metal,other bonds, another wire (common wiresexcluded),other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package including the plane of the lid to be attached.	a. Any wire with a separation of less than one wire diameter to unglassivated operating metal, other bonds, another wire (common wires excluded), other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any conductive portion of the package or the plane of the lid to be attached.
NOTE: For condition A only. Within a 5.0 mil radial distance from the perimeter of the bond on the die the separation shall be 1.0 mil minimum.	NOTE: For condition B only. Within a 10.0 mil radial distance from the perimeter of the bond on the die a line of separation must be visible.

NOTE: For SOS devices, exclude the unglassivated insulator areas.

b. Nicks, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

c. Tearing at the junction of the wire and bond.

d. Any wire making a straight line run from a die bonding pad to a package post that has no arc.

Condition A Class level S	Condition B Class level B
e. Wire(s) crossing wire(s) when viewed from above, (excluding common conductors) except in multitiered packages, where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed or packages with down bond(s). In these situations, the wires that cross are acceptable if they maintain a minimum clearance of two wire diameters (see figure 2010-35). NOTE: No bond wire shall cross more than one other bond wire and there shall be no more than 4 crossovers or crossovers involving more than 10 percent of the total number of wires, whichever is greater for any single package cavity.	e. Wire(s) crossing wire(s) when viewed from above, (excluding common conductors) except that wires crossing wires bonded to package posts that are at difference heights, or wires bonded into the package cavity that cross are acceptable if they maintain a minimum clearance of two wire diameters (e.g., multitiered packages or packages with down bond chips).
f. Wire(s) not in accordance with bonding diagram.	

3.2.3 Die mounting.

3.2.3.1 Die mounting eutectic. No device shall be acceptable that exhibits:

a. Die mounting material buildup that extends onto the top surface or extends vertically above the top surface of the die.

b. Die mounting material (eutectic wetting) not visible around at least two complete sides or 75 percent of the die perimeter, except for transparent die.

c. Transparent die with less than 50 percent of the area bonded.

d. Flaking of the die mounting material.

e. Balling or buildup of the die mounting material that does not exhibit a minimum of 50 percent peripheral fillet when viewed from above or the accumulation of die mounting material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point (see figure 2010-36).

FIGURE 2010-35. Class level S criteria for wire(s) crossing wire(s).

DETAIL A
FRONT VIEW,ACCEPT

REJECT: NO FILLET VISIBLE

ACCEPT: FILLET VISIBLE

ACCEPT: FILLET 50 PERCENT OR GREATER

DETAIL A
TOP VIEW

FIGURE 2010-36. Balling of die attach material.

Condition A Class level S	Condition B Class level B

3.2.3.2 Die mounting noneutectic. No device shall be acceptable that exhibits:

a. Adhesive material immediately adjacent to the die that extends onto or vertically above the top surface of the die.

b. Adhesive fillet not visible along 75 percent of each side of the die.

c. Any flaking, peeling, or lifting of the adhesive material.

d. Separation, cracks, or fissures greater than or equal to 2 mils in width in the adhesive at the cavity wall or cavity floor.

e. Crazing in the adhesive.

f. Adhesive material on the top surface of the die.

g. Adhesive that bridges package posts or is on the post bond area.

h. Any adhesive material that is connected to the fillet or conductive cavity (e.g. metal package base or metallized floor of ceramic package), and extends up the cavity wall to within 1.0 mil of the package post.

i. Transparent die with less than 50 percent of the area bonded.

3.2.3.3 Die orientation. No device shall be acceptable that exhibits:

a. Die not located or oriented in accordance with the applicable assembly drawing.

b. Die that appears to be obviously tilted (i.e., more than 10 degrees) with respect to the package cavity.

3.2.4 Beam lead construction.

3.2.4.1 Bonds. This inspection criteria shall apply to the completed bond area made, using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.

b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.

c. Bonds where the tool impression length is less than 1.0 mil (see figure 2010-37).

d. Bonding tool impression less than 1.0 mil from the die edge (see figure 2010-37).

Condition A Class level S	Condition B Class level B

e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2010-37).

FIGURE 2010-37. Beam lead bond area and location.

Condition A Class level S	Condition B Class level B

f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.

g. Bonds placed so that the separation between bonds and between bonds and operating metallization not connected to them is less than 0.1 mil.

h. Bonds lifting or peeling.

3.2.4.2 Beam leads. No device shall be acceptable that exhibits the following:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.

b. Beam separation from the die.

c. Missing or partially fabricated beam leads unless by design.

d. Beam leads that are not bonded.

e. Bonded area closer than 0.1 mil to the edge of the passivation layer.

f. Less than 0.1 mil passivation layer between the die and the beam visible at both edges of the beam (see figure 2010-37 and 2010-38).

FIGURE 2010-38. Beam lead die faults.

Condition A Class level S	Condition B Class level B

3.2.5 Foreign material. Die inspections shall be at high magnification. Package and lid inspections shall be at low magnification. Die criteria may be examined at high magnification prior to die mounting provided they are re-examined at low magnification during preseal inspection. No device shall be acceptable that exhibits:

NOTE: Foreign material may be removed, if possible, by subjecting the device to a nominal gas blow (less than 25 psig). After this gas blow off at inspection, all wire bonded devices shall be inspected/reinspected for possible wire damage. Use of a higher psig value is permitted provided that the manufacturer has characterized the process and has data to assure that no damage is done to the wire bonds. This data shall be available upon request to the preparing or acquiring activities.

a. Foreign particle(s) on the surface of the die that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).

b. Foreign particle(s) other than on the surface of the die within the package or on the lid or cap that is (are) large enough to bridge the narrowest spacing between unglassivated operating materials and are not the following: Semiconductor material, glass splatter, gold imperfections in the die attach area, gold eutectic material or package ceramic material.

NOTE: As an alternative to 100 percent visual inspection of lids or caps, the lids or caps may be subjected to a suitable cleaning process and quality verification, approved by the qualifying activity. The lids or caps shall subsequently be held in a controlled environment until capping or preparation for seal.

c. Foreign material attached to or embedded in the die surface that appears to bridge the active circuit elements including metallization unless verified as only attached but not embedded by high power dark field illumination.

d. Liquid droplets, chemical stains, ink, or photoresist on the die surface that appear to bridge any combination of unglassivated metallization or bare semiconductor material areas.

e. A particle of gold eutectic material, package ceramic material or semiconductor material, not attached to the die, large enough to bridge the narrowest spacing between unglassivated operating materials, that does not exhibit a minimum of 50 percent cumulative peripheral fillet or whose height is greater than the longest base dimension.

NOTE 1: This criteria shall not be cause for rejection when the assembly process contains a gas blow (less than 60 psig) after die attach and again Less than 25 psig) after wire bond provided rejectable materials (not attached and large enough to bridge) have been removed from the cavity.

NOTE 2: Gold imperfections in the die attach area that do not interfere with proper die attachment, sealing glass splatter (provided it does not suggest inadequately controlled process and does not interfere with the die attach area) or internal glass run out from frit seal (provided it is confined to package walls and does not interfere with the die attach area) are not rejectable.

Condition A Class level S	Condition B Class level B

3.2.5.1 Foreign material, die coated devices. This inspection and criteria shall be required on all devices that receive a die coat during the assembly process. This inspection will be done after die coat cure. No device shall be acceptable that exhibits:

a. Unattached foreign particles on the surface of the die coat or within the package that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.). Note: Semiconductor particles shall be considered as foreign material.

b. Partially embedded foreign material with an "unembedded portion" that is large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).

c. Foreign material attached to or embedded in the die coat that appears to bridge unglassivated operating material when viewed from above (e.g., bare semiconductor material, bond pads, bonding wire, mounting material, etc.).

3.2.6 GaAs backside metallization. GaAs inspection shall be performed with low magnification prior to die mounting. (Verification at high magnification is permitted.) With the approval of the acquiring activity, the manufacturer may substitute a sample inspection plan at the wafer level for 100 percent inspection in dice form. The sample inspection plan shall be documented in the manufacturer's baseline documentation and shall be performed to the requirements of test method 5013. No devices shall be acceptable that exhibit the following.

a. Evidence of metal corrosion, lifting, peeling, blistering.

b. Voids or scratches that expose underlying metal or substrate whose cumulative areas are more than 25 percent of the cell area or device area.

NOTE: Absence of gold in the die separation area (saw street) of devices with electroplated backside metallization is not a cause for rejection. Small voids at edges due to die separation are acceptable if they comprise less than 10 percent of the backside area.

c. Any voids or scratches in the substrate via metallization that effects more than 25 percent of the metallization or cause unintended isolation of the metallization path.

d. Underetched vias.

e. Overetched vias.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Test condition (see 3).

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison (see 2).

d. Where applicable, specific magnification (see 3).

METHOD 2011.7

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. PURPOSE. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, *and added sample provisions shall be observed, as applicable.* Unless otherwise specified, for conditions A, C, and D, the sample size number specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H, while involving two or more bonds shall count as a single pull for bond strength and sample size number purposes. Unless otherwise specified, for conditions F, G, and H the sample size number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices (all conditions), a minimum of 4 die or use all die if four are not available on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions:

3.1.1 Test condition A - Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition C - Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.3 Test condition D - Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction approximately normal to the die or substrate surface or approximately normal to a straight line between the bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded. The minimum bond strength shall be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I. For wire diameter or equivalent cross section >0.005 inch, where a hook will not fit under the wire, a suitable clamp can be used in lieu of a hook.

3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.5 Test condition G - Push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.6 Test condition H - Pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

a. For internal wire bonds:

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

b. *For external bonds connecting device to wiring board or substrate:*

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$$V_1 = V_2 \sin \Theta$$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
Θ = Greatest calculated wire loop angle (figure 2011-2).

Also, RF/microwave hybrids that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, and schedule. The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2011-3).

TABLE I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	—	—	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-clip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2011-1 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

c. Sample size number and accept number or number and selection of bond pulls to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90°, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

NOTE: The minimum bond strength should be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I.

FIGURE 2011-1. Minimum bond pull limits.

FIGURE 2011-2. Wire loop angle.

FIGURE 2011-3. Flat loop wire pull testing.

METHOD 2012.7

RADIOGRAPHY

1. Purpose. The purpose of this examination is to nondestructively detect defects within the sealed case, especially those resulting from the sealing process and internal defects such as foreign objects, improper interconnecting wires, and voids in the die attach material or in the glass when glass seals are used. It establishes methods, criteria, and standards for radiographic examination of semiconductor and hybrid devices.

NOTE: For certain device types, opacity of the construction materials (packages or internal attachment) may effectively prevent radiographic identification of certain types of defects from some or all possible viewing angles. This factor should be considered in relation to the design of each device when application of this test method is specified.

2. Apparatus. The apparatus and material for this test shall include:

a. Radiographic equipment with a sufficient voltage range to penetrate the device. The focal distance shall be adequate to maintain a sharply defined image of an object with a major dimension of 0.0254 mm (0.001 inch).

b. Radiographic film: Very fine grain industrial X-ray film grade, either single or double emulsion.

c. Radiographic viewer: Capable of 0.0254 mm (0.001 inch) resolution in major dimension.

d. Holding fixtures: Capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

e. Radiographic quality standards: Capable of verifying the ability to detect all specified defects.

f. Film holder: A 1.6 mm (0.0625 inch) minimum lead-topped table or lead-backed film holders to prevent back scatter of radiation.

3. Procedure. The X-ray exposure factors, voltage, milliampere and time settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details within the sensitivity requirements for the device or defect features the radiographic test is directed toward. The X-ray voltage shall be the lowest consistent with these requirements and shall not exceed 200 kV.

3.1 Mounting and views. The devices shall be mounted in the holding fixture so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture and masking with lead diaphragms or barium clay may be employed to isolate multiple specimens provided the fixtures or masking material do not block the view from X-ray source to the film of any portion of the body of the device.

3.1.1 Views.

3.1.1.1 Flat packages, dual-in-line packages, hybrid packages, and single ended cylindrical devices. Flat packages, dual-in-line packages, hybrid packages, and single ended cylindrical devices, unless otherwise specified, shall have one view taken with the X-rays penetrating in the Y direction as defined on figures 1 and 2 of MIL-STD-883, GENERAL REQUIREMENTS. When more than one view is required, the second and third views, as applicable, shall be taken with the X-rays penetrating in the Z and X direction respectively (either Z or X for flat packages). The die/cavity interface shall be positioned as close as possible to the film to avoid distortion.

3.1.1.2 Stud-mounted and cylindrical axial lead devices. Stud-mounted and cylindrical axial lead devices, unless otherwise specified, shall have one view taken with the X-rays penetrating in the X direction as defined on figures 1 and 2 of MIL-STD-883, GENERAL REQUIREMENTS. When more than one view is required, the second and third views, as applicable, shall be taken with the X-rays penetrating in the Z direction and at 45° between the X and Z direction. The die/cavity interface shall be positioned as close as possible to the film to avoid distortion.

3.2 Radiographic quality standard. Each radiograph shall have at least two quality standards exposed with each view, located (and properly identified) in opposite corners of the film. These penetrameters shall be of a radiographic density nearest the density of the devices being inspected. The radiographic quality standard shall consist of a suitable ASTM penetrameter as described in the DOD adopted standard ASTM E 801 Standard Practice for Controlling Quality of Radiographic Testing of Electronic Devices, or equivalent.

3.3 Film and marking. The radiographic film shall be in a film holder backed with a minimum of 1/16 inch lead or the holder shall be placed on the lead topped table. The film shall be identified using techniques that print the following information, photographically, on the radiograph:

a. Device manufacturer's name or code identification number.

b. Device type or Part or Identifying Number.

c. Production lot number or date code or inspection lot number.

d. Radiographic film view number and date.

e. Device serial or cross reference numbers, when applicable.

f. X-ray laboratory identification, if other than device manufacturer.

3.3.1 Nonfilm techniques, when specified. The use of nonfilm techniques is permitted if permanent records are not required and the equipment is capable of producing results of equal quality when compared with film techniques, and all requirements of this method are complied with, except those pertaining to the actual film.

3.3.2 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. They shall be radiographed in consecutive, increasing serial order. When a device is missing, the blank space shall contain either the serial number or other X-ray opaque object to readily identify and correlate X-ray data. When large skips occur within serialized devices, the serial number of the last device before the skip and the first device after the skip may be used in place of the multiple opaque objects.

3.3.3 Special device marking. When specified (see 4.c), the devices that have been X-rayed and found acceptable shall be identified with a blue dot on the external case. The blue dot shall be approximately 1.6 mm (0.0625 inch) in diameter. The color selected from FED-STD-595 shall be any shade between 15102-15123 or 25102-25109. The dot shall be placed so that it is readily visible but shall not obliterate other device marking.

3.4 Tests. The X-ray exposure factor shall be selected to achieve resolution of 0.0254 mm (0.001 inch) major dimension, less than 10 percent distortion and an "H" and "D" film density between 1 and 2.5 in the area of interest of the device image. Radiographs shall be made for each view required (see 4).

3.5 Processing. The radiographic film manufacturer's recommended procedure shall be used to develop the exposed film, and film shall be processed so that it is free of processing defects such as fingerprints, scratches, fogging, chemical spots, blemishes, etc.

3.6 Operating personnel. Personnel who will perform radiographic inspection shall have training in radiographic procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. The following minimum vision requirements shall apply for personnel inspecting film:

a. Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.

b. Near vision shall be such that the operator can read Jaeger type No. 2 at a distance of 16 inches, corrected or uncorrected.

c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year. Personnel authorized to conduct radiographic tests shall be required to pass the vision test specified in 3.6 a and b.

3.7 Personnel safety precautions. The safety precautions described in National Institute of Standards and Technology (NIST) Handbook 76 - X-ray Protection; NIST Handbook 73 - Protection Against Radiations From Sealed Gamma Sources; Nuclear Regulatory Commission Book Title 10, Part 20 - Standard for Protection Against Radiation, Part 30 - Licensing of By-Product Material, Part 31 - Radiation Safety Requirements for Radiographic Operations, shall be complied with when applicable.

3.8 Interpretation of radiographs. Utilizing the equipment specified herein, radiographs shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected. Interpretation of the radiograph shall be made under low light level conditions without glare on the radiographic viewing surface. The radiographs shall be examined on a suitable illuminator with variable intensity or on a viewer suitable for radiographic inspection on projection type viewing equipment. The radiograph shall be viewed at a magnification between 6X and 25X. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the features in the radiographic quality standards is not acceptable and another radiograph of the devices shall be taken.

3.9 Reports of records.

3.9.1 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the radiographic inspection, and list the purchase order number or equivalent identification, the PIN, the date code, the quantity inspected, the quantity rejected, and the date of test and which devices utilize the note in 3.10.2.1. For each rejected device, the PIN, the serial number, when applicable, and the cause for rejection shall be listed.

3.9.2 Radiograph submission. Photographic reproduction of complete radiographs may be submitted, but artistic renditions are not acceptable.

3.9.3 Radiograph and report retention. When specified, the manufacturer shall retain a set of the radiographs and a copy of the inspection report. These shall be retained for the period specified.

3.10 Examination and acceptance criteria for monolithic devices.

3.10.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.10.2 Individual device defects. The individual device examination shall include, but not be limited to, inspection for foreign particles, solder or weld "splash", build-up of bonding material, proper shape and placement of lead wires or whiskers, bond of lead or whisker to semiconductor element and lead or whisker to terminal post, semiconductor metallization pattern, and mounting of semiconductor element. Any device for which the radiograph reveals any of the following defects shall be rejected:

3.10.2.1 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, loose or attached, greater than 0.025 mm (0.001 inch) (see figure 2012-1), or of any lesser size which is sufficient to bridge nonconnected conducting elements of the semiconductor device.

b. Any wire tail extending beyond its normal end by more than two wire diameters at the semiconductor die pad or by more than four wire diameters at the semiconductor package post (see figure 2012-1).

c. Any burr on a post (header lead) greater than 0.08 mm (0.003 inch) in its major dimension or of such configuration that it may break away.

d. Excessive semiconductor element bonding material build-up.

(1) A semiconductor element shall be mounted and bonded so that it is not tilted more than 10° from the normal mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor element whether or not it touches the side of the semiconductor element shall not accumulate to a thickness greater than the height of the semiconductor element (see figures 2012-2 and 2012-3), or any lead or post, or be separated from the main bonding material area (see 2012-7).

(2) There shall be no visible extraneous material 0.025 mm (0.001 inch) or larger in the major dimension inside the semiconductor device. Loose bonding material will be considered extraneous material. Excessive (but not loose) bonding material will not be considered extraneous unless it fails to meet the requirements of 3.10.2.1.d.(1) or unless the accumulation of bonding material is such that the height of the accumulation is greater than the width of its base or that the accumulation necks down at any point (see figures 2012-2 and 2012-3).

NOTE: Devices with suspect foreign particles or extraneous material (in accordance with 3.10.2.1a and 3.10.2.1.d(2) may be verified as acceptable provided the following conditions are met:

(a) A visual inspection of the die attach area at 30X to 60X shall have been conducted prior to die attach sufficient to assure there are no anomalies in the die attach area which could interfere with effective die attach.

(b) The precap inspection shall have been conducted 100 percent to condition A of method 2010 of MIL-STD-883 and the devices shall have been inspected and prepared for sealing in a class 100 environment.

(c) All devices with X-ray defects to other criteria of 3.10 shall have been removed from the lot.

(d) Serialized devices with less than 5 suspect foreign particles and extraneous material shall be vibrated and shocked in accordance with PIND method 2020, condition A with the detector off.

(e) A second X-ray examination of the failed view of the serialized devices after the PIND vibration/shock shall be conducted and each individual device shall be compared to its previous X-ray record.

(f) Any evidence of the suspect particle(s) having moved or having disappeared from their original location shall cause the device to be rejected. If the particle(s) exhibit no evidence of movement, the device may be accepted.

(g) The manufacturer doing the reinspection for suspect foreign particles or extraneous material shall implement a process monitor visual inspection of the cavity of the reinspected devices to assure that accepted devices do not have actual rejectable foreign particles or extraneous material (see 3.2.3.1a, 3.2.3.1d, and 3.2.3.1e, 3.2.3.2a, 3.2.3.2c, 3.2.3.2f, 3.2.3.2g, 3.2.3.2h, and 3.2.5 of method 2010). If any reinspected device fails the process monitor visual inspection, then all reinspected devices in the lot that have been inspected are subject to disposition. Corrective action, when appropriate, must be instituted. A procedure is required for the traceability, recovery, and disposition of all reinspected units accepted since the last successful monitor. The records for this monitor shall include identification of all lots which are reinspected to this note, identification of those lots which are monitored by this visual inspection, sample size, frequency of sampling, results of the visual inspections, and the package types reinspected.

In the case of a failed monitor, the records must identify all lots affected, their final disposition and a rationale for their disposition. Additionally, for a failed monitor, the records must also contain a description of any instituted corrective action together with its rationale. Records of this type shall be made available to the qualifying activity upon request.

e. Gold flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

3.10.2.2 Unacceptable construction. In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit any of the following defects shall be rejected.

a. Voids: When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see figure 2012-1).

(1) Contact area voids in excess of one-half of the total contact area.

(2) A single void which traverses either the length or width of the semiconductor element and exceeds 10 percent of the total intended contact area.

b. Wires present, other than those connecting specific areas of the semiconductor element to the external leads. Device designs calling for the use of such wires including jumper wires necessary to trim load resistors are acceptable (see figure 2012-1).

c. Cracks, splits, or chips of the electrical elements.

d. Excessive undercutting of the electrical elements (X and Z plane only, see figure 2012-4).

e. Defective seal: Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75 percent. Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is continuous, uniform and attached to the parent material and does not exhibit a ball, splash or tear-drop configuration (i.e., where the base support least dimension is smaller than the dimension it is supposed to support).

f. Inadequate clearance: Acceptable devices shall have adequate internal clearance to assure that the elements cannot contact one another or the case. No crossover shall be allowed except as permitted by 3.2.2e of method 2010 (condition A). Depending upon the case type, devices shall be rejected for the following conditions:

NOTE: Any of the following criteria for bond wires shall not apply, if the wires are not visible In the X-ray.

(1) Flat pack and dual-in-line (see figure 2012-5).

(a) Any lead wire that appears to touch or cross another lead wire or bond, (Y plane only).

(b) Any lead wire that deviates from a straight line from bond to external lead and appears to be within 0.05 mm (.002 inch) of another bond or lead wire (Y plane only).

(c) Lead wires that do not deviate from a straight line from bond to external lead and appear to touch another wire or bond, excluding common wires, (Y plane only).

(d) Any lead wire that touches or comes within 0.05 mm (0.002 inch) of the case or external lead to which it is not attached (X and Y plane).

(e) Any bond that is less than 0.025 mm (0.001 inch) (excluding bonds connected by a common conductor) from another bond (Y plane only).

(f) Any wire making a straight line run from die bonding pad to package post that has no arc.

(g) Lead wires that sag below an imaginary plane across the top of the die bond (X plane only) except by design.

(2) Round or "box" transistor type (see figure 2012-6).

(a) Any lead wire that touches or comes within 0.05 mm (0.002 inch) of the case or external lead to which it is not attached (X and Y plane).

(b) Lead wires that sag below an imaginary plane across the top of the die bond (X plane only) except by design.

(c) Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

(d) Any lead wire that deviates from a straight line from bond to external lead and appears to touch or to be within 0.05 mm (0.002 inch) of another wire or bond (Y plane only).

(e) Any bond that is less than 0.025 mm (0.001 inch) (excluding bonds connected by a common conductor) from another bond (Y plane only).

(a) PARTICLE LOCATIONS, PIGTAILS, AND TRIMMING WIRES

(b) VOIDS

FIGURE 2012-1. Particle locations, pigtails, trimming wires, and voids.

(f) Any wire making a straight line run from die bonding pad to package post that has no arc, unless specifically designed in this manner (e.g., clips or rigid connecting leads).

(g) Any internal post that is bent more than 10° from the vertical (or intended design position) or is not uniform in length and construction or comes closer than one post diameter to another post.

(h) Where a low profile case (such as TO-46) is used, any post which comes closer to the top of the case than 20 percent of the total inside dimension between the header and the top of the case. In devices which have the semiconductor element vertical to the header, any device where the semiconductor element comes closer than 0.05 mm (0.002 inch) to the header or to any part of the case.

(i) Any case which does not have a header design incorporating a header edge or other feature (e.g., a "splash ring") to prevent solder or weld splash from entering the interior of the case.

(3) Cylindrical axial lead type (see figure 2012-8).

(a) Whisker to case distance less than one-half of the diameter of the external lead wire.

(b) Distance from case to semiconductor die or to any eutectic bonding material less than 0.05 mm (0.002 inch).

(c) Whisker tilted more than 5° in any direction from the device lead axis or deformed to the extent that it touches itself.

(d) C and S shaped whisker with air gap between any two points on it less than twice the diameter or thickness of the whisker wire. On diodes with whiskers metallurgically bonded to the post and to the die, the whisker may be deformed to the extent that it touches itself if the minimum whisker clearance zone specified in figure 2012-8 (a) is maintained.

(e) Whiskerless construction device with anode and cathode lead connections displaced more than 0.25 mm (0.01 inch) with respect to the central axis of the device.

(f) Semiconductor element mounting tilted more than 15° from normal to the main axis of the device.

(g) Die hanging over edge of header or pedestal more than 10 percent of the die area.

(h) Less than 75 percent of the semiconductor element base area is bonded to the mounting surface.

(i) Voids in the welds, from any edge, between the leads and the heat sink slugs greater than 15 percent of the lead wire diameter. Any voids whatever in the central part of the area that should be welded.

(j) Devices with package deformities such as, body glass cracks, incomplete seals (voids, position glass, etc), die chip outs and severe misalignment of S and C shaped whisker connections to die or post.

FIGURE 2012-2. Acceptable and unacceptable bonding material build-up.

FIGURE 2012-3. Extraneous bonding material build-up.

3.11 Examination and acceptance criteria for hybrid devices.

3.11.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.11.2 Individual device defects. The individual device examination shall include, but not be limited to, extraneous matter, location and orientation of elements, cracks in the substrate that exceed 0.127 mm (0.005 inch) in length or point toward active metallization, adhesive build-up, solder splashes, placement of wires, voids in the lid seal (this may not apply to power hybrid devices), and improper wetting between the substrate(s) and the package. Any device for which the radiograph reveals any of the following defects shall be rejected:

3.11.2.1 Presence of extraneous matter (foreign particles).

a. Unattached foreign material greater than 0.025 mm (0.001 inch), or of any lesser size which is sufficient to bridge metallization or nonconnected conducting elements, that appears to be on the surface of the die, component, substrate, or within the package.

b. Attached foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.

NOTE: Attached or unattached material may be verified by comparing two identical views with a mild mechanical shock, such as PIND test, between the two views.

c. Wire tails or extra wires which make contact with any metallization not connected to the wire, or which exceed four wire diameters in length at the substrate pad or package post, or two wire diameters at the top of a die or component.

d. Any evidence of solder, alloy, or conductive adhesive that appears to bridge noncommon metallization (i.e., wire(s), bonding post, active metallization or any combination thereof) not intended by design.

e. Gold flaking on the bonding post or anywhere inside the case.

3.11.2.2 Unacceptable construction.

a. voids in substrate or component attachment medium.

(1) Contact area voids in excess of one-half of the total contact area.

(2) A single void which traverses either the length or width of the substrate or semiconductor element and whose area exceeds 10 percent of the total intended contact area.

NOTE: To obtain, and/or verify substrate attachment the use of a thermal resistance analyzer, which measures the thermal characteristics (heat dissipation), is strongly recommended.

b. Wires present, other than those connecting specific areas as per the drawing, except wires designated as tuning devices on the bonding diagram, and except where bond-offs are allowed.

c. Improper component placement.

d. Cracks, splits, or chips in the component or substrate which enter the active circuit area.

NOTE: Angle A shall be greater than 45°.

FIGURE 2012-4 Undercutting.

FIGURE 2012-5. Clearance in dual-in-line or flat pack type device.

e. Voids in the lid seal in which the seal is not continuous or is reduced from its design sealing width by more than 75 percent.
NOTE: Sealing voids may not be detectable within power hybrid packages.

f. Inadequate clearance.

* (1) Any wire that comes closer than 0.025 mm (0.001 inch) to another wire (excluding common wires) within a spherical radial distance from the bond perimeter of 0.127 mm (0.005 inch) for ball bonds, or 0.254 mm (0.010 inch) for ultrasonic and thermocompression wedge bonds.
NOTE: Insulated wires defined in the device specification/drawing are excluded from this criteria.

* (2) Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization, die, or portion of a package after a spherical radial distance from the bond perimeter of 0.127 mm (0.005 inch) for ball bonds or 0.254 mm (0.010 inch) for ultrasonic and thermocompression wedge bonds.
NOTE: Insulated wires defined in the device specification/drawing are excluded from this criteria.

* (3) Missing or extra wire(s) or ribbon(s) not in conformance with the bonding diagram except those wire(s) or ribbon(s) designated as microwave tuning devices on the bonding diagram.
NOTE: Extra wires added for statistical process control lot or lot sample bond strength/process machine/operator evaluation in accordance with MIL-PRF-38534 are excluded from this criteria.

(4) Any wire that has no arc and makes a straight line run from die bonding pad to package post.

(5) Wires crossing wires except common conductors or as allowed in 3.2.2e of method 2010 (condition A).

(6) Excessive height in any component or wire loop such that it is closer than 0.127 mm (0.005 inch) to the lid when installed.

(7) Any wires which are broken.
NOTE: Wire bond tails, as defined by method 2017, are excluded from this criteria.

(8) Excessive sag where the wire lies on the substrate for a distance greater than 1/2 the distance between the edge of the substrate bonding pad and the chip to which the wire is bonded, or comes closer than 0.025 mm (0.001 inch) to runout of any conductive epoxy which mounts the chip.

(9) Bonds placed so that the wire exiting from the bond crosses over another bond, except for common bonds.
NOTE: For RF/microwave devices, bonds placed so that the wire exiting from a bond crosses over another bond, except by design, in which case the clearance shall be two wire diameters minimum (common bonds are excluded from this criteria).

FIGURE 2012-6. Clearance in round or box transistor type device.

ACCEPTABLE

UNACCEPTABLE

FIGURE 2012-7. Acceptable and unacceptable excess material.

FIGURE 2012-8. Clearance in cylindrical axail lead type device.

4. Summary. The following details shall be specified in the applicable acquisition document:

   a. Number of views, if other than indicated in 3.1.1.

   b. Radiograph submission, if applicable (see 3.9.2).

   c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).

   d. Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 3.10.

   e. Radiograph and report retention, if applicable (see 3.9.3).

* f. Test reports when required for class level B.

METHOD 2013.1

INTERNAL VISUAL INSPECTION FOR DPA

1. PURPOSE. This is an internal visual inspection for use in destructive physical analysis (DPA) procedures. The purpose of this destructive test is to examine devices opened for post test evaluation to verify that there is no evidence of defects or damage resulting from prior testing.

2. APPARATUS. The apparatus required for the performance of this test shall include binocular normal-incident illumination microscopes capable of 30X to 60X and 75X to 150X magnification with both light and dark field illumination, and any visual or mechanical standards to be used for measurements or comparison.

3. PROCEDURE. The device shall be opened using a technique which does not damage or contaminate the internal structure or in any way impair the ability to observe defects in the devices or the effects of preceding test exposures. The device(s) shall be examined microscopically at 30X to 60X for particles other than those produced by opening. After examination for particles is complete, the opened device(s) shall be blown off with a nominal gas blow (approximately 20 psig) to remove unattached material from the delidding process. The device shall then be microscopically examined to determine the existence of other visual defects as described in 3.1 and 3.2.

3.1 Low magnification defects (30X to 60X). No device shall be acceptable that exhibits the following defects:

a. Improper substrate or bonding post plating material.

b. Improper bond wire material or size.

c. Metallic contamination or foreign material (see method 2010).

d. Lifted or broken wires.

e. Lifted, cracked, or broken die/substrate.

f. Improper die mounting (see method 2010).

g. Excessive lead wire loop or sag (see method 2010).

h. Improper bond technique and size (see method 2010).

i. Improper assembly die location and orientation as compared to the applicable assembly drawing.

j. Particles (see method 2010) other than those introduced during opening.

3.2 High magnification defects (75X to 150X). No device shall be acceptable that exhibits the following defects:

a. Metallization voids, corrosion, peeling, lifting, blistering, or scratches (see method 2010).

b. Bond intermetallics extending radially more than 0.1 mil beyond the bond periphery in any direction.

c. Improper die or substrate metallization design layout topography or identification.

d. Die cracks (see method 2010).

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Where applicable, gauges, drawings, or photographs to be used as standards for the operator comparison (see 2).

   b. Any applicable requirements for materials, design, or construction.

   c. Requirement for photographic record, if applicable, and disposition of the photographs.

   d. Where applicable, any additions or modifications to the specified procedure and criteria.

METHOD 2014

INTERNAL VISUAL AND MECHANICAL

1. PURPOSE. The purpose of this examination is to verify that internal materials, design and construction are in accordance with the applicable acquisition document. This test is destructive and would normally be employed on a sampling basis in qualification or quality conformance inspection of a specific device type to demonstrate compliance with the acquisition document and to reveal any undocumented changes to the part type.

2. APPARATUS. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the applicable acquisition document and shall include optical equipment capable of magnification sufficient to verify all structural features of the devices.

3. PROCEDURE. The device shall be examined under a sufficient magnification to verify that all the internal materials, design and construction are in accordance with the requirements of the applicable design documentation or other specific requirements (see 4). Specimens of constructions which do not contain an internal cavity (e.g., encapsulated or embedded devices) or those which would experience destruction of internal features of interest as a result of opening, may be obtained by interception during manufacturing prior to encapsulation. Specimens of constructions with an internal cavity shall be selected from devices which have completed all manufacturing operations and they shall be delidded or opened or both taking care to minimize damage to the areas to be inspected. When specified by the applicable acquisition document, the interception procedure may be used to obtain specimens of constructions with an internal cavity.

3.1 Photographs of die topography and intraconnection pattern. When specified, an enlarged color photograph or transparency shall be made showing the topography of elements formed on the die or substrate and the metallization pattern. This photograph shall be at a minimum magnification of 80X except that if this results in a photograph larger than 8 inches x 10 inches, the magnification may be reduced to accommodate an 8 inches x 10 inches view.

3.2 Failure criteria. Devices which fail to meet the detailed requirements for materials, design and construction shall constitute a failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Any applicable requirements for materials, design and construction.

b. Allowance for interception procedure of internal cavity devices, when applicable (see 3).

c. Requirement for photographic record, if applicable (see 3.1), and disposition of photographs.

METHOD 2015.11

RESISTANCE TO SOLVENTS

1. PURPOSE. The purpose of this test is to verify that the markings will not become illegible on the component parts when subjected to solvents. The solvents will not cause deleterious, mechanical or electrical damage, or deterioration of the materials or finishes.

1.1 Formulation of solvents. The formulation of solvents herein is considered typical and representative of the desired stringency as far as the usual coatings and markings are concerned. Many available solvents which could be used are either not sufficiently active, too stringent, or even dangerous to humans when in direct contact or when the fumes are inhaled.

1.2 Check for conflicts. When this test is referenced, care should be exercised to assure that conflicting requirements, as far as the properties of the specified finishes and markings are concerned, are not invoked.

2. MATERIALS.

2.1 Solvent solutions. The solvent solutions used in this test shall consist of the following: 1/

a. At 20-30°C a mixture consisting of the following:

* (1) One part by volume of an aliphatic alcohol and/or aliphatic ester, USP grade or better.

(2) Three parts by volume of mineral spirits in accordance with TT-T-291, type II, grade A, or three parts by volume of a mixture of 80 percent by volume of kerosene and 20 percent by volume of ethylbenzene.

* b. A semiaqueous or nonaqueous based organic solvent e.g., a terpene or heterocyclic compound. 2/

c. This solvent has been deleted. When a suitable replacement for this solvent has been found, it will be added as solution c.

d. At 63°C to 70°C, a mixture consisting of the following: 1/

(1) 42 parts by volume of deionized water.

(2) 1 part by volume of propylene glycol monomethyl ether.

* (3) 1 part by volume of monoethanolamine or equivalent inorganic base to achieve the same pH.

1/ Normal safety precautions for handling these solutions (e.g., same as those for diluted ammonium hydroxide) based on O.S.H.A rules for Monoethanolamine or other precautionary measures with regard to flash point, toxicity, etc.

* 2/ Or any EPA demonstrated equivalent. When using EPA approved alternative solutions for test, the device manufacturer should consider the recommended temperature for cleaning specified by the solvent supplier.

2.1.1 Solvent solutions, safety aspects. Solvent solutions listed in a through d above exhibit some potential for health and safety hazards. The following safety precautions should be observed:

a. Avoid contact with eyes.

b. Avoid prolonged contact with skin.

c. Provide adequate ventilation.

d. Avoid open flame.

e. Avoid contact with very hot surfaces.

2.2 Vessel. The vessel shall be a container made of inert material, and of sufficient size to permit complete immersion of the specimens in the solvent solutions specified in 2.1.

2.3 Brush. The brush shall be a toothbrush with a handle made of a nonreactive material. The brush shall have three long rows of hard bristles, the free ends of which shall lie substantially in the same plane. The toothbrush shall be used exclusively with a single solvent and when there is any evidence of softening, bending, wear, or loss of bristles, it shall be discarded.

3. PROCEDURE. The specimens subjected to this test shall be divided into three equal groups. Metal lidded leadless chip carrier (LCC) packages shall be preconditioned by immersing the specimens in room temperature flux type symbols "A" or "B" (flux types "L0" or "L1") in accordance with ANSI/J-STD-004 previously designated as RMA flux in accordance with MIL-F-14256, for 5 to 10 seconds. The specimens shall then be subjected to an ambient temperature of 215°C ±5°C for 60 seconds +5, -0 seconds. After the preconditioning, each device lid shall be cleaned with isopropyl alcohol. Each group shall be individually subjected to one of the following procedures:

a. The first group shall be subjected to the solvent solution as specified in 2.1a maintained at a temperature of 25°C ±5°C.

b. The second group shall be subjected to the solvent solution as specified in 2.1b maintained at a suitable temperature.

c. This solution has been deleted, (see 2.1c).

d. The fourth group shall be subjected to the solvent solution as specified in 2.1d maintained at a temperature of 63°C to 70°C.

The specimens and the bristle portion of the brush shall be completely immersed for 1 minute minimum in the specified solution contained in the vessel specified in 2.2. Immediately following emersion, the specimen shall be brushed with normal hand pressure (approximately 2 to 3 ounces) for 10 strokes on the portion of the specimen where marking has been applied, with the brush specified in 2.3. Immediately after brushing, the above procedure shall be repeated two additional times, for a total of three immersions followed by brushings. The brush stroke shall be directed in a forward direction, across the surface of the specimen being tested. After completion of the third immersion and brushing, devices shall be rinsed and all surfaces air blown dry. After 5 minutes, the specimens shall be examined to determine the extent, if any, of deterioration that was incurred.

3.1 Optional procedure for the fourth group. The test specimens shall be located on a test surface of known area which is located 15 ±2.5 centimeters (6 ±1 inches) below a spray nozzle(s) which discharges 0.6 ±0.02 liters/minute (0.139 gpm) of solution (2.1d) per 6.5 square centimeters (1 in^2)surface area at a pressure of 140 ±30 kilopascal (20 ±5 psi). The specimens shall be subjected to this spray for a period of 10 minutes minimum. After removal and within 5 minutes the specimens shall be examined in accordance with 3.1.1. The specimens may be rinsed with clear water and air blow dried prior to examination.

3.1.1 Failure criteria. After subjection to the test, evidence of damage to the device and any specified markings which are missing in whole or in part, faded, smeared, blurred, or shifted (dislodged) to the extent that they cannot be readily identified from a distance of at least 15.0 cm (6 inches) with normal room lighting and without the aid of magnification or with a viewer having a magnification no greater than 3X shall constitute a failure.

4. SUMMARY. The following detail shall be specified in the individual specification: The number of specimens to be tested (see 3).

METHOD 2016

PHYSICAL DIMENSIONS

1. PURPOSE. The purpose of this examination is to verify that the external physical dimensions of the device are in accordance with the applicable acquisition document.

2. APPARATUS. Equipment used in this examination shall include micrometers, calipers, gauges, contour projectors, or other measuring equipment capable of determining the actual device dimensions specified in the applicable acquisition document.

3. PROCEDURE. Unless otherwise specified, the physical dimensions on the case outline drawing shall be measured.

3.1 Failure criteria. Any device which exhibits a dimension or dimensions outside the specified tolerances or limits shall constitute a failure.

4. SUMMARY. The following detail shall be specified in the applicable acquisition document:

External dimensions which are capable of physically describing the device (see 3). Dimensions to be considered shall include case outline dimensions; special lead shapes (e.g., required bend positions, angles of bend), where applicable; dimensions of any projecting or indented features used for coding of lead arrangement, automatic handling and similar purpose; and any other information which affects the installed size or orientation of the device in normal applications.

METHOD 2017.7

INTERNAL VISUAL (HYBRID)

1. PURPOSE. The purpose of this test is to visually inspect the internal materials, construction, and workmanship of hybrid, multichip and multichip module microcircuits.

* 1.1 SCOPE. This test is for both Class H (Class level B) and Class K (Class level S) quality levels, SAW and hybrid/multichip/multichip module microcircuits. The following types of microcircuits may be inspected:

a. Passive thin and thick film networks.

b. Active thin and thick film circuits.

c. Multiple circuits, including combinations, stacking or other interconnections of 1.1.a and 1.1.b.

This test will normally be used on microelectronic devices prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects that could lead to device failure in normal application. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturers quality control and handling procedures.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and visual standards/aids (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3. PROCEDURE.

a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the specified test condition.

b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Where obscuring mounting techniques (e.g., beam lead devices, stacked substrates, components mounting in holes or cutaways, flip chip devices, packaged devices) are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to mounting the element or substrate. The inspection criteria of 3.1.1 may be performed at the option of the manufacturer prior to element attachment.

* c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections (see 3.b), to ensure that defects created during subsequent handling will be detected and rejected at final preseal inspection. Devices examined to 3.1 criteria shall be inspected and prepared for sealing in a class 100,000 controlled environment for Class H (Class level B) and class 100 controlled environment for Class K (Class level S), as defined in Federal Standard 209, except that the allowable relative humidity shall be less than 65 percent. During the time interval between internal visual inspection and preparation for sealing, devices shall be stored in a Class 1000 controlled environment. Devices shall be in covered containers when transferred from one controlled environment to another.

* d. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. Where sample inspection is used rather than 100 percent reinpsection, the sampling plans of MIL-PRF-38534 or Appendix A of MIL-PRF-38535 shall apply.

e. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

f. Definitions.

(1) Active circuit area includes all areas of functional circuit elements, operating metallization or connected combinations thereof excluding beam leads.

(2) Add-on substrate is a supporting structural material into and/or upon which glassivation, metallization and circuit elements are placed and the entire assembly is in turn placed on, and attached to the main substrate.

(3) Attachment media is defined as the material used to effect the attachment of an element to an underlying surface (e.g., adhesive, solder, alloy).

(4) Bonding site is a metallized area on a substrate or element intended for a wire or ribbon interconnecting bond.

(5) Cold solder joint is defined as a solder joint whose appearance is "grainy" or "dull". Where a "grainy" or "dull" appearance is characteristic of certain solder materials (e.g., AuSn, etc.), this criteria shall not be rejectable for these materials.

(6) Compound bond is one bond on top of another.

(7) Conductive attach is the process and materials used for the attachment that also provides an electrical contact or thermal dissipation path (e.g., solder, eutectic, solder-impregnated epoxy).

(8) Dielectric attach is the process and materials used for attachment that does not provide electrical contact or thermal dissipation considerations.

(9) Edge metallization is the metallization that electrically connects the metallization from the top surface to the opposite side of the substrate; also called wrap around metallization.

(10) Element is a constituent of a hybrid microcircuit; such as integral deposited or screened passive elements, substrates, discrete or integrated electronic parts including dice, chips and other microcomponents; also mechanical piece parts as cases and covers; all contributing to the operation of a hybrid microcircuit.

(11) Electrically common is satisfied when two or more conductive surfaces or interconnects are of equal DC voltage/signal potential.

(12) End terminated or wrap around elements are those elements which have electrical connections on the ends (sides) and/or bottom of their bodies.

(13) Foreign material is defined as any material that is foreign to the microcircuit of any non-foreign material that is displaced from its original or intended position within the microcircuit package. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in glassivation when there is evidence of color fringing around the periphery of the particle.

(14) Glassivation is the top layer(s) of transparent insulating material that covers the active area including metallization, except bonding pads and beam leads. Crazing is the presence of minute cracks in the glassivation.

(15) Insulating layer is a dielectric layer used to isolate single or multilevel conductive and resistive material or to protect top level conductive resistive material.

(16) Intermetallics (Purple Plague) is one of several gold-aluminum compounds formed when bonding gold to aluminum and activated by re-exposure to moisture and high temperature (>340°C). Purple plague is purplish in color and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

(17) Mechanical strength tests are tests, such as Mechanical Shock or Constant Acceleration, which demonstrate adequate attachment process and materials.

(18) Non-monometallic compound bond consists of two lead bonds, made of dissimilar metals, which are stacked one on top of the other (i.e., the interface between the two lead bonds are made up of dissimilar metals such as an aluminum lead bond stacked on top of a gold lead bond or vice-versa.

(19) Operating metallization (conductors) is all metal or any other material used for interconnections except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.

(20) Original design separation is the separation dimension or distance that is intended by design.

(21) Original width is the width dimension or distance that is intended by design (i.e., original metal width, original diffusion width, original beam width, etc.).

(22) Passivation is the silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of the final metal layers.

(23) String is a filamentary run-out or whisker of polymer material.

(24) Substrate is the supporting structural material into and/or upon which the passivation, metallization, and circuit elements are placed.

(25) Tuning is the adjustment of signals from an RF/Microwave circuit by altering lines or pads; adding, deleting or manipulating wires/ribbons; and/or changing resistance, inductance or capacitance values to meet specific electrical specifications.

(26) Through hole metallization is the metallization that electrically connects the metallization on the top surface of the substrate to the opposite surface of the substrate.

(27) Unused component or unused deposited element is one not connected to a circuit or connected to a circuit path at one and only one point. A connection may be made by design or by visual anomaly.

(28) Void is any region in the material (interconnects, bonding sites, etc.) where underlying material is visible that is not caused by a scratch.

(29) Visible line is defined as 0.5 mil at 60X magnification.

g. Interpretations. References herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used to confirm that a reject condition does not exist, they shall be approved by the acquiring activity.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for the presence of foreign material on the die surface, or within the package. This audit may be satisfied during routine internal visual inspection. If the presence of any type of foreign material/contamination is discovered, the manufacturer shall perform the necessary analysis on a sample of suspect devices to determine the nature of the foreign material. The manufacturer shall then document the results of his investigation and corrective actions to eliminate the foreign material and shall make this information available to the Government QAR, the acquiring activity, or the qualifying activity, as required. Corrective action responses shall be obtained within a maximum of ten (10) working days of discovery. The intent of this procedure is to require investigation and resolution of foreign material/contamination problems which do not have effective screening or detection methodology, but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality Assurance, or their equivalents, to continue processing.

3.1 Examination. Internal visual examination as required in 3.1.1 through 3.1.9 shall be conducted on each SAW, hybrid/multichip microcircuit, or microwave hybrid microcircuit. The magnifications required for each inspection shall be those identified in the particular test method used (i.e., 2010, 2017, or 2032 of MIL-STD-883 and 2072, 2073 of MIL-STD-750).

3.1.1 Active and passive elements. All integrated circuit elements shall be examined in accordance with MIL-STD-883, method 2010.

Class H	Class K
(Class level B Monolithic)	(Class level S Monolithic)

Method 2010; Para. 3.1.1: Metallization defects.

Method 2010; Para. 3.1.2: Diffusion and passivation layer(s) faults.

Method 2010; Para. 3.1.3: Scribing and die defects.

Method 2010; Para. 3.2.5: Foreign material.

Method 2010; Para. 3.1.4: Glassivation defects.

Method 2010; Para 3.1.6: Film resistors defects.

Method 2010; Para. 3.1.7: Laser trimmed film resistor defects.

Transistor and semiconductor diode elements shall be examined in accordance with MIL-STD-883, method 2010 (paragraphs referenced above) or the identified paragraphs of MIL-STD-750, methods 2072 and 2073 as indicated below. Passive elements (including substrates) shall be examined in accordance with MIL-STD-883, method 2032.

Visual Inspection	MIL-STD-750 Method 2072	MIL-STD-750 Method 2073	MIL-STD-883 Method 2010
Die metallization defects	4.1.1	4.1.3, 4.1.5	3.1.1
Diffusion and passivation layer(s)	4.1.2	4.1.2	3.1.2
Scribing and die defects	4.1.3	4.1.1, 4.1.4	3.1.3

3.1.2 Element attachment (assembly), "magnification 10X to 60X". Figures 2017-1 and 2017-2 are example visual representations of attachment media types.

NOTE: Rejection criteria are not to be derived from these examples but rather from the specific criteria paragraphs that follow.

FIGURE 2017-1. Element attachments.

FIGURE 2017-2. Element attachments.

Class H	Class K
Note: Mechanical strength or Radiography may be used to verify attachment in lieu of visual criteria.	Dielectric attachment may be assessed through Mechanical Strength Testing. For conductive attachment, the Qualifying Activity may approve alternate methods for verifying attachment integrity.

No device shall be acceptable that exhibits:

a. For non-end terminated elements, attachment media not visible around at least 50 percent of the perimeter unless *it is continuous on two full nonadjacent sides of the element.*

NOTE: The criteria of paragraph 3.1.2.a shall not apply when attachment material is applied directly to more than 50 percent of the element attach area by use of a method such as preforms or printing.

b. End terminated elements that do not have conductive attachment media visible around at least 50 percent of the visible bonding pad perimeter on each end termination. For dielectric attachment of end terminated elements (i.e., where the body of the element between the end terminations is attached), the criteria of (a) above applies.	End terminated elements that do not have conductive attachment media visible around at least 75 percent of the visible bonding pad perimeter on each end termination. For dielectric attachment of end terminated elements (i.e., where the body of the element between the end terminations is attached), the criteria of (a) above applies.

c. Glass substrates or transparent die, when viewed from the bottom, which exhibit attach area less than 50 percent.

NOTE: This criterion may be employed in lieu of 3.1.2.a.

d. Flaking of the attachment media material.

e. Balling of the solder or alloy material that does not exhibit a fillet. (see Figure 2017-3)

DETAIL A
FRONT VIEW

REJECT, NO FILLET
VISIBLE

ACCEPT, FILLET
VISIBLE

DETAIL A
TOP VIEW

FIGURE 2017-3. Balling of die attach material.

Class H | Class K

f. Conductive attachment media which comes closer than 1.0 mil to any functional metallization or element which is not electrically common.

g. Cracks in the surface of the attachment media greater than 5.0 mils in length or 10 percent of the contact periphery, whichever is greater.

NOTE: Irregularities such as fissures or pullback at the edges of the adhesive are not considered cracks. (see Figure 2017-3a)

FIGURE 2017-3a. Adhesive irregularities and cracks.

h. Adhesive strings where the diameter of the string at the point of attachment is less than 50 percent of the maximum length of the string. (see Figure 2017-3b)

FIGURE 2017-3b. Adhesive String Criteria.

Class H | Class K

i. For element connection to a package post lead, attachment media visible for less than 25 percent of the post perimeter. When the post also serves for substrate attachment, media shall be visible for no less than 50 percent of the post perimeter. (see Figure 2017-3C)

j. Cold solder joints.

k. For thin film NiCr only, nonconductive adhesive material that covers more than 10 percent of the active area of deposited resistor material.

FIGURE 2017-3c. Package Post Criteria.

3.1.3 Element orientation. Element not located or oriented in accordance with the applicable assembly drawing of the device. Elements whose bond and electrical configuration is symmetrical may be rotated unless otherwise stated in the assembly drawings.

FIGURE 2017-3d. Acceptable Symmetrical Element Orientation.

Class H | Class K

3.1.4 Separation. Elements shall not overhang the edge of the substrate. A minimum clearance of 1.0 mil shall be maintained between any uninsulated portion of the element and any non-common conductive surface.

3.1.5 Bond inspection, magnification 30X to 60X. This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.

Note: Wire tail shall not be considered part of the bond when determining physical bond dimensions.

3.1.5.1 Ball bonds. *No device shall be acceptable that exhibits:*

a. Ball bond diameter less than 2.0 times or greater than 5.0 times the wire diameter.

b. Ball bonds where the wire exit is not completely within the periphery of the ball.

c. Ball bonds where the wire center exit is not within the boundaries of the bonding site.

3.1.5.2 Wire wedge bonds. No device shall be acceptable that exhibits: (see Figure 2017-4a)

a. Ultrasonic and thermosonic wedge bonds that are less than 1.0 times or greater than 3.0 times the wire diameter in width or less than 0.5 times the wire diameter in length or no evidence of tool impression.

b. Devices with thermocompression wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width or less than 0.5 times the wire diameter in length or no evidence of tool impression.

FIGURE 4a. Bond Dimensions.

Class H | Class K

3.1.5.3 Tailless bonds (crescent). No device shall be acceptable that exhibits:

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width. (see Figure 2017-4).

b. A tailless bond of a gold wire bonded on the aluminum pads of a die.

FIGURE 2017-4b. Bond Dimensions.

3.1.5.4 Compound bond. No device shall be acceptable that exhibits the following:

NOTE: Broken or lifted bonds as a result of electrical troubleshooting or tuning shall be considered rework and shall not apply to the 10 percent repair limitation.

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a. One bond used to secure two common wires. (see Figure 2017-5)

FIGURE 2017-5. One bond used to secure two common wires.

b. More than one bond on top of original bond.

NOTE: When required by design and based on a justifiable technical need, and with the approval of the qualifying or acquiring activity, additional compound bonds may be allowed in addition to the limitations of a and b above. Demonstration of acceptable N+1 bond stacks (N = maximum number of compound bonds allowable by the manufactures process) and establishment of necessary process controls shall be required for approval.

c. Compound bond where the contact area of the second bond with the original bond is less than 75 percent of the bottom bond.

d. Non-monometallic compound bond (i.e., between dissimilar metals, excluding the bond pad metallization).

3.1.5.5 Beam lead. This inspection and criteria shall apply to the completed bond area made using direct tool contact. No device shall be acceptable that exhibits:

a. Bonds which do not exhibit 100 percent bond/weld impression(s) across the width of the beam lead.

NOTE: Gaps between bonds/welds on the beam lead caused by the natural footprint of a bond/weld tip (i.e., split tip, etc.), are acceptable provided the total of all gaps does not exceed 25 percent of the beam lead width.

b. Complete or partial beam separation from the die.

c. Bonds on the substrate where the tool impression is not visible on the beam.

d. Beam lead width increased by greater than 60 percent of the original beam width.

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e. Bonds where the tool impression length is less than 1.0 mil (see Figure 2017-6)

FIGURE 2017-6. Beam Lead Area and Location.

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f. Bonding tool impression less than 1.0 mil from the die edge (see Figure 2017-6).

g. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see Figure 2017-6).

h. Any tears in the beam lead between the bond junction nearest the die body and the die or in the bonded area of the beam lead within a distance equal to 50 percent the beam lead width (see Figure 2017-7).

FIGURE 2017-7. Acceptable/rejectable tears or voids in ribbon weld area.

i. An absence of visible separation between the bond and the edge of the passivation layer (see Figure 2017-6).

j. An absence of visible separation between a beam lead and non-electrically common metallization. This criteria applies for both glassivated and unglassivated metallization.

3.1.5.6 Mesh bonding. No device shall be acceptable that exhibits the following:

a. Less than 50 percent of the bond is on substrate metallization.

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b. The number of continuous strands along the mesh is less than 50 percent of lengthwise strands through each section. (see Figure 2017-8a).	
c. Less than one continuous conducting path(s) through a bond (see Figure 2017-8b).	Less than two continuous conducting path(s) through a bond (see Figure 2017-8b).

REJECT: LESS THAN HALF OF THE LENGTHWISE STRANDS ARE CONTINUOUS (2 OF 3 STRANDS ARE DISCONTINUOUS)

ACCEPT: 2 (HALF) OR MORE OF THE LENGTHWISE STRANDS ARE CONTINUOUS THROUGH EACH SECTION

FIGURE 2017-8a. Criteria for strands along the mesh.

REJECT: NO CONTINUOUS PATH THROUGH THE MESH BETWEEN BONDS

ACCEPT: AT LEAST ONE CONTINUOUS PATH THROUGH THE MESH BETWEEN BONDS

FIGURE 2017-8b. Criteria for continuous conducting paths.

Class H	Class K

3.1.5.7 Ribbon bonds. No device shall be acceptable that exhibits the following:

a. Any tears in the ribbon at the junction between the ribbon loop and bond/weld.

b. Bonds which do not exhibit 100 percent bond/weld impression(s) across the width of the ribbon overlapping underlying metallization.

NOTE: Gaps between welds on the ribbon caused by the natural footprint of a weld tip (i.e., split tip, etc.) are acceptable provided the total of all gaps do not exceed 25 percent of the ribbon width.

c. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned ribbon.

d. Bond tails longer than one ribbon width or 10.0 mils, whichever is less, or bridging adjacent metallization.

e. The unbonded end of a ribbon bond tuning stub longer than one ribbon width of 10.0 mils, whichever is less, that is not secured by polymer adhesive.

3.1.5.8 General. No device shall be acceptable that exhibits:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding site.	Monometallic bonds on the die where less than 50 percent of the bond is within the unglassivated bonding site. Bimetallic bonds on the die where less than 75 percent of the bond is within the unglassivated bonding site.

b. Bonds on the package post or substrate that are not completely within the bonding site.

NOTE: For cases where the substrate bonding site is smaller than 1.5 times the minimum bond size, bonds on the substrate where less than 50 percent of the bond is within the bonding site.

c. Bonds placed so that the wire exiting from a bond crosses over another bond, except by design, in which case the clearance shall be 2.0 wire diameters minimum (common bonds are excluded from this criteria).

d. An absence of a visible line of separation between non-electrically common bonds.

e. An absence of a visible line of separation between a bond and non-electrically common metallization. This criteria applies to both glassivated and unglassivated metallization.

f. Wire bond tails that extend over or make contact with any noncommon, unglassivated active metal.

g. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

h. Bonds on element attach media or on contaminated or foreign material.

i. Any lifted or peeling bond.

j. Intermetallic formation extending completely around the metallic interface of any bond between dissimilar metals.

Class H | Class K

k. Wedge or crescent bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe.

NOTE: Criteria of 3.1.5.8 (k) can be excluded when the entering conductor is >2 mils in width and the bond pad dimension on the entering conductor side is >3.5 mils.

NOTE: For Class H only, the requirements for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, provided the following condition exists. Bond is located more than 0.1 mil from the intersecting line of the entering metallization stripe and the bonding pad and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

NOTE: Criteria 3.1.5.8 (k) is not applicable to interdigitated (Lange) couplers or when the interface between a thermosonic/ultrasonic (i.e., non-thermocompression) bond and underlying metal is monometallic.

l. Polymeric adhesive which may be material or residue as evidenced by discoloration within 5.0 mils of the outer periphery of a wire bond.

m. Tearing at the junction of the wire and bond. The junction is the line of deformation of the wire at the bonding site.

3.1.6 Internal leads (e.g., wires, ribbons, beams, wireloops, ribbon loops, beams, etc.), "magnification 10X to 60X". No device shall be acceptable that exhibits:

a. Within the first 5.0 mils of wire from the die surface for ball bonds, or 10.0 mils for wedge bonds, any wire that comes closer than 1.0 mil to any non-common conductive surface (e.g., unglassivated operating metallization, unpassivated edge of conductive die).

NOTE: Insulated wires and electrically common wires are excluded from this criteria.

b. After the first 5.0 mils of wire from the die surface for ball bond(s), or 10 mils for wedge bonds, any wire that comes closer than two wire diameters to any non-common, uninsulated conductive surface (e.g., unglassivated operating metallization, unpassivated edge of conductive die).

NOTE: Insulated wires and electrically common wires are excluded from this criteria.

c. Nicks, cuts, crimps, scoring, sharp bends, or neckdown in any lead that reduces the lead diameter/width by more than 25 percent.

d. Missing or extra lead(s) not in conformance with bonding diagram.

NOTE: Leads designated for tuning on the bonding diagram are excluded.

e. Any lead making a straight line run from bond to bond that has no arc, unless specifically allowed by the bonding diagram.

f. Wire(s) crossing wire(s) with a separation of less than 2 lead widths. Common or insulated conductors and insulated wires are excluded.

g. Complete or partial separation of the lead from the body of the element.

h. Excessive loop height such that the wire would contact the lid when it is installed.

Class H | Class K

3.1.7 Screw tabs and through hole mounting, magnification 3X to 10X. No device shall be acceptable that exhibits:

a. Misaligned tabs.

b. Missing or broken tabs.

c. Cracks emanating from mounting holes.

d. Loose substrates.

e. Missing or loose screws.

3.1.8 Connector and feedthrough center contact soldering, magnification 10X to 30X. No device shall be acceptable that exhibits:

a. Less than 50 percent of center contact overlaps onto metallized pattern (see Figure 2017-9).

b. Center contact to substrate protrudes over onto circuit less than 1 diameter of a round pin or the width of a flat pin (see Figure 2017-10).

c. Voids in solder (see Figure 2017-11a).

d. Cracked solder joint (see Figure 2017-11b).

e. Poor adhesion of solder to center contact or substrate (see Figure 2017-11b).

f. Insufficient or excess solder (see Figures 2017-11c through 2017-11e).

g. Less than full coverage of solder along the length of the center contact and the metallization.

FIGURE 2017-9 Center contact orientations to substrate.

FIGURE 2017-10. Center Contact overlap to substrate.

FIGURE 2017-11a. Void criteria.

FIGURE 2017-11b. Crack/adhesion criteria.

FIGURE 2017-11c. Excess solder criteria.

FIGURE 2017-11d. Insufficient solder criteria.

FIGURE 2017-11e. Solder criteria.

Class H | Class K

3.1.9 Package conditions, "magnification 10X to 60X". No device will be acceptable that exhibits:

a. Unattached foreign material within the package or on the seal flange.

NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring activity. All foreign material or particles may be verified as attached with a nominal gas blow (approximately 20 psig).

NOTE: Semiconductor chips shall be considered foreign particles.

b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.

c. Liquid droplets or any chemical stain that bridges any combination of unglassivated operating metallization.

d. Physical damage or contamination (eutectic or polymer material) that prevents adequate sealing of the seal surface.

e. Presence of any residual flux.

NOTE: Use 10X to 15X magnification.

f. Foreign material in melt that does not exhibit a fillet.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Where applicable, gages, drawings and photographs that are to be used as standards for operator comparison (see 2).

c. Where applicable, specific magnification if other than that specified (see 3).

METHOD 2018.3

SCANNING ELECTRON MICROSCOPE (SEM) INSPECTIONS

1. PURPOSE. This method provides a means of judging the quality and acceptability of device interconnect metallization on integrated circuit wafers or dice. It addresses the specific metallization defects that are batch process orientated and which can best be identified utilizing this method. Conversely, this method should not be used as a test method for workmanship and other type defects best identified using method 2010.

Samples submitted to SEM shall not be shipped as functional devices unless it has been shown that the device structure, in combination with the equipment operating conditions, is nondestructive.

1.1 Definitions.

1.1.1 Barrier adhesion metal. The lower layer of multi-layer metal system deposited to provide a sound mechanical bond to silicon/silicon oxide surfaces or to provide a diffusion barrier of a metal into an undesired area such as aluminum into a contact window.

1.1.2 Cross-sectional plane. An imaginary plane drawn perpendicular to current flow and which spans the entire width of the metallization stripe as illustrated in figure 2018-1. Metallization stripes over topographical variations (e.g., passivation steps, cross-overs, bird's head), which are nonperpendicular to current flow, are projected onto cross-sectional planes for purposes of calculating cross-sectional area reductions.

1.1.3 Destructive SEM. The use of specific equipment parameters and techniques that result in unacceptable levels of radiation damage or contamination of the inspected semiconductor structure.

1.1.4 Directional edge. A directional edge (see figure 2018-2) is typically the edge(s) of a rectangular contact window over which metallization may be deposited for the purpose of carrying current into, through, or out of the contact window for device operation. It should be noted that contact geometry, site of concern, or both may vary and if so, the directional edge concept should be modified accordingly.

1.1.5 General metallization (conductors). The metallization at all locations including metallization (stripes) in the actual contact window regions with the exception being at areas of topographical variation (e.g., passivation steps, bird's head, cross-overs).

1.1.6 Glassivation. Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area (including metallization), except bonding pads and beam leads.

1.1.7 Interconnection. The metal deposited into a via to provide an electrical conduction path between isolated metal layers.

1.1.8 Major current-carrying directional edge. The directional edge(s) which is designed to provide a path for the flow of current into, through, or out of a contact window or other area(s) of concern (see figure 2018-2).

1.1.9 Multi-layer metallization (conductors). Two or more layers of metal used for electrical conduction that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

1.1.10 Multi-level metallization (conductors). A single layer or a multi-layer of metal shall represent a single level of metallization. A combination of such levels, isolated from each other by a grown or deposited layer of insulating material, shall comprise the multi-level metallization interconnection system. The use of vias to selectively connect portions of such level combinations through the isolation shall not effect this definition.

1.1.11 Nondestructive SEM. The use of specific equipment parameters and techniques that result in negligible radiation damage, contamination, or both of the inspected semiconductor structure (see 3.10 and 3.11).

1.1.12 Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited on the die prior to metallization.

1.1.13 Passivation steps. The vertical or sloped surface resulting from topographical variations of the wafer surface (e.g., contact windows, diffusion cuts, vias, etc.).

1.1.14 Via. The opening in the insulating layer to provide a means for deposition of metal to interconnect layers of metal.

1.1.15 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group and assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process.

2. APPARATUS. The apparatus for this inspection shall be a scanning electron microscope (SEM) having resolution of 250Å or less as measured on the photograph at use conditions and a variable magnification of 1,000X to 20,000X. The apparatus shall be such that the specimen can be tilted to a viewing angle (see figure 2018-3) between 0° and 85°, and can be rotated through 360°.

2.1 Calibration. The magnification shall be within ±10 percent of the nominal value when compared with National Institute of Standards and Technology standard 484 or an equivalent at the magnification(s) used for inspection. The resolution shall be 250Å or less as verified with National Institute of Standards and Technology standard SRM-2069 or equivalent. Magnification and resolution verification shall be performed on a frequency defined by the manufacturer based on statistical data for his SEM equipment.

2.2 Operating personnel. Personnel who perform SEM inspection shall have received adequate training in equipment operation and interpretation of the images and resulting photographs prior to attempting certification for metallization inspection. Procedures for certification of SEM operators for metallization inspection shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity. This shall include provisions for recertification procedures once a year as a minimum.

Operator certifications and recertifications shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

2.3 Procedures. There shall be written procedures for metallization inspection. These procedures shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

3. PROCEDURE.

3.1 Sample selection. Statistical sampling techniques are not practical here because of the large sample size that would be required. The wafer sampling requirements defined in table I, taken in conjunction with specific dice locations within the sampled wafers, minimize test sample size while maintaining confidence in test integrity. These dice are in typical or worst case positions for the metallization configuration.

Die area submitted for SEM evaluation shall not have been or be located immediately adjacent to the wafers edge, and they shall be sufficiently free of smearing, so that the required inspection can be conducted in an area of undisturbed metallization. Acceptance of the interconnect metallization shall be based on examination of selected die area, using either a single wafer acceptance basis or a wafer lot acceptance basis.

Reference to die or dice within this test method implies the evaluation of a complete function or device. When approved by the qualifying activity, this requirement may be satisfied by the evaluation of a special SEM test vehicle existing within the scribe line (kerf), within each die, or within a special process drop in.

3.1.1 Sampling conditions. This sampling condition applies to devices which have glassivation over the metallization. Steps 1 and 2, which follow, both apply when acceptance is on a wafer lot acceptance basis. Step 2 applies only when acceptance is on a single wafer acceptance basis.

3.1.1.1 Step 1: Wafer selection. From each lot to be examined on a wafer lot acceptance basis, wafers shall be selected as defined by table I. If more than one wafer lot is processed through the metallization operation at one time, each wafer lot shall be grouped as defined by table I and a separate set of wafers shall be selected for each wafer lot being examined on a wafer lot acceptance basis.

3.1.1.2 Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer acceptance basis, or with one or more other wafers on a wafer lot acceptance basis), one of the following sampling conditions may be used at the manufacturer's option:

3.1.1.2.1 Sampling quadrants. Immediately following the dicing operation (e.g., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart. The glassivation shall then be removed from the dice using a suitable etchant process(es) (see 3.3) followed by SEM examination.

3.1.1.2.2 Sampling segment, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

Two segments shall be separated from the opposite side of each wafer (i.e., subsequent to metallization and etching but prior to glassivation). These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination.

3.1.1.2.3 Sampling segment, after glassivation. After completion of all processing steps and prior to dicing, two segments shall be separated from opposite sides of each wafer. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination after the glassivation has been removed using a suitable etchant process(es) (see 3.3).

3.1.1.2.4 Sampling whole wafers, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

After completion of the metallization and etching steps and specimen preparation operation, if applicable (see 3.3), the complete wafer shall be placed into the SEM equipment and four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

No die or contiguous die from the inspected wafer shall be shipped as a functional device unless it is shown that the examination is nondestructive (see 3.10 and 3.11).

3.1.1.2.5 Sampling whole wafers, after glassivation. This condition is destructive. The complete wafer shall be subjected to the specimen preparation operation, if applicable (see 3.3), and then placed into the SEM equipment. Four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

TABLE I. Wafer sampling procedures for various metallization chamber configurations.

Metallization chamber configuration 1/ 2/	Number of wafer lots in chamber 3/	Required number of samples per wafer lot		Sampling plans per wafer lot
		Evaporation	Sputtering	
Projected plane view of the Wafer-holder is a circle. Wafer-holder is stationary or "wobbulates"	1 4/	5	2	Four from near the periphery of the wafer-holder and 90° apart. One from the center of holder. See figure 4.
	2	3, 4, or 5	2	See figure 4.
	3	3 or 4	2	See figure 4.
	4	3	2	See figure 4.
Wafer-holder is symmetrical (i.e., circular, square, etc.). Deposition source(s) is above or below the wafer-holder. Wafer-holder rotates about its center during deposition.	1, 2, 3, or 4 4/	2	2	For each wafer lot, one from the periphery of the wafer-holder, and one from close proximity to the center of rotation. See figure 4. 5/
Planetary system. One or more symmetrical wafer-holders (planets) rotate about their own axes while simultaneously revolving about the center of the chamber. Deposition source(s) is above or below the wafer-holders.	1, 2, 3, or 4 per planet 4/	2	2	For each wafer lot, one from near the periphery of a planet and one from near the center of the same planet. See figure 4. 6/
Continuous feed. Wafers are continuously inserted into deposition chamber through a separate pump down of an airlock (25 wafer nominal load)	1 1/	2	2	Two randomly selected wafers from each wafer lot.

1/ In this case, a wafer lot shall be defined as a batch of wafers which have received together those common processes which determine the slope and thickness of the passivation steps on these wafers.
2/ If a wafer-holder has only one circular row, or if only one row is used on a multi-rowed wafer-holder; the total number of specified sample wafers shall be taken from that row.
3/ If there is more than one wafer lot in a metallization chamber, each wafer lot shall be grouped approximately in a separate sector within the wafer-holder. A sector is an area of the circular wafer-holder bounded by two radii and the subtended arc; quadrants and semicircles are used as examples on figure 4.
4/ If the wafer lot size exceeds the loading capacity of the metallization system each processed sub-lot will be sampled as if it was a unique lot.
5/ When evaluation data shows that there is no relationship between SEM results and the physical location of the wafers during the metallization process. It shall be permissible to substitute two randomly selected wafers from each wafer lot. This analysis shall be repeated after each major equipment repair.
6/ Sample wafers need be selected from only one planet if all wafer lots contained in the chamber are included in that planet. Otherwise, sample wafers of the wafer lot(s) not included in that planet, shall be selected from another planet(s).

3.1.2 Sampling Destructive Physical Analysis (DPA) evaluation. Finished product, wafers, or die may be subjected to the test conditions and criteria defined within this test method for the purpose of a DPA evaluation.

3.2 Lot control during SEM examination. After dice selection for SEM examination, the manufacturer may elect either of two options:

3.2.1 Option 1. The manufacturer may continue normal processing of the lot with the risk of later recall and rejection of product if SEM inspection, when performed, shows defective metallization. If this option is elected, positive control and recall of processed material shall be demonstrated by the manufacturer by having adequate traceability documentation.

3.2.2 Option 2. Prior to any further processing, the manufacturer may store the dice or wafers in a suitable environment until SEM examination has been completed and approval for further processing has been granted.

3.3 Specimen preparation. When applicable, glassivation shall be removed from the dice using an etching process that does not damage the underlying metallization to be inspected (e.g., chemical or plasma etch). Specimens shall be mounted for examination in a manner appropriate to the apparatus used for examination. Suitable caution shall be exercised so as not to obscure features to be examined.

Specimens may be examined without any surface coating if adequate resolution and signal-to-noise levels are obtained. If the specimens need to be coated, they shall be coated with no more than 100Å of a thin vapor-deposited or sputtered film of a suitable conductive material (e.g., Au). The coating deposition process shall be controlled such that no artifacts are introduced by the coating.

3.4 Specimen examination, general requirements. The general requirements for SEM examination of general metallization and passivation step coverage are specified below in terms of directional edge, magnification, viewing angle, and viewing direction.

3.4.1 Directional edge. All four directional edges of every type of passivation step (contact window or other type of passivation step) shall be examined on each specimen (see table II).

3.4.2 Magnification. The magnification used for examination of general metallization and passivation steps shall be within the range defined by table II.

3.4.3 Viewing angle. Specimens shall be viewed at whatever angle is appropriate to accurately assess the quality of the metallization. Contact windows, metal thickness, lack of adhesion, and etching defects are typically viewed at the angles of 0° to 85° (see figure 2018-3).

3.4.4 Viewing direction. Specimens shall be viewed in an appropriate direction to accurately assess the quality of the metallization. This inspection shall include examination of metallization at the edges of contact windows and other types of passivation steps (see 3.4) in any direction that provides clear views of each edge and that best displays any defects at the passivation step. This may mean that the viewing angle is perpendicular to an edge, or in parallel with an edge, or at some oblique angle to an edge, whichever best resolves any question of defects at the passivation step (see figure 2018-5).

3.5 Specimen examination detail requirements. Examination shall be as specified herein and summarized in table II. The specimen examination shall be documented in accordance with 3.8.

3.5.1 General metallization. At low magnification, inspect at least 25 percent or 10,000 square mils, whichever is less, of the general metallization on each die for defects such as lifting, peeling, blistering, and voiding. Inspection shall be performed for each layer of each level of metallization.

3.5.1.1 Multi-layer and multi-level metal interconnection systems. Each layer of each metallization level that is deposited shall be examined. The current- carrying layer(s) shall be examined with the SEM after removal of the glassivation layer (if applicable) with a suitable etchant (see 3.3).

3.5.1.2 Barrier/adhesion layers. The examination of barrier/adhesion layers may be implemented in two different ways as specified below:

3.5.1.2.1 Barrier/adhesion layer as a nonconductor. When a barrier/adhesion layer is designed to conduct less than ten percent of the total current, this layer must be considered as only a barrier/adhesion layer. Consequently, this barrier/adhesion layer shall not be used in current density calculations and shall not be required to satisfy the step coverage requirements. The barrier/adhesion layer shall be required to cover only those regions where a barrier/adhesion function is designed with the manufacturer providing suitable verification of this function. The thickness of the barrier/adhesion layer shall not be permitted to be added to the thickness of the principal conducting layer when estimating the percentage metallization step coverage. Therefore, the principal conducting layer shall satisfy the percentage step coverage by itself.

3.5.1.2.2 Barrier/adhesion layer as a conductor. The barrier/adhesion layer shall be considered as a conductor (considering the layer thickness and relative conductivity) provided that the following conditions are satisfied: At least ten percent of the current is designed to be carried by this layer; and this layer is used in the current density calculations. When this occurs both the barrier/ adhesion layer and the principal conducting layer shall satisfy all of the step coverage requirements individually. Specimen examination shall be in accordance with 3.5 and the accept/reject criteria as defined in 3.7.1. The barrier/adhesion layer(s) shall be examined using either the SEM or optical microscope. The following methods may be used to examine these barrier/adhesion layers:

3.5.1.2.2.1 The Etchback procedure. This involves the stripping of each successive unique layer of metal by selective etching, with suitable etchants, layer by layer, to enable the examination of each layer. Typically, each successive layer of metal will be stripped in sequence to expose the next underlying layer for examination. Successive layer removal on a single die area may be impractical. In this case the wafer area or additional die (dice) immediately adjacent on the slice to the original die area shall be stripped to meet the requirement that all unique layers shall be exposed and examined.

3.5.1.2.2.2 In-line procedure. The wafer(s) shall be inspected for the defined accept/reject criteria immediately after being processed through each unique deposition and corresponding etching operation.

3.5.2 Passivation steps. Inspect the metallization at all types of passivation steps in accordance with the requirements of 3.5.1.1 and table II.

TABLE II. Examination procedure for specimens.

Device type	Area of examination	Examination	Minimum-maximum magnification	Photographic documentation 1/
Integrated circuit devices	Passivation steps (contact windows and other types of passivation steps) 2/	At least one of each type of passivation step present	5,000X to 20,000X	Two of the worst case passivation steps
	General metallization 2/	25 percent	1,000X to 6,000X	Worst case general metallization

1/ See 3.8 (an additional photograph may be required).
2/ See 3.7 for accept/reject criteria.

3.6 Acceptance requirements.

3.6.1 Single wafer acceptance basis. The metallization on a single wafer shall be judged acceptable only if all the sampled areas or dice from that wafer are acceptable.

3.6.2 Wafer lot acceptance basis. An entire wafer lot shall be judged acceptable only when all the sampled areas or dice from all sample wafers are acceptable. If a wafer lot is rejected in accordance with this paragraph each wafer from that wafer lot may be individually examined; acceptance shall then be in accordance with 3.6.1.

3.7 Accept/reject criteria. Rejection of dice shall be based on batch process defects and not random defects such as scratches, smeared metallization, tooling marks, etc. In the event that the presence of such random defects obscures the detailed features being examined, an additional adjacent sample shall be inspected. Illustrations of typical defects are shown in figures 2018-6 through 2018-22.

3.7.1 General metallization. Any evidence of poor metallization adhesion shall be unacceptable. Any defects (see figure 2018-18 and 2018-20), such as voids, cracks, separations, depressions, notches, or tunnels, which singly or in combination reduce the cross-sectional area of the general metallization stripe by more than 50 percent shall be unacceptable. Two specific cases of general metallization are specified below:

3.7.1.1 Conductor stripes. In the examination of the other metal layers for the specific case of conductor stripes (exclusive of the contact window area), a defect consuming 100 percent of the thickness of the barrier/adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe (see figure 2018-22).

3.7.1.2 Barrier layers in contact window areas. No defects of any kind in a barrier layer which would bring the overlying metal layer in contact with the semiconductor material surface shall be permitted.

3.7.1.3 Overlying adhesion layers. For the metal layer(s) above the principal conducting layer, a defect consuming 100 percent of the thickness of the adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe.

3.7.2 Passivation steps. Metallization over a passivation step shall be unacceptable if any combination of defects (see figure 2018-23) or thinning of the metal reduces the cross-sectional area of the metallization stripe along any cross-sectional plane in a major current-carrying direction to less than 50 percent of the cross-sectional area of the stripe. A 30 percent minimum acceptance criteria shall be allowed for metallization over a passivation step when the criteria of 3.7.2.1 through 3.7.2.3 are satisfied. Metallization over passivation steps nonperpendicular to the major current-carrying directional flow shall be projected onto cross-sectional planes perpendicular to the major current-carrying directional flow for purposes of calculating cross-sectional area reductions. In the absence of a visible edge or a smooth transition or taper which clearly shows effective coverage, the cross-sectional area percentage step coverage shall be verified by physical cross-sectioning or test structures. Verification of passivation step coverage for geometries $\leq$ 1.5 microns shall only be acceptable by using physical cross-sectioning or test structures.

3.7.2.1 Current density. The calculated current density is less than 2×10^5 A/cm^2.

3.7.2.2 Contact dimensions. The contact dimensions of any side or diameter are three microns or less.

3.7.2.3 Metallization coverage. The metallization covers at least 75 percent of the perimeter or circumference of the contact window, unless by design.

3.7.2.4 Nonrejectable cross-sectional area. In the event that the metallization cross-sectional area at a particular directional edge profile is less than 50 percent (or 30 percent when 3.7.2.1 through 3.7.2.3 have been met), this shall not be cause for rejection if the following two conditions occur:

3.7.2.4.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.4.2 Condition 2. Acceptance shall be on a single wafer basis only.

3.7.2.5 Nonrejectable, noncovered directional edge. For passivation steps to be acceptable, all directional edges shall be covered with metallization and be acceptable to the requirements of 3.7.2.4, unless by design. In the event that a directional edge profile of a particular type of passivation step is not covered with metallization, this shall not be cause for rejection if the following two conditions occur:

3.7.2.5.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.5.2 Condition 2. None of the other specimens from the sampled wafers representing the lot exhibit a directional edge profile from which metal is absent in the major current-carrying directional edge.

NOTE: If both 3.7.2.5.1 and 3.7.2.5.2 are satisfied, a wafer lot acceptance basis shall be used. However, if only 3.7.2.5.1 is satisfied, a single wafer acceptance basis shall be used.

3.7.3 Verification of potential rejects. At the option of the manufacturer, it shall be permissible to subject the specimen, or an adjacent sample that exhibits the same reject mode, to a verification test. Given below are some examples of suitable verification tests:

3.7.3.1 Cross-sectioning. A passivated sample shall be cleaved or lapped down to bisect the area of concern. The sample may then be subjected to an etchant that will remove the interconnecting metallization at the inspection surface (i.e., approximately perpendicular to the die surface). Specimens may be examined without any special surface coating if surface charging is not a significant problem and adequate resolution and signal-to-noise levels are obtained. If the specimens are coated, they shall be coated with a thin vapor-deposited or sputtered film of a suitable conductive material (i.e., 100Å gold). The coating deposition processes shall be controlled such that no artifacts are introduced by the coating. The sample shall be prepared (see 3.3) and examined in the SEM for interconnect metallization thickness or percentage coverage at the passivation step, or any other relevant parameter. Note: This cross-sectioning technique is not conclusive for hairline microcracks as they are not adequately filled by the passivation material.

3.7.3.1.1 Dimensional errors. Care must be taken to ensure that the cross-section is close to the center of a contact in order to avoid dimensional errors due to the rounding of the contact corners.

3.7.3.2 Surface etchback. The unpassivated sample surface is subjected to a chemical etch which removes the interconnection metallization from the surface of the die at a known controlled rate. The etching is stopped when the required metal thickness has been removed. The sample is then prepared (see 3.3) and examined within the SEM for residual metal at the passivation step/contact window interface. Photographic evidence shall then be taken of the sample(s) to support the acceptance or rejection of the material.

3.7.3.3 Topographical integration. A graphical representation of the worst case cross-sectional area is drawn to scale on appropriate graph paper from comprehensive photographs taken eucentrically about the directional edge. The cross-sectional area is then graphically integrated. This technique is useful for evaluating metallization with irregular surface topography.

3.8 Specimen documentation requirements. A minimum of three photographs for each layer of each level of metallization inspected per lot shall be taken and retained for a minimum of five years after performance of the inspection. Two photographs shall be of worst case passivation steps and the third photograph of worst case general metallization. If any photograph shows an apparent defect within the field of view, another photograph shall be taken to certify the extent of the apparent defect (see table II).

NOTE: Alternate methods of image storage (e.g., video disk or video tape) shall be acceptable with the prior approval of the qualifying activity.

3.8.1 Required information. The following information shall be traceable to each photograph:

a. Date of SEM photograph.

b. Device or circuit identification (type or part number).

c. Area of photographic documentation.

d. Electron beam accelerating voltage.

e. Magnification.

f. Manufacturer.

g. Manufacturer's lot identification number.

h. Record of calculated/measured percentage step coverage.

i. SEM operator or inspector's identification.

j. Viewing angle.

3.9 Disposition of inspected specimens. SEM samples and contiguous die shall not be shipped as functional devices unless nondestructive SEM conditions and requirements are met (see 3.10). In order to be considered nondestructive, suitable life-test data (see 3.11) shall be submitted for approval to the qualifying activity to substantiate the nondestructive aspects of the test (e.g., radiation hardness degradation-RHD). Additionally, all of the conditions in 3.10 and 3.11 must be satisfied.

3.10 Nondestructive SEM conditions. For nondestructive SEM, the following conditions shall apply:

3.10.1 Equipment conditions.

a. The accelerating voltage shall be within the 0.5 kV to 2.0 kV range.

b. The absorbed specimen current (as measured with a Faraday cup) shall be less than 500 pA.

c. Total scan time for each test site on the wafer shall not exceed ten minutes.

d. Resolution for metal inspection shall be in accordance with 2 above at the accelerating voltage of 3.10.1a. When used for other in-line nondestructive SEM evaluations (e.g., photoresist, critical dimension (cd) inspection, etc.) the resolution shall be sufficient to clearly verify the measurement.

3.10.2 Wafer conditions.

a. The wafer lot shall satisfy the thermal stability criteria defined within MIL-STD-883, method 5007, table I.

b. Weekly monitoring of particle counts shall be conducted in the SEM inspection area. The particle count limits shall be less than or equivalent to the specified wafer fab limits.

c. The wafer shall be clean and free of any surface coating.

* 3.11 Required data for nondestructive SEM validation. Data demonstrating that the method is nondestructive as defined in 40.3.2.2 of Appendix A of MIL-PRF 38535 shall be submitted to the qualifying activity following the procedure detailed in 3.11.1 through 3.11.3.

3.11.1 Sample conditioning. Expose a sufficient number of devices to the following conditions to yield a quantity of life test samples that meet a quantity (accept number) of 45(0) for each validation sample:

a. Sample A: Expose at the worst case SEM operating conditions (i.e., accelerating voltage, absorbed specimen current and tilt) and normal SEM metallization inspection procedure for a duration of 10 ± 1 minutes.

b. Sample B: Expose at the worst case SEM operating conditions and normal SEM metallization inspection procedure for an increased duration of 30 ± 3 minutes.

c. Sample C: (Optional at the discretion of the manufacturer.) Control group without any SEM exposure.

3.11.2 Procedure. Process test groups through all normal screening steps to complete post burn-in electricals, serialize test samples, and complete 3.11.2a through 3.11.2d.

a. Data log variables on all 25°C dc parameters and record attributes data for all other group A electrical test parameters, conditions and limits specified in the device specification or drawing (i.e., complete group A, not only specified life test endpoints).

b. Place test samples, including the control group if applicable, on life test in accordance with method 1005 at 125°C minimum for 1630 hours or equivalent (130°C for 1,135 hours, 135°C for 800 hours, 140°C for 565 hours, 145°C for 405 hours, 150°C for 295 hours, 155°C for 215 hours, 160°C for 155 hours, 165°C for 115 hours, 170°C for 85 hours, 175°C for 65 hours) with cooldown under bias using test condition C.

c. Repeat 3.11.2a for post life test endpoints.

d. Provide qualifying activity with one set of test results for each sample in terms of variables and attributes data on pre and post life test endpoints plus analysis of mean and standard deviation of variables data and indication of any devices which failed any group A test parameters.

3.11.3 Criteria for validating SEM as nondestructive. If sample A passes single duration and sample B passes triple duration SEM exposure and life test without failing any device specification or drawing parameters, conditions and limits (or delta parameter requirements when they are specified), the SEM procedure shall be validated as nondestructive for the process flow represented by the sample devices and for other devices from the same process flow. With the approval of the qualifying activity, this SEM nondestructive qualification may be performed on appropriate process monitor structures or standard evaluation circuits (SEC's) which represent the process flow.

4. SUMMARY. The following details may be specified in the applicable acquisition document:

4.1 Detail 1. Single wafer acceptance basis when required by the acquiring activity.

4.2 Detail 2. Requirements for photographic documentation (number and kind) if other than as specified in 3.8.

NOTES:

1. Cross-sectional planes are denoted by dashed lines.
2. All passivation steps nonperpendicular to current flow must be projected onto cross-sectional planes perpendicular to current flow for purpose of cross-sectional area calculations.
3. The purpose of this cross-sectional plane illustration is two-fold:

   To provide a consistent and convenient means to facilitate the calculation of the appropriate cross-sectional area.

   To insure that the cross-sectional area of the metallization in a major current carrying direction is reduced to no more than 50 percent (30 percent when appropriate) for the topographical variation under consideration.

FIGURE 2018-1. Cross-sectional planes at various passivation steps.

NOTES:
1. 1, 2, 3, and 4 are directional edges.
2. 1 is a major current carrying edge.

FIGURE 2018-2. Directional edge.

FIGURE 2018-3. Viewing angle.

STATIONARY WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I).

One wafer lot

Two wafer lots

Three wafer lots

Four wafer lots

ROTATING AND PLANETARY WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I) - Continued.

FIGURE 2018-5. Viewing direction.

FIGURE 2018-6. (3,400X).
Voiding at passivation step (accept).

FIGURE 2018-7. 5,000X.
Voiding at passivation step (reject).

NOTE: Tunnel does not extend to surface of metal; does not reduce cross-sectional area more than 50 percent.

FIGURE 2018-8. (10,000X).
Tunnel/cave at passivation step (accept).

FIGURE 2018-9. 5,000X.
Tunnel/cave at passivation step (reject).

FIGURE 2018-10. (10,000X).
Separation of metallization at
passivation step (base contact) (accept).

FIGURE 2018-11. 7,000X.
Separation of metallization at
passivation step (base contact) (reject).

FIGURE 2018-12. (6,000X).
Crack-like defect at passivation step (accept).

FIGURE 2018-13. 6,000X.
Crack-like defect at passivation step (reject).

FIGURE 2018-14. (7,200X).
Thinning at passivation step with more than 50 percent of cross-sectional area remaining at step (multi-level metal) (accept).

FIGURE 2018-15. 7,200X.
Thinning at passivation step with less than 50 percent of cross-sectional area remaining at step (multi-level metal) (reject).

FIGURE 2018-16. (6,000X).
Steep passivation step (MOS) (accept).

FIGURE 2018-17. 9,500X.
Steep passivation step (MOS) (reject).

FIGURE 2018-18. (5,000X).
Peeling or lifting general metallization
in contact window area (reject).

FIGURE 2018-19. 10,000X.
General metallization voids (accept).

FIGURE 2018-20. (5,000X).
General metallization voids (reject).

FIGURE 2018-21. 5,000X.
Etch-back/undercut type of notch at
passivation step (multi-layered metal) (accept).

FIGURE 2018-22. (5,000X). Barrier or adhesion layer etch-back/undercut type of notch at passivation step (multi-layered metal) (accept).

METALLIZATION AT PASSIVATION
STEP SHOWING TYPICAL DEFECTS

CROSS-SECTION AREA (ENLARGED) OF METALLIZATION
AT PASSIVE STEP SHOWN ABOVE

FIGURE 2018-23. Concept of reduction of cross-sectional area of metallization as accept/reject criteria (any combination of defects and thinning over a step which reduces the cross-sectional area of the metal to less than the percentage defined within 3.7.2 of metal cross-sectional area as deposited on the flat surface) is cause for rejection.

APPENDIX A

Metal integrity alternate to SEM inspection

10. PURPOSE. Metal integrity is achieved through a system of designing and building in quality and reliability. It is not practical or cost effective to rely solely on end-of-line testing to ensure metal integrity. This procedure provides a system for designing, building, and monitoring a metal system that withstands the operating conditions of the device for the specified lifetime.

20. SCOPE

20.1 Utilization of this method provides an alternate to the requirements defined in TM2018. This procedure must be used in conjunction with the requirements of alternate 2 of TM5004, paragraph 3.3.1 as it applies to metallization.

20.2 This procedure describes a method by which metal integrity is assured through a combination of design rules and techniques, process development, manufacturing controls and end-of-line screening and reliability testing.

20.2.1 Design controls.

a. Reliability rules.

b. Layout rules.

c. Rules checking.

d. Process development.

20.2.2 Manufacturing controls. Statistical control of the manufacturing process and equipment defect and foreign material control.

20.2.3 Reliability testing. Accelerated tests.

30. DEFINITIONS

Lifetime. The mean time to failure of a technology at operating conditions defined to be normal. The mean time to failure is measured on a large sample of devices stressed at temperatures and current densities well above the normal operating conditions and extrapolated to normal operating temperature and current density.

* Current density. The maximum allowable current density calculated as described in appendix A of MIL-PRF-38535.

Specification limits. Minimum or maximum boundaries for the value of a measured parameter. Material whose measured values are beyond these boundaries must be reviewed and dispositioned.

Worst case operating conditions. Conditions of current and temperature at which a device would normally operate, that would result in the greatest likelihood of failure.

APPENDIX A

40. REQUIREMENTS

40.1 Design controls. Design includes device design and process development. Device design includes all steps and supporting systems needed to translate a functional description for a device into a pattern generating data base. Process development includes selection of materials, tooling, and process conditions that may significantly affect metal integrity. The design process is a major consideration in establishing metal integrity.

* 40.1.1 A manufacturer's design system must include controlled, documented rules based on the manufacturer's processing capabilities. These rules shall specify feature size and spacing requirements, taking into account size changes that occur during processing. Manufacturers shall be able to justify their rules based on expected process variations. In addition, documented reliability rules shall exist which establish the electrical characteristics for each technology, taking into account processing materials, tolerances and limitations. The manufacturer shall have a system for checking designs for rule violations, and a system for correcting violations. Design rules shall consider the maximum current density (calculated as described in appendix A of MIL-PRF-38535) which shall be determined using worst case operating conditions and taking into consideration current crowding at contacts and vias. The manufacturer shall ensure that worst case processing conditions (such as alignment, metal thickness, line width, and contact/via size) do not result in violation of current density. Current density for a technology shall be at a level such that there is sufficient margin to ensure that failure will not result from electromigration in the specified lifetime of the device.

40.1.2 Process development. The manufacturer's design must take into consideration known levels of defects in the process. The process developed by the manufacturer must produce metallization that has the electrical and mechanical properties consistent with the design rules of 40.1.1, and reliability goals for the technology. Mechanical stress in the metal after final processing shall be understood. The manufacturer shall demonstrate, with results from appropriate designed experiments, that the desired electrical and mechanical properties have been achieved, and that the interaction of other process parameters on metal integrity parameters (minimum list in 40.2) is understood. The initial process specification limits shall be chosen such that metal integrity parameters are within the capability of the process. The manufacturer shall have a change control system in place such that new or changed processes are not put into production without the appropriate reliability evaluation.

* 40.2 Manufacturing controls. The manufacturer shall establish manufacturing controls in order to achieve uniformly good quality and reliability in their metal system, and to assure that the product is being manufactured according to the assumptions made during design. The manufacturer shall determine which parameters are critical to metal integrity and control those parameters in accordance with EIA 557. The manufacturer shall be able to demonstrate control of metal thicknesses, step coverage and cross-sectional areas, metal line width, contact and via sizes, contact and via resistance, and sheet resistance as a minimum, and show that they are being controlled to limits that are consistent with the way the metal system was designed. Specification limits shall be established for these parameters. In addition, defects that threaten metal integrity must be controlled in accordance with the alternate visual procedure (alternate 2) in appendix A of TM5004.

40.3 Reliability testing. While it is desirable to design in and build in reliability rather than to achieve reliability by screening finished product, there is valuable information to be gained from screening and reliability testing. Screening test such as burn-in not only eliminate the weaker parts in a population, but also provide information on failure mechanisms which can be used to improve design, materials, processes, or electrical test. Similarly, accelerated testing is used to speed up failure mechanisms likely to occur under normal operating conditions of a device. These failure mechanisms can then be analyzed to provide a basis for improvement. Accelerated test that a manufacturer may use to this end include but are not limited to electromigration testing, life testing, temperature-humidity-bias testing, and temperature cycling. Structures used in accelerated test must be typical of the technology represented. Failure mechanisms experienced during accelerated testing must be typical of those experienced during normal use of the device.

APPENDIX A

40.3.1 Reliability evaluating. The manufacturer must have in place a system for evaluating the reliability of the metal system. The system shall enable the manufacturer to determine the probability of failure in a given lifetime. The lifetime and failure rate data of the metal system associated with a given technology shall be made available to the customer. The manufacturer's systematically collected data must indicate that there is a high probability of meeting the specified lifetimes and/or failure rates.

50. DOCUMENTATION

NOTE: Certain information considered proprietary may only be available under non-disclosure agreement.

50.1 The manufacturer must have available for customer review controlled reliability rules, layout rules, and current density for each technology for which this procedure is used. In addition, the manufacturer must have available for review the method by which the above rules are checked and verified.

50.2 The manufacturer shall be able to demonstrate the manufacturing controls and system for disposition of out of control occurrences that are in place to control the processes determined critical to metal integrity.

50.3 The manufacturer must have available for customer review any testing performed to evaluate the reliability of the metal system.

50.4 The manufacturer shall specify the metal lifetime to the customer upon request.

METHOD 2019.5

DIE SHEAR STRENGTH

1. PURPOSE. The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. APPARATUS. The test equipment shall consist of a load-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is the greater tolerance. A circular dynamometer with a lever arm or a linear motion force-applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

a. A die contact tool which applies a uniform distribution of the force to an edge of the die (see figure 2019-1).

b. Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die; i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2019-2).

d. A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing.

3. PROCEDURE. The test shall be conducted, as defined herein, or to the test conditions specified in the applicable specific acquisition document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

3.1 Shear strength. A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (figure 2019-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.

b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

c. The die contact tool shall load against an edge of the die which most closely approximates a 90° angle with the base of the header or substrate to which it is bonded (see figure 2019-3).

d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.c are met.

3.2 Failure criteria. A device which fails any of the following criteria shall constitute a failure.

a. Fails die strength requirements (1.0X) of figure 2019-4.

b. Separation with less than 1.25 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 50 percent adhesion of the die attach medium.

c. Separation with less than 2.0 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 10 percent of adhesion of the die attach medium.

NOTE: For eutectic die attach, residual silicon attached in discrete areas of the die attach medium shall be considered as evidence of such adhesion. For metal glass die attach, die attach material on the die and on the package base shall be considered as evidence of acceptable adhesion.

3.2.1 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be recorded.

a. Shearing of die with residual silicon remaining.

b. Separation of die from die attach medium.

c. Separation of die and die attach medium from package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum die attach strength if other than shown on figure 2019-4.

b. Number of devices to be tested and the acceptance criteria.

c. Requirement for data recording, when applicable (see 3.2.1).

FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle ≈ 90° with the header/substrate.

NOTES:

1. All die area larger than 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force of 2.5 kg or a multiple thereof (see 3.2).

2. All die area smaller than 5 x 10^{-4} $(IN)^2$ shall withstand a minimum force (1.0X) of 0.04 kg/10^{-4} $(IN)^2$ or a minimum force (2X) of 0.08 kg/10^{-4} $(IN)^2$.

FIGURE 2019-4. Die shear strength criteria (minimum force versus die attach area).

METHOD 2020.7

PARTICLE IMPACT NOISE DETECTION TEST

1. PURPOSE. The purpose of this test is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer.

2. APPARATUS. The equipment required for the particle impact noise detection (PIND) test shall consist of the following (or equivalent):

a. A threshold detector to detect particle noise voltage exceeding a preset threshold of the absolute value of 20 ±1 millivolt peak reference to system ground.

b. A vibration shaker and driver assembly capable of providing essentially sinusoidal motion to the device under test (DUT) at:

(1) Condition A: 20 g peak at 40 to 250 Hz.

(2) Condition B: 10 g peak at 60 Hz minimum.

c. PIND transducer, calibrated to a peak sensitivity of -77.5 ±3 dB in regards to one volt per microbar at a point within the frequency of 150 to 160 kHz.

d. A sensitivity test unit (STU) (see figure 2020-1) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ±20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.

e. PIND electronics, consisting of an amplifier with a gain of 60 ±2 dB centered at the frequency of peak sensitivity of the PIND transducer. The noise at the output of the amplifier shall not exceed 10 mV peak.

f. Attachment medium. The attachment medium used to attach the DUT to the PIND transducer shall be the same attachment medium as used for the STU test.

g. Shock mechanism or tool capable of imparting shock pulses of 1,000 ±200 g peak to the DUT. The duration of the main shock shall not exceed 100 μs. If an integral co-test shock system is used the shaker vibration may be interrupted or perturbed for period of time not to exceed 250 ms from initiation of the last shock pulse in the sequence. The co-test duration shall be measured at the 50 ±5 percent point.

3. PROCEDURES.

3.1 Test equipment setup. Shaker drive frequency and amplitude shall be adjusted to the specified conditions. The shock pulse shall be adjusted to provide 1,000 ±200 g peak to the DUT.

3.2 Test equipment checkout. The test equipment checkout shall be performed a minimum of one time per operation shift. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.

3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency and the shaker amplitude specified. The drive system shall be calibrated so that the frequency settings are within ±8 percent and the amplitude vibration setting are within ±10 percent of the nominal values. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between 0.04 and 0.12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of 0.040 inch (1.02 mm).

3.2.2 Detection system checkout. With the shaker deenergized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the attachment medium used for testing the devices. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope. Not every application of the STU will produce the required amplitude. All pulses which are greater than 20 mV shall activate the detector.

3.2.3 System noise verification. System noise will appear as a fairly constant band and must not exceed 20 millivolts peak to peak when observed for a period of 30 to 60 seconds.

3.3 Test sequence. The following sequence of operations (a through i) constitute one test cycle or run.

a. 3 pre-test shocks.

b. Vibration 3 ±1 seconds.

c. 3 co-test shocks.

d. Vibration 3 ±1 seconds.

e. 3 co-test shocks.

f. Vibration 3 ±1 seconds.

g. 3 co-test shocks.

h. Vibration 3 ±1 seconds.

i. Accept or reject.

3.3.1 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT.

Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the largest flat surface against the transducer at the center or axis of the transducer for maximum sensitivity. Where more than one large surface exists, the one that is the thinnest in section or has the most uniform thickness shall be mounted toward the transducer, e.g., flat packs are mounted top down against the transducer. Small axial-lead, right circular cylindrical parts are mounted with their axis horizontal and the side of the cylinder against the transducer. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

(1) Low mass.

(2) High acoustic transmission (aluminum alloy 7075 works well).

(3) Full transducer surface contact, especially at the center.

(4) Maximum practical surface contact with test part.

(5) No moving parts.

(6) Suitable for attachment medium mounting.

3.3.2 Test monitoring. Each test cycle (see 3.3) shall be continuously monitored, except for the period during co-test shocks and 250 ms maximum after the shocks. Particle indications can occur in any one or combinations of the three detection systems as follows:

a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.

b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.

c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.

3.4 Failure criteria. Any noise bursts as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods shall be cause for rejection of the device. Rejects shall not be retested except for retest of all devices in the event of test system failure. If additional cycles of testing on a lot are specified, the entire test procedure (equipment setup and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

3.5 Screening lot acceptance. Unless otherwise specified, the inspection lot (or sublot) to be screened for lot acceptance shall be submitted to 100 percent PIND testing a maximum of five times in accordance with condition A herein. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices in that run is less than 1 percent. All defective devices shall be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected and resubmission is not allowed.

TABLE I. Package height vs. test frequency for 20 g acceleration (condition A).

Average internal cavity height		Frequency
Mils	mm	Hz
<40	<1.02	130
41-50	1.03-1.27	120
51-60	1.28-1.52	110
61-70	1.53-1.78	100
71-80	1.79-2.03	90
81-90	2.04-2.29	80
91-100	2.30-2.54	70
>100	>2.54	60

NOTE: The approximate average internal package height shall be measured from the floor of the package cavity or the top of the major substrate for hybrid or multichip assemblies and shall exclude the thickness of the die mounted inside the package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test condition letter A or B.

   b. Lot acceptance/rejection criteria (if other than specified in 3.5).

   c. The number of test cycles, if other than one.

   d. Pre-test shock level and co-test shock level, if other than specified.

NOTES:

1. Pushbutton switch: Mechanically quiet, fast make, gold contacts. E.G. T2 SM4 microswitch.
2. Resistance tolerance 5 percent noninductive.
3. Voltage source can be a standard dry cell.
4. The coupled transducers must be coaxial during test.
5. Voltage output to STU transducer 250 microvolts, ±20 percent.

FIGURE 2020-1 Typical sensitivity test unit.

METHOD 2021.3

GLASSIVATION LAYER INTEGRITY

1. PURPOSE. The purpose of this test is to assess the structural quality of deposited dielectric films (e.g., CVD, sputtered or electron beam evaporated glass or nitride, etc.) over aluminum metallized semiconductor devices or microcircuits. The test is directed at identifying process and materials related glass layer defects which result in localized contamination buildup and loss of the advantage given to properly glassivated devices in terms of electromigration behavior at elevated temperature and current density. This is a destructive test.

2. APPARATUS. The apparatus for this test shall consist of suitable sample handling and chemical etching facilities as required for personnel safety. Standard optical microscopes such as those employed in method 2010 shall be used for device inspection. Standard A.C.S. Reagent Grade chemicals shall be used as etchant materials.

3. PROCEDURE. Unless otherwise specified, this test shall be applied to devices which have been through the complete assembly cycle including final package seal. Packaged devices shall be mechanically delidded with minimum thermal stresses applied. Unless otherwise specified, the test sample shall consist of a minimum of one device selected randomly from the inspection lot. One of the following etching procedures shall be used.

3.1 Procedure A. Delidded sample devices shall be completely immersed in the following aluminum etch:

40 Volumes H_3PO_4 (85%)

19 Volumes H_20

4 Volumes HNO_3 (70%)

This solution shall be maintained at a temperature of 50°C ±5°C.

Devices shall be examined during the etching procedure with an optical system, such as a monocular, binocular or stereomicroscope compatible with observation of the immersed samples. Devices shall be etched for twice the amount of time required to completely remove aluminum metallization from exposed bonding pads.

Properly etched devices shall be removed from the heated solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

3.2 Procedure B. Delidded sample devices shall be completely immersed for 20 to 30 minutes at room temperature in the following aluminum etch:

5 Volumes $HN0_3$ (70%)

80 Volumes H_3P0_4 (85%)

5 Volumes Acetic Acid

10 Volumes Deionized Water

NOTE: The use of a commercial equivalent (e.g., Mity Etch 2) is acceptable.

Properly etched devices shall be removed from the solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

FIGURE 2021-1. Category A - missing glassivation over aluminum.

FIGURE 2021-2. Category B - cracks in glass over aluminum.

FIGURE 2021-3. Category C - cracks in glass or improper glass coverage along edge of aluminum.

FIGURE 2021-4. Category D - pinholes in glass on top surface and edges of aluminum.

3.2.1 Failure criteria. Lot rejection shall be based on the appearance of etched aluminum, as shown on figures 2021-1 to 2021-7, at any location other than along the edges immediately adjacent to intentionally unglassed areas (e.g., bonding pads, die edge, scribe line, etc.) (see 4). This criteria shall be applied only to the interconnect levels which exceed a calculated current density of 2×10^5 A/cm^2. Category C and D defects, shown on figures 2021-3, -4, -6, and -7 shall not be a cause for rejection unless aluminum is completely removed from the entire width of the conductor stripe. Etched aluminum is determined by changes in the reflecting properties or transparent appearance of areas normally covered with glassivated aluminum.

Failures shall be recorded in terms of the number of devices tested (if other than one) and the number of failures by failure category as defined below:

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. When applicable, any intentional omission of glass over the aluminum metallization layer (see 3.1).

   b. If applicable, specific magnification requirements other than as stated in 3.

   c. Sample size if other than one (see 3).

   d. If applicable, special reporting requirements (see 3.1).

FIGURE 2021-5. Etched device exhibiting failure category A missing glass over aluminum.

FIGURE 2021-6. Etched device exhibiting failure categories,
B - Cracks in glass over aluminum,
C - Cracks in glass or improper glass,
coverage along edge of aluminum.

FIGURE 2021-7. Etched device exhibiting category D defects pinholes in glass over aluminum.

METHOD 2022.2

WETTING BALANCE SOLDERABILITY

1. PURPOSE. The purpose of this test method is to determine the solderability of all ribbon leads up to 0.050 inch (1.27 mm) in width and up to 0.025 inch (0.64 mm) in thickness which are normally joined by a soldering operation and used on microelectronic devices. This determination is made on the basis of the wetting time and wetting force curve produced by the specimen while under test.

These processes will verify that the treatment used in the manufacturing process to facilitate soldering is satisfactory and that it has been applied to the required portion of the part which is designated to accommodate a solder connection.

2. APPARATUS.

2.1 Solder meniscus force measuring device (wetting balance). A solder meniscus force measuring device (wetting balance) which includes a temperature- controlled solder pot containing approximately 750 grams of solder shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified in 3.4. The meniscograph apparatus also includes a strip chart recorder which records the force curve for the device tested.

2.2 Dipping device. A mechanical dipping device is incorporated in the Meniscograph, and is preset to produce an immersion and emersion rate as specified in 3.4. The specimen dwell time is operator controlled to the time specified in 3.4.

2.3 Container and cover. A noncorrodable container of sufficient size to allow the suspension of the specimens 1.5 inches (38.10 mm) above the boiling distilled or deionized water shall be used. (A 2,000 ml beaker is one size that has been used satisfactorily for smaller components.) The cover shall be of one or more noncorrodable plates and shall be capable of covering approximately .875 of the open area of the container so that a more constant temperature may be obtained. A suitable noncorrodable method of suspending the specimens shall be improvised. Perforations or slots in the plates are permitted for this purpose.

2.4 Materials.

* 2.4.1 Flux. The flux shall conform to flux type symbol "A" (flux type "L0") of ANSI/J-STD-004 (previously designated as type "R" of MIL-F-14256).

* 2.4.2 Solder. The solder shall conform to type Sn63A or Pb37A (previously designated as Sn63 in QQ-S-571) or type Sn60A or Pb40A (previously designated as Sn60 in QQ-S-571).

3. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the applicable acquisition document. During handling, care shall be exercised to prevent the surface to be tested from being abraded or contaminated by grease, perspirants, etc. The test procedure shall consist of the following operations:

a. Proper preparation of the terminations (see 3.1), if applicable.

b. Aging of all specimens (see 3.2).

c. Application of flux and immersion of the terminations into molten solder (see 3.3 and 3.4).

d. Examination and evaluation of the recordings upon completion of the solder-dip process (see 3.5).

3.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the applicable acquisition document.

3.2 Aging. Prior to the application of the flux and subsequent solder dips, all specimens assigned to this test shall be subjected to aging by exposure of the surfaces to be tested to steam in the container specified in 2.3. The specimens shall be suspended so that no portion of the specimen is less than 1.5 inches (38.10 mm) above the boiling distilled or deionized water with the cover specified in 2.3 in place for 4 to 8 hours. In effect while the manufacturer may accept on the basis of 4 hours aging, the customer/user shall be able to reject on the basis of results after 8 hours aging. Means of suspension shall be a nonmetallic holder. If necessary, additional hot distilled water may be gradually added in small quantities so that the water will continue to boil and the temperature will remain essentially constant.

3.3 Application of flux. Flux, type R shall be used (see 2.4.1). Terminations shall be immersed in the flux, which is at room ambient temperature, to the minimum depth necessary to cover the surface to be tested. Unless otherwise specified in the applicable acquisition document, terminations shall be immersed to 0.16 inch (4 mm) from end of lead. The surface to be tested shall be immersed in the flux for a period of from 5 to 10 seconds.

3.4 Solder dip. The dross and burned flux shall be skimmed from the surface of the molten solder specified in 2.4.2. The molten solder shall be maintained at a uniform temperature of 245 ±5°C. The surface of the molten solder shall be skimmed again just prior to immersing the terminations in the solder. The part shall be attached to a dipping device (see 2.2) and the flux-covered terminations immersed once in the molten solder to the same depth specified in 3.3. The immersion and emersion rates shall be 1 ±.25 inches (25.40 ±6.35 mm) per second and the dwell time in the solder bath shall be 5 ±0.5 seconds.

3.5 Evaluation of resultant meniscograph curves from testing of microelectronic leads. The criteria for acceptable solderability during the evaluation of the recordings are:

a. That the recorded signal trace crosses the zero balance point at or before 0.59 seconds of test time.

b. That the recorded signal trace reaches two-thirds of its maximum value in 1 second or less of test time (see figure 2022-1).

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. The number of terminations of each part to be tested (see 3).

b. Special preparation of the terminations, if applicable (see 3.1).

c. Depth of immersion if other than 0.16 inch (4 mm) (see 3.3).

d. Solder dip if other than specified in 3.4.

e. Evaluation of meniscograph curves if other than specified in 3.5.

f. Solder composition, flux, and temperature if other than those specified in 2.4 and 3.4.

g. Number of cycles, if other than one. Where more than one cycle is specified to test the resistance of the device to heat as encountered in multiple solderings, the examinations and measurements required shall be made at the end of the first cycle and again at the end of the total number of cycles applied. Failure of the device on any examination and measurement at either the one-cycle or the end-point shall constitute failure to meet this requirement.

FIGURE 2022-1. Wetting balance curve evaluation criteria.

METHOD 2023.5

NONDESTRUCTIVE BOND PULL

1. PURPOSE. The purpose of this method is to reveal nonacceptable wire bonds while avoiding damage to acceptable wire bonds. This procedure is applicable for all bonds made by either ultrasonic or thermal compression techniques, except those larger than 0.005 inch diameter (or equivalent cross section area) which do not have sufficient clearance to permit use of a hook.
The alternate procedure defined in 3.2 may be used for devices with packages having 84 or more external terminations and with nominal bonding wire pitch at the package post of less than or equal to 12 mils.

2. APPARATUS. The apparatus of this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ±5 percent or ±0.3 gf, whichever is greater.

a. The diameter of the wire used to make the hook utilized to apply force to the interconnect wire shall be as follows:

Wire diameter	Hook diameter (x wire dia)
≤ 0.002 inch	2.0 x min
> 0.002 inch - ≤ 0.005 inch	1.5 x min
> 0.005 inch	1.0 x min

For ribbon wire, use the equivalent round wire diameter which gives the same cross sectional area as the ribbon wire being tested. Flat portion of hook (horizontal) shall be ≥1.25 x the diameter of the wire being tested.

b. The hook shall be smooth and free of defects which could compromise the test results or damage the wire being pulled.

c. Travel speed of the hook shall be controlled to that impact loading as the hook initially contacts the wire shall be no more than 20 percent of the specified nondestructive bond pull force.

d. Final hook placement shall be accomplished under observation at 15X minimum magnification. A microscope with a zoom capability may be used for indexing the hook.

e. The fixturing which holds the package shall allow positioning the hook for optimum force application to the wire.

f. An indicator shall either (1) measure the force required to cause failure of the interconnect; or (2) provide visual indication that the predetermined load has been applied.

g. The hook shall be in a fixed position which restricts motion along a straight line between each bond, so that it will not rise to the highest point which could result in a test for only one bond (e.g., as for a ball bond).

3. PROCEDURE. The test shall be conducted as specified in the applicable acquisition document, as a sample or as a screen, and shall be consistent with the particular bond materials and construction. All bond wires in each device shall be pulled and counted, and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Where there is any adhesive, encapsulant or other material under, on, or surrounding the wire such as to increase the apparent bond strength, the test shall be performed prior to the application of the material.

a. Set the rate of force application.

b. Mount the specimen to be tested and set the lifting mechanism to apply the specified force for the appropriate wire size and material.

c. The device shall be rotated and positioned such that the hook contacts the wire between midspan and loop apex (for forward wedge and ball bonding, this would be between midspan and die edge; for reverse bonding, this would be between midspan and package edge) and the pulling force is applied in a direction approximately normal to the die or substrate, or *approximately normal to a straight line between the bonds. The manufacturer* should pull as close to midspan as possible without causing adverse wire deformation.

d. The lifting mechanism shall be actuated to stress the wire bond such that the specified stress is applied with minimum impact loading and with no overshoot greater than specified accuracy of the indicator at any time during the bond pull. The dwell time of maximum force application shall be a maximum of one second.

e. Observe whether the bond breaks.

f. If the bond breaks, reject the device and proceed to the next device, unless rework is acceptable. If so, record the identification of the broken bond and the device containing the bond. If rework is permitted, all bonds shall be tested prior to any bond rework and reworked bonds shall be tested.

g. If no bonds on the device break, accept the device as satisfactory.

h. Repeat a through g for all bonds to be tested.

i. Record the total number of wires or wire bonds that fail when subjected to the predetermined stress.

j. Record the number of devices that failed the test.

3.1 Failure criteria. Any bond pull which results in separation (of bonds at the bond interface or breakage of the wire or interconnect anywhere along the entire span including bond heels) at an applied stress less than the specified stress for the applicable material and construction shall constitute a failure. Unless otherwise specified, the applied nondestructive pull stress shall be 80 percent of the preseal minimum bond strengths for the applicable material, size and construction given in table I of method 2011 or figure 2011-1 of method 2011. Table I herein lists pull force values for commonly used wire sizes.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$V_1 = V_2 \sin \theta$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
θ = Greatest calculated wire loop angle (figure 2023-1).

Also, RF/microwave hybrids that contain tuning wires (designated wires that will alter RF performance when moved) or wires that cannot be accessed with a pull hook must be simulated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, schedule, and elements (electrical rejects may be used). The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2023-2).

TABLE I. Nondestructive pull forces.

AL and AU wire diameter (inches)	Pull force (gf) AL	Pull force (gf) AU
0.0007	1.2	1.6
0.0010	2.0	2.4
0.00125	2.5	3.2
0.0013	2.5	3.2
0.0015	3.0	4.0
0.0030	9.5	12.0

NOTES:
1. Nondestructive pull force values for wire sizes not specified shall be 80 percent of the preseal pull forces for aluminum or gold wire given in method 2011.
2. Tolerances shall be ±0.3 gf for pull forces up to 6 gf and ±5 percent for pull forces above 6 gf.
3. Any bond subjected to a nondestructive pull force exceeding the specified pull force and the positive tolerance shall be eliminated and not counted toward the PDA failures.

3.2 Alternative procedure. This alternate procedure may be used where 100 percent non-destructive bond pull cannot be performed because of high pin count (greater than or equal to 84 terminals) and small bonding wire pitch at the package post (less than or equal to 12 mils).

* 3.2.1 In-process controls. In order for a manufacturer to use the alternate procedure, a SPC program shall be implemented for the wire bond operation in accordance with EIA-557-A, Statistical Process Control Systems. Any change in the various effects shown to be significant by the characterization with respect to wire bond strength shall require a re-characterization of the wire bonding process for the changed effect(s) on wire bond integrity. For QML, the SPC program and the requirements listed herein shall be approved by the qualifying activity and may be subject to an audit at any time by the government qualification activity. For Non-Jan devices, the SPC program and the requirements listed herein are subject to review by the government agency responsible for the acquisition or their designee. All statistical evaluation, characterizations, and designed experiments shall be available for review.

* 3.2.1.1 Applicable incoming materials. Applicable incoming materials including wafer pad metallization targets, package bonding post, and bonding wire shall have their critical characteristics determined and made requirements for acceptance using either incoming inspection or vendor SPC data. Critical characteristics shall include possible sources of material contamination (e.g. excessive carbon content in aluminum wire). Also, the applicable incoming inspection requirements of MIL-PRF-38535 or MIL-PRF-38534 shall apply.

3.2.1.2 Applicable manufacturing processes. Applicable manufacturing processes including bond pad metal disposition, glassivation etch, and worst case package seal excursion shall have their critical characteristics determined and placed under SPC control. Also, the process control requirements of the applicable general specification shall apply for these operations including contamination controls, preventative maintenance procedures and schedules, and complete removal of glassivation from the bonding pad.

3.2.1.3 For packages with gold plated posts. For packages with gold plated posts, the device manufacturer shall perform a bake test on one device from each incoming package lot. This test shall evaluate for basic plating or contamination anomalies of the package post. The package shall be wire bonded post-to-post. The wire bonded package shall be baked at 300 degrees celsius for 1 hour in either air or inert atmosphere. Bond strength shall then be tested in accordance with MIL-STD-883, method 2011, using a sample size number = 45, C = 0 on the number of wires pulled. If any bond strength failure is determined to be package plating or contamination related then the package lot shall not be used for this alternative unless the defect can be effectively screened and the package lot resampled to a tightened sample size number = 76, C = 0 for the number of wires pulled.

3.2.1.4 An active foreign material control program. An active foreign material control program shall be in accordance with MIL-STD-883, method 2010 or method 2017. A procedure and system for storing and handling wafers, packages, related piece parts, and unsealed devices that will prevent contamination through package seal including face masks, lint free gloves, restrictions on particle generating make-up, hair covers, and cleanroom gowns.

3.2.1.5 A 100 percent pre-bond visual inspection procedure. A 100 percent pre-bond visual inspection procedure of the die pads and package post shall be documented. The visual inspection shall be performed at 100-200X in a class 100 environment. Cleaning to remove rejectable contamination is allowed. No device shall exhibit evidence of the following criteria:

a. Glassivation on the designed open contact area of the bond pads.

b. Chemical, film, photoresist or liquid contamination on the pads or posts.

c. Particulate and /or foreign material contamination on the pads or the critical bond area of the posts greater than 0.25 mils in diameter.

d. Die pads and package posts that do not meet all applicable requirements of MIL-STD-883, method 2010, condition A or method 2017.

NOTE: 100 percent pre-bond visual inspection may be waived by the qualifying activity provided a 100 percent pre-clean of pads and posts is performed, and all pads and posts for five (5) randomly selected devices pass the inspection criteria. Precleaning may also be waived by the qualifying activity if historical data demonstrates the cleaning is unnecessary. No cleaning is allowed during sample inspection. A 100 percent pre-clean and sample inspection of 5(0) may be repeated a maximum of two times. Rejection of the sample after the second pre-clean shall result in a 100 percent pre-bond inspection of the lot in accordance with 3.2.1.5. An investigation of the rejects in the lot and sample shall be required and corrective action, as necessary shall be instituted. Until then, 100 percent pre-bond inspection is required. Once the effectiveness of any corrective action has been determined, the 100 percent pre-bond inspection may be eliminated.

3.2.1.6 Bonding machine parameters. Bonding machine parameters (e.g., temperatures, pressure, timing, fixtures, wire size, wire material, height settings, etc.) must be defined for each die/package combination. The bonding equipment parameters ranges shall be optimized by designed experiments. The experiments shall consider variations in bonding wire geometry (e.g., loop height, wire length, shelf height, etc.). The experiments shall establish the predicted strength and tolerance of the bonding operation. The allowable performance ranges of the bonding parameters determined by controlled experiments shall be documented. Equipment parameter changes outside the allowable limits must be evaluated and documented as to still meeting the predicted wire pull strength and tolerance.

Note: ASTM Standards F 458 and F 459 may be used as guideline documents.

3.2.1.7 Process capability study. After the wirebond process has been demonstrated to be in a condition of stability and statistical control, a process capability study shall demonstrate that the probability of any device failing the minimum post-seal bond strength is P <.0001. The probability must meet the accumulative probability at the device level and not at the individual wire level. The distributional form of the post-seal bond strengths shall be statistically evaluated for conformance to the selected sampling distribution (e.g., Gaussian, lognormal, Wiebull, etc.). The capability study sample size shall be sufficient to detect a shift in the distribution of the worst case package/die combination to a 100 parts per million level. The beta risk to the consumer shall be .001 or less. (See Appendix A for normal distribution example.) The process capability study shall be performed periodically. The capability study may be accomplished by characterizing the wire pull strengths of one or more worst case package/die combinations. Selection of the worst case package/die combinations should consider wire geometry, number of wires, pads and post sizes, etc. The characterization results from worst case package/die combinations must be readily extended to all devices.

3.2.1.8 Control limits and action procedures. The results of the evaluations in 3.2.1.6 and 3.2.1.7 shall be used in determining control limits and action procedures for the wire bond operation. A destructive wire bond strength sampling plan for each wire bonder shall include start and completion of each assembly lot, frequency of sampling the assembly lot, and changes in operators (manual wire bonding only), wire spools, package lots, or setup conditions. The bond strength data shall include the force required for failure, the physical location of failure, and the nature of the failure. Electrical rejects from the same wafer lot may be used for the destructive wire bond pulls. In the event that bond wire strengths are outside the predicted values for the wire, or class of wires with similar geometry, the bonder shall be inactivated immediately and not returned to production until tests show that the operation is back under statistical control. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test is required.

3.2.1.9 Time and temperature characterization. Initially, a time and temperature characterization shall be performed for each major type of wire bond metallurgical interface (e.g., gold/aluminum, etc.) to determine the electrical and mechanical integrity of the wire bonds with respect to such factors as; flexing of wire bonds due to thermal expansion, and microcracks or microvoids at the metallurgical interface. Evidence from the characterization shall demonstrate that the integrity of the bonds is sufficient for a device to function over its expected life. Life usage conditions shall exceed 50,000 cycles from a 0 - 85 degree Celsius temperature range at the bonds. Time and temperature degradation factors for accelerated testing must be justified against these minimal life usage conditions.

3.2.1.10 Wire bond integrity. If pre-burn-in, interim and post burn-in electrical failures (opens/shorts), qualification, or quality conformance inspection failures indicate questionable wire bond integrity then an analysis is required to verify the bond integrity. If any bond is confirmed to be defective; the applicable inspection lot or sublot will be rejected, an evaluation performed to determine the cause of the bond failure, corrective actions implemented based on the evaluation, and disposition of other affected inspection lots or sublots. The failure analysis and corrective actions will be retained and made available to the qualifying activity upon request.

3.2.2 Lot acceptance procedure. Each assembly lot shall receive a post-seal bond wire integrity acceptance test. A separate assembly lot acceptance test is required for each wire bonder, and for any changes in setup conditions, wire spool, package lot, or wafer lot, unless such differences have been demonstrated to be statistically insignificant. A post-seal destructive wire bond sampling and test plan with the following minimum requirements shall be documented.

a. More than one device shall be subjected to the acceptance test. Electrical, non-wire bond related visual, or package seal rejects may be used for the post-seal wire bond test.

b. The destructive wire pulls shall be evaluated in meeting the post-seal bond strength limits in MIL-STD-883, Method 2011, or as established in 3.2.1.7. The assembly lot shall be accepted if the wire bond strengths meet the requirements of sections c, d, and e below.

c. All wires or a minimum of 50 randomly selected wires shall be pulled from each sampled device. The post-seal bond strength distribution(s) must demonstrate that the wire bond process is in statistical control, has not changed with respect to the distribution characterized for a one-sided lower control limit, and no single destructive pull is less than the specified post-seal bond strength limit. The sample size shall be sufficient to demonstrate that the statistical distribution of all wires pulled has not changed with respect to central tendency or dispersion in such a way as to violate a $p < .0001$ at the device level. The beta risk to the consumer shall be .01 or less. The method of statistical analysis shall be documented and approved by the qualifying activity.

d. A minimum of 8 wires shall be evaluated from each sampled device to represent the worst case wires as determined to potentially violate the lower specification limit. Their wire pull strengths shall be within the predicted tolerances established in 3.2.1.6. Any wire pull strengths outside the predicted tolerance in the characterized distribution shall require evaluation as to the cause of the out of control condition, and additional worst case wires shall be pulled to determine whether the wire bond strength distribution meets a probability at the wire level of $P < 1-[.9999^{**}(1/n)]$ (n = number of bonding wires in the package). The lot is rejected if this criteria is not met.

e. If any bond fails the acceptance criteria, a documented action plan shall be followed to determine the cause of the failure. Wire bond failures verified as non-bond related shall be documented, and additional post-seal wire bond pulls shall be conducted to demonstrate statistical control as described in 3.2.2.1.c and d. If a failure is verified as bond integrity related (e.g., contamination on wire, glassivation on the bonding pad, etc.), all devices within the applicable assembly lot shall be rejected. Wire bonding shall be suspended on the applicable bonding equipment until a failure analysis, MIL-STD-883, method 5003, of the failed bond is performed and corrective action is implemented and recorded.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The applied lifting force if other than as specified in 3.1.

b. The sampling, acceptance, or screening requirements.

c. The percent defective allowable (PDA) as applied to the number of failures with respect to the number of wires tested.

d. The requirements for reporting of failure categories, when applicable.

FIGURE 2023-1. Wire loop angle.

FIGURE 2023-2. Flat loop wire pull testing.

APPENDIX A

Capability Study Example

The worst case die/package combination for the example product line is a 100 wire package with the smallest die. The worst case die/package combination is based on the characterized worst case wire geometry and number of bonding wires. A post seal bond pull of 2 grams or less is considered unacceptable for 1.25 mil diameter aluminum wire. The proposed military standard requires a failure rate of no greater than 100 parts per million.

The distribution of bond pulls across devices is examined for each wire length. A statistical test is done for normality and in this example there is no reason to reject the assumption of normality. The worst case wire length in terms of variability and closeness to the specification of 2 grams is identified. The mean of this worst case distribution is found to be 4.26 grams with a standard deviation of .5 grams.

Thus, for this distribution the 2 gram specification is 4.52 standard deviations away [(4.26-2)/(.5)] and corresponds to a ppm level of approximately 3.1. If the distribution was to shift to the 100 ppm level such that 2 grams corresponds to 100 ppm (i.e., the 2 gram spec is now only 3.719 standard deviations below the mean), a shift of about .8 sigma [4.52-3.719] from the present bond pull mean of 4.26 would be required. This information is used to determine the number of devices needed for the capability study.

The following table can be used where the data is normally distributed:

Sigma shift to 100 ppm level	Devices needed
.4	140
.5	90
.6	62
.7	46
.8	35
.9	28
1.0	22
1.1	19
1.2	16
1.3	13
1.4	11
1.5 or greater	10

n = [(Z_alpha + Z_beta)**2]/(d**2)

d = standard deviation shift = 0.8

alpha = .05 ; Z_alpha = -1.645

beta = .001 ; Z_beta = -3.09

[see Diamond, 1989, Practical Experiment Designs, pages 45-47]

Therefore, n = [(1.645 + 3.09)**2]/(.8)**2 = 22.42/.64 = 35. Thirty five devices are used in this capability study.

Using the standard bonding process, the 35 devices (each having 100 wires) are submitted to package seal, and post-seal bond strength measured.

For each wire position a mean and standard deviation is calculated across the 35 devices.
mean = xbar
standard deviation = sd

The distributions are evaluated and show no significant departure from normality.

The lower spec limit is determined: Here a lower bond pull of 2 grams.

For each wire position a "Z" is calculated:

Z = (xbar - LSL) / sd

For each wire position a probability of wire failure is determined by finding the probability of being below the Z value. Use of normal probability tables are utilized in this example because of the distributions being normally distributed. For this example there will be 100 values.

The probability of device failure is calculated by summing the 100 p values for failure of a wire position.

P(Device Failure) = Summation of P(failure of wire position)

= .00005 for this example or 50 parts per million

For this example it has been demonstrated that the probability of any device failing the minimum post-seal bond strength is less than .0001.

FIGURE 2023-3. Bond strength versus probability.

METHOD 2024.2

LID TORQUE FOR GLASS-FRIT-SEALED PACKAGES

1. PURPOSE. The purpose of this test is to determine the shear strength of the seal of glass-frit-sealed microelectronic packages. This is a destructive test.

2. APPARATUS. The test equipment shall consist of suitable fixed or adjustable clamps and fixtures to secure devices while applying a torque to the seal area. The torque mechanism and holding fixtures should provide adequate support to the base and lid (especially for flat packs, chip carrier packages, or other thin profile packages) to assure that the torque is applied predominantly to the seal area without significant bending, warping or displacement of the package being tested. A torsion wrench or torque-applying mechanism capable of applying a torque of at least 12.8 newton meter (114 in-lbf) with a gauge capable of measuring the force with an accuracy and precision of ±5 percent of the reading or ±0.2 newton meter, whichever is greater, shall be used to apply torque to the lid. For smaller seal area packages a torsion wrench or torque-applying mechanism with sufficient capacity to separate the package and with an accuracy and precision of ±5 percent of the reading or ±0.2 newton meter whichever is greater, may be used to allow for a more accurate reading. The torque mechanism shall have a peak indicator for retaining the maximum stress applied or other equivalent stress recording system.

3. PROCEDURE. The device shall be held by the device body and torque applied to the lid of the device or vice versa. The lid torque fixtures shall be placed to assure that it only applies torque to the side area of the package lid, base, or spacer. Contact to the sealing glass should be avoided. The lid torque fixture may touch the package leads but not in such a way that significant torque is transferred directly through the leads. The torque shall be applied gradually and smoothly until package separation occurs, or the reaching of the 12.8 newton meter torque limit. The torque required for package separation or the reaching of the 12.8 newton meter torque limit shall be recorded. The torque shall be applied such that the axis of rotation is perpendicular to the sealing plane and the axis of rotation shall be located at the geometric center of the sealing area (see figure 2024-2).

3.1 Separate glass seals. For packages with more than one glass-frit-seal (e.g., separate glass-frit-seals for the lid and the lead frame), each seal shall be torqued and rated separately against the failure criteria. A failure of either seal shall constitute failure of the test. Alternatively, the two seals may be simultaneously stressed by holding only the lid and base and applying the torque specified for the larger seal area.

3.2 Failure criteria. A device where package separation or breakage occurs at a torque value less than specified in table I shall constitute a failure. If the entire package (lid, seal, and base) breaks in a direction normal to the plane of the applied torque (i.e., showing evidence of improperly applied torque) with parts of lid and base still fused together, the package may be discarded without counting as a failure and a replacement sample substituted to complete the required testing.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The minimum torque if other than the value specified in table I.

b. Number of devices to be tested.

c. Requirement for data recording where applicable.

TABLE I. Minimum torque limits versus design seal area.

Design seal area (cm2)	Torque		
	Newton meter (N-m)	Inch-pounds force (in-lbf)	Meter-grams force (m-gf)
<0.22	0.5	4	50
0.221-0.32	0.7	6	70
0.321-0.47	1.0	9	100
0.471-0.65	1.7	15	170
0.651-0.85	2.5	22	250
0.851-1.08	3.4	30	350
1.081-1.41	4.4	39	450
1.411-1.73	5.9	52	600
1.731-2.05	7.4	65	750
2.051-2.50	8.8	78	900
2.501-3.00	10.8	96	1100
>3.00	12.8	114	1300

Various units are presented for the convenience of those using conventional torque wrenches scaled in metric or English system units. All values have been rounded off from the direct conversion values beginning with N-m and are acceptable for use in quality conformance and qualification inspection.

1 m-gf = 0.009807 N-m
1 in-lbf = 0.1130 N-m

a. TWO PIECE PACKAGE

Seal area = ed - xy

If the cavities in the lid and base are not equal, the area "XY" shall be determined from the larger of the cavities in the lid or base.

b. THREE PIECE PACKAGE

FIGURE 2024-1. Design seal area.

FIGURE 2024-2. Application of torque.

METHOD 2025.4

ADHESION OF LEAD FINISH

1. PURPOSE. This destructive test is intended to determine the integrity of all primary and undercoat lead finishes.

2. APPARATUS. This test requires suitable clamps and hardware necessary to apply the bending stress through the specified bend angle. Optical equipment capable of magnification of 10X to 20X.

3. PROCEDURE. Unless otherwise specified, the bend stress shall be applied to randomly selected leads from each device selected for test and shall be performed after application of the primary finish and after sealing. Unless otherwise specified, the sampling shall be sample size number = 15, C = 0 based on the number of leads tested chosen from a minimum of three devices. The leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. The coated lead shall be bent repeatedly in the same direction (or plane) through an angle of at least 90° at a radius of less than four times the lead thickness or diameter at approximately the mid point of the lead lengths until fracture (i.e., lead breaks off) of the base metal occurs.

3.1 Failure criteria. No cracking, flaking, peeling, blistering, loosening, or detachment of the coating(s) at the interface(s) shall result from probing the bend/break area with a sharp instrument. Cracks in the base metal shall not be considered a failure unless accompanied by cracking, flaking, peeling, blistering, loosening, or detachment of the primary coating(s) or undercoating(s).

NOTE: In tin lead or heavy tin coatings, the failure criteria listed should not be confused with shearing and tearing associated with fatigue fractures and slip-planes which develop into cracks and result in rupture.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Sampling criteria, if other than specified (see 3).

b. Failure criteria, if other than specified (see 3.1).

METHOD 2026

RANDOM VIBRATION

1. PURPOSE. This test is conducted for the purpose of determining the ability of the microcircuit; to withstand the dynamic stress exerted by random vibration applied between upper and lower frequency limits to simulate the vibration experienced in various service-field environments. Random vibration is more characteristic of modern-field environments produced by missiles, high-thrust jets, and rocket engines. In these types of environments, the random vibration provides a more realistic test. For design purposes, however, a swept frequency sinusoidal test may yield more pertinent design information.

2. APPARATUS.

2.1 Vibration system. The vibration system, consisting of the vibration machine, together with its auxiliary equipment shall be capable of generating a random vibration for which the magnitude has a gaussian (normal) amplitude distribution, except that the acceleration magnitudes of the peak values may be limited to a minimum of three times the rms (three-sigma (α) limits). The machine shall be capable of being equalized so that the magnitude of its spectral-density curve will be between specified limits (for example, see figures 2026-1 and -2). When the test item, or a substitute equivalent mass, is appropriately secured to the vibration machine. The equalization of an electrodynamic vibration machine system is the adjustment of the gain of the electrical amplifier and control system so that the ratio of the output-vibration amplitude to the input-signal amplitude is of a constant value (or given values) throughout the required frequency spectrum.

2.1.1 Control and analysis of vibration.

a. Spectral-density curves. The output of the vibration machine shall be presented graphically as power-spectral density versus frequency. 1/ The spectral-density values shall be within +40 and -30 percent (±1.5 dB) of the specified values between a lower-specified frequency and 1,000 Hz, and within +100 and -50 percent (±3 dB) of the specified values between 1,000 and an upper-specified frequency (2,000 Hz). A filter bandwidth will be a maximum of one-third-octave or a frequency of 25 Hz, whichever is greater.

1/ Power-spectral density is the mean-square value of an oscillation passed by a narrow-band filter per unit-filter bandwidth. For this application it is expressed as G^2/f where G^2/f is the mean-square value of acceleration expressed in gravitational units per number of cycles of filter bandwidth. The spectral-density curves are usually plotted either on a logarithmic scale, or in units of decibels (dB). The number of decibels is defined by the equation:

$$dB = 10 \log \frac{G^2 / f}{G_r^2 / f} = 20 \log \frac{G / \sqrt{f}}{G_r / \sqrt{f}}$$

The rms value of acceleration within a frequency band between f_1 and f_2 is:

$$G_{rms} = \left[\int_{f_1}^{f_2} G^2 / f \, df \right]^{1/2}$$

where G_r^2/f is a given reference value of power-spectral density, usually the maximum specified value.

b. Distribution curves. A probability density-distribution curve may be obtained and compared with a gaussian-distribution curve. The experimentally-obtained curve should not differ from the gaussian curve by more than ±10 percent of the maximum value.

2.2 Monitoring. Monitoring involves measurements of the vibration excitation and of the test-item performance. When specified, the device shall be monitored during the test. The details of the monitoring circuit, including the method and points of connection to the specimen, shall be specified.

2.2.1 Vibration input. The vibration magnitude shall be monitored on a vibration machine, on mounting fixtures, at locations that are as-near as practical to the device mounting points. When the vibration input is measured at more than one point, the minimum input vibration shall be made to correspond to the specified test curve (see figures 2026-1 and 2026-2). For massive test-items and fixtures, and for large-force exciters or multiple-vibration exciters, the input-control value may be an average of the average magnitudes of three or more inputs. Accelerations in the transverse direction, measured at the test-item attachment points, shall be limited to 100 percent of the applied vibration.

3. PROCEDURE. The device(s) shall be rigidly fastened on the vibration platform and the leads adequately secured. The vibration machine shall then be operated and equalized or compensated to deliver the required random frequencies and intensities conforming to the curves specified in test condition I, figure 2026-1 or test condition II, figure 2026-2. The device(s) shall be subjected to a random vibration specified by the test condition letter (see tables I and II) for a duration of 15 minutes in each of the orientations X, Y, and Z. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Measurements after test (see 3 and 3.1).

c. Test condition I or II and letter (A-K).

d. Test duration if other than specified.

e. Requirement for test to be conducted with device powered up, when applicable.

FIGURE 2026-1. Test condition I, random vibration test-curve envelope (see table I).

TABLE I. Values for test condition I. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.2
B	.04	7.3
C	.06	9.0
D	.1	11.6
E	.2	16.4
F	.3	20.0
G	.4	23.1
H	.6	28.4
J	1.0	36.6
K	1.5	44.8

1/ For duration of test, see 4.

FIGURE 2026-2. Test condition II, random vibration test-curve envelope (see table II).

TABLE II. Values for test condition II. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.9
B	.04	8.3
C	.06	10.2
D	.1	13.2
E	.2	18.7
F	.3	22.8
G	.4	26.4
H	.6	32.3
J	1.0	41.7
K	1.5	51.1

1/ For duration of test, see 4.

METHOD 2027.2

SUBSTRATE ATTACH STRENGTH

1. PURPOSE. The purpose of this test is to determine the strength of the element attachment system when subjected to force in the Y1 axis. This method is applicable to semiconductor die attached to headers or substrates by means of organic materials. Uses include material evaluations and process control.

2. APPARATUS. The test equipment shall consist of a tensile strength tester capable of applying a force equal to 1,000 psi (6895 kpa) times the area of the largest die to be tested with an accuracy of ±5 percent or 1.75 ounces (50 gm) force, whichever is less. The test equipment shall have the following capabilities.

a. A range of replaceable die contact tools such that each contacting surface shall be 60 to 100 percent of the area of the die under test.

b. Provision to assure that the die contact tool is held perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability between the die contact tool and the header/ substrate holding fixture.

3. PROCEDURE. The test shall be conducted by placing a small amount of a quick setting adhesive on the contacting tool which is then attached to the die surface (figure 2027-1). After sufficient adhesive curing the sample is subjected to a vertical pull force as defined herein.

3.1 Force applied. A force sufficient to lift the die from its mounting or equal to twice the minimum specified tensile strength (figure 2027-2) whichever occurs first, shall be applied to the die using the apparatus of 2 above.

3.2 Failure criteria. If the separation occurs between the die surface and the die contacting tool at less than twice the minimum specified tensile strength, the particular die pull test will not be counted in the sample as either passing or failing. The following criteria constitute a failure when the die is lifted from the header/substrate:

a. Separation at less than the minimum die tensile strength (1.0X) as shown on figure 2027-2).

b. Separation at less than 200 percent of the minimum die attach strength (2.0X) as shown on figure 2027-2 and no evidence of attachment at the interface between the die attach medium and the die or header/substrate.

3.2.1 Recording. When specified, the force required to achieve separation will be recorded with the failure category.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Minimum die pull strength if other than that shown on figure 2027-2.

b. Number of die to be tested and the acceptance number.

c. Requirements for data recording.

FIGURE 2027-1. Die contact tool adhered to die top surface prior to lift off.

NOTE: The X-axis is a log scale and intermediate points not shown must be calculated based on the formulas, (1.0 X: $y = 3.32 \log X + 13.3$, 2.0 X: $y = 6.63 \log X + 26.6$) not extrapolated from the graph.

FIGURE 2027-2. Die attach strength criteria (minimum force versus die attach area).

METHOD 2028.4

PIN-GRID PACKAGE DESTRUCTIVE LEAD PULL TEST

1. PURPOSE. This method provides a test for determining the integrity of pin-grid type package leads by measuring the capability of the package leads to withstand an axial force.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for supplying the specified stress to the package lead. A calibrated measurement and indication of the applied stress in grams-force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 kgf, whichever is greater.

3. PROCEDURE. The stress shall be applied to the leads to be tested randomly selected from a minimum of 3 devices prior to start of the test. Tension only shall be applied, without shock, to each lead to be tested in a direction parallel to the axis of the lead. The tension shall be increased until the minimum acceptable pull strength is reached or upon separation of the lead from the braze pad. The tension shall be applied as close to the end of the lead as possible.

3.1 Failure criteria. The minimum acceptable lead pull strength shall be 1.70×10^7 grams-force per square inch of cross-sectional lead area (e.g., the minimum pull strength of a lead with an average cross-sectional area of 2.5×10^{-4} in^2 will be 4.3 kgf.)

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Number and selection of leads, if different from above.

b. Measured lead pull strength and minimum required pull strength, if different from above.

METHOD 2029

CERAMIC CHIP CARRIER BOND STRENGTH (DESTRUCTIVE PUSH TEST)

1. PURPOSE. The purpose of this test method is to measure strengths of bonds external to leadless microelectronic packages (e.g., solder bonds from chip carrier terminals to substrate or wiring board).

2. APPARATUS. The apparatus for this test method shall consist of suitable equipment for applying the specified stress to the device terminals. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the following test procedure. All push tests shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. A minimum of 4 chip carriers (or use all chip carriers if 4 are not available) on each of a minimum of 2 completed substrates or wiring boards shall be used. Where there is any adhesive, encapsulant, or other material under, on, or surrounding the chip carrier such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

3.1 Test samples. When packages are bonded to substrates or wiring boards other than those in completed devices, the following conditions shall apply:

a. The sample of packages for this test shall be taken at random from the same chip carrier population as that used in the completed devices that they are intended to represent.

b. The packages for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test package substrates shall be processed and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1.1 Sample preparation. Substrates must be prepared as follows:

a. A roughly circular area comprising 50 percent, +5 percent, -0 percent of the bonded side of each package to be tested shall be exposed by either end-mill drilling of the test substrate or other suitable means. If it is not possible to expose the ceramic in this manner, the packages shall be bonded onto test substrates into which the proper hole(s) and hole size(s) has (have) been manufactured, providing all other conditions of 3.1 have been met.

b. Suitable support must be provided for the test substrate so that there is a minimum of flexure of the substrate during the test. This support, if necessary, may be provided by bonding the substrate to a rigid metal plate having a hole pattern matching that of the test substrate.

c. A cylindrical rigid metal test post must be prepared for each hole size, which will be inserted through the support plate and test substrate holes. The post will be used to transmit the specified stress from the stress-source equipment to the exposed package surface. The diameter of the post shall be 85 percent (+5 percent, -0 percent) of the corresponding test hole diameter. The length of the post shall be sufficient to extend 1 inch (+100 percent, -0 percent) from the open end of the test hole when the post is inserted completely into the hole.

3.2 Testing. The test shall be performed in the following manner:

a. A single package shall be pushed during each test sequence.

b. A layer of teflon tape in accordance with MIL-T-27730 or equivalent shall be placed between the exposed chip carrier surface and the test post prior to testing.

c. Insert test post into test hole. The contact of the test post to the ceramic chip carrier shall be made without appreciable impact (≤0.1 inch/minute). With the stressing element of the test equipment traveling at a constant rate of 0.02 ±1 percent inch/second, apply sufficient force to chip carrier (through test post) to break all chip carrier to substrate bonds on at least three edges of chip carrier under test. When failure occurs, the force at the time of failure and the failure category shall be recorded. Any test resulting in the fracturing of either the chip carrier or test substrate shall be considered unacceptable. The data from the test shall be discarded, and the test performed again.

3.3 Failure criteria. Any push test which results in separation with a bond strength of less than 30 kg-force per linear inch (1180 g-force per linear mm) of solder pad width shall constitute a failure. The bond strength shall be determined by dividing the separating force by the total of the solder pad widths as measured on the substrate at the package edge, in a direction parallel to the package edge.

3.3.1 Failure category. Failure categories are as follows. When specified, the stress required to achieve separation and the predominant category of separation shall be recorded.

a. Device fracture.

b. Failure in package-bond interface.

c. Terminal break at point not affected by bonding process.

d. Failure in bond-substrate conductor interface.

e. Conductor lifted from board or substrate.

f. Fracture within board or substrate.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum bond strength if other than specified in 3.3 or details of required strength distributions if applicable.

* b. Sample size number and accept number and selection and number of devices to be tested on each substrate, if other than 4.

c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.3.1).

METHOD 2030

ULTRASONIC INSPECTION OF DIE ATTACH

1. PURPOSE. The purpose of this examination is to nondestructively detect unbonded regions and voids in the die attach material of semiconductor devices through the measure of acoustic continuity. It establishes methods and criteria for ultrasonic inspection of semiconductor devices.

a. For certain die attach materials, a dramatic distinction between well-bonded and poorly bonded conditions may be difficult to achieve. This factor should be considered in relation to the design of each device when application of this test method is specified.

b. The term "die attach interface" as used in this document refers to the entire area between the silicon die and the substrate to which it is bonded. This includes the interface between the die attach material and the die, the interface between the die attach material and the substrate, plus the die attach material itself.

c. The term ultrasonic inspection as used in this document refers to high frequency ultrasonic visualization (imaging) which produces a grey scale output such as may be provided by ultrasonic scanning (US) or C-SCAN, scanning laser acoustic microscopy (SLAM), or C-mode scanning acoustic microscopy (C-SAM).

2. APPARATUS. The apparatus and materials for this test shall include:

a. Ultrasonic imaging equipment with a test frequency sufficient to penetrate to the die attach interface. The test frequency and focal distance shall be adequate to detect voids as small as 0.0254 mm (0.001 inch) in diameter.

b. Output device: A hard copy grey scale recording unit or other direct recording device (computer storage) shall be used to produce an image for analysis (manual or automated). The dynamic range of the output image shall be at least sixteen discernible colors or levels of grey. The image shall be large enough to be viewed at 10X or lower magnification.

c. Ultrasonic detector: Shall be capable of detecting an acoustic signal which enters the back or bottom of the package and is reflected by or transmitted through the die attach interface. The reflected mode of imaging shall be used where the opening of a sealed, hermetic device is undesirable.

3. PROCEDURE. The ultrasonic generator, receiver, and line scan recorder settings (when used) shall be selected or adjusted as necessary to obtain satisfactory images and achieve maximum image details within the sensitivity requirements for the device or defect features the test is directed toward. In the case of reflection mode or transmission mode images, care must be exercised to insure that the ultrasound penetrates and is sensitive to the entire die attach interface.

3.1 Mounting and views. The devices shall be mounted in the holding tank so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture provided the fixtures do not block the view from the ultrasonic transducer to any portion of the body of the device. The coupling fluid in the holding tank shall be distilled water or other suitable noncorrosive liquid. The devices shall remain in the coupling fluid for as short a time as possible. Subsequent to the ultrasound inspection, proper cleaning and drying of the samples are required.

3.1.1 Views. All devices, shall have one view made with the acoustic signal penetrating the device in a direction perpendicular to the plane of the die attach, and for which there is acoustic continuity from the case exterior surface to the die attach interface (generally, the Y1 direction with the die attach parallel to the XZ plane). For devices with no sealed air gap above the active surface of the semiconductor element (unlidded devices), a view made with the acoustic signal directed from or through the active surface of the semiconductor element to the die attach interface may be specified.

3.2 Recording and marking. The acoustic image shall be printed by equipment using dry electrosensitive paper and with a resolution of 150 data elements per inch nominal. The image shall be identified by unambiguously marking the paper on which the image is printed with the following information:

a. Device manufacturer's name or code identification number.

b. Device type or part number.

c. Production lot number or date code or inspection lot number.

d. Ultrasonic image view number and date.

e. Device serial or cross reference numbers, where applicable.

f. Ultrasonic laboratory identification, if other than device manufacturer.

3.2.1 Nonprint techniques, when specified. The use of other than paper recording techniques is permitted if permanent records are not required and the equipment is capable of producing results of equal quality when compared to printed recording techniques, and all requirements of this method are complied with, except those pertaining to the actual recording.

3.2.2 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. They shall be imaged in consecutive, increasing serial order. When a device is missing, the blank space shall contain the serial number or other marking to readily identify and correlate ultrasonic image data. When large skips occur within serialized devices, the serial number of the last device before the skip and the first device after the skip may be used in place of large physical spacing of the devices.

3.2.3 Calibration. When specified, at least one open lid device of the same type and construction should be available to set up the visualization instruments. The device may be a scrap, nonoperational device which will be used to identify internal landmarks and insure the equipment is properly operating.

3.3 Tests. Acoustic frequency gate settings, receiver attenuation, and other equipment settings shall be selected to achieve resolution of 0.0254 mm (0.001 inch) in major dimension, optimize the signal reflected from the die attach interface, and to demark image features with as great a contrast as possible. Ultrasonic images shall be made for each view required.

3.4 Operating personnel. Personnel who will perform ultrasonic inspection shall have training in ultrasonic imaging procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. The following minimum vision requirements shall apply for visual acuity of personnel inspecting images:

a. Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.

b. Near vision shall be such that the operator can read Jaeger type number 2 at a distance of 16 inches, corrected or uncorrected.

c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year. Personnel authorized to conduct ultrasonic imaging tests shall be required to pass the vision tests specified in 3.4a and 3.4b.

3.5 Interpretation of ultrasonic images. Ultrasonic images shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected. Interpretation of the image shall be made under moderate light level conditions without a glare on the recording paper's surface. The image shall be viewed at a magnification between 1X and 10X.

3.6 Reports of records.

* 3.6.1 Reports of inspection. For class level S devices, or when specified for other device class levels, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the ultrasonic inspection, and list the purchase order number or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

3.6.2 Acoustic micrograph and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report. These shall be retained for the period specified.

3.7 Examination and acceptance criteria. In the examination of devices, the following aspects shall be considered unacceptable die mounting, and devices that exhibit any of the following defects shall be rejected.

Voids: When imaging devices ultrasonically, certain types of mounting material may not give true representation of voids. When such devices are inspected, the mounting shall be noted on the inspection report.

a. Contact area voids in excess of 50 percent of the total intended contact area.

b. A single void which exceeds 15 percent of the intended contact area, or a single corner void in excess of 10 percent of the total intended contact area (see figure 2030-1).

c. When the image is divided into four equal quadrants by bisecting both pairs of opposite edges, any quadrant exhibiting contact area voids in excess of 70 percent of the intended quadrant contact area (see figure 2030-1).

In case of dispute, the percent of voiding shall be determined by actual measurement from the image.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Number of views, if other than indicated in 3.1.1.

b. Marking, if other than indicated in 3.2 and marking of samples to indicate they have been ultrasonically imaged, if required.

c. Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 3.7.

d. Image and report retention, if applicable (see 3.6.2).

* e. Test reports when required for class level B devices.

REJECT: SINGLE VOID LARGER THAN 15 PERCENT OF TOTAL INTENDED CONTACT AREA.

REJECT: CORNER VOID LARGER THAN 10 PERCENT OF TOTAL INTENDED CONTACT AREA.

ACCEPT: NO SINGLE VOID LARGER THAN 15 PERCENT OF TOTAL INTENDED CONTACT AREA.

ACCEPT: CORNER VOID OF AREA LESS THAN 10 PERCENT OF TOTAL INTENDED CONTACT AREA.

= VOID OR UNBONDED AREA.

REJECT: QUADRANT MORE THAN 70 PERCENT UNBONDED.

ACCEPT: ALL QUADRANTS LESS THAN 70 PERCENT UNBONDED.

FIGURE 2030-1. Void criteria.

METHOD 2031.1

FLIP-CHIP PULL-OFF TEST

1. PURPOSE. The purpose of this test is to measure the strength of internal bonds between a semiconductor die and a substrate to which it is attached in a face-bond configuration.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bonds. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

* 3. PROCEDURE. The test shall be conducted using the following procedure. All die pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. The sample size number and accept number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices, a minimum of 4 die or all die if four are not available on a minimum of 2 completed devices shall be used. All pull tests shall be performed prior to the application of encapsulants, adhesive, or any material which may increase the apparent bond strength.

When flip chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Testing. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) having a cross-sectional area of 75 percent, +3 percent, -5 percent of the chip surface area. The rod shall make connection with a hard setting adhesive material (for instance, a cyanoacrylate or other adhesive possessing high tensile strength) on the back of the flip chip. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The die shall be pulled without shock, within 5° of the normal at a rate of 500 grams ±100 grams per second, until the die separates from the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any flip-chip pull which results in separation under an applied stress less than 500 kg/in^2 x average solder bump area (in^2) x number of solder bumps shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the predominant category of separation or failure shall be recorded.

a. Silicon broken.

b. Lifted metallization from chip.

c. Separation at bond-chip interface.

d. Failure within bond.

e. Separation at bond-substrate interface.

f. Lifted metallization from substrate.

g. Substrate broken.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

b. Sample size number and accept number and selection and the number of die to be tested, if other than 4

c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

METHOD 2032.1

VISUAL INSPECTION OF PASSIVE ELEMENTS

* 1. PURPOSE. The purpose of this test is to inspect passive elements used for microelectronic applications, including RF/microwave, for the visual defects described herein. This test can be performed at the unmounted element level, or prior to sealing or encapsulation, on a 100 percent inspection basis, to detect and eliminate elements with visual defects that could lead to failure in normal application. It may also be performed on a sample inspection basis at the unmounted element level, or prior to sealing or encapsulation, to determine the effectiveness of the manufacturer's quality control and handling procedures for passive elements. Visual inspection criteria are presented in four sections. The first (see 3.1), concerns planar thin film elements (resistors, capacitors, inductors, single-level patterned substrates and multilevel patterned substrates). The second (see 3.2), concerns planar thick film elements (resistors, capacitors, single-level patterned hard substrates, and multilevel patterned hard substrates). The third (see 3.3), concerns nonplanar elements (ceramic chip capacitors, tantalum chip capacitors, parallel plate chip capacitors, chip resistors, inductors, and transformers). The fourth (see 3.4) concerns surface acoustic wave (SAW) elements. The inspection criteria contained in each section define the visual requirements for class H and class K elements (classes of passive elements refer to screening requirements of MIL-PRF-38534).

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (drawings, photographs, etc.) necessary to perform effective inspection and to enable the operator to make objective decisions as to the acceptability of the element being inspected. Adequate fixturing shall be provided for handling elements during inspection to promote efficient operation without inflicting damage to them.

3. PROCEDURE.

a. General. The element shall be inspected in a suitable sequence of observations within the specified magnification ranges to determine compliance with class H or class K visual requirements. If a specified visual inspection requirement is in conflict with element design, topology or construction, it shall be documented and specifically approved by the acquiring activity. Inspection for all of the visual defect criteria in this test shall be performed on all elements to which they are applicable. Where a criterion is intended for a specific element type, process, or technology, it has been so indicated.

b. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

c. Inspection control. In all cases, inspections prior to the final pre-seal inspection shall be performed under the same quality program that is required at final pre-seal inspection. Care shall be exercised after unmounted element inspection to prevent any handling induced defects from occurring and to insure that defects created during such handling will be detected and rejected at final pre-seal inspection. If an element is electrostatic discharge (ESD) sensitive, then appropriate precautions shall be taken.

d. Inspection environment. Unmounted element inspection shall be conducted in a class 100,000 minimum environment, as defined in Federal Standard 209, except that the maximum allowable relative humidity shall not exceed 65 percent. Mounted element inspection shall be conducted in a class 100,000 minimum environment for class H and a class 100 minimum environment for class K. During the time interval between final pre-seal inspection and preparation for sealing, mounted elements shall be placed in a controlled environment (see 3.i.(7)). Both mounted and unmounted elements shall be in covered containers when transported from one controlled environment to another.

e. Magnification. "High magnification" inspection shall be performed perpendicular to the element with illumination normal to the element surface. Other angles at which the inspection can be performed, and at which the element can be illuminated, may be used at the option of the manufacturer if the visual presentation is the same as used in the originally specified conditions. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereo microscope with the element under suitable illumination, tilted at an angle not greater than 30° from the perpendicular. The magnification ranges to be used for inspection are specified at the start of each section and are called out at the start of each major criteria grouping.

* f. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection shall be performed at the magnification specified herein, unless a specific magnification is required by the acquisition document.

g. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly drawing.

* h. Format and conventions. For ease of understanding and comparison, visual criteria are presented side-by-side in a columnar format. Class H criterion are presented in the left column and class K criterion are presented in the right column. When there are differences, the applicable parts of the class H criterion are underlined, for ease of comparison and clarity, and the differences only are shown in the class K column. When there are similarities, the phrase "same as class H" is used with no underlining of the class H criterion. If a requirement is not applicable to either product class, this is indicated by "N/A." A note in the class H column is applicable to class K unless otherwise specified in the class K column. A note in the class K column is applicable to class K only. Two kinds of notes are used herein, regular notes (NOTE:) and precautionary notes (PRECAUTIONARY NOTE:). A regular note is a integral part of a criterion. A precautionary note is not an integral part of the criterion but serves to alert the user to a requirement of the General Specification for Hybrids, MIL-PRF-38534. The phrases "except by design," "intended by design," "by design," or "unless otherwise specified by design" require that the element drawing be referenced to determine intent. For inspections performed at 100X, the criteria of "0.1 mil of passivation, separation, or metal" is satisfied by a "line of passivation, separation, or metal." Reference herein to "that exhibits" is satisfied when the visual image or visual appearance of the element under examination indicates a specific condition is present that does not require confirmation by any other method of testing. When other methods of test are used to confirm that a defect does not exist, they shall be approved by the acquiring activity. In the figures, cross-hatched areas represent metallization, blank areas represent resistor material and shaded areas represent exposed underlying material. The letters "x", "y", or "z" represent the dimension of interest and the letter "d" represents the original dimension. Most figures show the reject condition only.

i. Definitions:

(1) Active circuit area is all functional circuitry, operating metallization, or any connected combinations of these. In the case of resistors, it includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads).

(2) Block resistor is a solid, rectangularly shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

(3) Bonding pad is a metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element.

(4) Bridging is complete connection between circuit features not intended to be connected.

(5) Conductive substrate is one that can conduct electricity. Copper or doped silicon, for example, are conductive substrates. Alumina and quartz, for example, are nonconductive (insulating) substrates.

(6) Contact window is an opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate.

(7) Controlled environment is one that is in accordance with the requirements of Federal Standard 209, class 1000 environment, except that the maximum allowable relative humidity shall not exceed 65 percent.

(8) Corrosion is the gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product.

(9) Crazing is the presence of numerous, minute, interconnected surface cracks.

(10) Crossover is the transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing.

(11) Detritus is fragments of original or trim-modified resistor or conductor material.

(12) Dielectric is an insulating material that does not conduct electricity but may be able to sustain an electric field. It can be used in crossovers, as a passivation or a glassivation, or in capacitors.

(13) Foreign material is any material that is foreign to the element or any nonforeign material that is displaced from its original or intended position in the element. It is considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of color fringing around the periphery of the particle.

(14) Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads. Crazing is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.

(15) Kerf is the clear area in a trimmed resistor resulting from the removal of resistor material by the trimming operation. In laser trimming, the kerf is bounded by the reflow zone (which is characterized by adherent, melted resistor material), the scorched heat-affected zone (which is characterized by discoloration of the resistor film without alteration of its physical form), and the undisturbed zone.

(16) Mar is a nontearing surface disturbance such as an indentation or a buff mark.

(17) Metallization, multilevel (conductors) is alternate layers of metallization, or other material used for interconnection, that are isolated from each other by a grown or deposited insulating material. The term "overlaying metallization" refers to any metallization layer on top of the insulating material.

(18) Metallization, multilayered (conductors) is two or more layers of metallization, or other material used for interconnection, that are not isolated from each other by a grown or deposited insulating material. The term "underlying metallization" refers to any metallization layer below the top layer of metallization.

(19) Metallization, operating (conductors) is all metallization (gold, aluminum, or other material) used for interconnection. Bonding pads are considered to be operating metallization. Alignment markers, test patterns, and identification markings are not considered to be operating metallization.

(20) Narrowest resistor width is the narrowest portion of a given resistor prior to trimming; however, the narrowest resistor width for a block resistor may be specified in the approved manufacturer's design documentation.

(21) Neck-down is tapering of a resistor line at a metallization interface. Resistor material taper is typically equal on both sides of the line and is less abrupt than a void.

(22) Nicking (partial cut) is incomplete or inadvertent trimming of a resistor adjacent to the one being trimmed or of the next ladder rung of the same resistor.

(23) Nonplanar element is one that is essentially three-dimensional.

(24) Original separation is the separation dimension or space that is intended by design.

(25) Original width is the width dimension that is intended by design.

(26) Oxide defect is an irregularly shaped defect in the oxide characterized by two or three colored fringes at it edges.

(27) Passivation is the silicon oxide, silicon nitride, or other insulating material, that is grown or deposited directly on the element prior to the deposition of metal.

(28) Passivation step is a change in thickness of the passivation layer by design.

(29) Passive elements are planar resistors, capacitors, inductors, and patterned substrates (both single-layer and multilayer), and nonplanar chip capacitors, chip resistors, chip inductors, and transformers.

(30) Patterned substrate is a substrate on which conductors, and components such as resistors or capacitors, are formed using thick or thin film manufacturing techniques.

(31) Planar element is one that is essentially two-dimensional with all points in a common plane.

(32) Protrusion is a jutting-out of a circuit feature. Protrusion is typically caused by a photolithographic or screening defect.

(33) Resistor ladder is a resistor structure resembling a ladder in appearance that can be trimmed in incremental steps. A coarse ladder structure is one in which trimming of a rung results in a large incremental resistance change (one that can cause an out-of-tolerance condition to occur). A fine ladder structure is one in which trimming of a rung results in a small incremental resistance change (one that can not cause an out-of-tolerance condition to occur).

(34) Resistor ladder rung is that portion of a resistor ladder structure intended to be laser trimmed to result in an incremental change in resistance.

(35) Resistor loop is a resistor structure resembling a loop in appearance that can be trimmed. A coarse loop structure is one in which trimming results in a large resistance change (one that can cause an out-of-tolerance condition to occur). A fine loop structure is one in which trimming results in a small resistance change (one that cannot cause an out-of-tolerance condition to occur).

(36) Resistor material, self passivating is one on which a conformal insulating layer can be thermally grown (such as tantalum nitride on which tantalum pentoxide is grown).

(37) Scorching is discoloration of laser trimmed thin film resistor material without alteration of its physical form.

(38) Scratch, metallization is any tearing defect, including probe marks, in the surface of the metallization. A mar on the metallization surface is not considered to be a scratch.

(39) Scratch, resistor is any tearing defect in the resistor film. A mar on the resistor surface is not considered to be a scratch.

(40) Sidebar is that portion of a resistor ladder structure to which rungs are attached. Sidebars are not intended to be laser trimmed.

(41) Substrate is the supporting structural material into or upon which, or both, functional circuits are formed.

(42) Surface Acoustic Wave (SAW) element is a planar element fabricated typically using thin film manufacturing techniques on various substrate materials. Size varies as a function of frequency and design features include interdigitated fingers.

(43) Terminal is a metal area used to provide an electrical access point to functional circuitry.

(44) Thick film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.

(45) Thin film is conductive, resistive or dielectric material, usually less than 50,000Å in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.

(46) Underlying material is any layer of material below the top-layer metallization. This includes metallization, resistor, passivation or insulating layers, or the substrate itself.

(47) Via is an opening in the insulating material in which a vertical conductive electrical connection from one metallization layer to another in a multilayer substrate is made.

(48) Vitrification is conversion into glass or a glassy substance by heat and fusion.

(49) Void, metallization is any missing metallization where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

(50) Void, resistor is any missing resistor material where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

(51) Wraparound conductor is one which extends around the edge of the substrate by design.

(52) Coupling (air) bridge is a raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material.

(53) Pit is a depression produced in a substrate surface typically by nonuniform deposition of metallization or by nonuniform processing such as excessively powered laser trim pulses.

(54) Substrate, hard is the inorganic, rigid material into or upon which or both, functional circuits are formed. Typical materials are alumina and silicon.

(55) Blister, metallization is a hollow bump that can be flattened.

(56) Nodule, metallization is a solid bump that cannot be flattened.

3.1 Thin film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thin film passive element. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 30X to 60X for both class H and class K. When inspection is performed prior to mounting, then elements utilizing ceramic or glass type substrates, without backside metallization, shall be inspected using backlighting for conditions of hair-line voiding or bridging. Patterned substrates that have geometries of 2.0 mils or greater shall be inspected at 10X to 60X magnification.

Class H	Class K
3.1.1 Operating metallization defects "high magnification". No element shall be acceptable that exhibits: NOTE: The metallization defect criteria contained in this section apply to operating metallization only.	
3.1.1.1 Metallization scratches.	
a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes under-lying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see 2032-1h). NOTE: These criteria do not apply to capacitors (see 3.1.1.1e). NOTE: Underlying material does not have to be exposed along the full length of the scratch.	a. Same as Class H.

FIGURE 2032-1h. Class H metallization scratch criteria.

Class H

3.1.1.1 b. Scratch in the bonding pad area that both exposes underlying material and *reduces the metallization path width*, where it enters the bonding pad, and leaves less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-2h).

FIGURE 2032-2h. Class H metallization width reduction at bonding pad criteria.

c. Scratch that completely crosses metallization and damages the metallization on either side.

d. Scratches or probe marks in the bonding pad area that expose underlying material over greater *than 25 percent of the original* unglassivated metallization area.

Class K

3.1.1.1 b. Less than 75 percent (see figure 2032-2k).

FIGURE 2032-2k. Class K metallization width reduction at bonding pad criteria.

c. *Not applicable.*

d. Same as class H.

Class H	Class K
3.1.1.1 e. For capacitors only, a scratch in the metallization, other than in the bonding pad area, that exposes the dielectric material.	3.1.1.1 e. Same as class H.
3.1.1.2 Metallization voids.	
* a. Void(s) in the metallization, excluding bonding pads, that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-3h).	a. Same as Class H

FIGURE 2032-3h. Class H metallization void criteria.

b. Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately. NOTE: Figures 2032-2h and 2032-2k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.	b. Less than 75 percent

	Class H	Class K
3.1.1.2 c.	Void(s) in the bonding pad area that expose underlying material over greater than 25 percent of the original unglassivated metallization area. NOTE: For RF/microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.	3.1.1.2 c. Same as class H.
d.	For capacitors only, void(s) in metallization, other than in the bonding pad area, that reduces the metallization to an extent greater than an area equivalent to 25 percent of the capacitor metallization.	d. Same as class H.
e.	For interdigitated capacitors only, void(s) in the metallization that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-4h).	e. Less than 75 percent (see figure 2032-4k).

FIGURE 2032-4h. Class H interdigitated capacitor metallization void criterion.

FIGURE 2032-4k. Class K interdigitated capacitor metallization void criterion.

Class H	Class K
3.1.1.3 Metallization corrosion.	
a. Any metallization corrosion.	a. Same as class H. NOTE: Metallization having any localized discolored area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.
3.1.1.4 Metallization adherence.	
a. Any metallization lifting, peeling, or blistering. NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister. NOTE: These criteria are not applicable to undercutting or separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.	a. Same as class H.
3.1.1.5 Metallization protrusion.	
a. Protrusion of metallization that reduces the original separation between adjacent operating metallization by greater than 50 percent (see figure 2032-5h).	a. Same as class H.

FIGURE 2032-5h. Class H operating metallization protrusion criterion.

Class H	Class K
3.1.1.5 b. For interdigitated capacitors only, protrusion of metallization that reduces the original separation by greater than 50 percent (see figure 2032-6h).	3.1.1.5 b. Same as class H.

FIGURE 2032-6h. Class H interdigitated capacitor metallization protrusion criterion.

3.1.1.6 Metallization alignment.

a. A contact window that has less than 50 percent of its area covered by metallization.	a. Less than 75 percent.

Class H

3.1.1.6 b. A contact window that has less than a continuous 40 percent of its perimeter covered by metallization (see figure 2032-7h).
NOTE: When, by design, metallization is completely contained in a contact window, or does not cover the entire contact perimeter, 3.1.1.6a, area coverage, or 3.1.1.6b, perimeter coverage, can be deleted as applicable provided that the design criteria are satisfied.

FIGURE 2032-7h. Class H metallization alignment criteria.

* c. A metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil unless by design.

3.1.1.7 Metallization bumps or indentations.

a. For capacitors only, a bump or indentation in the overlaying metallization.

Class K

3.1.1.6 b. 50 percent of its perimeter (see figure 2032-7k).

FIGURE 2032-7k. Class K metallization alignment criteria.

c. Same as Class H.

a. Same as class H.

Class H	Class K
3.1.1.8 Metallized through-hole defects, "high magnification". No element shall be acceptable that exhibits:	
a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.	a. Same as class H.
3.1.1.9 Wrap-around connection defects, "high magnification". No element shall be acceptable that exhibits:	
a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-8h).	a. Same as class H.

FIGURE 2032-8h. Class H wrap-around connection unmetallized area criterion.

Class H	Class K
3.1.2 Passivation defects "high magnification". No element shall be acceptable that exhibits:	
a. Either multiple lines (color fringing) or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2032-8Ah). A passivation defect that exhibits a tine of separation from the metallization is acceptable. NOTE: These criteria apply to conductive substrate elements only. NOTE: Double or triple lines at the edge of the passivation defect indicate it can have sufficient depth to penetrate down to the bare substrate.	a. Same as class H.

FIGURE 2032-8Ah. Class H passivation defect criteria.

Class H	Class K
3.1.3 Glassivation defects, "high magnification". No device shall be acceptable that exhibits:	
NOTE: Criteria of 3.1.3 can be excluded when the defects are due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation defects, equal to or greater than 50 percent of the narrowest resistor width, (see figure 2032-9h).	

FIGURE 2032-9h. Class H laser trimmed glassivation defect criteria.

a. Glass crazing or damage that prohibits the detection of visual criteria contained herein.	a. Same as class H.

	Class H		Class K
3.1.3	b. Any lifting or peeling of the glassivation. NOTE: Lifting or peeling of the glassivation is acceptable when it does not extend more than 1.0 mil from the designed periphery of the glassivation, provided that the only exposure of metallization is of adjacent bonding pads or of metallization leading from those pads.	3.1.3	b. Same as class H.
	c. A void in the glassivation that exposes two or more adjacent operating metallization paths, excluding bonding pad cutouts, unless by design.		c. Same as class H.
	d. Unglassivated nonactive circuit areas greater than 5.0 mils in any dimension, unless by design.		d. Same as class H.
	e. Unglassivated areas at the edge of a bonding pad exposing the conductive substrate.		e. Same as class H.
	f. Glassivation covering more than 25 percent of a bonding pad area.		f. Same as class H.
	g. *Crazing in glassivation over a resistor.*		g. Same as class H.
	h. Misalignment of the glassivation that results in incomplete coverage of a resistor, unless by design.		h. Same as class H.
	i. Glassivation scratches or voids that expose any portion of a resistor or fusible link except for polycrystalline silicon links where the glassivation is opened by design.		i. Same as class H.
	j. Scratches in the glassivation that disturb metallization and bridge metallization paths.		j. Same as class H.
	k. Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallization paths.		k. Same as class H.

Class H	Class K
3.1.4 Substrate defects "high magnification". No element shall be acceptable that exhibits:	
* a. Less than 0.1 mil of separation between the operating metallization and the edge of the element unless by design (see figure 2032-10h). NOTE: For elements containing wraparound conductors or for bonding pads of RF/microwave elements that are coincident with the element edge (as documented on the design drawing) this criteria does not apply. When bond pad metallization is coincident with the element edge, a minimum separation of 1.0 mil shall exist between the bonding pad metallization at the element edge and any noncommon conductive surface.	a. Same as Class H.
b. A chipout that extends into the active circuit area (see figure 2032-10h).	b. Same as class H.

FIGURE 2032-10h. Class H separation and chipout criteria.

	Class H	Class K
* 3.1.4 c.	Any crack that exceeds 5.0 mils in length (see figure 2032-11h). NOTE: For fused quartz or crystalline substrates, no cracking is allowed.	3.1.4 c. Same as Class H.
d.	Any crack that does not exhibit 0.1 mil of separation from any active circuit area or operating metallization (see figure 2032-11h).	d. 0.25 mil (see figure 2032-11k).
e.	Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-11h).	e. Same as class H.

FIGURE 2032-11h. Class H crack criteria.

Class H	Class K
3.1.4 f. N/A	3.1.4 f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-12k).

FIGURE 2032-12k. Class K semicircular crack criterion.

g. An attached portion of an active circuit area from an adjacent element.	g. Same as class H.
h. Any crack that does not originate at an edge.	h. Same as class H.
i. Holes through the substrate, unless by design.	i. Same as class H.

Class H	Class K
3.1.5 Foreign material defects "low magnification". No element shall be acceptable that exhibits:	
a. For mounted elements, unattached, conductive foreign material on the surface of the elements. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization paths, active circuitry, or any combination of these. NOTE: If an element has an insulating layer (such as glassivation or self-passivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of unattached, conductive foreign material, that is large enough to bridge these features, is acceptable since the features are protected by the insulating layer. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.), or by a suitable cleaning process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 20 psig). NOTE: Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above. NOTE: Semiconductor particles are considered to be foreign material.	a. Same as class H.
b. Attached, conductive foreign material that bridges metallization paths, active circuitry, or any combination of these.	b. Same as class H.
c. Liquid droplets, ink drops, or chemical stains that appear to bridge any unglassivated or unpassivated active circuit areas.	c. Same as class H.
d. Attached foreign material that covers greater than 25 percent of a bonding pad area.	d. Same as class H.

Class H	Class K
3.1.6 Thin film resistor defects, "high magnification". No element shall be acceptable that exhibits:	
* a. Voids at the terminal that reduces the resistor width to less than 50 percent of the original resistor width (see figure 2032-13h).	a. Same as Class H

FIGURE 2032-13h. Class H film resistor width reduction at terminal by voids criterion.

* b. Neckdown at the terminal that reduces the resistor width to less than 75 percent of the original resistor width (see figure 2032-14h).	b. Same as Class H.

FIGURE 2032-14h. Class H film resistor width reduction at terminal by necking criterion.

		Class H			Class K
3.1.6	c.	Any sharp (clearly defined) color change within 0.1 mil of the terminal. NOTE: A sharp color change close to the terminal usually indicates an abrupt reduction of resistor film thickness. This color change usually occurs in a straight line parallel to the terminal. A gradual color change, or a nonuniform or mottled color anywhere in the resistor, is not cause for rejection.	3.1.6	c.	Same as class H.
	d.	Any resistor film lifting, peeling or blistering.		d.	Same as class H.
	e.	Reduction of resistor width, resulting from voids, scratches, or a laser trim kerf or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-15h). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.		e.	Same as class H.

FIGURE 2032-15h. Class H resistor width reduction by voids and scratches criteria.

	Class H	Class K
* 3.1.6 f.	Contact overlap between the metallization and the resistor in which the width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-16h).	3.1.6 f. Same as Class H.

FIGURE 2032-16h. Class H metal/resistor overlap criterion.

g.	Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 0.25 mil (see figure 2032-17h).	g. Same as class H.

FIGURE 2032-17h. Class H contact overlap criterion.

	Class H	Class K
3.1.6 h.	More than a 50 percent reduction of the original separation, between any two different resistors, or a resistor and metallization not associated with it (see figure 2032-18h).	3.1.6 h. Same as class H.

FIGURE 2032-18h. Class H resistor separation criteria.

i.	Any resistor that crosses a substrate irregularity (such as a void or scratch) (see figure 2032-19h). NOTE: This criterion is applicable to conductive substrates only.	i. Same as class H.

FIGURE 2032-19h. Class H substrate irregularity criterion.

Class H	Class K
3.1.6 j. Any increase in resistor width of a block resistor greater than 25 percent of the original resistor width (see figure 2032-20h).	3.1.6 j. Same as class H.

FIGURE 2032-20h. Class H resistor width increase criterion.

k. Protruding resistor material within the same resistor structure that reduces the original separation to less than 50 percent (see figure 2032-21h). NOTE: This criteria applies to protrusion of resistor material resulting from a photo-lithographic defect.	k. Same as class H.

FIGURE 2032-21h. Class H protusion of resistor material criterion.

Class H	Class K
3.1.6 l. Bridging within the same resistor pattern where the width of the bridge is less than 50 percent of the narrowest line being bridged (see figure 2032-22h).	3.1.6 l. Same as class H.

FIGURE 2032-22h. Class H bridging of resistor material criteria.

3.1.7 Laser trimmed thin film resistor defects, "high magnification". No element shall be acceptable that exhibits:
NOTE: The laser trim defect criteria contained in this section apply to active resistor areas only.

Class H	Class K
3.1.7 a. A kerf width less than 0.1 mil (see figure 2032-23h). NOTE: This does not apply to edge trimming.	3.1.7 a. Same as class H.

FIGURE 2032-23h. Class H kerf width criteria.

b. A kerf containing particles of detritus. NOTE: For resistor materials that are self-passivating (such as tantalum nitride), detritus in the kerf is allowed provided *that a clear path of at least 0.1 mil in* width exists in the kerf. Such detritus shall be attached. Verification of attachment shall be accomplished using the techniques described in 3.1.5a (see figure 2032-24h). NOTE: This does not apply to edge trimming.	b. Same as class H.

Class H | Class K

3.1.7 b. (Continued.)

FIGURE 2032-24h. Class H detritus criterion for self-passivating resistor materials.

NOTE: In the case of a resistor loop made with self-passivating resistor material which is similar in configuration to the one shown in figure 2032-25h, there shall be at least one kerf that contains a clear path of at least 0.1 mil in width; otherwise, the element shall be rejected.

FIGURE 2032-25h. Class H resistor loop element detritus criterion for self-passivating resistor materials.

		Class H			Class K
3.1.7	c.	Bridging of detritus between rungs in the active area of a resistor ladder structure (see figure 2032-26h). NOTE: Bridging of detritus in inactive areas is acceptable.	3.1.7	c.	Same as class H.

FIGURE 2032-26h. Bridging of detritus between rungs in the active area of a resistor ladder structure criterion.

Class H	Class K
3.1.7 d. No nicking or scorching is allowed except as permitted below. NOTE: This does not apply to rungs in a fine resistor ladder structure (see figure 2032-27h). NOTE: See 3.i.(33) for a definition of coarse and fine resistor ladder structures. The element drawing must be referenced to determine if a given resistor ladder structure is coarse or fine.	3.1.7 d. Same as class H.

FIGURE 2032-27h. Class H resistor ladder structure nicking and scorching criteria exceptions.

Class H | Class K

3.1.7 d. (Continued.)
NOTE: This criteria does not apply to the second rung of a resistor loop since the second rung is inactive. This criteria does not apply to a fine loop or to a resistor structure that is comprised of fine loops (see figure 2032-28h).

NOTE: See 3.i.(35) for a definition of coarse and fine resistor loop structures. The element drawing must be referenced to determine if a given resistor loop structure is coarse or fine.

		COARSE LOOPS	FINE LOOPS
NICK IN FIRST (ACTIVE) RUNG		REJECT	ACCEPT
SCORTCH IN FIRST (ACTIVE) RUNG		REJECT	ACCEPT
NICK IN SECOND (INACTIVE) RUNG		ACCEPT	ACCEPT
SCORTCH IN SECOND (INACTIVE) RUNG		ACCEPT	ACCEPT

FIGURE 2032-28h. Class H resistor loop nicking and scorching criteria exceptions.

Class H	Class K
3.1.7 d. (Continued.) NOTE: This criterion does not apply to the last rung of a resistor ladder if the last rung is inactive (see figure 2032-29h).	

FIGURE 2032-29h. Class H laser nicking criteria exception for the last rung of a resistor ladder.

e. A kerf or scorch which extends into a resistor ladder sidebar (see figure 2032-30h).	e. Same as class H.

FIGURE 2032-30h. Class H resistor ladder sidebar trim criterion.

Class H	Class K
3.1.7 f. Kerf or scorch misalignment (see figure 2032-31h).	3.1.7 f. Same as class H.

FIGURE 2032-31h. Class H laser trim misalignment criteria.

g. A kerf which extends into metallization and leaves less than 75 percent of the metallization width undisturbed (see figure 2032-32h). NOTE: Opening a metallization link by design is acceptable.	g. Same as class H.

FIGURE 2032-32h. Class H laser trim kerf extension into metallization criteria.

Class H	Class K
3.1.7 h. A kerf in a resistor, at the interface of the resistor material with the metallization, that leaves less than 50 percent of the original resistor width, unless by design. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded. (see figure 2032-33h).	3.1.7 h. Same as class H.

FIGURE 2032-33h. Class H resistor width reduction at metallization interface criteria.

i. A kerf in a resistor that leaves less than 50 percent of the original resistor width, unless by design. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded (see figure 2032-34h).	i. Same as class H.

FIGURE 2032-34h. Class H resistor width reduction by trimming criteria.

Class H	Class K
3.1.7 j. A kerf in a resistor that leaves less than 50 percent of the narrowest resistor width unless by design (see figure 2032-35h). NOTE: A floating kerf (one that is completely contained within the resistor) must meet this criteria. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	3.1.7 j. Same as class H.

FIGURE 2032-35h. Class H resistor width reduction and untrimmed resistor material criteria.

k. Pits into the silicon dioxide of conductive substrate elements in the kerf which does not show a line of separation between the pit and the resistor material (see figure 2032-36h).	k. Same as class H.

Class H | Class K

3.1.7 k. (Continued.)

FIGURE 2032-36h. Class H laser trim pitting criterion.

3.1.8 Multilevel thin film defects, "high magnification". No element shall be acceptable that exhibits:

a. Insulating material that does not extend beyond the width of the upper and lower metallization by 0.3 mil minimum (see figure 2032-37h).

a. Same as class H.

FIGURE 2032-37h. Class H insulating material extension criteria.

	Class H		Class K
3.1.8 b.	Voids in the insulating material.	3.1.8 b.	Same as class H.
c.	A bump or indentation in the upper (overlaying) metallization. NOTE: This criteria is not applicable to coupling (air) bridges.	c.	Same as class H.
d.	Scratch that completely crosses the metallization and damages the insulating material surface on either side.	d.	Same as class H.

3.1.9 Coupling (air) bridge defects "high magnification". No element shall be acceptable that exhibits:

Class H	Class K
a. A void in the coupling (air) bridge metallization that leaves less than 50 percent of the original metallization width undisturbed. (See figure 2032-37Ah).	a. Same as class H.
b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2032-37Ah).	b. Same as class H.
c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2032-37Ah).	c. Same as class H.
d. Attached, conductive foreign material that is greater, in any dimension, than 50 percent of the original coupling (air) bridge metallization width.	d. Same as class H.
e. No visible separation between the coupling air) bridge and the underlying operating metallization. NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2032-37Ah).	e. Same as class H.
f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2032-37Ah).	f. Same as class H.
g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.	g. Same as class H.

FIGURE 2032-37Ah. Class H and class K coupling (air) bridge criteria.

3.2 Planar thick film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thick film passive element. All inspection shall be performed at "low magnification" within the range of 10X to 60X magnification for both class H and class K.

Class H	Class K
3.2.1 Operating metallization defects "low magnification". No element shall be acceptable that exhibits: NOTE: The metallization defect criteria contained in this section apply to operating metallization only.	
3.2.1.1 Metallization scratches	
a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-38h). NOTE: Underlying material does not have to be exposed along the full length of the scratch. NOTE: This criteria does not apply to capacitors.	a. Same as Class H.

FIGURE 2032-38h. Class H metallization scratch criteria.

Class H

3.2.1.1 b. Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, to less than 50 percent its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-39h).

FIGURE 2032-39h. Class H metallization width reduction at bonding pad criteria.

c. Scratch or probe marks in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area.

Class K

3.2.1.1 b. Less than 75 percent (see figure 2032-39k).

FIGURE 2032-39k. Class K metallization width reduction at bonding pad criteria.

c. Same as class H

Class H	Class K
3.2.1.2 Metallization voids.	
a. Void(s) in the metallization, excluding *bonding pads, that leaves less than 50 percent* of the original metallization width undisturbed (see figure 2032-40h).	a. Same as Class H.

FIGURE 2032-40h. Class H metallization void criteria.

b. Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately. NOTE: Figures 2032-39h and 2032-39k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.	b. Less than 75 percent.
c. Void(s) in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area. NOTE: For RF microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.	c. Same as class H.

Class H	Class K
3.2.1.3 Metallization corrosion.	
a. Any metallization corrosion.	a. Same as class H.
3.2.1.4 Metallization adherence.	
a. Any metallization lifting, peeling, or blistering. NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister. NOTE: These criteria are not applicable to separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.	a. Same as class H.
3.2.1.5 Metallization protrusion.	
a. More than 50 percent reduction of the original design separation, between any protruding metallization and adjacent metallization paths (see figure 2032-41h).	a. Same as class H.

FIGURE 2032-41h. Class H metallization protrusion criterion.

Class H	Class K
3.2.1.6 Metallization overlap.	
a. Contact overlap between the upper and lower metallizations that is less than 50 percent of the designed contact overlap area (see figure 2032-42h). NOTE: The overlap area is that area in which the upper metallization actually contacts the lower metallization.	a. Same as class H.

FIGURE 2032-42h. Class H metallization overlap criterion.

Class H	Class K
3.2.1.7 Metallized through-hole defects, "low magnification". No element shall be acceptable that exhibits:	
a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.	a. Same as class H.
3.2.1.8 Wrap-around connection defects, "low magnification". No element shall be acceptable that exhibits:	
a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-43Ah).	a. Same as class H.

FIGURE 2032-43Ah. Class H wrap-around connection unmetallized area criterion.

Class H	Class K
3.2.2 Substrate defects, "low magnification". *No element shall be acceptable that exhibits:*	
a. Less than 1.0 mil separation between the operating metallization and the edge of the element unless by design (see figure 2032-43h). NOTE: This criterion does not apply to substrates designed for wraparound conductors.	a. Same as class H.
b. A chipout that extends into the active circuit area (see figure 2032-43h).	b. Same as class H.

FIGURE 2032-43h. Class H separation and chipout criteria.

* c. Any crack that exceeds 5.0 mils in length (see figure 2032-44h). NOTE: For fused quart or crystalline substrates, no cracking is allowed.	c. Same as Class H.
d. Any crack that does not exhibit 1.0 mil of separation from any active circuit area or operating metallization (see figure 2032-44h).	d. Same as class H.

Class H

Class K

FIGURE 2032-44h. Class H additional crack criteria.

3.2.2 e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-44h).

f. N/A

3.2.2 e. Same as class H.

f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-45k).

FIGURE 2032-45k. Class K semicircular crack criterion.

		Class H			Class K
3.2.2	g.	An attached portion of a circuit area from an adjacent element.	3.2.2	g.	Same as class H.
	h.	Any crack that does not originate at an edge.		h.	Same as class H.
	i.	Holes through the substrate, unless by design.		i.	Same as class H.
	j.	Patterned substrates having a section broken out around a substrate mounting hole (intended for substrate-to-post attachment) that is greater than 25 percent of the mounting hole circumference.		j.	Same as class H.

Class H	Class K
3.2.3 Thick film resistor defects, "low magnification". No element shall be acceptable that exhibits:	
* a. A reduction of the resistor at the terminal due to voids to less than 50 percent of the original resistor width (see figure 2032-46h).	a. Same as Class H.

FIGURE 2032-46h. Class H resistor width reduction at terminal caused by voids criterion.

* b. Reduction of the resistor at the terminal, due to neckdown less than 50 percent, to of the original resistor width (see figure 2032-47h).	b. Same as Class H.

Class H	Class K

FIGURE 2032-47h. Class H resistor width reduction at terminal by neckdown criterion.

Class H			Class K		
3.2.3	c.	Any resistor film lifting, peeling, or blistering.	3.2.3	c.	Same as class H.
	d.	Crack in the resistor greater than 1.0 mil in length. NOTE: Irregularities such as fissures in resistor material that are created during firing, and that do not expose the underlying material, are not considered to be cracks.		d.	Same as class H.
	e.	Evidence of resistor repair by overprinting or any other means.		e.	Same as class H.
	f.	Separation between any two resistors that is less than 50 percent of the original separation.		f.	Same as class H.
	g.	Separation between any resistor and conductor combination that is less than 50 percent of the original separation.		g.	Same as class H.
	h.	Increase in resistor width greater than 25 percent of the original design width.		h.	Same as class H.
	i.	Resistor that is closer than 1.0 mil to the edge of the substrate.		i.	Same as class H.

	Class H		Class K
3.2.3 j.	Reduction of resistor width resulting from voids, scratches, or chipouts, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-48h). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	3.2.3 j.	Same as class H.

FIGURE 2032-48h. Class H resistor width reduction criteria.

k.	Contact overlap between the metallization and the resistor in which the actual width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-49h).	k.	Less than 75 percent (see figure 2032-49k).

FIGURE 2032-49h. Class H resistor overlap criterion.

FIGURE 2032-49k. Class K resistor overlap criterion.

Class H	Class K
3.2.3 l. Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 3.0 mils (see figure 2032-50h).	3.2.3 l. Same as class H.

FIGURE 2032-50h. Resistor overlap criterion.

m. Voids or misalignment of glassivation that results in less than 90 percent coverage of the resistor area, unless by design.	m. Same as class H.
n. Crazing of glassivation over a resistor.	n. Same as class H.
o. Glassivation scratches, lifting, or peeling that expose any portion of a resistor.	o. Same as class H.

Class H	Class K
3.2.4 Trimmed thick film resistor defects, "low magnification". No element shall be acceptable that exhibits: NOTE: The trim defect criteria contained in this section apply to active resistor areas only.	
a. A kerf width less than 0.5 mil (see figure 2032-51h). NOTE: This does not apply to edge trimming.	a. Same as class H.

FIGURE 2032-51h. Class H kerf width criteria.

b. A kerf containing detritus.	b. Same as class H.
c. A kerf which extends into metallization and leave less than 75 percent of the metallization width undisturbed (see figure 2032-52h). NOTE: Opening a metallization link by design is acceptable.	c. Same as class H.

FIGURE 2032-52h. Class H laser trim kerf extension into metallization criteria.

Class H	Class K
3.2.4 d. A kerf that leaves less than 50 percent of the original width of a resistor, unless by design (see figure 2032-52Ah). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	3.2.4 d. Same as class H.

FIGURE 2032-52Ah. Class H resistor width reduction and untrimmed resistor material criteria.

e. A trim that does not originate from the edge of the resistor.	e. Same as class H.

3.2.5 Multilevel thick film defects, "low magnification". No element shall be acceptable that exhibits:

a. Any insulating material that does not extend beyond the width of the upper and lower metallization by 3.0 mils minimum (see figure 2032-53h).	a. Same as class H.

FIGURE 2032-53h. Class H dielectric extension criteria.

	Class H		Class K
3.2.5	b. Voids in the insulating material that expose underlying metallization.	3.2.5	b. Same as class H.
	c. Vias that are less than 50 percent of the original design area.		c. Same as class H.
	d. Scratch that completely crosses the metallization and damages the insulating material surface on either side.		d. Same as class H.

3.2.6 All thin film capacitors and those overlay capacitors used in GaAs microwave devices,"low magnification". No element shall be acceptable that exhibits:

a. Scratches that expose an underlying material.

b. Any peeling or lifting of the metallization.

c. Excess top metal which extend beyond the capacitor bottom metal.

d. Voids in the capacitor bottom metal which extend under the capacitor top metal.

e. Voids in the top metallization which leaves less than 75% of the metallization area undisturbed.

3.3 Nonplanar element inspection. Inspection for visual defects described in this section shall be conducted on each nonplanar passive element. The "low magnification" inspection shall be within the range of 10X to 60X.

	Class H	Class K
3.3.1	General nonplanar element defects, "low magnification". No element shall be acceptable that exhibits:	
	a. Peeling or lifting of any metallization.	a. Same as class H.
	b. Protrusion between metallization terminals that leaves less than 5.0 mils separation (see figure 2032-54h).	b. Same as class H.

FIGURE 2032-54h. Class H metallization protrusion criterion.

	Class H		Class K
3.3.1	c. *Lifting, blistering, or peeling* of insulation.	3.3.1	c. Same as class H.
	d. Voids in metallized terminals that expose underlying material over greater than 25 percent of any side of the metallized terminal area.		d. Same as class H.
3.3.2	Foreign material defects "low magnification". No element shall be acceptable that exhibits:		
	a. For mounted elements, unattached, conductive foreign material on the surface of the element. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization path, active circuitry, or any combination of these. NOTE: If an element has an insulating layer (such as glassivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of *unattached conductive foreign material* that is large enough to bridge these features is acceptable since the features are protected by the insulating layer. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.) by *a suitable cleaning* process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material. NOTE: Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.		a. Same as class H.
	b. Attached, conductive foreign material that bridges metallization paths, active circuitry, *or any combination of these.*		b. Same as class H.
	c. Liquid droplets, inkdrops, or any chemical stain that appear to bridge any unglassivated active circuit areas.		c. Same as class H.
	d. Attached foreign material that covers more than 25 percent of a bonding pad area.		d. Same as class H.

Class H	Class K
3.3.3 Ceramic chip capacitor defects "low magnification". No element shall be acceptable that exhibits:	
a. Crack, chip or void in the body that exposes metal plates, (see figure 2032-55h).	a. Same as class H.

FIGURE 2032-55h. Class H metal plate exposure criteria.

b. Crack that is greater than 50 percent of the width of the unmetallized sides, top, or bottom, or that extends around a corner (see figure 2032-56h).	b. Crack. NOTE: No cracks are allowed.

FIGURE 2032-56h. Class H crack criteria.

Class H	Class K
3.3.3 c. Evidence of separation (delamination) of metal plates or cracks along the plane of the metal plates (see figure 2032-57h). NOTE: Narrow grooves or channel less than 1.0 mil wide that exhibit a glass-like appearance and do not expose metal plates are acceptable.	3.2.3 c. Delamination. NOTE: No delamination is allowed.

FIGURE 2032-57h. Class H delamination criteria.

d. Crack or void in the metallization that exposes metal plates, or voids that are greater than 25 percent of the area of the metallized terminal (see figure 2032-58h).	d. Same as class H.

FIGURE 2032-58h. Class H termination defect criteria.

	Class H	Class K
3.3.3 e.	Void in the metallized edges of the element that are greater than 10 percent of the metallized edge dimension, or bare corners of metallized terminals (see figure 2032-59h). NOTE: This criteria ia applicable to solder attached elements only.	Same as class H.

FIGURE 2032-59h. Class H metallized edge defect criteria.

	f. Attached foreign material on the body that covers an area greater than 5.0 mils square on any side.	f. Same as class H.
3.3.4 Tantalum chip capacitor defects, "low magnification." No element shall be acceptable that exhibits:		
	a. Flaking or peeling of the encapsulant that exposes any underlying material.	a. Same as class H.
	b. A metallized terminal that is less than 90 percent free of encapsulant material.	b. Same as class H.
	c. Less than 50 percent continuous metallized terminal weld area without cracks.	c. Same as class H.
	d. Metallized terminal containing residue from the welding operation that is not firmly attached metallurgically to the anode cap.	d. Same as class H.

Class H	Class K
3.3.4 e. Metallized terminal not aligned as shown in the applicable drawing.	3.3.4 e. Same as class H.
f. Encapsulant preventing the metallized terminal from resting on the substrate bonding pads when the capacitor is in the bonding position except where the metallized terminal electrical contact is made by alternate means.	f. Same as class H.
g. Lifting, blistering or peeling of metallized terminal encapsulant.	g. Same as class H.
3.3.5 Parallel plate chip capacitor defects, "low magnification". No element shall be acceptable that exhibits:	
a. Metallization that extends greater than 50 percent around the edge of the capacitor (see figure 2032-60h).	a. Same as class H.

FIGURE 2032-60h. Class H metallization extension criterion.

3.3.5 b. Evidence of cracks in the dielectric body (see figure 2032-61h).	3.3.5 b. Same as class H.

FIGURE 2032-61h. Class H crack in dielectric criterion.

3.3.6 Inductor and transformer defects, "low magnification". No element shall be acceptable that exhibits:

a. Peeling, lifting or blistering of winding *metallization or insulation.*	a. Same as class H.
b. Evidence of shorts between adjacent turns or windings.	b. Same as class H.
c. Cracks or exposure of bare magnetic core material.	c. Same as class H.
d. Pits or voids in the core insulation greater than 5.0 mils area that expose the magnetic core material.	d. Same as class H.
e. Separation less than 5.0 mils between wire termination points of the same or adjacent windings.	e. Same as class H.
f. Missing polarity identification unless by design.	f. Same as class H.
g. *Operating metallization and multilevel* thick film defects as described in 3.2.1 and 3.2.5 herein.	g. Same as class H.

3.3.7 Chip resistor defects, "low magnification". No element shall be acceptable that exhibits:

a. Reduction of the resistor width resulting from voids, bubbles, nicks, or scratches, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-62h).	a. Same as class H.

FIGURE 2032-62h. Class H resistor width reduction criterion.

	Class H	Class K
* 3.3.7 b.	A kerf that leaves less than 50 percent of the original width of the resistor unless by design.	3.3.7 b. Same as class H.
c.	Metallized termination width less than 10.0 mils unless by design (see figure 2032-63h).	c. Same as class H.

FIGURE 2032-63h. Class H termination width criterion.

d.	A crack, chipout or void in the substrate greater than 3.0 mils in any direction (see figure 2032-64h).	d. Same as class H.

FIGURE 2032-64h. Class H substrate defect criteria.

Class H	Class K
3.3.7 e. Build-up of termination material on metallized termination areas greater than 3.0 mils high for weldable metallized terminations or 8.0 mils high for solderable metallized terminations (see figure 2032-65h).	3.3.7 e. Same as class H.

FIGURE 2032-65h. Class H termination material buildup criteria.

Class H	Class K
f. Termination material splattered throughout the resistor (see figure 2032-66h).	f. Same as class H.

FIGURE 2032-66h. Class H termination material splatter criteria.

3.4 Surface acoustic wave (SAW) element inspection. Inspection for visual defects described in this section shall be conducted on each SAW element. When inspection is performed prior to mounting, then SAW elements may be inspected using backlighting. All inspection shall be performed at "low magnification" within the range of 10X to 60X for both class H and class K.

3.4.1 Defect control. The manufacturer shall perform an audit on a weekly basis for the presence of process related defects which impact SAW device performance (e.g., metallization voids, metallization scratches, metallization bridging, or crystal material pits/scratches/chipouts). This audit may be satisfied during routine internal visual inspection. If the presence of process related defects are discovered, the manufacturer shall monitor for a defect pattern to be used for the improvement of process controls. The manufacturer shall document the results of his investigation and corrective action to eliminate trends. The intent of this procedure is to require monitoring of process related defects which affect SAW device performance but do not cause reliability degradation leading to eventual failure of device function.

Class H	Class K
3.4.2 Operating metallization defects "low magnification." No element shall be acceptable that exhibits:	
3.4.2.1 Metallization corrosion.	
a. Any metallization corrosion.	a. Same as class H.
3.4.2.2 Metallization adherence.	
a. Any metallization lifting, peeling or blistering.	a. Same as class H.
3.4.3 Substrate material defects "low magnification". No element shall be acceptable that exhibits:	
a. Any crack that exceeds 5.0 mils in length.	a. Same as class H.
b. Any crack that is within 0.1 mil of any active circuit area or operating metallization.	b. Same as class H.
c. Any crack exceeding 1.0 mil in length extending from the element edge directly toward the active circuit area or operating metallization.	c. Same as class H.

Class H	Class K
3.4.4 Foreign material defects "low magnification". No element shall be acceptable that exhibits:	
a. For mounted and unmounted elements, unattached conductive foreign material on the surface of the element that is large enough to bridge operating metallization paths. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with a mechanical device (i.e., needle, probe, pick, etc.) or by a suitable cleaning process approved by the acquiring activity, or by a nominal gas blow (approximately 20 psig). Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.	a. Same as class H.
b. Liquid droplets, ink drops, or chemical stains that appear to bridge unglassivated metallization.	b. Same as class H.
c. Attached foreign material that covers greater than 25 percent of a bonding pad area.	c. Same as class H.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Class H or class K visual requirements.

b. Where applicable, any conflicts with element design, topology or construction (see 3).

c. Where applicable, gauges, drawings and photographs that are to be used as standards for operator comparison (see 2).

d. Where applicable, magnifications other than those specified (see 3).

METHOD 2035

ULTRASONIC INSPECTION OF TAB BONDS

1. Purpose. The purpose of this method is to detect unbonded and insufficiently bonded sites in TAB (Tape automated bonding) devices in the open package condition, through the measurement of bond area by means of Scanning Laser Acoustic Microscope (SLAM) techniques. It establishes methods and criteria for ultrasonic inspection of these TAB semiconductor devices.

NOTES:

1. For various metallurgical constitutions, absolute strengths expressed as pull strengths per unit area of bond differ. A scalar equivalency must be established for each alloy and process, to relate bond area to anticipated bond strength.

2. The term TAB bond in this document refers to one of the multiplicity of bonds, inner lead (ILB) or outer lead (OLB) formed by a tape automated bonding (TAB) process. In the case of ILB, it refers to that area of the device defined by the intersection of the beam lead, the semiconductor bonding pad area, and the contact outline of the thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the semiconductor die surface and the beam lead. In the case of OLB, it refers to that area of the device defined by the intersection of the beam lead, the substrate bonding pad area, and contact outline of thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the substrate surface and the beam lead.

3. The terms ultrasonic inspection and SLAM as used in this document refer to the process and instrument performing high frequency ultrasonic inspection and produce grey-scale images of the internal features of devices by means of scanning laser acoustic microscopy, and by which bond area measurement may be performed.

2. Apparatus. The apparatus and materials for this evaluation shall include:

a. Ultrasonic imaging equipment of the scanning laser acoustic microscope type, of frequency and resolution sufficient to penetrate the bond area and render an image which discloses the size and shape of the bond area with a linear dimensional allowance no greater than 20 percent of a bond dimension. Frequency is dictated by consideration of the wavelength of sound in the materials and the limit of resolution. Whereas lower frequencies have been used for inspection of larger scale device types, the present size of TAB sites requires frequencies of from one hundred to several hundred megahertz.

b. A visual output/storage device. A method of producing, displaying, and storing a scale image of adequate grey-scale range (minimum of 64 levels) shall be used. Such device may include a grey-scale printer/plotter, or preferably CRT display with an image digitizer capable of rendering images in digital code for bulk media storage and retrieval, and algorithmic processing and evaluation. The images so stored shall be suitable for manual, or preferably, automated analysis. The output devices shall be capable of producing and storing the images to a spatial and grey-scale resolution at least equal to the resolution of their acquisition by the ultrasonic imaging equipment. The output/storage device must be capable of presenting, storing, and retrieving image label information.

3. Procedure. The equipment used shall be adjusted as necessary to obtain satisfactory images of good contrast to achieve maximum image detail within the sensitivity requirements of the bond type being examined. The appropriate operator methodology will be used to insure adequate positioning and insonification (irradiation by ultrasound) of the device for purposes of producing its image. Additional protocols will be followed as required. The normal intrinsic strength of the bond metallurgy shall be known and established, and the metallurgy of the devices to be tested should be qualified as in agreement with that strength.

3.1 Calibration of the instrument. When specified, at least one device of the type and construction to be tested shall be available to set up the ultrasonic inspection equipment and peripherals. The device may be a scape non-operational device with TAB bonded leads which will be used to identify device landmarks and ensure the equipment is properly functional.

3.2 Labeling and identifying. The devices tested and the image records made of them shall be labeled in a standard format to include the following information:

a. Device manufacturer's name or code identification number.

b. Device type or part number.

c. Production lot number and/or inspection date code lot number.

d. Ultrasonic image view number and date; to include description or code for the region or bond number (s) viewed.

e. Device serial/cross reference number if applicable.

f. Ultrasonic operator identification.

3.3 Serialized devices. When device serialization is required, each device shall be readily identifiable by a serial number, and this serial number must be included in a form readable in the stored image. In the event of a skipped piece in the serialization, a blank space representing the skipped piece, and labeled with its serial number should appear in the storage medium. In the event of a large contiguous range of skipped pieces, a similar blank space advising of the range of pieces skipped should appear in the storage medium in place of the large physical space of the many skips.

3.4 Data back-up. When required, data back-up shall be specified from a choice of multiple floppy disk, multiple track data tape, or a video format tape, or other options having sufficient volume, resolution, speed, and reliability to suit the requirements for storage and labeling.

3.5 Mounting. The devices shall be mounted for ultrasonic inspection in a fixture which insures correct positioning in all dimensions, and adequately safeguards the potentially fragile bonds from mechanical contact with any substance other than the coupling fluid. Positioning thereafter must continue in a fashion which continues the above condition, and furthermore exposes each inspected bond area to the correct acoustic environment and portion of the instrumental field.

3.6 Angle of insonification. The angle of insonification must be specified by prior analysis, and if the mounting fixture is goniometrically agile it must be set to the correct angle by adjustment or selection.

3.7 Conditions of operation. Adjustments, selections, options, and settings used in the performance of the ultrasonic inspection must be recorded if they are of a nature critical to the proper operation of equipment; not to be recorded are those casual adjustments which are done as an obvious matter of course, and the performance of which are guided by such rules as trimming for maximum, minimum, or optimum, and which are not controlled by calibrated interfaces.

3.8 Operating personnel. Operating personnel shall have a basic familiarity of the nature of sound and the use of ultrasonic instruments in the inspection of devices. They shall be specifically trained and certified in the operation of the ultrasound and peripheral equipment used so that defects revealed by the method can be validly interpreted and compared with applicable standards.

3.9 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results from the ultrasonic inspection, and list the purchase order number, or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of the test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

3.10 Acoustic micrograph and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report, for the period specified.

3.11 Examination and acceptance criteria. Once the manufacturer has established the total bond area to be sought, based upon studies of the device to be bonded, and the inclusion of a prudent excess margin, then the following shall be considered the minimum bond area percentage:

a. In the case of solder bonds of lead-tin alloys a bond area percentage of 75 percent of the total bond area shall be considered minimum.

b. In the case of gold-tin eutectic and gold-gold thermocompression, a bond area percentage of 50 percent of the total bond area shall be considered minimum, except in the case of lead misalignment; when lead misalignment is a contributing factor a bond area percentage of 75 percent shall be considered minimum.

In the examination of devices, the following aspects shall be considered unacceptable bonding, and devices which exhibit any of the following defects shall be rejected:

a. A bond having a total bond area less than the minimum bond area. The failure may be caused by any reason, including lateral or longitudinal misalignment.

b. A bond meeting the minimum bond area, but with this area being discontinuous so that no single bonded area meets or exceeds the minimum bond area.

4. Summary. The following details shall be specified in the applicable acquisition document:

a. Number of views to be taken by SLAM inspection of each piece or bonding site, in accordance with 3.10, if other than one view.

b. Markings of devices, or labeling of images, if other than in accordance with 3.2, or special markings of devices to indicate that they have been ultrasonically imaged, if required.

c. Defects to be sought in the devices, and criteria for acceptance or rejection, if other than in 3.11.

d. Image and report retention when applicable (see 3.10).

FIGURE 2035-1. Bond area.

FIGURE 2035-2. Acceptable bond area.

FIGURE 2035-3. Rejectable bond area.

FIGURE 2035-4. Rejectable discontinuous bond area.

FIGURE 2035-5. Lateral misaligned bond area.

FIGURE 2035-5. Longitudinal misaligned bond area.

METHOD 3001.1

DRIVE SOURCE, DYNAMIC

1. PURPOSE. This method establishes a drive source to be used in measuring dynamic performance of digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The drive source shall supply a smooth transition between specified voltage levels. The signal characteristics shall not vary outside of their prescribed tolerances when interfaced with the device under test (device in the test socket).

3. PROCEDURE. The drive source shall be measured at the input terminal of the test socket (no device in the test socket). Figure 3001-1 shows typical driving source waveforms and should be used specifying the parameters shown, unless otherwise stated in the applicable acquisition document.

3.1 Pulse amplitude. The specified HIGH level of the driving source shall be greater than the V_{OH} of the device. The specified LOW level of the driving source shall be less than V_{OL} of the device.

3.2 Transition times. The transition times of the driving source (t_{THL} and t_{TLH}) shall be faster than the transition time of the device being tested, unless otherwise stated in the acquisition document. The transition times shall normally be measured between the 10 percent and 90 percent levels of the specified pulse.

3.3 Pulse repetition rate (PRR). Unless the pulse repetition rate is the parameter being tested, it shall be chosen so that doubling the rate or reducing by a half will not affect the measurement results.

3.4 Duty factors (duty cycles). The duty cycles of the driving source shall be chosen so that a 10 percent variation in the duty cycle will not affect the measurement results. The duty cycle shall be defined with respect to either a positive or negative pulse. The pulse width (t_p) of the input pulses shall be measured between the specified input measurement levels. When more than one pulse input is needed to test a device, the duty cycle of the prime input (i.e., clock, etc.) shall be specified. The phase relationship of all other input pulses shall be referenced to the prime input pulse.

4. SUMMARY. The following details, when applicable, shall be specified in the applicable acquisition document:

a. Levels V_{IL} and V_{IH}.

b. Driving signal transition times.

c. Pulse repetition rate.

d. Duty factors.

e. Recommended pulse generator, if required.

f. Input measurement levels, if other than those shown in figure 3001-1.

FIGURE 3001-1. Drive sources.

METHOD 3002.1

LOAD CONDITIONS

1. PURPOSE. This method establishes the load conditions to be used in measuring the static and dynamic performance of digital microelectronic devices such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The load for static tests shall simulate the worst case conditions for the circuit parameters being tested. The load for dynamic tests shall simulate a specified use condition for the parameters being tested. The loads shall be specified in the applicable acquisition document.

2.1 Discrete component load. The load will consist of any combination of capacitive, inductive, resistive, or diode components.

2.1.1 Capacitive load (C_L). The total load capacitance of the circuit under test shall include probe and test fixture capacitance and a compensating capacitor as required. The value of the capacitance, measured at 1 MHz ±10 percent, shall be specified in the applicable acquisition document.

2.1.2 Inductive load (L_L). The total load inductance of the circuit under test shall include probe and test fixture inductance and a compensating inductor as required. The value of the inductance, measured at 1 MHz ±10 percent, shall be specified in the applicable acquisition document.

2.1.3 Resistive load (R_L). The resistive load shall represent the worst case fan out conditions of the device under test for static tests and a specified fan out condition for dynamic tests. For sink loads, the resistor shall be connected between the power supply (V_{CC} or V_{DD}) and the circuit output for TTL, DTL, RTL, C-MOS, and MOS (N-Channel) and between circuit output and ground for MOS (P-Channel). For source loads, the resistor shall be connected between circuit output and ground for TTL, DTL, RTL, C-MOS, and MOS (N-Channel) and between V_{DD} and the circuit output for MOS (P-Channel). For ECL devices, the load resistors are connected from the output to a specified negative voltage.

2.1.4 Diode load (D_L). The diode load shall represent the input diode(s) of the circuit under test. The equivalent diode, as specified in the applicable acquisition document, will also represent the base-emitter or base-collector diode of any transistor in the circuit path of the normal load.

2.2 Dynamic load change. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular family of circuits being tested. One method of accomplishing this dynamic change is to simulate devices or use actual devices from the same logic family equal to the specified load.

3. PROCEDURE. The load will normally be paralleled by a high impedance voltage detection indicator. The indicator may be either visual or memory storage.

4. SUMMARY. The following shall be defined in the applicable acquisition document:

a. Capacitive load (see 2.1.1).

b. Inductive load (see 2.1.2).

c. Resistive load (see 2.1.3).

d. Diode load, the 1NXXX number and any associated critical parameters shall be specified (see 2.1.4).

e. Negative voltage, when using a resistive load for ECL (see 2.1.3).

METHOD 3003.1

DELAY MEASUREMENTS

1. PURPOSE. This method established the means for measuring propagation delay of digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

1.1 Definitions. The following definitions for the purpose of this test method shall apply.

1.1.1 Propagation delay time (t_{PHL}). The time measured with the specified output changing from the defined HIGH level to the defined LOW level with respect to the corresponding input transition.

1.1.2 Propagation delay time (t_{PLH}). The time measured with the specified output changing from the defined LOW level to the defined HIGH level with respect to the corresponding input transition.

2. APPARATUS. Equipment capable of measuring elapsed time between the input signal and output signal at any percentage point or voltage point between the maximum LOW level and minimum HIGH level shall be provided. The input shall be supplied by a driving source as described in method 3001 of this standard. It is desirable for this equipment to have data logging capability so that circuit dynamic performance can be monitored. The test chamber shall be capable of maintaining the device under test at any specified temperature.

3. PROCEDURE. The test circuit shall be loaded according to method 3002 of this standard. The driving signal to the test circuit shall be provided according to method 3001 of this standard. The device shall be stabilized at the specified test temperature.

3.1 Measurements at a voltage point. t_{PLH} and t_{PHL} shall be measured from the threshold voltage point on the driving signal to the threshold voltage point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. The device under test shall be conditioned according to the applicable acquisition document with nominal bias voltages applied. Figures 3003-1 and 3003-2 show typical delay measurements.

3.2 Measurements at percentage points. t_{PLH} and t_{PHL} shall be measured from a specified percentage point on the driving signal to a specified percentage point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. The device under test shall be conditioned according to the applicable acquisition document with nominal bias voltages applied. Figures 3003-1 and 3003-2 show typical delay measurements.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. t_{PLH} and t_{PHL} limits.

b. Parameters of the driving signal: t_{THL}, t_{TLH}, high Level, low Level, pulse width, repetition rate.

c. Load conditions.

d. Conditioning voltages (static or dynamic).

e. Measurement points (see 3.1 and 3.2).

f. Power supply voltages.

g. Test temperature.

FIGURE 3003-1. Propagation delay-positive input pulse.

FIGURE 3003-2. Propagation delay - negative input pulse.

METHOD 3004.1

TRANSITION TIME MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the output transition times of digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

1.1 Definitions. The following definitions shall apply for the purpose of this method.

1.1.1 Rise time (t_{TLH}). The transition time of the output from 10 percent to 90 percent or voltage levels of output voltage with the specified output changing from the defined LOW level to the defined HIGH level.

1.1.2 Fall time (t_{THL}). The transition time of the output from 90 percent to 10 percent or voltage levels of output voltage with the specified output changing from the defined HIGH level to the defined LOW level.

2 APPARATUS. Equipment capable of measuring the elapsed time between specified percentage points (normally 10 percent to 90 percent on the positive transition and 90 percent to 10 percent on the negative transition) or voltage levels. The test chamber shall be capable of maintaining the device under test at any specified temperature.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. The device under test shall be loaded as specified in the applicable acquisition document. The load shall meet the requirements specified in method 3002 of this document. The driving signal shall be applied as specified in method 3001 or the applicable acquisition document.

3.1 Measurement of t_{TLH} and t_{THL}. Unless otherwise stated, the rise transition time (t_{TLH}) shall be measured between the 10 percent and 90 percent points on the positive transition of the output pulse and the fall transition time (t_{THL}) shall be measured between the 90 percent and 10 percent points on the negative transition of the output pulse. The device under test shall be conditioned according to the applicable acquisition document with nominal bias voltages applied. Figure 3004-1 shows typical transition time measurement.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. t_{TLH} limits.

b. t_{THL} limits.

c. Transition time measurement points if other than 10 percent or 90 percent.

d. Parameters of the driving signal.

e. Conditioning voltages (static or dynamic).

f. Load condition.

g. Power supply voltages.

h. Test temperature.

FIGURE 3004-1. Transition time measurements.

METHOD 3005.1

POWER SUPPLY CURRENT

1. PURPOSE. This method establishes the means for measuring power supply currents of digital microelectronic devices such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. Equipment capable of applying prescribed voltage to the test circuit power supply terminals and measuring the resultant currents flowing in these terminals shall be provided. The test chamber shall be capable of maintaining the device under test at any specified temperature.

3. PROCEDURE. The device shall be stabilized at the specified test temperature.

3.1 I_{CCH} (logic gate). Inputs of the device under test shall be conditioned in such a way as to provide a HIGH level at the output, the worst case supply voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.2 I_{CCL} (logic gate). Inputs of the device under test shall be conditioned in such a way as to provide a LOW level at the output, the worst case supply voltages(s) shall be applied and the resultant current flow in the supply terminals measured.

3.3 I_{CC} or I_{EE} of combinatorial digital circuits. The inputs of the device under test shall be conditioned to put the device into its worst case power dissipating state. The current flowing into the V_{CC}, (positive supply) terminal, or out of the V_{EE} (negative supply) terminal shall be measured with the V_{CC} and V_{EE} voltages at their maximum specified operating levels.

3.4 I_{CC} or I_{EE} of sequential digital circuits. The inputs of the device under test shall be exercised to put the device in a known output state (either HIGH or LOW) that causes worst case power dissipation. The current flowing into the V_{CC} (positive supply) terminal, or out of the V_{EE} (negative supply) terminal shall be measured with the V_{CC} and V_{EE} voltages at their maximum specified operating levels.

3.5 I_{DD} (MOS logic gate). Inputs of the device under test shall be conditioned in such a way as to provide a HIGH level at the output of MOS (P-Channel and C-MOS) or a LOW level at the output of MOS (N-Channel and C-MOS); worst case voltage(s) shall be applied and the resultant current in the supply terminals measured.

3.6 I_{GG} (MOS P-Channel and N-Channel logic gates). Inputs of the device under test shall be conditioned in such a way as to provide a HIGH level at the output of MOS (P-Channel) or a LOW level at the output of MOS (N-Channel); worst case voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.7 I_{DD} of MOS combinatorial circuits. See 3.3 above.

3.8 I_{DD} of MOS sequential circuits. See 3.4 above.

3.9 I_{GG} of MOS combinatorial circuits. See 3.3 above.

3.10 I_{GG} of MOS sequential circuits. See 3.4 above.

3.11 I_{DD} dynamic (MOS logic gating and flip flop circuits). The driving signal to the test circuit shall be provided according to method 3001 of this standard; the worst case voltage(s) shall be applied and the resultant average current in the supply terminals measured.

4. SUMMARY. *The following details shall be specified in the applicable acquisition document:*

   a. Test temperature.

   b. Power supply voltages.

   c. I_{CCH}, I_{CCL}, I_{DD}, I_{GG}, and I_{EE} limits.

   d. Conditioning voltages.

   e. Dynamic input parameters (see 3.11).

METHOD 3006.1

HIGH LEVEL OUTPUT VOLTAGE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to HIGH level output drive, which may be specified as a minimum value V_{OH} min. or as a maximum V_{OH} max. This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The test instrument shall be capable of loading the output of the circuit under test with the specified positive or negative currents (I_{OH}). Resistors may be used to simulate the applicable current levels. The test instrument shall also be capable of supplying the worst case power supply and input voltages. The test chamber shall be capable of maintaining the device under test at any specified test temperature.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall be applied to the test circuit to provide a HIGH level output. Forcing current, equal to the circuit worst case high level fan out, shall then be applied to the test circuit output terminal and the resultant output voltage measured. The output measurement shall be made after each input is conditioned.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Current to be forced from or into output terminal.

   c. Power supply voltage(s).

   d. Input levels.

   e. V_{OH} min. or V_{OH} max. limits.

METHOD 3007.1

LOW LEVEL OUTPUT VOLTAGE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document with regard to LOW level output drive which is specified as a maximum value (V_{OL} max) or a minimum value (V_{OL} min). This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The test instrument shall be capable of loading the output of the circuit under test with the specified positive or negative currents (I_{OL}). Resistors may be used to simulate the applicable current levels. The test instrument shall be capable of supplying the worst case power supply and input voltages. The test chamber shall be capable of maintaining the device under test at any specified temperature.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall be applied to the test circuit to provide a LOW level output. Forcing current, equal to the circuit worst case LOW level fan out, shall be applied to the test circuit output and the resultant output voltage measured. The output measurement shall be made after each input is conditioned.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Current to be forced into or from the output terminal.

   c. Power supply voltage(s).

   d. Input levels.

   e. V_{OL} max or V_{OL} min limits.

METHOD 3008.1

BREAKDOWN VOLTAGE, INPUT OR OUTPUT

1. PURPOSE. This method establishes the means for assuring device performance to the limits specified in the applicable acquisition document in regard to input and output breakdown voltage symbolized as V_{IH} (max), V_{OH} (max), V_{IL} (min), and V_{OL} (min) as applicable. This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified temperature.

2.1 Method A. This test is generally performed to assure that breakdown does not occur on a device. An instrument shall be provided that has the capability of forcing a specified voltage at the input or output terminal of the test circuit and measuring the resultant current flowing in that terminal. The test instrument shall also have the capability of applying voltage levels to all other terminals. Care should be taken to assure that the test equipment does not inadvertently apply voltage to the device under test that will exceed the maximum rating of each terminal and that the current from the test equipment is sufficiently limited so that the device is not destroyed. This method can also be used to test the ability of power supply terminals to withstand a voltage overload.

2.2 Method B. This test is generally performed to assure that breakdown does occur on a device as specified in the applicable acquisition document. An instrument shall be provided that has the capability of forcing a specified current at the input or output terminal of the test circuit and measuring the resultant voltage at that terminal. The test instrument shall also have the capability of applying voltage levels to all other terminals. Care should be taken to assure that the test equipment does not inadvertently apply voltage to the device under test that will exceed the maximum rating of each terminal so that the device is not destroyed. The minimum compliance voltage of the current source shall be specified when applicable.

3. PROCEDURE. The device shall be stabilized at the specified test temperature.

3.1 Method A. All terminals, with the exception of the test terminal, shall be conditioned according to the applicable acquisition document. A prescribed voltage shall be applied to the designated input or output terminal and the resultant current measured. When testing for breakdown, all input and output terminals shall be tested individually. At the conclusion of the test, the device shall be functional.

3.2 Method B. All terminals, with the exception of the test terminal, shall be conditioned according to the applicable acquisition document. The specified current shall be forced at the designated input or output terminal, and the voltage at the terminal measured. At the conclusion of the test, the device shall be functional.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test temperature.

b. Forced voltages (method A).

c. Conditioning voltages for all other terminals.

d. Forced current (method B).

e. Maximum breakdown current limits (method A).

f. Minimum breakdown terminal voltage (method B).

METHOD 3009.1

INPUT CURRENT, LOW LEVEL

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to LOW level input load which may be specified as a minimum value (I_{IL} min) or as a maximum value (I_{IL} max). This method applied to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified test temperature. An instrument shall be provided that has the capability of applying the worst case LOW voltage to the input terminal of the test circuit, (and worst case levels on the other inputs), and measuring the resultant current at the input terminal.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Worst case power supply voltages and worst case input voltages shall be applied to the test circuit and the resultant current at the input terminal shall be measured. Inputs shall be tested individually.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Power supply voltages.

   c. Input voltage.

   d. Voltages at other input terminals which cause worst case current at the input under test.

   e. I_{IL} max or I_{IL} min.

METHOD 3010.1

INPUT CURRENT, HIGH LEVEL

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to HIGH level input load which may be specified as a maximum value (I_{IH} max) or a minimum value (I_{IH} min). This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified temperature. An instrument shall be provided that has the capability of applying the worst case HIGH voltage to the input terminal of the test circuit, and worst case levels at the other inputs, and measuring the resultant current at the input terminal.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Worst case power supply voltages and worst case input voltages shall be applied to the test circuit and the resultant current at the input terminal shall be measured. Inputs shall be tested individually.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Power supply voltages.

   c. Input voltage.

   d. Input voltages at other input terminals which cause worst case current at the input under text.

   e. I_{IH} max.

METHOD 3011.1

OUTPUT SHORT CIRCUIT CURRENT

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to output short circuit current (I_{OS}). This method applied to digital microelectronic devices, such as TTL, DTL, RTL, and MOS.

2. APPARATUS. A test chamber capable of maintaining the device under test at any specified temperature. An instrument will be provided that has the capability of forcing a voltage specified in the applicable acquisition document at the output terminal of the device under test and measuring the resultant current flowing in that terminal. The test instrument shall also have the capability of applying specified voltage levels to all other inputs.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Each output per package shall be tested individually.

3.1 TTL, DTL, RTL, MOS (P-Channel and N-Channel). Inputs of the device under test shall be conditioned in such a way as to provide a HIGH level at the output for TTL, DTL, RTL, and MOS (N-Channel) and a LOW level at the output for MOS (P-Channel). The output terminal shall be forced to 0 volt potential and the resultant current flow measured.

3.2 C-MOS I_{OSH}. Inputs of the device under test shall be conditioned in such a way as to provide a HIGH level at the output. The output terminal shall be forced to 0 volt potential and the resultant current flow measured.

3.3 C-MOS I_{OSL}. Inputs of the device under test shall be conditioned in such a way as to provide a LOW level at the output. The output terminal shall be forced to a voltage potential specified in the acquisition document and the resultant current flow measured.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test temperature.

b. Input conditioning voltages.

c. Power supply voltages.

d. I_{OS} max and I_{OS} min limits.

METHOD 3012.1

TERMINAL CAPACITANCE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to terminal capacitance. This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. The instrument shall be capable of applying a 1 MHz controllable amplitude signal superimposed on a variable plus or minus dc voltage. The instrument will also have the capability of measuring the capacitance of this terminal to within the limits and tolerance specified in the applicable acquisition document.

3. PROCEDURE. This test may be performed at 25°C ±3°C. The capacitance measuring bridge shall be connected between the input or output terminal and the ground terminal of the test circuit. The bridge shall be adjusted for a signal of 1 MHz, riding a bias level specified in the applicable acquisition document; the signal amplitude shall not exceed 50 mV rms. With no device in the test socket the bridge shall then be zeroed. For capacitance values below 20 pF, the device shall be connected directly to the bridge with leads as short as possible to avoid the effects of lead inductance. After inserting the device under test and applying the specified bias conditions, the terminal capacitance shall be measured and compared to the limits listed in the applicable acquisition document.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Circuit bias conditions.

   b. Bias level at which measurements are to be made.

   c. Maximum capacitance limits.

METHOD 3013.1

NOISE MARGIN MEASUREMENTS FOR DIGITAL MICROELECTRONIC DEVICES

1. PURPOSE. This method establishes the means of measuring the dc (steady- state) and ac (transient) noise margin of digital microelectronic devices or to determine compliance with specified noise margin requirements in the applicable acquisition document. It is also intended to provide assurance of interchangeability of devices and to eliminate misunderstanding between manufacturers and users on noise margin test procedures and results. The standardization of particular combinations of test parameters (e.g., pulse width, pulse amplitude, etc.) does not preclude the characterization of devices under test with other variations in these parameters. However, such variations shall, where applicable, be provided as additional conditions of test and shall not serve as a substitute for the requirements established herein.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

a. Noise margin. Noise margin is defined as the voltage amplitude of extraneous signal which can be algebraically added to the noise-free worst case "input" level before the output voltage deviates from the allowable logic voltage levels. The term "input" (in quotation marks) is used here to refer to logic input terminals or ground reference terminals.

b. DC noise margin. DC noise margin is defined as the dc voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output exceeds the allowable logic voltage levels.

c. AC noise margin. AC noise margin is defined as the transient or pulse voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output voltage exceeds the allowable logic voltage levels.

d. Maximum and minimum. Maximum and minimum refer to an algebraic system where "max" represents the most positive value of the range and "min" represents the least positive value of the range.

1.2 Symbols. The following symbols shall apply for the purposes of this test method and shall be used in accordance with the definitions provided (see 1.2.1, 1.2.2, and 1.2.3) and depicted on figures 3013-1, 3013-2, and 3013-3.

1.2.1 Logic levels.

V_{IL} max: The maximum allowed input LOW level in a logic system.

V_{IL} min: The minimum allowed input LOW level in a logic system.

V_{IH} max: The maximum allowed input HIGH level in a logic system.

V_{IH} min: The minimum allowed input HIGH level in a logic system.

V_{OL} max: The maximum output LOW level specified for a digital microelectronic device.
V_{OL} max is also the noise-free worst case input LOW level, V_{OL} (max) $\leq V_{IL}$ (max)

V_{OH} min: The minimum output HIGH level specified for a digital microelectronic device.
V_{OH} min is also the noise-free worst case input HIGH level, V_{OH} (min) $\geq V_{IH}$ (min)

Noise margin levels.

V_{NL}: The LOW level noise margin or input voltage amplitude which can be algebraically added to V_{OL} (max) before the output level exceeds the allowed logic level.

V_{NH}: The HIGH level noise margin or input voltage amplitude which can be algebraically added to V_{OH} (min) before the output level exceeds the allowed logic level.

V_{NG+}: The positive voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NG-}: The negative voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP+}: The positive voltage which can be algebraically added to the noise-free worst case most positive power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP-}: The negative voltage which can be algebraically added to the noise-free worst case most negative (least positive) power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

1.2.3 Noise pulse widths.

t_{PL}: The LOW level noise pulse width, measured at the V_{IL} (max) level.

t_{PH}: The HIGH level noise pulse width, measured at the V_{IH} (min) level.

2. APPARATUS. The apparatus used for noise margin measurements shall include a suitable source generator (see 2.1), load (see 2.2), and voltage detection devices for determining logic state.

2.1 Source generator. The source generator for this test shall be capable of supplying the required ac and dc noise inputs. In the case of pulsed inputs the transition times of the injected noise pulse shall each be maintained to less than 20 percent of the pulse width measured at the 50 percent amplitude level. For the purpose of this criteria, the transition times shall be between the 10 percent and 90 percent amplitude levels. The pulse repetition rate shall be sufficiently low that the element under test is at steady-state conditions prior to application of the noise pulse. For the purpose of this criteria, doubling the repetition rate or duty cycle shall not affect the outcome of the measurement.

2.2 Load. The load for this test shall simulate the circuit parameters of the normal load which would be applied in application of the device under worst-case conditions. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular device load. The load shall be paralleled by a high impedance voltage detection device.

3. PROCEDURE. The device shall be connected for operation using a source generator and load as specified (see 2), and measurements shall be made of V_{NL}, V_{NH}, V_{NG}, V_{NP}, t_{PL}, and t_{PH} following the procedures for both ac noise margin and dc noise margin (see 3.2 through 3.3.3).

3.1 General considerations.

3.1.1 Nonpropagation of injected noise. As defined in 1.1, noise margin is the amplitude of extraneous signal which may be added to a noise-free worst case "input" level before the output breaks the allowable logic levels. This definition of noise margin allows the measurement of both dc and ac noise immunity on logic inputs or power supply lines or ground reference lines by detection of either a maximum LOW level or a minimum HIGH level at the output terminal. Since the output level never exceeds the allowable logic level under conditions of injected noise, the noise is not considered to propagate through the element under test.

3.1.2 Superposition of simultaneously injected noise. Because the logic levels are restored after one stage, and because the noise margin measurement is performed with all "inactive" inputs at the worst case logic levels, the proper system logic levels are guaranteed in the presence of simultaneous disturbances separated by at least one stage.

3.1.3 Characterization of ac noise margin. Although the purpose of this standard test procedure is to insure interchangeability of elements by a single- point measurement of ac noise margin, the test procedure is well suited to the measurement of ac noise margin as a function of noise pulse width. In particular, for very wide pulse widths, the ac noise margin asymptotes to a value identically equal to the dc noise margin.

3.2 Test procedure for dc noise margin.

3.2.1 Worse case configuration. The measurement of dc noise margin using a particular logic input terminal should correspond to the worst case test configuration in the applicable acquisition document. For example, the measurement of LOW level noise margin for a positive-logic inverting NAND gate should be performed under the same worst case test conditions as the dc measurement of V_{OH} (min). If the worst case dc test conditions for V_{OH} (min) are high power supply voltage, all unused logic inputs connected to V_{OH} (min) and output current equal to zero, these conditions should be applied to the corresponding dc noise margin measurement.

3.2.2 LOW level noise margin, V_{NL}. The LOW level noise margin test is normally performed during the V_{OH} test for inverting logic and during the V_{OL} test for noninverting logic. The noise margin is calculated from the following expression:

$$V_{NL} = V_{IL} \text{ (max)} - V_{OL} \text{ (max)}$$

3.2.3 HIGH level noise margin, V_{NH}. The HIGH level noise margin test is performed during the V_{OL} test for inverting logic and during the V_{OH} test for noninverting logic. The noise margin is calculated from the following expression:

$$V_{NH} = V_{OH} \text{ (min)} - V_{IH} \text{ (min)}$$

3.2.4 Negative ground noise margin, V_{NG}. With all power supply and output terminals connected to the appropriate worst case conditions, apply V_{OL} (max) to the inputs specified in the applicable acquisition document and decrease the voltage applied to the ground terminal until the output levels equal V_{IH} (min) for inverting logic and V_{IL} (max) for noninverting logic. The dc ground noise margin is the voltage measured at the device ground terminal. The dc source resistance of the injected ground line voltage shall be negligible.

3.2.5 Positive ground noise margin, V_{NG+}. With all power supply and output terminals connected to the appropriate worst case conditions, apply V_{OH} (min) to the inputs specified in the applicable acquisition document and increase the voltage applied to the ground terminal until the output levels equal V_{IL} (max) for inverting logic and V_{IH} (min) for noninverting logic. The dc ground noise margin is the voltage measured at the device ground terminal. The dc source resistance of the injected ground line voltage shall be negligible.

3.2.6 Power supply noise margin, V_{NP+} or V_{NP-}. With all input, power supply, and output terminals connected to the appropriate worst case conditions, increase (or decrease) the power supply voltage(s) until the output level equals the appropriate logic level limit. The power supply noise margin is the difference between the measured supply voltage(s) and the appropriate noise-free worst case supply voltage level(s). If more than one power supply is required, the noise margin of each supply should be measured separately.

3.3 Test procedure for ac noise margin.

3.3.1 AC noise margin test point. If, for any combination of noise pulse width or transition times, the ac noise margin is less than the dc noise margin, the noise pulse amplitude, pulse width, and transition time which produce the minimum noise margin shall be used as the conditions for test. If the ac noise margin exceeds the dc noise margin, the dc noise margin tests only shall be performed.

3.3.2 LOW level noise margin, pulse width, T_{PL}. With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a positive-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OH} (min) minus V_{OL} (max); the pulse amplitude shall be equal to V_{OH} (max); and the transition times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the 0.9 amplitude level to one and one quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{IH} (max) for inverting logic and equal to V_{IL} (min) for noninverting logic. The noise margin pulse width is then measured at the input pulse V_{IL} (max) level.

3.3.3 HIGH level noise margin, pulse width, T_{PH}. With all unused logic input, power supply, and output terminals connected to the appropriate worst case conditions, a negative-going noise pulse shall be applied to the input under test. The pulse amplitude shall be equal to V_{OH} (min) minus V_{OL} (max); the pulse shall be superimposed on a dc level equal to V_{OH} (min); and the transition times shall be much less than the minimum transition times of the device under test. The test is performed by initially adjusting the input pulse width at the 0.1 amplitude level to one and one quarter times the rise time. The pulse width is increased until the output voltage is equal to V_{IL} (min) for inverting logic and V_{IH} (max) for noninverting logic. The noise margin pulse width is then measured at the input pulse V_{IH} (min) level.

4. SUMMARY. The following details, when applicable, shall be specified in the applicable acquisition document:

a. V_{IL} (max).

b. V_{IL} (min).

c. V_{IH} (min).

d. V_{IH} (max).

e. V_{OL} (max).

f. V_{OH} (min).

g. V_{NL}.

h. V_{NH}.

i. V_{NG}.

j. V_{NP}.

k. t_{PL}.

l. t_{PH}.

m. Test temperature. Unless otherwise specified, dc noise margin measurements shall be made at the rated operating temperature extremes in addition to any other nominal test temperatures.

n. Specific noise margin measurements and conditions which are to be performed.

o. Power supply voltages.

p. Input conditioning voltages.

q. Output loads.

r. Parameters of noise signal.

FIGURE 3013-1. Definitions of noise pulse width.

FIGURE 3013-2. Inverting logic gate transfer characteristic defining test points.

FIGURE 3013-3. Noninverting logic gate transfer characteristic defining test points.

METHOD 3014

FUNCTIONAL TESTING

1. PURPOSE. This method establishes the means for assuring circuit performance in regard to the test requirements necessary to verify the specified function and to assure that all logic element paths are not open, stuck-at-HIGH level or stuck- at-LOW LEVEL. This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS.

2. APPARATUS. An instrument shall be provided which has the capability of applying logic patterns (sequentially, if specified) to the logic network input(s) in accordance with the applicable acquisition document. The test instrument shall also be capable of applying nominal power supply voltages and monitoring the outputs for the specified logic levels. The output monitoring circuit may be either a single or double comparator type. The threshold voltage (trip point) for a single comparator or V_{OL} (max) and V_{OH} (min) for a double comparator shall be specified in the applicable acquisition document. The test chamber shall be capable of maintaining the device under test at any specified test temperature.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Nominal power supply voltages and the specified input logic patterns shall be applied to the logic network under test and the output(s) monitored.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Power supply voltage.

   c. Input voltage levels.

   d. Input and output logic patterns.

   e. Output threshold voltage (see 2).

   f. V_{OH} (min) and V_{OL} (max) (see 2).

METHOD 3015.7

ELECTROSTATIC DISCHARGE SENSITIVITY CLASSIFICATION

1. PURPOSE. This method establishes the procedure for classifying microcircuits according to their susceptibility to damage or degradation by exposure to electrostatic discharge (ESD). This classification is used to specify appropriate packaging and handling requirements in accordance with MIL-PRF-38535, and to provide classification data to meet the requirements of MIL-STD-1686.

1.1 Definition. The following definition shall apply for the purposes of this test method.

1.1.1 Electrostatic discharge (ESD). A transfer of electrostatic charge between two bodies at different electrostatic potentials.

2. APPARATUS.

2.1 Test apparatus. ESD pulse simulator and device under test (DUT) socket equivalent to the circuit of figure 3015-1, and capable of supplying pulses with the characteristics required by figure 3015-2.

2.2 Measurement equipment. Equipment including an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of figure 3015-2.

2.2.1 Oscilloscope and amplifier. The oscilloscope and amplifier combination shall have a 350 MHz minimum bandwidth and a visual writing speed of 4 cm/ns minimum.

2.2.2 Current probe. The current probe shall have a minimum bandwidth of 350 MHz (e.g., Tektronix CT-1 at 1,000 MHz).

2.2.3 Charging voltage probe. The charging voltage probe shall have a minimum input resistance of 1,000 MΩand a division ratio of 4 percent maximum (e.g., HP 34111A).

2.3 Calibration. Periodic calibration shall include but not be limited to the following.

2.3.1 Charging voltage. The meter used to display the simulator charging voltage shall be calibrated to indicate the actual voltage at points C and D of figure 3015-1, over the range specified in table I.

2.3.2 Effective capacitance. Effective capacitance shall be determined by charging C1 to the specified voltage (with table I), with no device in the test socket and the test switch open, and by discharging C1 into an electrometer, coulombmeter, or calibrated capacitor connected between points A and B of figure 3015-1. The effective capacitance shall be 100 pF ±10 percent over the specified voltage range and shall be periodically verified at 1,000 volts. (Note: A series resistor may be needed to slow the discharge and obtain a valid measurement.)

2.3.3 Current waveform. The procedure of 3.2 shall be performed for each voltage step of table I. The current waveform at each step shall meet the requirements of figure 3015-2.

2.4 Qualification. Apparatus acceptance tests shall be performed on new equipment or after major repair. Testing shall include but not be limited to the following.

2.4.1 Current waveform verification. Current waveform shall be verified at every pin of each test fixture using the pin nearest terminal B (see figure 3015-1) as the reference point. All waveforms shall meet the requirements of figure 3015-2. The pin pair representing the worst case (closest to the limits) waveform shall be identified and used for the verification required by 3.2.

3. PROCEDURE.

3.1 General.

3.1.1 Test circuit. Classification testing shall be performed using a test circuit equivalent to figure 3015-1 to produce the waveform shown on figure 3015-2.

3.1.2 Test temperature. Each device shall be stabilized at room temperature prior to and during testing.

3.1.3 ESD classification testing. ESD classification testing of devices shall be considered destructive.

3.2 ESD simulator current waveform verification. To ensure proper simulator operation, the current waveform verification procedure shall be done, as a minimum, at the beginning of each shift when ESD testing is performed, or prior to testing after each change of the socket/board, whichever is sooner. If the simulator does not meet all requirements, all classification testing done since the last successful verification shall be repeated. At the time of initial facility certification and recertifications, photographs shall be taken of the waveforms observed as required by 3.2c through 3.2e and be kept on file for purposes of audit and comparison. (Stored digitized representations of the waveforms are acceptable in place of photographs.)

a. With the DUT socket installed on the simulator, and with no DUT in the socket, place a short (figure 3015-1) across two pins of the DUT socket and connect one of the pins to simulator terminal A and the other pin to terminal B.

b. Connect the current probe around the short near terminal B (see figure 3015-1). Set the simulator charging voltage source V_s to 4,000 volts corresponding to step 4 of table I.

c. Initiate a simulator pulse and observe the leading edge of the current waveform. The current waveform shall meet the rise time, peak current, and ringing requirements of figure 3015-2.

d. Initiate a simulator pulse again and observe the complete current waveform. The pulse shall meet the decay time and ringing requirement of figure 3015-2.

e. Repeat the above verification procedure using the opposite polarity (V_s = -4,000 volts).

f. It is recommended that the simulator output be checked to verify that there is only one pulse per initiation, and that there is no pulse while capacitor C1 is being charged. To observe the recharge transient, set the trigger to the opposite polarity, increase the vertical sensitivity by approximately a factor of 10, and initiate a pulse.

TABLE I. Simulator charging voltage (V_s) steps versus peak current (I_p). 1/

Step	V_s (volts)	I_p (amperes)
1	500	0.33
2	1,000	0.67
3	2,000	1.33
4	4,000	2.67

1/ I_p is the current flowing through R2 during the current waveform verification procedure and which is approximately V_s/1,500 ohms.

3.3 Classification testing.

a. A sample of devices (see 4.c) shall be characterized for the device ESD failure threshold using the voltage steps shown in table I, as a minimum. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure voltage. Testing may begin at any voltage step, except for devices which have demonstrated healing effects, including those with spark gap protection, which shall be started at the lowest step. Examination of known technology family input or output V/I damage characteristics (i.e., curve tracer), or other simplified test verification techniques may be used to validate the failure threshold (e.g., cumulative damage effects may be eliminated by retesting at the failure voltage step using a new sample of devices and possibly passing the step).

b. A new sample of devices shall be selected and subjected to the next lower voltage step used. Each device shall be tested using three positive and three negative pulses using each of the pin combinations shown in table II. A minimum of 1 second delay shall separate the pulses.

c. The sample devices shall be electrically tested to subgroups 1 and 7 as applicable (room temperature dc parameters and *functional* tests).

d. If one or more of the devices fail, the testing of 3.3b and 3.3c shall be repeated at the next lower voltage step used.

e. If none of the devices fail, record the failure threshold determined in 3.3a. *Note the highest step passed, and use it to* classify the device according to table III.

TABLE II. Pin combinations to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	*All pins except* V_{ps1} 3/	All V_{ps1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ *Repeat pin combination 1 for each named* power supply and for ground (e.g., where V_{ps1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc.)

3.4 Pin combination to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} or V_{SS2} or V_{SS3} or V_{CC1} or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the *other input and output pins shall be open.*

TABLE III. Device ESD failure threshold classification.

Class 1	0 volt to 1,999 volts
Class 2	2,000 volts to 3,999 volts
Class 3	4,000 volts and above

4. SUMMARY. The following details shall be specified in the applicable purchase order or contract, if other than specified herein.

a. Post test electricals.

b. Special additional or substitute pin combinations, if applicable.

c. Sample size, if other than three devices.

R1 = 10^6 ohms to 10^7 ohms
C1 = 100 picofarads ±10 percent (Insulation resistance 10^{12} ohms minimum)
R2 = 1,500 ohms ±1 percent
S1 = High voltage relay (Bounceless, mercury wetted, or equivalent)
S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

NOTES:

1. The performance of this simulator circuit is strongly influenced by parasitics. Capacitances across relays and resistor terminals, and series inductance in wiring and in all components shall be minimized.
2. As a precaution against transients upon recharge of C1, the supply voltage V_s may be reduced before switch S1 is returned to the charging position.
3. Piggybacking DUT sockets is not permitted during verification or classification testing.
4. Switching terminals A and B internal to the simulator to obtain opposite polarity is not recommended.
5. C1 represents the effective capacitance (see 2.3.2).
6. The current probe connection shall be made with double shielded cable into a 50-ohm termination at the oscilloscope. The cable length shall not exceed 3 feet.

FIGURE 3015-1. EDS classification test circuit (human body model).

NOTES:

1. The current waveforms shown shall be measured as described in the waveform verification procedure of 3.2, using equipment meeting the requirements of 2.
2. The current pulse shall have the following characteristics:

Tri (rise time) ———— Less than 10 nanoseconds.
Tdi (delay time) ———— 150 ±20 nanoseconds.
I_p (peak current) ———— Within ±10 percent of the I_p value shown in table II for the voltage step selected.
I_r (ringing) ———— The decay shall be smooth, with ringing, break points, double time constants or discontinuities less than 15 percent I_p maximum, but not observable 100 nanoseconds after start of the pulse.

FIGURE 3015-2. EDS classification test circuit waveforms (human body model).

METHOD 3016

ACTIVATION TIME VERIFICATION

1. PURPOSE. This method establishes a means for assuring circuit performance during cold temperature start up. It defines an activation time for digital microelectronic devices such as TTL, DTL, RTL, ECL, and MOS and establishes the procedure necessary to accomplish the required testing. This method will ensure that a specified capability is available a known time interval after application of power.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

a. Activation time. Activation time is defined as the time required for a device to become functionally operable after initial power is applied at the operating temperature extremes as specified by the applicable acquisition document. Note that activation time may be due to device and test system limitations, or both.

b. Maximum and minimum. Maximum and minimum refer to an algebraic system where "max" represents the most positive value of the range and "min" represents the least positive value of the range. This is consistent with MIL-STD-1331, 30.1 and 30.2 for logic levels only.

c. Maximum operating frequency. Maximum operating frequency is defined as the frequency of operation resulting from use of the minimum clock period for devices requiring a clock, or the frequency of operation resulting from the use of the minimum cycle time for devices not requiring a clock (such as memory devices) as specified in the applicable acquisition document.

1.2 Symbols. The following symbols and definitions shall apply for the purposes of this method.

1.2.1 Logic levels.

a. V_{LW} = worst case nominal low level logic input. The maximum allowable V_{IL} specified in the applicable acquisition document minus 100 millivolts to allow for uncertainty in the drive level capability of high speed functional test equipment. ($V_{LW} = V_{IL}$ (max) - 100 mV).

b. V_{HW} = worst case nominal high level logic input. The minimum allowable V_{IH} as specified by the applicable acquisition document plus 100 millivolts ($V_{HW} = V_{IH}$ (min) + 100 mV).

c. V_{OH} (min) = minimum output high level specified for a digital microelectronic device.

d. V_{OL} (max) = maximum output low level specified for a digital microelectronic device.

1.2.2 Activation times.

a. t_{AH} = maximum allowable activation time requirement, measured at V_{CC} (max).

b. t_{AL} = maximum allowable activation time requirement, measured at V_{CC} (min).

2. APPARATUS. An instrument shall be provided which has the capability of applying sequential logic patterns to the device under test in accordance with the applicable acquisition document. The test instrument shall also be capable of applying nominal power supply voltage(s) and monitoring the output for the specified logic levels. The output monitoring circuit shall be of the double comparator type. The threshold voltage (trip point) for a comparator shall be V_{OL} (max) and V_{OH} (min) as specified in the applicable acquisition document. The test chamber shall be capable of maintaining the device under test at any specified test temperature.

3. PROCEDURE. The device shall be thermally stabilized at the minimum specified test temperature with no power applied to the device. The specified power supply voltage and the specified input logic patterns using V_{LW} and V_{HW} input voltage levels shall then be applied to the device under test and the outputs shall be monitored as described in section 2. This functional test shall be performed at a speed of at least 75 percent of F(max) using a test vector pattern as called out in the applicable acquisition document that has been designed for maximum fault coverage with no more than 4 K vectors.

3.1 Activation time, maximum supply voltage, t_{AH}. Available test equipment has inherent delays (due to test program statement execution, voltage driver rise/fall times, etc.) between the time power is applied to the device under test and actual execution of the test. Therefore, the activation time stated in the applicable acquisition document should not be specified as less than the test system delay (even though device performance may be better). The test sequence shall be as follows.

3.1.1 Device under test. The device under test shall be thermally stabilized at the minimum specified test temperature, with the device unpowered.

3.1.2 Device under test shall then be powered up at V_{CC} (max). After waiting the time specified by T_{AH} (taking into account test equipment delays), the functional test pattern (using V_{LW} and V_{HW}) logic levels) shall be applied to verify proper operation.

3.1.3 Repeat sequences 3.1.1 and 3.1.2 at the maximum specified test temperature.

3.2 Activation time, minimum supply voltage, t_{AL}. Repeat sequence described in 3.1.1 to 3.1.3 using a supply voltage of V_{CC} (min).

3.3 Failure criteria. The device must pass the functional test pattern and is a failure if the device fails any single pattern or vector in the specified test set.

4. SUMMARY. The following details, when applicable, shall be as specified in the applicable acquisition document:

a. V_{IL} (max).

b. V_{IH} (min).

c. V_{OH} (min).

d. V_{OL} (max).

e. V_{CC} (min).

f. V_{CC} (max).

g. Test temperature (min and max operating temperature).

h. t_{AH} (max).

i. t_{AL} (max).

j. Functional test pattern (see 3).

k. Maximum operating frequency, F (max) (see 1.1.c).

METHOD 3017

MICROELECTRONICS PACKAGE DIGITAL SIGNAL TRANSMISSION

1. PURPOSE. This method establishes the means of evaluating the characteristic impedance, capacitance, and delay time of signal lines in packages used for high frequency digital integrated circuits. It is intended to assure a match between circuit performance and interconnecting wiring to minimize signal degradation.

1.1 Definitions.

1.1.1 Characteristic impedance. The impedance that a section of transmission line exhibits due to its ratio of resistance and inductance to capacitance.

1.1.2 Delay time. The time delay experienced when a pulse generated by a driver with a particular drive impedance is propagated through a section of transmission line.

1.2 Symbols.

R: Resistance
L: Inductance
C: Capacitance
t_{pd}: Propagation delay time

2. APPARATUS. The approaches for transmission performance measurements shall include a suitable time domain reflectometer (TDR) (see 2.1) and dc resistance measuring equipment (see 2.2).

2.1 Time domain reflectometer. The TDR used for this test shall have a system rise time for the displayed reflection that is not less than 5 times and preferably 10 times the rise time (method 3004) for the candidate integrated circuits to be packaged. Interconnecting cables and fixtures shall be designed such that this ratio is not degraded due to reflections and ringing in the test setup.

2.2 DC resistance. DC resistance measuring equipment and probe fixtures shall be capable of measuring the resistance of the package leads and the chip-to- package interconnect media with an accurancy of no greater than ±10 percent of the actual value including errors due to the mechanical probing interface contact resistance.

3. PROCEDURE. The test equipment configuration shall be as shown on figure 3017-1 using a time domain reflectometer as specified (see 2). The characteristic impedance (Z_o), propagation time (t_{pd}), resistance and load capacitance (C_L) shall be measured for all representative configurations as determined by a review of the package drawings, and the intended applications (see 3.2 through 3.3).

3.1 General considerations.

3.1.1 TDR measurements. Accurate measurement of transmission performance of a package pin using a TDR requires careful design and implementation of adapter fixtures to avoid reflections due to transmission line discontinuities in the cables and junctions between the TDR and the package being tested. The accuracy of the measurement will be enhanced if the coaxial cable used to interface to the package is of a characteristic impedance as close as possible to the package pin impedance. The interface to the package should be a soldered connection and mechanical design of the actual coax-to-package interface should minimize the length of the uncontrolled impedance section. Stripline interfaces are the best method for surface mount package styles.

3.1.2 Test configurations. Obtaining a good high frequency ground is also important. Connection of the package ground plane (if the package design has one) to the test set-up ground plane should be accomplished with a pin configuration similar to actual usage in the intended package applications.

Pin selection for testing may vary according to package complexity. For packages with very symmetrical pin configurations only a few pins need be tested but configurations must include pins adjacent and nonadjacent to the ground pins. Packages with complex wiring and interconnection media should be tested 100 percent.

3.2 Test procedure for package transmission characteristics. Using a section of coaxial cable of known, calibrated characteristic impedance (Z_{Ref}) as a reference measure the minimum (Z_{Min}) maximum (Z_{Max}) and average (Z_o) values of reflection coefficient (ρ) for the section of line on the TDR display that has been carefully determined to be the package pin (locate using zero-length short circuits).

Calculate characteristic impedance (Z_o) for each of the cases from the formula:

$$Z_0 = Z_{Ref} \; x \; \frac{(1+\rho)}{(1-\rho)}$$

3.2.2 Delay time measurement. From the TDR display of 3.2.1 measure the time difference in picoseconds from the point identified as the start of the exterior package pin (t_1) to the chip interface point (t_2) ($\Delta t = t_1 - t_2$)

Form the package design drawings, determine the physical length of the package run (L)

$$Time\ delay\ t_{pd} = \frac{\Delta t}{L}$$

3.2.3 Load capacitance calculation.

$$Load\ capacitance\ \ C_L = \frac{t_{pd}}{Z_o}$$

3.2.4 Load inductance calculation.

$$Load\ inductance\ (series) = \frac{(t_{pd})^2}{C_L}$$

3.3. Series resistance measurement.

Using the test setups of figure 3017-2, separately measure the dc resistance of the chip-to-package interface media (R_M) and the package lead (R_L).

4. SUMMARY. The following details, when applicable, shall be specified in the applicable acquisition document:

a. Z_{Max}.

b. Z_{Min}.

c. Z_o (max).

d. Z_o (min).

e. t_{pd} (max).

f. t_{pd} (min).

g. C_L (max).

h. C_L (min).

i. L_L (max).

j. L_L (min).

k. R_M (max).

l. R_M (min).

m. R_L (max).

n. R_L (min).

o. Package pins to be tested.

p. Package ground configuration.

FIGURE 3017-1. Time domain reflectometer test setup.

FIGURE 3017-2. Test setup for dc resistance using a milliohmmeter.

METHOD 3018

CROSSTALK MEASUREMENTS FOR DIGITAL MICROELECTRONICS DEVICE PACKAGE

1. PURPOSE. This method establishes the means of measuring the level of cross-coupling of wideband digital signals and noise between pins in a digital microcircuit package. The method may be used to gather data that are useful in the prediction of the package's contribution to the noise margin of a digital device. The technique is compatible with multiple logic families provided that the drive and load impedance are known.

1.1 Definitions.

1.1.1 Crosstalk. Signal and noise waveforms coupled between isolated transmission lines, in this case, package conductors.

1.1.2 Coupling capacitance. The effective capacitance coupling between a pair of conductors in a package as measured by the time constant of the charge pulse applied on one line and measured on the other.

1.1.3 Noise pulse voltage. The voltage of a crosstalk measured at the minimum noise pulse width as measured on a receiver input line.

1.1.4 Peak noise voltage. The peak value of the noise pulse measured on a receiver input line.

1.2 Symbols. The following symbols shall apply for the purpose of this test method and shall be used in accordance with the definitions provided (see 1.2.1 and 1.2.2).

1.2.1 Logic levels.

V_{OL}(max): The maximum output low level specified in a logic system.

V_{OH}(min): The minimum output high level specified in a logic system.

V_{IL}(max): The maximum allowed input low voltage level in a logic system.

V_{IH}(min): The minimum allowed input high level in a logic system.

1.2.2 Noise pulse width.

t_{PL}: The low level noise pulse width, measured at the V_{IL} (max) level (see method 3013).

t_{PH}: The high level noise pulse width, measured at the V_{IH} (min) level (see method 3012).

1.2.3 Transition times (see method 3004).

t_{LH}: Rise time. The transition time of the output from the 10 percent to the 90 percent of the high voltage levels with the output changing from low to high.

t_{HL}: Fall time. The transition times from the 90 percent to the 10 percent of the high voltage level with the output changing from high to low.

1.2.4 Crosstalk parameters.

C_c: Coupling capacitance (see 1.1.2).

V_N: Noise pulse voltage (see 1.1.3).

V_{NPK}: Peak noise voltage (see 1.1.4).

2. APPARATUS. The apparatus used for crosstalk measurements shall include a suitable source generator (see 2.1), wideband oscilloscope (see 2.2), low capacitance probe (see 2.3) and load resistors (see 2.4).

2.1 Source generator. The source generator for this test shall be capable of duplicating (within 5 percent) the transition times, V_{OH} and V_{OL} levels of the logic system(s) being considered for application using the package style under evaluation. The source generator shall have a nominal characteristic source impedance of 50 ohms.

2.2 *Wideband oscilloscope*. The oscilloscope used to measure the crosstalk pulse shall have a display risetime that is less than 20 percent of the risetime of the logic systems being considered for application in the package style under evaluation. A sampling-type oscilloscope is recommended.

2.3 Low capacitance probe. The interface between the oscilloscope and the unit under test shall be a high impedance low capacitance probe. The probe impedance shall be 10 kΩ, minimum and the capacitance shall be 5 pF, maximum, unless otherwise specified in the acquisition document.

2.4 Load resistor. The load resistors specified for this test shall be low inductance, low capacitance, chip style resistors with a tolerance of ±5 percent. Load resistor values(s) shall be specified by the acquisition document to match the load impedance levels of the application logic family for a single receiver load.

3. PROCEDURE. The test equipment configuration shall be as shown on figure 3018-1 using a source generator, oscilloscope, probe and loads as specified (see 2). Measurements shall be made of coupling capacitance, (see 3.2) and if required by the acquisition document, of noise pulse voltage, peak noise pulse voltage, and noise pulse width (see 3.3).

3.1 General considerations.

3.1.1 Package test configuration. It is important to ground the package using the same pins as would be used in the microcircuit application. If the package has an internal ground plane or ground section, this should be connected via package pin(s) to the exterior test set-up ground plane. The package should be connected to the test set-up with coaxial cable or stripline. Unshielded conductor medium should not be used between the signal source and package. Coaxial shields must be grounded at both ends of the cable. Package sockets should not be used unless these are to be part of the microcircuit application configuration. Package leads must be formed and trimmed as specified in the application. Package-to-chip interconnecting media shall be installed in the package and used to connect to the load resistors.

3.1.2 Pin selection. For simple packages with symmetrical, parallel pin conductors, only a sample of pin combinations need be tested. Unless otherwise specified by the acquisition document, all combinations adjacent to the ground pin(s) and combinations opposite the ground pin(s) shall be tested, as a minimum. Complex packages with nonparallel conductors or multilayer wiring shall be tested for all adjacent-pair combinations, unless otherwise specified.

3.2 Coupling capacitance measurements. Connect the test equipment as shown on figure 3018-1. Use a 50 ohm chip resistor load in the driven pin channel, unless otherwise specified. For the pick-up channel, use the load resistor value(s) as specified by the acquisition document. (Load resistor values should be set such that the parallel combination of load resistance and probe impedance matches as closely as practical the specified load impedance of a single receiver in the logic system to be used in the microcircuit application.) Check the residual cross-coupling of the measuring set-up by touching the probe to the pick-up channel load before the pick-up pin is connected to the resistor. Measure and record the peak pulse voltage observed. *This peak pulse reading must be less than 50 percent of the reading observed with the pin* connected to the resistor for a reading to be valid. Adjust the test set-up cable orientation and configuration to minimize this residual cross-coupling.

Connect the pick-up pins to the load resistor and adjust the pulse width so that the time required to charge the coupling capacitance to 0 V can be observed. Measure the time at the 63 percent voltage point on the waveform (T) and calculate coupling capacitance (C_c) as follows:

$$Determine\ R_{Total} = \frac{R_{Probe}\ x\ R_{Load}}{R_{Probe} + R_{Load}}$$

$$C_{Total} = \frac{T}{R_{Total}}$$

$$C_C = C_{Total} - C_{Probe}$$

Values of C_C can be used as a relative measure for comparison of potential crosstalk among several packages to a standard package. The coupling capacitance (C_c) can also be used to predict levels of crosstalk for various logic systems or circuit configurations by performing a pulse response analysis using a circuit simulator.

3.3 Noise pulse measurements. Using the same test setup as in 3.2, measure the crosstalk noise pulse voltage at the minimum noise pulse width specified for the logic system or as specified by the acquiring agency.

Measure the peak noise voltage value of the coupled crosstalk.

4. SUMMARY. The following details, when applicable, shall be specified in the acquisition document:

a. C_c.

b. V_{OL} (max).

c. V_{OH} (min).

d. V_{IL} (max).

e. V_{IH} (min).

f. t_{PL}.

g. t_{PH}.

h. t_{tLH}.

i. t_{tHL}.

j. V_N.

k. V_{NPK}.

FIGURE 3018-1. Test setup for coupling capacitance measurement.

METHOD 3019.1

GROUND AND POWER SUPPLY IMPEDANCE MEASUREMENTS FOR MICROELECTRONICS DEVICE PACKAGE

1. PURPOSE. This method establishes the means of measuring the series impedance of the ground and power supply circuit pin configurations for packages used for complex, wide bandwidth microcircuits. The method provides data that are useful in the evaluation of the relative performance of various packages and can be used to predict the contribution of the package to power supply noise and ground noise.

1.1 Definition.

1.1.1 Ground or power supply impedance. The series combination of inductive reactance and resistance exhibited by all of the conductor paths between the semiconductor chip interface and the exterior package interface in either the ground circuit or the power supply circuit. The impedance of a series inductive circuit is defined by the equation:

$$Z = \sqrt{R^2 + X^2 L}$$

1.2 Symbols. The following symbols shall apply for purposes of this test method and shall be used in conjunction with the definition provided in 1.1.

L_G: Series inductance of the ground circuit path in a package (henries).

L_p: Series inductance of the power supply circuit path in a package (henries).

X_G: Series inductive reactance of ground path = $2 \pi f L_p$ (ohms).

X_p: Series inductive reactance of power supply path = $2 \pi f L_p$ (ohms).

f: Frequency (Hz).

f_t: Frequency of primary component of digital pulse transition = $\frac{1}{t_t}$ (Hz).

f_{tp}: Frequency related to noise pulse width specified for the logic system:

$$f_{tp} = \frac{1}{t_{Pmin}} \text{ (Hz)}$$

t_t: Transition time from logic system. Equal to the smaller value of low to high or high to low transition.

Z_G: Series impedance of ground path at frequency:

$$Z_G = \sqrt{R_G^2 + Z_G^2}$$

Z_p: Series impedance of power supply path at frequency:

$$Z_p = \sqrt{R_p^2 + Z_p^2}$$

t_{Pmin}: The minimum noise pulse width at either the V_{IH} or V_{IL} level specified for a given logic system.

2. APPARATUS. The apparatus used for ground impedance measurements shall include a suitable RF inductance meter and a suitable milliohmmeter.

2.1 RF inductance meter. The RF inductance meter (or multi-frequency LCR meter) shall be capable of ac measurements of series inductance over the range of 1 nH to 1,000 nH at a frequency of 100 kHz with an accuracy of ±5 percent including test fixture errors.

2.2 Milliohmmeter. The milliohmmeter (or LCR meter) shall be capable of measuring resistance using a 4-wire method over the range from 10 MΩ to 10 Ω with an accuracy of ±5 percent, including test fixture errors.

3. PROCEDURE. Measurement of series ground impedance (Z_G) and power supply impedance (Z_p) shall be made for all standard power and ground configurations specified for the package application. Measurements shall be performed in accordance with 3.2.

3.1 General considerations. Accurate measurement of series impedance requires careful design and implementation of test adapters to minimize errors. Since the inductance and resistance values being measured are usually quite small, means must be provided to null out the tare resistance and inductance of the test adapters through 4-wire methods and substraction techniques. The tare values of the interconnecting circuits must be small to enable the meters to read on ranges that provide adequate resolution and accuracy. The techniques specified herein are adequate for predicting impedance at frequencies up to 1 GHz. Impedance shall be evaluated at a frequency related to either the transition time:

$$f_{tr} = \frac{1}{t_{tr}}$$

or to the noise pulse width of the logic system used in the package:

$$f_{tp} = \frac{1}{t_{Pmin}}$$

The frequency f shall be as specified in the acquisition document.

The configuration of the package being tested must be the same as in the application. Wirebonds and other interconnection media must be included in the measurement. The package should be mounted on a dielectric holding fixture to avoid stray capacitance between the package and test equipment ground planes. Sockets should not be used unless specified. Package leads must be trimmed to applications specifications.

3.2 Test procedure for series impedance.

3.2.1 Series inductance. With the inductance meter, measure the series inductance of the power supply circuit (L_p) between the external package solder interface and the chip power supply location. Similarly, measure the inductance of the ground circuit (L_G). Calculate $X_p = 2\pi fL_p$ and $X_G = 2\pi fL_G$.

3.2.2 Series resistance. With the milliohmmeter, measure the series resistance of the same power and ground circuits: R_P and R_G.

3.2.3 Calculation of impedance.

$$Calculate\ \ Z_p = \sqrt{X^2{}_p + R_p{}^2}$$

$$A_G = \sqrt{X_G{}^2 + R_G{}^2}$$

4. SUMMARY. The following details, when applicable, shall be specified in the applicable acquisition document.

a. Z_p (max).

b. Z_G (max).

c. L_P (max).

d. L_G (max).

e. R_P (max).

f. R_G (max).

g. f.

h. f_{tr}.

i. f_{tp}.

j. t_t.

k. t_{Pmin}.

METHOD 3020

HIGH IMPEDANCE (OFF-STATE) LOW-LEVEL OUTPUT LEAKAGE CURRENT

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to output leakage current when an output is in the high-impedance state with a low-level voltage applied. This current should normally be specified as a maximum negative value (I_{OLZ} maximum). This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL, and MOS that have tristate outputs.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified test temperature. An instrument shall be provided that has the capability of applying the specified low level voltage to the output terminal and measure the resultant current flowing in the terminals.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Apply voltages to the test circuit as follows:

a. Worst-case power supply voltage (V_{CC}) applied to the V_{CC} terminal.

b. Threshold-level voltages (V_{IH} minimum or V_{IL} maximum) applied to the control inputs which forces the output under test into the high-impedance (off) state.

c. Nonthreshold level voltage applied to the logic input terminals controlling the output under test so as to produce a "hard" high voltage level at that output if the output was not in the high-impedance state. Apply the specified low logic level voltage to the output terminal under test and measure the resultant leakage current. Outputs shall be measured individually.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test temperature.

b. Worst case power supply voltages.

c. Threshold voltage levels for control inputs.

d. Voltages at logic input terminals for output under test.

e. Output voltage.

f. I_{OLZ} maximum negative limit.

METHOD 3021

HIGH IMPEDANCE (OFF-STATE) HIGH-LEVEL OUTPUT LEAKAGE CURRENT

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to output leakage current when an output is in the high-impedance state with a high-level voltage applied. This current should normally be specified as a maximum positive value (I_{OHZ} maximum). This method applies to digital microelectronic devices, such as TTL, DTL, RTL, ECL and MOS that have tristate outputs.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified test temperature. An instrument shall be provided that has the capability of applying the specified high level voltage to the output terminal and measure the resultant current flowing out of the terminals.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Apply voltages to the test circuit as follows:

a. Worst-case power supply voltage (V_{CC}) applied to the V_{CC} terminal.

b. Threshold level voltage (V_{IH} minimum or V_{IL} maximum) applied to the control inputs which will cause the output under test to be in the high-impedance (off) state.

c. Nonthreshold level voltage applied to the logic input terminals controlling the output under test so as to produce a "hard" low voltage level at that output if the output was not in the high-impedance state. Apply the specified high logic level voltage to the output terminal under test and measure the resultant leakage current. Outputs shall be measured individually.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test temperature.

b. Worst case power supply voltages.

c. Threshold voltage levels for control inputs.

d. Voltages at logic input terminals for output under test.

e. Output voltage.

f. I_{OLZ} maximum positive limit.

METHOD 3022

INPUT CLAMP VOLTAGE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable acquisition document in regard to input voltage levels in a region of relatively low differential resistance that serve to limit the input voltage swing. Input clamp voltage is specified as a maximum positive value (V_{IC} POS) or the maximum negative value (V_{IC} NEG). This method applies to digital microelectronic devices.

2. APPARATUS. The test chamber shall be capable of maintaining the device under test at any specified test temperature. The test apparatus shall be capable of supplying the worst case power supply voltage and shall be capable of loading the input of the circuit under test with the specified negative current or the specified positive current, both referred to as I_{IN}. Resistors may be used to simulate the applicable current levels.

3. PROCEDURE. The device shall be stabilized at the specified test temperature. Apply worst-case power supply voltage (V_{CC}) to the V_{CC} terminal. Force the specified negative current from or the positive current into the input under test and measure the resultant input voltage. (NOTE: Any input for which the I_{IL} would influence the negative input current (I_{IN}) should have V_{IC} measured with the V_{CC} terminal open). All input terminals not under test may be high, low, or open to minimize or inhibit any outside factors (noise, transients, etc.) from affecting the test. Inputs shall be tested individually.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test temperature.

   b. Worst case power supply voltage.

   c. Current to be forced from the input terminal.

   d. V_{IC} (POS) or V_{IC} (NEG) maximum limit.

METHOD 3023

STATIC LATCH-UP MEASUREMENTS FOR DIGITAL CMOS MICROELECTRONIC DEVICES

Latchup shall be performed in accordance with JEDEC-STD-17 dated August 1988.

METHOD 3024

SIMULTANEOUS SWITCHING NOISE MEASUREMENTS FOR DIGITAL MICROELECTRONIC DEVICES

1. Purpose. This method establishes the procedure for measuring the ground bounce (and V_{CC} bounce) noise in digital microelectronic devices or to determine compliance with specified ground bounce noise requirements in the applicable acquisition document. It is also intended to provide assurance of interchangeability of devices and to eliminate misunderstanding between manufacturers and users on ground bounce noise test procedures and requirements. This procedure is not intended to predict the amount of noise generated on an end product board, but for use in measuring ground bounce noise using a standardized method for comparing noise levels between logic families and vendors.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

a. Ground bounce noise. The voltage amplitude (peak) of extraneous signals present on a low-level non-switching output with a specified number of other outputs switching. Ground bounce noise on a logic low output can be of sufficient amplitude to exceed the high level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

b. V_{CC} bounce noise. The voltage amplitude (peak) of extraneous signals present on a high-level non-switching output with a specified number of other outputs switching. V_{CC} bounce on a logic high output can be of sufficient amplitude to exceed the low level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

c. Simultaneous switching noise. Noise generated across the inductance of a package pin as a result of the charge and discharge of load capacitance through two or more transitioning output pins.

d. Quiet low. A non-switching output which is driving a nominal low level.

e. Quiet high. AQ non-switching output which is driving a nominal high level.

f. Signal skew. The amount of time measured between any two signal transitions at the 1.5 V voltage level (for TTL threshold devices) and at $V_{CC}/2$ (for CMOS threshold devices).

1.2 Symbols. The following symbols shall apply for the purposes of this test method:

1.2.1 Logic levels.

V_{IL} max: The maximum allowed input low level on a digital microelectronic device.

V_{IL} min: The minimum allowed input low level on a digital microelectronic device.

V_{IH} max: The maximum allowed input high level on a digital microelectronic device.

V_{IH} min: The minimum allowed input high level on a digital microelectronic device.

1.2.2 Noise levels.

V_{OLP} max: The largest positive amplitude transient allowed on a logic low output.

V_{OLV} max: The largest negative amplitude transient allowed on a logic low output.

V_{OHP} max: The largest positive amplitude transient allowed on a logic high output.

V_{OHV} max: The largest negative amplitude transient allowed on a logic high output.

1.2.3 Transition times.

T_{TLH}: The transition time of a rising edge (rise time) measured from 10 percent to 90 percent.

T_{THL}: The transition time of a rising edge (fall time) measured from 90 percent to 10 percent.

2. Apparatus. The apparatus used for ground bounce noise measurements shall include a suitable source generator (see 2.1), loads (see 2.2), an oscilloscope (see 2.3) and a low noise test fixture (see 2.4). See figure 3024-1 for proper connections.

2.1 Source generator. The pulse or pattern generator for this test shall be capable of supplying the required input pulses with transition times of 3.0 ±0.5 ns to minimize skew due to input threshold differences.

2.2 Loads. Loads shall consist of 50 pF capacitance (-0,+20%) and a 500 ohm (±1%) low inductance resistor from each output to ground. Capacitance value should include probe and test fixture capacitance. The 500 ohm resistor may be made up of a 450 ohm resistor in series with a 50 ohm oscilloscope input channel or 50 ohm termination.

2.3 Oscilloscope. The oscilloscope and probe combination shall have a minimum bandwidth of 1 GHz. Probes (if used) must be calibrated using the manufacturers instructions before accurate measurements can be made.

2.4 Test fixture. Test fixture construction has a large impact on the accuracy of the results. Therefore, the standard ESH test fixture or an equivalent approved fixture (one which demonstrates results within 10% of the standard) must be used to perform these tests. (The ESH fixture for DIP devices is LAB-350-28. Other standard fixtures will be determined at a later date.) Lead lengths should be 0.25 inches or less. The devices under test may be clamped to the test fixture, soldered to the fixture, or installed in a socket on the fixture. Use of a socket may result in higher readings.

3. Procedure. The device shall be installed on the low noise fixture. All outputs of the device under test shall be loaded as specified in 2.2. All outputs (as many as functionally possible) shall be conditioned to switch using the setup information in 3.1. Tests shall be performed using the procedures in 3.2.

3.1 Setup parameters.

3.1.1 Supply voltage. Power supply voltage shall be at nominal operating voltage (5.0 volts for most families).

3.1.2 Test temperature. All tests shall be performed at 25°C.

3.1.3 Input conditioning. Input voltage levels shall be 0.0 V low level and V_{CC} for CMOS and 3.0 V for TTL for high level for both static and switching inputs. Switching inputs shall be driven by 1 MHz signals with 2.0 ±0.5 ns transition times. Maximum skew (made at the device package inputs) between any two input signals (including out-of-phase signals) shall be less than 1 ns. See figure 3024-2.

FIGURE 3024-1. Simultaneous switching noise test setup.

FIGURE 3024-2. Input waveforms.

FIGURE 3024-3. Noise measurement technique.

3.2. Ground bounce test procedure. The output to be tested should be conditioned to a low level. The scope probe (if used) shall be connected to the output under test no more than 0.25 inches from the pin. The probe ground lead shall be attached to a suitable location (ground plane or pin) and have a maximum length of 1 inch. The ground bounce noise is the peak voltage in the positive (V_{OLP}) and negative (V_{OLV}) directions measured from the nominal V_{OL} level (see figure 3024-3). The noise must be measured at both the LOW to HIGH and the HIGH to LOW transition of the switching outputs. (Two consecutive areas of disruption need to be analyzed for the largest peak. If a second scope channel is available, it can be used to monitor the switching outputs and ease synchronization of the noise.) This test shall be repeated with each output at a low level with all others (functionally possible) switching. The largest peak on the worst output is the device ground bounce noise. Engineering judgement or experience may be used to reduce the number of pins tested provided that the rationale for this reduction of pins tested is documented and made available to the preparing activity or the acquiring activity upon request. (Generally, the noisiest pin on one device will be the noisiest pin on all devices of that type.)

3.3 V_{CC} bounce test procedure. The output to be tested should be conditioned to a high level. The scope probe (if used) shall be connected to the output under test no more than 0.25 inches from the pin. The probe ground lead shall be attached to a suitable location (ground plane or pin) and have a maximum length of 1 inch. The V_{CC} bounce noise is the peak voltage in the positive (V_{OHP}) and negative (V_{OHV}) directions measured from the nominal V_{OH} level. The noise must be measured at both the LOW to HIGH and the HIGH to LOW transition of the switching outputs. (Two consecutive areas of disruption need to be analyzed for the largest peak. If a second scope channel is available, it can be used to monitor the switching outputs and ease synchronization of the noise.) This test shall be repeated with each output at a high level with all others (functionally possible) switching. The largest peak on the worst output is the device V_{CC} bounce noise. Engineering judgement or experience may be used to reduce the number of pins tested provided that the rationale for this reduction of pins tested is documented and made available to the preparing activity or the acquiring activity upon request. (Generally, the noisiest pin on one device will be the noisiest pin on all devices of that type.)

4. Summary. The following details, when applicable, shall be specified in the acquisition document:

a. V_{CC} Supply voltage.

b. Test temperature.

c. Input switching frequency.

d. Number of outputs switching.

e. Package style of devices.

f. Conditioning levels of non-switching inputs.

g. Output pin(s) to be tested.

METHOD 4001.1

INPUT OFFSET VOLTAGE AND CURRENT AND BIAS CURRENT

1. PURPOSE. This method establishes the means for measuring input bias current and the offset in voltage and current at the input of a linear amplifier with differential inputs. Offset voltage may also be pertinent in some single input amplifiers. Input bias current will also be measured in this procedure.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Input offset voltage (V_{IO}). That dc voltage which must be applied between the input terminals through two equal resistances to force the quiescent dc output to zero or other specified level V_{OO}, generated by V_{OI}.

1.1.2 Input offset voltage drift (DV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage to the change of the circuit temperature.

$$DV_{IO} = \frac{\Delta V_{IO}}{\Delta T}$$

1.1.3 Input offset current (I_{IO}). The input offset current is the difference between the input bias currents entering into the input terminals of a differential input amplifier required to force the output voltage to zero or other specified level (V_{OO}).

1.1.4 Input offset current drift (DI_{IO}). The input offset current drift is the ratio of the change of input offset current to the change of circuit temperature.

$$DI_{IO} = \frac{\Delta I_{IO}}{\Delta T}$$

1.1.5 Input bias current (I_{IB}). The input bias currents are the separate currents entering into the two input terminals of a balanced amplifier, specified as $+I_{IB}$ and $-I_{IB}$. The bias current in a single ended amplifier is defined as I_{IB}.

1.1.6 Input offset voltage adjust ($\pm V_{IO\ adj}$). Bias adjustment which produces maximum offset at the output.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. An op amp null loop test figure is also shown as an alternate test setup. R_2 shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (10 x Z_{OUT}). Let R_2/R_1 = 100 or 0.1 x (open loop gain), whichever is smaller. Recommended stabilization and power supply decoupling circuitry shall be added. R_3 shall be no larger than the nominal input impedance. For methods using the null loop circuit, assume all switches (relays) normally closed.

3.1 Input offset voltage.

3.1.1 Differential input amplifier. The test setup is shown on figure 4001-1. Input offset voltage $V_{IO} = (R_1/R_2)(E_O - V_{OI})$. Switches S_1 and S_2 are closed for this test.

3.1.2 Single ended inverting amplifier. The test setup is shown on figure 4001-2. Input offset voltage $V_{IO} = (R_1/R_2)(E_O - V_{OI})$. Switch S is closed for this test.

3.1.3 Single ended noninverting amplifier. The test figure is shown on figure 4001-3. $V_{IO} = (R_1/R_2)(E_O - V_{OI})$. Switch S is closed for this test.

3.1.4 Differential input amplifier. This is an alternative method using the null loop circuit of figure 4001-4, in which all switches are closed. Set V_C to zero. Measure E_O. $V_{IO} = (R_1/R_2)(E_O)$.

3.2 Input offset current. This has a meaning for differential input amplifiers only.

3.2.1 Differential input amplifier. The test figure is shown on figure 4001-1. Measure E_{01} with S_1 and S_2 closed, measure E_{02} with S_1 and S_2 open.

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.2.2 Differential input amplifier using null loop. The test setup is shown on figure 4001-4, S_1 and S_4 are closed, set $V_C = 0$. Measure E_{01} as in 3.1.4. Open S_2 and S_3 and measure E_{02}.

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_{02} - E_{01}}{R_3}\right)$$

3.3 Input bias current.

3.3.1 Differential input amplifier. The test figure is shown on figure 4001-1. Measure E_{01} with S_1 and S_2 closed, measure E_{02} with S_1 closed and S_2 open. Measure E_{03} with S_1 open and S_2 closed.

$$I_{IB+} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

$$I_{IB-} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{03}}{R_3}\right)$$

3.3.2 Single ended inverting amplifier. The test figure is shown on figure 4001-2. Measure E_{01} with S closed, measure E_{02} with S open.

$$I_{IB} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.3.3 Single ended noninverting amplifier. The test figure is shown on figure 4001-3. Measure E_{01} with S closed. Measure E_{02} with S open.

$$I_{IB} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.3.4 Differential input amplifier using null loop. The test setup is shown on figure 4001-4. Set V_C to zero with S_1 and S_4 closed. Measure E_{01} with S_2 closed and S_3 closed. Measure E_{02} wth S_2 open and S_3 closed. Measure E_{03} with S_2 closed and S_3 open.

$$I_{IB+} = \frac{R_1}{R_2}\left(\frac{E_{03} - E_{01}}{R_3}\right)$$

$$I_{IB-} = \frac{R_1}{R_2}\left(\frac{E_{02} - E_{01}}{R_3}\right)$$

3.4 Input offset voltage drift. Measurement of V_{IO1} is made at temperature T_1 in accordance with 3.1 and a second measurement at T_2 of V_{IO2} is made at the second temperature.

$$DV_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1}$$

3.5 Input offset current drift. Measurement of I_{IO1} is made at temperature T_1 and I_{IO2} at temperature T_2 in accordance with 3.2.

$$DI_{IO} = \frac{I_{IO2} - I_{IO1}}{T_2 - T_1}$$

3.6 Adjustment for input offset voltage. Use the value of E_o for 3.1.4. Measure E_{o1} with the offset null voltage (V_{ON}) set to the positive extreme.

$$V_{IO\,Adj}(+) = (E_O - E_{O1})\frac{R_1}{R_2}$$

Measure E_{o2} with the offset null voltage (V_{ON}) set to the negative extreme:

$$V_{IO\,Adj}(-) = (E_O - E_{O2})\frac{R_1}{R_2}$$

NOTE: V_{ON} may be implemented using a combination of resistors to obtain the proper voltage across the offset null terminals. This determination shall be based on the device under test (DUT) specifications.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, and R_3, R_4, R_5, R_L, and $\pm V_{CC}$ of the nulling amplifier.

a. V_{IO} maximum.

b. DV_{IO} maximum at specified temperature(s).

c. I_{IO} maximum when applicable.

d. DI_{IO} maximum, when applicable at specified temperature(s).

e. I_{IB+} and I_{IB-} maximum at specified temperature(s).

f. V_{OI} and V_{OO}, when applicable, at specified temperature(s).

g. $\pm V_{IO\,Adj}$ at specified temparature(s).

h. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at +25°C ambient.

FIGURE 4001-1. Differential input amplifier.

FIGURE 4001-2. Single ended inverting amplifier.

FIGURE 4001-3. Single ended noninverting amplifier.

FIGURE 4001-4. Differential input amplifier using null loop.

METHOD 4002.1

PHASE MARGIN AND SLEW RATE MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the stability and slew rate of a linear amplifier intended to be used with feedback.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Phase margin. The phase margin is 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity. The loop is the series path of the device under test and the feedback network which is opened at the inverting terminal. The inverting terminal is loaded down to simulate the load normally presented by the feedback network. Good practice dictates that the phase margin should be at least 45°.

1.1.2 Peaking. If a closed loop gain versus frequency plot is made, peaking is the amount by which the gain may increase over its nominal value just before it falls off. 3 dB of peaking will result from a phase margin of 45°. Thus, it is desirable to keep the peaking less than 3 dB.

1.1.3 Slew rate. Slew rate is the time rate of change of the closed-loop amplifier output voltage under large signal conditions (i.e., the maximum ac input voltage for which the amplifier performance remains linear). Stabilization networks will affect the slew rate and therefore these must be included in the measurement.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. Recommended stabilization networks should be added to compensate for the degree of feedback in the test. The circuit under test should have adequate power supply decoupling added. For differential output devices, the measurements described in 3.1 through 3.2.1 below, as applicable, shall be repeated for the other output using the same test figure except an oscilloscope shall be connected to the other output.

3.1 Phase margin. The test shall be setup as on figure 4002-1 for a gain of 1 noninverting. This is the maximum feedback case. R_2 and R_1 shall be the same value and shall be low compared to the amplifier input impedance. Figure 4002-2 shows the amplitude of the envelope of the output E_O. The peaking shall be less than 3 dB (1.414 times the flat band voltage) to indicate a 45° phase margin minimum. The circuit of figure 4002-3 shall be used for single ended inverting amplifiers (where no positive input terminal is brought out) or where the test is to be run at closed loop gains greater than 1. Closed loop gain = R_2/R_1. In the case of closed loop gains greater than one, the peaking shall be less than 3 dB.

3.2 Pulsed slew rate. Figure 4002-1 or 4002-3 is the test figure for this test. Values of R_2 and R_1 shall be the same values as those used in the phase margin test. Stabilization networks shall also be the same. The pulse amplitude V_1 shall be such that E_0 is the maximum large signal value for the amplifier. With the pulse V_1 having a rise and fall time much faster than the specified slew rate for the amplifier, the rise and fall time for the amplifier shall be measured and shall be within specified limits (see 4). The test shall be repeated for both polarities of V_1.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, and V_1.

a. Maximum peaking.

b. Maximum rise time for E_0 positive pulses.

c. Maximum fall time for E_0 positive pulses.

d. Maximum rise time for E_o negative pulses.

e. Maximum fall time for E_o negative pulses.

f. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

FIGURE 4002-1. Test setup noninverting amplifier.

FIGURE 4002-2. Amplitude of E_o.

FIGURE 4002-3. Test setup single ended inverting amplifier.

METHOD 4003.1

COMMON MODE INPUT VOLTAGE RANGE
COMMON MODE REJECTION RATIO
SUPPLY VOLTAGE REJECTION RATIO

1. PURPOSE. This method establishes the means for measuring common mode input voltage range, common mode rejection ratio, and supply voltage rejection ratio.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Common mode input voltage range (V_{CM}). The common mode input voltage range is that range of common mode input voltages which, if exceeded, will cause the amplifier to distort or is that range of voltage which may be applied to the input terminals of the device without decreasing the common mode rejection ratio (CMRR) by more than 6 dB.

1.1.2 Common mode rejecton ratio (CMRR). The common mode rejection ratio is the ratio of the differential open loop gain, A_D, to the common mode voltage gain, A_C.

$$CMRR = \frac{A_D}{A_C}$$

CMRR is usually expressed in decibels:

$$CMRR = 20 \log \frac{A_D}{A_C}$$

Common mode rejection ratio can also be expressed as the ratio of change in offset voltage to the change in common mode voltage.

$$CMRR = 20 \log \frac{\Delta V_{IO}}{\Delta V_{CM}}$$

1.1.3 Power supply rejection ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage ΔV_{IO}, to the corresponding change in one power supply voltage with all remaining power supply voltage(s) held constant.

$$+PSRR = \frac{\Delta V_{IO}}{\Delta V_{CC}} \qquad V_{BB} = constant$$

$$-PSRR = \frac{\Delta V_{IO}}{\Delta V_{BB}} \qquad V_{CC} = constant$$

$$PSRR = \frac{\Delta V_O}{A_D \, \Delta V_{CC}}$$

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. Assume all switches normally closed. The feedback resistance, R_2 for figure 4003-1, shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (100 x Z_{OUT}). Specified stabilization and power supply decoupling shall be added where applicable.

3.1 Common mode input voltage range.

3.1.1 Differential input amplifier. This test shall be an implied measurement. The maximum common mode input voltage specified for the amplifier shall be used in making the common mode rejection ratio test of 3.2.

3.2 Common mode rejection ratio.

$$CMRR = \left| \frac{A_D}{A_C} \right|$$

where A_D = differential gain, and A_C = common-mode gain.

3.2.1 Differential input amplifier using null loop. The test figure is shown on figure 4003-1, all switches are closed. Raise V+, V-, and V_C to V_{CM} volts above nominal (i.e., if V+ = 15, V- = -15, V_C = 0, V_{CM} = 10, then set V+ = 25, V- = -5, and V_C = 10). Measure E_{01}. Lower V+, V-, and V_C to V_{CM} volts below nominal. Measure E_{02}.

$$CMRR = 20 \log \frac{R_1}{R_2} \frac{(E_{01} - E_{02})}{\Delta V_{CM}}$$

3.3 Power supply rejection ratio.

3.3.1 Differential input amplifier. The power supply shall be adjusted for a value equal to the average of the maximum and minimum allowable supply voltage. The signal generator connected to the power supply under test shall be adjusted such that the voltage input at the amplifier under test swings between maximum and minimum specified values. Then:

$$PSRR = 20 \log \frac{R_1}{R_2} \frac{(\Delta V_O)}{\Delta V_{CC}}$$

where: ΔV_0 = Change in output voltage (peak)
ΔV_{CC} = Change in supply voltage (peak)

The frequency used shall be as specified.

3.3.2 Differential input amplifier using null loop. The test figure is shown on figure 4003-1. Set V_C to zero. For +PSRR set V- to constant voltage and set V+ to minimum value and measure E_{01}; set the V+ supplies to maximum values and measure E_{02}.

$$+PSRR = 20 \log \frac{R_1}{R_2} \frac{(E_{02} - E_{01})}{DV_{CC}}$$

where DV_{CC} is the total change in power supply voltage (if the supplies vary from +5 to +20 V, DV_{CC} = 20 - 5 = 15 V). For -PSRR repeat the above measures with V+ supply held constant and V- varied between the minimum and the maximum value, measure E_{03} and E_{04} respectively.

$$-PSRR = 20 \log \frac{R_1}{R_2} \frac{(E_{04} - E_{03})}{DV_{CC}}$$

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of C_1, C_2, R_1, R_2, R_L and $\pm V_{CC}$ for the nulling amplifier.

a. V_{CM} at specified temperature(s).

b. CMRR at specified temperature(s). V_I signal frequency when applicable.

c. PSRR, when applicable, at specified temperature(s).

d. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

FIGURE 4003-1. Differential input amplifier using null loop.

METHOD 4004.1

OPEN LOOP PERFORMANCE

1. PURPOSE. The purpose of this test procedure is to measure gain, bandwidth, distortion, dynamic range, and input impedance. Gain, dynamic range, and distortion are combined into a large signal test where the distortion measurement will indicate either lack of dynamic range or inherent distortion.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Maximum output voltage swing (V_{OP}). The maximum output voltage swing is the maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent dc output voltage is set at a specified reference level. The swing levels are denoted by $+V_{OP}$ and $-V_{OP}$.

1.1.2 Single ended input impedance (Z_{IN}). The single ended input impedance is the ratio of the change in input voltage to the change in input current seen between either input and ground with the other input terminal ac grounded. In case of single input amplifiers, it is the impedance between that terminal and ground. It is measured at the quiescent output dc level.

1.1.3 Differential input impedance (Z_{DI}). The differential input impedance is the ratio of the change in input voltage to the change in input current seen between the two ungrounded input terminals of the amplifier at the quiescent output dc level.

1.1.4 Voltage gain (A_{VS}). The voltage gain (open loop) is the ratio of the output voltage swing to the single ended or differential input voltage, required to drive the output to either swing limit.

1.1.5 Bandwidth, open loop (BW_{01}). The open loop bandwidth is the range of frequencies within which the open-loop voltage gain of the amplifier is not more than 3 dB below the value of the midband open loop gain.

1.1.6 Distortion. The total ratio of the RMS sum of all harmonics to the total RMS voltage at the output for a pure sine wave input.

1.1.7 Unity gain bandwidth (GBW): The unity gain bandwidth is the frequency at which the output voltage is equal to the input voltage.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. A differential input is shown, but if a single ended inverting amplifier is under test, the components shown at the positive input terminal shall not be used. If a noninverting amplifier is under test, it shall be necessary to either use fixed bias instead of the dc feedback or to use an inverting gain of one amplifier in the feedback path. For differential output devices, the measurements described in 3.1, 3.2, 3.3, and 3.4 below, as applicable, shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

3.1 Open loop gain using the null loop. The test figure is shown on figure 4004-3. The load resistor R_L is grounded. Set V_C to -10 V and measure E_{01}. Set V_C to +10 V and measure E_{02}.

$$A_{VS} = \frac{R_2}{R_1} \quad \frac{20}{E_{02} - E_{01}}$$

3.2 Distortion. Under the conditions of 3.1, read the distortion on the distortion meter or the voltage at the output of the rejection filter if that is used.

3.3 Maximum output voltage swing. The test figure is shown on figure 4004-3. Set V_C equal to zero. Switches S_1 - S_4 are closed. For $+V_{OP}$ apply a V_1 equal to the positive supply voltage $+V_{OP} = V_2$. For $-V_{OP}$ apply a V_1 equal to the negative supply voltage $-V_{OP} = V_2$.

3.4 Bandwidth. Establish the amplitude of V_2 within the linear region of the device under test at a frequency specified for the measurement of A_D. Increase the frequency, while maintaining the amplifier of V_1 constant, until V_2 reduces to 0.707 of the original value (3 dB down). This frequency shall be measured as the bandwidth for the device under test. The test figure is shown on figure 4004-1.

3.5 Input impedance. This will be specified as a minimum value and shall be measured by observing that the output voltage V_2 does not drop more than 6 dB (2:1 in voltage) when the switch S is opened. This test shall be performed at the specified frequency with a specific amplitude of V_2 within the linear region. R_2 shall be given as the value of the minimum input impedance. The test figure is shown on figure 4004-1.

3.6 Unity gain bandwidth. Increase the frequency of e_i (starting at 100 kHz) until $e_o = e_i$. The frequency at which this occurs is GBW. The test figure is shown on figure 4004-4. Set the input voltage V_1 to the required device voltage.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, C, $\pm V_{CC}$ for the nulling amplifier, R_3 and R_L.

a. V_{OP}, at specified temperature(s).

b. Z_{IN} (minimum), at specified temperature(s) and frequency.

c. Z_{OI}, where applicable, at specified temperature(s) and frequency.

d. A_{VS}, where applicable, at specified temperature(s) and frequency.

e. A_V, at specified temperature(s) and frequency.

f. BW_{01}, at specified temperature(s).

g. Distortion (%), at specified temperature(s).

h. V_{OI}, when applicable, at specified temperature(s).

i. GBW, at specified temperatures.

j. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

FIGURE 4004-1. Test figure for bandwidth and input impedance.

FIGURE 4004-2. Transfer function circuit.

FIGURE 4004-3. Test setup for open loop gain, distortion and maximum output voltage swing.

FIGURE 4004-4. Test setup for unity gain bandwidth.

METHOD 4005.1

OUTPUT PERFORMANCE

1. PURPOSE. This method establishes the means for measuring the power dissipation and output impedance.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Output impedance (Z_0). The output impedance is the impedance between the output terminal and ground. It is measured at a specific quiescent dc output voltage and with no ac feedback around the amplifier.

1.1.2 Power dissipation (P_D). The power dissipation is the total power dissipated in the amplifier with the amplifier biased into its normal operating range and without any output load.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figure shown will be used for all three tests. R_1 should be no larger than the nominal input impedance nor less than a value which will load the amplifier ($100 \times Z_{OUT}$). $2 \pi f R_1C_1$ shall be at least $10 A_D$ where A_D is the open loop gain and f is the test frequency. C_2 should be at least $10/2 \pi f R_2$ and R_2 should be about equal to the nominal amplifier Z_0.

3.1 Power dissipation. For this test, the signal generator is off. Measure the positive supply voltage and current V_{CC} and I_C and the negative supply voltage and current V_{EE} and I_E. The power dissipation $P_D = V_{CC} I_C + V_{EE} I_E$.

3.2 Output impedance. For this test, the signal generator frequency is set to a specified value and the level is set to a specified V_2. V_0 is read on the ac voltmeter. The output impedance is then equal to:

$$Z_O = \frac{V_O \ R_2}{V_2 - V_0}$$

An alternate measurement would be to make R_2 equal to the maximum acceptable value of Z_0 and require that V_0 be no greater than $V_2/2$. For differential output devices, this measurement shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, C_1, and C_2.

a. Z_0 limits at the specified frequency.

b. P_D maximum.

c. V_2 where applicable.

d. V_{OI} where applicable at the specified temperature(s).

e. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at 25°C ambient.

FIGURE 4005-1. Test setup-output performance.

METHOD 4006.1

POWER GAIN AND NOISE FIGURE

1. PURPOSE. The purpose of this test procedure is to measure small signal power gain and the noise figure of an amplifier.

1.1. Definition. The following definitions shall apply for the purpose of this test method.

1.1.1 Power gain (PG). The power gain is the ratio, expressed in dB, of the signal power developed at the output of the amplifier to the signal power applied to the input.

$$PG = 10 \log \frac{P_{OUT}}{P_{IN}}$$

1.1.2 Noise factor (F). The noise factor is the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output.

$$F = \frac{\dfrac{P_{IN}}{N_{PIN}}}{\dfrac{P_{OUT}}{N_{POUT}}}$$

Where: P_{IN} = input signal power

P_{OUT} = output signal power

N_{PIN} = input noise power

N_{POUT} = output noise power

1.1.3 Noise figure (NF). The noise figure (NF) is the noise factor (F) expressed in dB.

$$NF = 10 \log F = 10 \log \frac{P_{IN} / N_{PIN}}{P_{OUT} / N_{POUT}}$$

The above expression for NF can be written in terms of voltage since the signal and its associated noise work into the same load.

$$NF = 2o \log \frac{\dfrac{V_{IN}}{N_{IN}}}{\dfrac{V_{OUT}}{N_{OUT}}} = 20 \log \frac{V_{IN}}{N_{IN}} - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

Where: V_{IN} = signal voltage IN

V_{OUT} = signal voltage OUT

N_{IN} = noise voltage IN

N_{OUT} = noise voltage OUT

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. The signal frequency, where applicable, shall be a specified value within the defined bandwidth of the amplifier.

3.1 Power gain. Figure 4006-1 is used for this test. Unless otherwise specified, R_2 shall be equal to the nominal output impedance of the device under test. If the input resistance (R_I) of the device under test is much greater than the source resistance (R_G), unless otherwise specified, a resistor (R) which makes $V_I = 1/2\ V_G$ should be added in series with R_G. The specified ac signal V_G at the specified frequency is applied to the inputs of the amplifier under test. V_I and V_L are recorded. Then:

$$PG(db) = 10 \log \frac{V_L^2}{V_I\,(V_G - V_I)} \times \frac{R_G}{R_2}$$

If the series resistor (R) has been added, then:

$$PG(db) = 10 \log \frac{V_L^2}{V_I\,(V_G - V_I)} \times \frac{R_G^1}{R_2}$$

where: $R_G^1 = R_G + R$

3.2 Power gain (insertion method). If the input resistance (R_I) to the device under test is known, the power gain can be measured by this procedure. On figure 4006-2 with switch S in position 1, and the attenuator set to zero insertion loss, a reference level is established on the oscilloscope. The switch is then moved to position 2, switching in the circuit under test, and the attenuation increased until the output is brought to the previous reference level. The voltage insertion gain of the circuit under test equals attenuator setting in dB. The power gain is then calculated from the following expression:

$$PG(dB) = (Attenuator\ reading) + 20 \log \frac{R_I\,(R_G + R_2)}{R_2\,(R_G + R_I)}$$

where: R_2 equals the nominal output impedance of the circuit under test.

R_G equals the source resistance.

R_I equals the input impedance of the circuit under test, unless otherwise specified.

The accuracy of this measurement is dependent upon the accuracy of the attenuator.

3.3. Noise figure. Figure 4006-3 is used for this test. The input noise voltage shall be calculated from the following expression:

$$N_{IN} = \sqrt{4KT\Delta f \pm R_G}$$

where: K = Boltzmann's constant (1.38×10^{-23} joules/°K)
T = Temperature (°K)
Δf = Noise bandwidth
R_G = Source resistance

The input signal level is then set to ten times (20 dB) N_{IN}. R_X is now adjusted so that the ac voltmeter reads 10 dB on some convenient scale. The input signal V_G is then reduced to zero and the reduction in dB on the output recorded. The noise figure NF is obtained by subtracting this drop in dB from 20 dB. The error in this measurement can be calculated from the following expression:

$$Error\ (dB) = 10 \log \left[\left(\frac{V_{OUT}}{N_{OUT}} \right)^2 + 1 \right] - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

It should be noted that the error will always be in a direction to indicate a lower noise figure than the true noise figure.

3.4 Noise figure, alternate method. In this test, a diode noise generator, as shown on figure 4006-4, is used to measure the noise figure. In this test, with switches S_1 and S_2 in position 1 and the source resistance (R_S) adjusted to a specified value, a reference voltage is read on the ac voltmeter. The switches S_1 and S_2 are then moved to position 2 and the diode source current (I) increased until the previous reference level is read on the ac voltmeter. Using the value of I and R_S, the noise figure is determined for the following expression:

$$NF = 10 \text{ Log } 20\ IR_S$$

The accuracy of this technique is established by the accuracy of the 3 dB pad and the current meter in the noise diode circuit.

3.5 Noise factor. The noise factor can be determined from the following expression:

$$NF = 10 \text{ Log } F$$

In this expression, NF is in dB and F is a numeric.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_2 and R_G:

a. PG, at specified temperature(s) and frequency, and R_2.

b. NF, at specified temperature(s) and frequency.

c. F, at specified temperature(s) and frequency.

d. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

e. Noise bandwidth (Δf) (see 3.3).

f. R_S (see 3.4).

g. R and R_2, when applicable (see 3.1).

FIGURE 4006-1. Power gain test circuit.

FIGURE 4006-2. Power gain test circuit (insertion method).

FIGURE 4006-3. Noise figure test circuit.

FIGURE 4006-4. Noise figure (double power technique).

METHOD 4007

AUTOMATIC GAIN CONTROL RANGE

1. PURPOSE. This method establishes the means for measuring the automatic gain control range of a linear amplifier.

1.1 Definitions. The following definition shall apply for the purpose of this test method.

1.1.1 Automatic gain control range (AGC). The AGC range is the total change in voltage gain which may be achieved by application of a specified range of dc voltages to the AGC input terminal of the device.

$$AGC = 20 \log \frac{A_v \text{ max}}{A_v \text{ min}}$$

2. APPARATUS. The apparatus shall consist of a sweep generator, voltage source, resistors, capacitors, an ac voltmeter, and a distortion analyzer.

2.1 Sweep generator. The sweep generator must cover the frequency range of the amplifier under test. It shall have an adjustable output level which is flat over the sweep range. It shall be capable of single frequency operation.

2.2 Voltage source. The voltage source shall be capable of supplying the specified AGC voltages to the test circuit. The voltage source shall be free of noise or ripple at its outputs.

2.3 Capacitors and resistors. The capacitors and resistors shall be within 1 per cent or better of the specified values and stable over the test temperature range.

2.4 AC voltmeter. The ac voltmeter shall be capable of measuring the amplifier output voltage without loading and shall have a frequency range that will cover the amplifier under test.

2.5 Distortion analyzer. The distortion analyzer or meter shall be usable over the passband of the amplifier and shall not load the amplifier.

3. PROCEDURE. The test circuit shown on figure 4007-1 shall be used for this test. R_L and C_1 shall be selected to properly load and decouple the circuit, respectively. The AGC voltage is set for maximum gain. The input signal is applied (constant frequency) and increased until the output exhibits maximum allowable distortion. The generator is swept over the prescribed range and the bandwidth noted.

The AGC voltage is varied over the specified range and the reduction in gain is measured. The above measurements are repeated and the bandwidth and signal handling capability recorded.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of C_1 and R_L.

a. AGC range.

b. Test frequency range.

c. Increase in bandwidth over the AGC range.

d. Maximum reduction in output impedance, where applicable.

e. Minimum reduction in input signal capability, where applicable.

f. Any other variations when applicable, such as power variation, overloading, limitations as to linearity of gain response versus AGC voltage, etc.

g. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

FIGURE 4007-1. AGC test circuit.

METHOD 5001

PARAMETER MEAN VALUE CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a conformance to a maximum or minimum mean of a parameter measured in any test method listed in section 3000 and 4000 of this standard. This method is not intended for general application to acquisitions where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the average or mean value for a given parameter throughout a lot of shipment of devices. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment to have data logging capability in addition to the capabilities listed in section 3000 and 4000. The data shall be recorded and analyzed to compute the average value of a group of microelectronic devices. The size of the group shall be specified in the applicable acquisition document.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested in accordance with the specified test method. The reading from each device will be recorded. When all devices in the group have been tested, the recorded data shall be averaged (or the mean value computed) and compared against a maximum or minimum limit specified in the applicable acquisition document.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Absolute maximum and minimum limits.

b. Maximum or minimum limits on the average or mean.

c. Group size.

d. Requirements for data logging, special marking, and special provisions for group packaging and shipment, where applicable.

METHOD 5002.1

PARAMETER DISTRIBUTION CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a normal distribution for any test method listed in the 3000 or 4000 series of this standard. This method is not intended for general application to acquisitions where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the distribution of parameter values within the specified group. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment, in addition to the capabilities listed in section 3000 and 4000, to have the capability of rejecting and counting the devices above or below the specified extreme limits, and to also separate and count the devices that fall above or below the sigma limits. If the equipment does not have this capability, the units shall be read to the specified parameter conditions and the data recorded. Identification of units to the data shall also be required. Data analysis and unit separation shall be hand performed in the case where automatic equipment is not used.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested, in accordance with the specific method for the maximum and minimum limits specified in the applicable acquisition document. All failures will be removed from the original group. The remaining units will be tested for the following: Not less than 12 percent but not greater than 18 percent of units tested will fall below the mean -1σ limit. Not greater than 18 percent but not less than 12 percent of units tested will fall above the mean $+1\sigma$ limit.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Absolute maximum and minimum limits.

b. Mean value.

c. $+1\sigma$ and -1σ value.

d. Group size.

e. Requirements for data logging, special markings, and special provisions for packaging and shipment, where applicable.

METHOD 5003

FAILURE ANALYSIS PROCEDURES FOR MICROCIRCUITS

1. PURPOSE. Failure analysis is a post mortem examination of failed devices employing, as required, electrical measurements and many of the advanced analytical techniques of physics, metallurgy, and chemistry in order to verify the reported failure and identify the mode or mechanism of failure as applicable. The failure analysis procedure (as indicated by test condition letter) shall be sufficient to yield adequate conclusions, for determination of cause or relevancy of failure or for initiation of corrective action in production processing, device design, test or application to eliminate the cause or prevent recurrence of the failure mode or mechanism reported.

1.1 Data requirements. When required by the applicable acquisition document the failure analyst shall receive, with the failed part, the following information:

a. Test conditions: This shall include the type of test or application, the in-service time (when available), temperature, and other stress conditions under which the device failed.

b. System conditions: This shall include the exact location of failure in the equipment, date, test and inspection or both, at which defect was first noted, any unusual environmental conditions and all related system anomalies noted at time of removal of the failed unit. The equipment symptoms shall also be recorded.

c. General device information: This shall include part type numbers and serial numbers (when applicable), date code, and other identifying information, and size of production or inspection lot (when applicable).

2. APPARATUS. The apparatus required for failure analysis includes electrical test equipment capable of complete electrical characterization of the device types being analyzed, micromanipulators capable of point-to-point probing on the surface of device dies or substrates, as required, and microscopes capable of making the observations at the magnifications indicated in the detailed procedures for the specified test condition. In addition, special analytical equipment for bright field, dark field and phase contrast microscopy, metallographic sectioning, and angle lapping are required for the test condition C. Special analytical equipment for test condition D are as detailed in the procedure and shall be available only as required for each specific device analysis at that level. Apparatus for x-ray radiography, hermeticity test, and other specific test methods shall be as detailed in the referenced method. Cleaning agents, chemicals for etching, staining, oxide, or metallization removal shall be available as required.

3. PROCEDURE. Failure analysis shall be performed in accordance with the specified test condition letter (see 4).

3.1. Test condition A. Failure verification. This represents a minimal diagnosis, comprised of the electrical verification of the failure including external and internal photographic recording of the suspected mode or mechanism of failure. The following steps (see 3.1.1 through 3.1.5) shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.1.1 External examination. This shall include an optical examination at a magnification of 30X minimum of:

a. The condition of the leads, plating, soldered, or welded regions.

b. Condition of external package material, seals, marking, and other failures as warranted.

Photographic records shall be made at suitable magnification of any unusual features.

3.1.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable acquisition document.

3.1.3 Additional electrical tests. These shall be performed specifically for the determination of opens and shorts:

a. Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or an abnormally high resistance current path.

b. Case isolation. (For metal packages or those with metal lids or headers only.) Apply a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.

c. As an alternative to a. and b. above, suitable electrical tests may be made to determine that no opens, shorts, or abnormal characteristics exist between pairs of pins, pins and die or substrate, or pins and device package.

3.1.4 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure.

3.1.5 Information obtainable. The following is a partial list of failure modes and mechanisms which may be identified using test condition A:

a. Overstress conditions resulting from device abuse, transients, or inadequate power supply regulation, evidenced as open or shorted leads, and other metallization problems, such as flashover between contacts with the circuit.

b. Excessive leakage currents indicating degraded junctions.

c. Resistance changes.

d. Degradation of time response or frequency dependent parameters.

e. Opens and shorted leads or metallization land areas.

f. Undercut metals.

g. Intermetallic formation.

h. Poor bond placement and lead dress.

i. Thin metal at oxide steps.

j. Migration of metal.

k. Oxide contamination - discoloration.

l. Oxide defects, cracks, pinholes.

m. Mask misregistration.

n. Reactions at metal/semiconductor contact areas.

o. Degradation of lead at lead frame.

p. Shorts through the oxide or dielectric.

q. Missing or peeling metals.

r. Corroded metals within package.

s. Cracked die or substrate.

3.2 Test condition B. This is a more extensive procedure which supplements test condition A with x-ray radiography, seal testing, additional electrical measurements, package cleaning, vacuum baking, and probing procedures to aid in confirmation of suspected modes and mechanisms. The following steps shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.2.1 External examination. This shall include an optional examination at a magnification of 30X minimum of:

a. The conditions of leads, platings, soldered, or welded regions.

b. Condition of external package material, seals, markings, and other features as warranted.

Photographic records shall be taken at suitable magnification of any unusual features.

3.2.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable acquisition document.

3.2.3 Additional electrical tests. In addition to the threshold and case isolation tests, this section provides for curve tracer pin to pin measurements and other nonstandard measurements which allow electrical characterization of significant physical properties.

a. Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or abnormally high resistance in the current path.

b. Case isolation. (For metal packages or those with metal lids or headers only.) Applying a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.

c. Pin-to-pin two and three terminal electrical measurements utilizing a transistor curve tracer, electrometer, picoammeter, capacitance bridge, and oscilloscope, as required, shall be performed and results recorded for lead combinations involving the defective portion of the microcircuit. Gain, transfer, input versus output, forward and reverse junction characteristics, shall be observed and interpreted. Resulting characteristics may be compared to those obtained from a good unit, and differences interpreted for their relation to the device failure.

3.2.4 X-ray radiography. A film record is required of the failed device taken normal to the top surface of the device, and where applicable, additional views shall be recorded. This shall be performed when open or shorted leads, or the presence of foreign material inside the device package are indicated from electrical verification of failure or there is evidence of excessive temperature connected with the device failures.

3.2.5 Fine and gross seal testing. This shall be performed in accordance with method 1014 of this standard.

3.2.6 External package cleaning. When there is evidence of contamination on the package exterior, the device shall be immersed in standard degreasing agents followed by boiling deionized water. After drying in clean nitrogen, critical parameters in the applicable acquisition document shall be remeasured in accordance with 3.2.1 above.

3.2.7 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction, at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure. Where there is evidence of foreign material inside the device package, it shall be removed using a stream of dry compressed inert gas or appropriate solvents. The relationship of the foreign material to device failure (if any) shall be noted and if possible, the nature of the material shall be determined.

3.2.8 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.9 Vacuum bake. This shall be performed at the suggested condition 10^{-5} torr, 150°C to 250°C for 2 hours noting any change in leakage current, as a result of baking, using a microammeter.

3.2.10 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.11 Multipoint probe. A multipoint probe shall be used as applicable to probe active regions of the device to further localize the cause of failure. A curve tracer shall be used to measure resistors, the presence of localized shorts and opens, breakdown voltages, and transistor gain parameters. A microammeter shall be used for measuring leakage currents, and where applicable, a capacitance bridge shall be employed for the determination of other junction properties. It may be necessary to open metallization stripes to isolate components.

3.2.12 Information obtainable. The procedures of test condition B can result in the following information in addition to that outlined in 3.1.5:

a. Hermeticity problems.

b. Radiographically determined defects such as poor wire dress, loose bonds, open bonds, voids in die or substrate mount, presence of foreign materials.

c. Further definition of failed device region.

d. Stability of surface parameters.

e. Quality of junctions, diffusions and elements.

3.3 Test condition C. In this procedure additional metallographic analysis techniques are provided to supplement the analysis accomplished in test condition B, and shall be performed after completion of the full procedure of test condition B. In test condition C, one of the procedures (see 3.3.1, 3.3.2, and 3.3.3) shall be selected as appropriate and the steps shall be followed in the sequences indicated. The sequence may be modified or additional tests performed when justified by the analysis of the results of previous steps in the sequence.

3.3.1 Total device cross section. This procedure shall be used where there are indications of defects in the package, die or substrate, bonds, seals, or structural elements. The following steps shall be performed:

a. Mount the device in the appropriate orientation for cross sectioning procedures.

b. Section to reveal desired feature(s) and stain where applicable.

c. Employ bright field, dark field, or polarized light photomicrography at suitable magnification.

d. Make photographic record of defective regions or features pertinent to the mode or mechanism of failure.

3.3.2 Oxide defect analysis. This procedure shall be used where there are indication of oxide (or other dielectric) structural anomalies or contamination within or under the oxide or where it is necessary to determine the specific location and structure of such defects. The following steps shall be performed:

a. Remove bonds to die or substrate and remove metallized interconnection layer(s).

b. Observe the oxide using interferometric or phase contrast photomicrography at suitable magnification and make appropriate photographic record.

c. Observe and probe semiconductor contact (window or cut) areas as applicable, recording appropriate electrical characteristics.

d. Mount the die or substrate in the appropriate orientation for sectioning (angle or cross) procedures, cut or lap to reveal desired features and stain where applicable.

e. Make photographic record at suitable magnification.

3.3.3 Diffusion defect analysis. This procedure shall be used where there are indications of diffusion imperfections, diffusion of contact metal into the semiconductor, structural defects in the semiconductor or anomalies in junction geometries. The following steps shall be performed:

a. Remove bonds to die or substrate and remove metallized interconnection layer(s).

b. Remove oxide or other dielectric passivation layer.

c. Probe contact regions recording appropriate electrical characteristics.

d. Stain surface to delineate junctions.

e. Mount the die or substrate in the appropriate orientation for cross sectioning or angle lapping, as applicable.

f. Cut or lap as required to expose significant features and stain junctions (may involve successive lap and stain operations to approach specific defect).

g. Make photographic record at suitable magnification of significant features and record pertinent electrical probing results.

3.3.4 Information obtainable. Failure analysis in accordance with test condition C provides additional capability for detecting or defining the following types of defects:

a. Oxide or dielectric imperfections.

b. Oxide or dielectric thicknesses.

c. Diffusion imperfections.

d. Junction geometries.

e. Intermetallic phase formation.

f. Voids at the bond/metallization interface.

g. Diffusion of contact metal into the semiconductor or substrate.

h. Migration of metals across, through, or under the oxide or dielectric.

i. Voids in die or substrate mount.

3.4 Optional measurements. The purpose of failure analysis is to obtain sufficient information to initiate corrective action in device design, production, test, or application. It may be necessary to obtain more detailed information than can be acquired in test conditions A, B, or C on the nature of contaminants or phases observed, concentrations, dimensions of submicroscopic features, etc. The selection and use of a number or less conventional analytical techniques by highly qualified personnel can provide this more extensive or fundamental knowledge of the precise chemical, physical, or electrical mechanisms of failure. The decision as to which techniques are appropriate and the point in the analytical sequence of test conditions A, B, or C at which they should be employed is contingent on the nature of information desired and previous results obtained from the specified analytical procedures, and must be left to the discretion of the analyst. Any of the following techniques may therefore be introduced into a failure analysis sequence at the appropriate point provided precautions are taken to avoid destruction of the evidence of failure which may be observed in subsequent procedures. Where multiple samples of the same type of device or failure exist, it shall be permissible to subdivide the quantity of devices and employ destructive techniques in parallel with the specified test condition provided all samples have been exposed to electrical verification tests and internal examination (see 3.1.1 through 3.1.3 and 3.2.1 through 3.2.5) prior to any of the optional measurements. When any of these optional measurements are employed, they shall be listed in the failure analysis report including the details of the method applied, conditions of test and results.

a. Residual gas analysis. When device surface contamination is indicated as a possible cause of failure, the lid of an unopened device shall be punctured and the internal gaseous ambient analyzed for the type and concentration of volatile products. This information then supplements electrical leakage current measurements and hermeticity tests.

b. Surface profilometer measurement. A mechanical determination of surface topography variations can be made using this type of instrument. This records the vertical motion of a stylus moved across the surface of the device. This information can be used to quantitatively determine oxide, dielectric, or metal thicknesses.

c. Photoscanning. A device, with leads and interconnections intact, after being opened, can be scanned with a small diameter beam of light which generates photovoltages in active p-n junctions. This generated photovoltage which is dependent on many physical junction properties indicates the presence of surface channels or inversion layers or both, caused by contamination on, in, or under the passivating oxide layer. It is also possible to locate certain regions of enhanced high field multiplication, mask misregistration, imperfect diffusions, as well as other device imperfections involving junction properties.

d. Infrared scanning. An IR detector, sampling infrared radiation from various points of the surface of an operating microcircuit, can detect the location of hot spots and other thermal abnormalities.

e. Scanning electron microscopy and electron beam microanalysis. The scanning electron microscope, employing an electron beam with a diameter on the order of a few hundred angstroms, is the most effective means of attaining device structural information without the need for special sample preparation procedures. The scanning electron microscope can perform chemical analysis, such as the microanalyzer, by incorporating a nondispersive x-ray detector. An electron beam microanalyzer can be used for x-ray spectrochemical analysis of micron sized volumes of material. Several other device structural properties are determinable through detection and display of back-scattered primary electrons and secondary electrons. These instruments are most generally used for:

(1) Determination of surface potential variations using secondary electron scanning microscopy. The small size of the electron beam coupled with the properties of secondary electrons result in the ability to examine physical defects with much higher resolution and depth of field than light microscopy.

(2) Analysis of micron sized defects such as oxide pin-holed, metallization grain structure.

(3) Determination of products of solid state reactions, such as diffusion, precipitation, and intermetallic formation.

(4) Corrosion product identification.

f. Electron microscopy. An examination at extremely high magnification of the structure of failed metallization and bulk materials is best accomplished using electron microscopy.

g. Special test structures. Often the amount of reacted material on a failed circuit is too small to allow definitive determination of chemical and structural properties. In addition, it is often necessary to reproduce the failure in a controlled experimental manner for verification of the mechanism of failure. Special test structures may be fabricated with variations in geometry and materials permitting study of the mechanism without extraneous influences. This is most advantageous when information is desired concerning the basic failure mechanism(s).

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Test condition letter (see 3.) for test conditions A, B, or C and where applicable, optional measurements (see 3.4), identifying the specific procedures to be applied and details as to their option application.

b. Any special measurements not described in the applicable test condition.

c. Requirements for data recording and reporting including instructions as to disposition of original data, photographs, radiographs, etc.

d. Physical and electrical specifications and limits for the device being analyzed.

METHOD 5004.10

SCREENING PROCEDURES

* 1. PURPOSE. This method establishes screening procedures for total lot screening of microelectronics to assist in achieving levels of quality and reliability commensurate with the intended application. It must be used in conjunction with other documentation such as appendix A of MIL-PRF-38535 or an applicable device specification to establish the design, material, performance, control, and documentation requirements which are needed to achieve prescribed levels of device quality and reliability. In recognition of the fact that the level of screening has a direct impact on the cost of the product as well as its quality and reliability, two standard levels of screening are provided to coincide with two device classes or levels of product assurance. Since it is not possible to prescribe an absolute level of quality or reliability which would result from a particular screening level or to make a precise value judgment on the cost of a failure in an anticipated application, two levels have been arbitrarily chosen. The method provides flexibility in the choice of conditions and stress levels to allow the screens to be further tailored to a particular source, product, or application based on user experience. The user is cautioned to collect experience data so that a legitimate value judgment can be made with regard to specification of screening levels. Selection of a level better than that required for the specific product and application will, of course, result in unnecessary expense and a level less than that required will result in an unwarranted risk that reliability and other requirements will not be met. In the absence of specific experience data, the class B screening level is recommended for general applications. Guidance in selecting screening levels or predicting the anticipated reliability for microcircuits may be obtained from MIL-HDBK-217 Military Standardization Handbook Reliability Prediction.

* NOTE: Reference to method 5004 on a stand alone basis (not indicating compliance or noncompliance to 883) requires full compliance to 1.2.1 of this standard.(See 1.2.2)

2. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

3. PROCEDURE.

* 3.1 Screening procedures for microcircuits. Screening of microcircuits shall be conducted as described in 3.1.1 through 3.1.19 and in the sequence shown except where variations in sequence are specifically allowed herein. This provision does not preclude the performance of additional tests or inspection which may be required for specific devices or which may be desirable to optimize results of screening; however, any such special test inspections shall be subjected to the requirements of 30.4.3 of appendix A of MIL-PRF-38535. Any burn-in in addition to that specified is only permitted when documented in the lot records, and any failures shall be counted in applicable PDA calculations. Where end-point or post-test measurements are required as part of any given test method used in the screening procedure and where such post test measurements are duplicated in the interim (post burn-in) or final electrical tests that follow, such measurements need not be duplicated and need be performed only as part of the interim (post burn-in) or final electrical tests. Devices which pass screening requirements of a higher reliability level shall be considered to meet the screening requirements of all lower levels. In no case shall screening to a lower level than that specified be permitted. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or which have a package mass of 5 grams or more may be treated in accordance with 3.2 as an alternative to 3.1.5.

* Qualified manufacturers list (QML) manufacturers who are certified and qualified to MIL-PRF-38535 or who have been granted transitional certification to MIL-PRF-38535 may modify the class level B screening table (table I) as specified in the applicable device specification or drawing and as permitted in 1.2 of MIL-STD-883 provided the modification is contained in the manufacturers quality management (QM) plan and the "Q" or "QML" certification mark, is marked on the devices. For contractor prepared drawings with specific references to individual test methods of MIL-STD-883 (e.g., method 1010, method 2001, etc.), these test methods may not be modified by a QML manufacturer without the knowledge and approval of the acquiring activity.

3.2 Constant acceleration procedure for large packages (see 3.1.5). Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be treated in accordance with provisions below as an alternate to the procedure of 3.1.5.

Delete test condition E and replace with test conditions as specified in the applicable device specification. Unless otherwise specified, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

3.3 Alternate procedures to method 2010 internal visual for microcircuits. Alternate procedures may be used on an optional basis on any microcircuit, provided that the conditions and limits of the alternate procedures are submitted to, and approved by the preparing activity, or the acquiring activity.

3.3.1 Alternate procedures.

* Alternate 1: The deletions and the changes stated in 3.3.1a are allowable for class level B product only if the requirements of 3.3.1b and 3.3.1c are imposed and any of the following conditions exists.

1. Minimum horizontal geometry is less than 3 micrometers (:m).
2. Interconnects consisting of two or more levels.
3. Opaque materials mask design features.

a. For inspection of each microcircuit die, delete the inspection criteria of 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.1.5, 3.1.6, 3.1.7, and 3.2.5 of condition B of method 2010 and for use in conjunction with alternate procedures add 3.1.1.1, 3.1.1.2, 3.1.1.6, 3.1.3, 3.1.4, and 3.2.5 to the low magnification inspection of method 2010.

b. Temperature cycling (3.1.4). The minimum total number of temperature cycles shall be 50. The manufacturer may reduce the number of temperature cycles from 50 to the 10 required as part of normal screening based upon data justifying the reduction in temperature cycles, approved by the preparing activity and an approved plan which shall include the following criteria:

(1) Reduction of test must be considered separately for each wafer fabrication line and each die family.

(2) The manufacturer shall demonstrate that the wafer fabrication line that produces product which will involve reduction of temperature cycles is capable and in process control.

(3) The manufacturer shall perform a high magnification visual inspection on a small sample of devices (e.g., 5(0)) to monitor the process. This inspection may be performed at wafer level.

c. Special electrical screening tests shall be applied to each microcircuit die at the wafer, individual die (chip) or packaged microcircuit level in accordance with the requirements of 3.3.2 of MIL-STD-883, method 5004. The conditions and limits of the electrical tests (in table III format) shall be submitted to the preparing activity for approval and subsequently maintained on file with the qualifying activity. These special screens are in addition to the required electrical parametric tests which the device must pass and shall be designed to screen out devices with defects that were not inspected to the full criteria of 3.1.3 (internal visual). Due to the nature of these tests, they are not to be repeated as part of the qualification and quality conformance procedures in accordance with method 5005.

* Alternate 2: The requirements and conditions for use of this alternate are contained in appendix A of this method. This option applies to both class level B and class level S microcircuits.

TABLE I. Class level S and level B screening.

Screen	Class level S		Class level B	
	Method	Reqt	Method	Reqt
3.1.1 Wafer lot acceptance 1/	5007	All lots		---
3.1.2 Nondestructive bond pull	2023	100%		—
3.1.3 Internal visual 2/	2010, test condition A	100%	2010, test condition B	100%
3.1.4 Temperature cycling 3/	1010, test condition C	100%	1010, test condition C	100%
3.1.5 Constant acceleration (see 3.2 and 3.4.2)	2001, test condition E (min) Y1 orientation only	100%	2001, test condition E (min) Y1 orientation only	100%
3.1.6 Visual inspection 4/		100%		100%
3.1.7 Particle impact noise detection (PIND)	2020, test condition A	100% 5/		—
3.1.8 Serialization		100% 6/		—
3.1.9 Pre burn-in electrical parameters (see 3.5.1)	In accordance with applicable device specification	100% 7/	In accordance with applicable device specification	100% 8/
3.1.10 Burn-in test (see 3.4.2)	1015 9/ 240 hours at 125°C minimum	100%	1015 160 hours at 125°C minimum	100%
3.1.11 Interim (post burn-in) electrical parameters (see 3.5.1)	In accordance with applicable device specification	100% 7/		—
3.1.12 Reverse bias burn-in (see 3.4.2) 10/	1015; test condition A or C, 72 hours at 150°C minimum	100%		—
3.1.13 Interim (post burn-in) electrical parameters (see 3.5.1)	In accordance with applicable device specification	100% 7/	In accordance with applicable device specification	100% 8/

See footnotes at end of table.

TABLE I. Class level S and level B screening - Continued.

Screen	Class level S		Class level B	
	Method	Reqt	Method	Reqt
3.1.14 Percent defective allowable (PDA) calculation	5 percent, see 3.5.1, 3 percent, functional parameters at 25°C	All lots	5 percent, see 3.5.1	All lots
3.1.15 Final electrical test (see 3.5.2)	In accordance with applicable device specification		In accordance with applicable device specification	
a. Static tests				
(1) 25°C (subgroup 1, table I, 5005)		100%		100%
(2) Maximum and minimum rated operating temperature (subgroups 2, 3, table I, 5005)		100%		100%
b. Dynamic or functional tests 11/				
(1) 25°C (subgroup 4 or 7, table I method 5005)		100%		100%
(2) Minimum and maximum rated operating temperature (subgroups 5 and 6, or 8 table I method 5005)		100%		100%
c. Switching tests at 25°C (subgroup 9, table I, method 5005)		100%		100%
3.1.16 Seal a. Fine b. Gross	1014	100% 12/	1014	100% 12/
3.1.17 Radiographic 13/	2012 two views 14/	100%		—
3.1.18 Qualification or quality conformance inspection test sample selection		15/		15/
3.1.19 External visual 16/	2009	17/	2009	17/
3.1.20 Radiation latch-up (see 3.5.3) 18/	1020	100%	1020	100%

See footnotes at top of next page.

TABLE I. Class level S and level B screening - Continued.

1/ All lots shall be selected for testing in accordance with the requirements of method 5007 herein.

2/ Unless otherwise specified, at the manufacturer's option, test samples for group B, bond strength (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam). Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3).

3/ For class level B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

4/ At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

5/ See appendix A of MIL-PRF-38535, 40.6.3. The PIND test may be performed in any sequence after 3.1.4 and prior to 3.1.13.

6/ Class level S devices shall be serialized prior to initial electrical parameter measurements.

7/ Post burn-in electrical parameters shall be read and recorded (see 3.1.13, subgroup 1). Pre burn-in or interim electrical parameters (see 3.1.9 and 3.1.11) shall be read and recorded only when delta measurements have been specified as part of post burn-in electrical measurements.

8/ When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.

9/ Dynamic burn-in only. Test condition F of method 1015 and 3.4.2 herein shall not apply.

10/ The reverse bias burn-in (see 3.1.12) is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameter measurements 3.1.11 are omitted. The order of performing the burn-in (see 3.1.10) and the reverse bias burn-in may be inverted.

11/ Functional tests shall be conducted at input test conditions as follows:
$V_{IH} = V_{IH}(min)$ +20 percent, -0 percent; $V_{IL} = V_{IL}(max)$ +0 percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

TABLE I. Class level S and level B screening - Continued.

12/ For class level B devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between constant acceleration (3.1.5) and external visual (3.1.19). For class level S devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between final electrical testing (3.1.15) and external visual (3.1.19). In addition, for class level S and level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal (3.1.16) or external visual (3.1.19) shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal (3.1.16), but before external visual (3.1.19) if the devices are installed in individual carriers during electrical test.

13/ The radiographic (see 3.1.17) screen may be performed in any sequence after 3.1.8.

14/ Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

15/ Samples shall be selected for testing in accordance with the specific device class and lot requirements of method 5005. See 3.5 of method 5005.

16/ External visual shall be performed on the lot any time after 3.1.17 and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

17/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Reinspection magnification shall be no less than that used for the original inspection for the failed criteria.

18/ Radiation latch-up screen shall be conducted when specified in purchase order or contract. Latch-up screen is not required for SOS, SOI, and DI technology when latch-up is physically not possible. At the manufacturer's option, latch-up screen may be conducted at any screening operation step after seal.

3.3.2 Description of special electrical screening tests. The special electrical screens shall consist of a series of electrical tests each of which can be categorized as either a voltage stress test or a low level leakage test.

3.3.2.1 Voltage stress tests. The purpose of voltage stress tests is to eliminate those failure mechanisms which are voltage sensitive. These tests shall be designed such that each circuit element (including metallization runs) within the microcircuit is stressed by an applied voltage which approaches or exceeds (under current limited conditions) the breakdown voltage of the circuit element under test. For those elements which cannot be placed in a reverse bias mode, the applied voltage must be equal to or greater than 120 percent of the normal operating voltage. Any device which exhibits abnormal leakage currents at the specified applied voltage conditions shall be rejected. The number of stress tests being performed will vary from a few for a simple gate to many for MSI or LSI functions.

3.3.2.2 Low level leakage tests. The purpose of the low level leakage tests (which must be performed after the voltage stress tests) is to eliminate any device that exhibits abnormal leakage. Since leakage currents can be measured only at the device terminals, the test conditions and limits will vary depending upon the type of device being tested and the function of the terminal under test (V_{CC}, input, output, etc.). However, there may be cases where this test cannot be performed, i.e., input terminals which are forwarded biased junctions or resistive networks. But, since these types of circuits are generally very sensitive to leakage currents, the device would fail parametrically if abnormal leakage currents were present. For all other cases, where these measurements can be made, the tests shall be designed as described below:

a. For inputs which can be reverse biased, measure the input leakage at each input terminal at a voltage level which is equal to one-half the maximum rated input voltage for that device with the supply terminal grounded. The maximum allowable input leakage shall be established as shown in 3.3.2.2.1. Inputs shall be tested individually with all other input terminals grounded.

b. For outputs which can be reverse biased, measure the output leakage at each output terminal at a voltage which is equal to the device's maximum rated input voltage with the supply terminal grounded (if possible). The maximum allowable output leakage limit shall be established as shown in 3.3.2.2.1. The input terminals shall be all grounded (if the supply terminal is grounded) or if the supply terminal is not grounded, the input terminals should be in such a state that the output terminal under test is in the reverse biased mode. All outputs shall be tested.

c. Measure the supply terminal leakage current at a voltage which is equal to 80 percent of the voltage required to forward-bias a single PN junction on the device under test. The maximum allowable supply terminal leakage shall be established as shown in 3.3.2.2.1.

3.3.2.2.1 Establishing maximum leakage current limits. The maximum allowable leakage current shall be the upper 3 sigma value as established through an empirical evaluation of three or more production lots which are representative of current production. Any process change which results in a substantial shift in the leakage distribution shall be cause for recalculation and resubmission of this limit. The low current sensitivity of the test system shall be no higher than 20 percent of the expected mean value of the distribution.

3.4 Substitution of test methods and sequence.

3.4.1 Stabilization bake. Molybdenum-gold multilayered conductors shall be subject to stabilization bake in accordance with method 1008, condition C immediately before performing internal visual inspection 3.1.3.

3.4.2 Accelerated testing. When test condition F of method 1015 for temperature/time accelerated screening is used for either burn-in (see 3.1.10) or reverse bias burn-in (see 3.1.12), it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test (3.1.5) shall be performed after burn-in and before completion of the final electrical tests (3.1.15) (i.e., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

3.5 Electrical measurements.

* 3.5.1 Interim (pre and post burn-in) electrical parameters. Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA, or 20 percent whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

* 3.5.2 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the applicable device specification or drawing and shall include, as a minimum, all parameters, limits, and conditions of test which are specifically identified in the device specification or drawing as final electrical test requirements. Final electrical test requirements that are duplicated in interim (post burn-in) electrical test (see 3.1.15) need not be repeated as final electrical tests.

* 3.5.3 Radiation latch-up screen. Latch-up screen shall be conducted when specified in purchase order or contract. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

* 3.6 Test results. When required by the applicable device specification or drawing, test results shall be recorded and maintained in accordance with the general requirements of 4.2 of this standard and 40.7 of appendix A of MIL-PRF-38535.

3.7 Failure analysis. When required by the applicable device specification, failure analysis of devices rejected during any test in the screening sequence shall be accomplished in accordance with method 5003, test condition A of this standard.

3.8 Defective devices. All devices that fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failures was observed. Once rejected and verified as a device failure, no device may be retested for acceptance.

4. SUMMARY. The following details shall be specified:

a. Procedure paragraph if other than 3.1, and device class.

b. Sequence of test, test method, test condition, limit, cycles, temperature, axis, etc., when not specified, or if other than specified (see 3).

c. Interim (pre and post burn-in) electrical parameters (see 3.5.1).

d. Burn-in test condition (see 3.1.10) and burn-in test circuit.

e. Delta parameter measurements or provisions for PDA including procedures for traceability where applicable (see 3.5.1).

f. Final electrical measurements (see 3.5.2).

g. Constant acceleration level (see 3.2).

h. Requirements for data recording and reporting, where applicable (see 3.6).

i. Requirement for failure analysis (see 3.7).

APPENDIX A

PURPOSE:

This document addresses two problems. First, TM2010 visual criteria for wafer fab induced defects is unsuitable for complex wafer process technologies, as in most cases the defects themselves cannot be seen through 200X magnification. Secondly, no current alternate suitably addresses defect control of complex wafer fab technologies. Section 2 of this document describes the conditions under which this procedure is invoked. This document implements a new technique for controlling and eliminating wafer fab induced defects, while preserving and extending the intent of the original test method 2010 visual criteria.

The essence of this procedure revolves around the concept that it is a manufacturer's responsibility to define and document its approach to defect reduction and control in a manner that is acceptable to the manufacturer and their qualifying activity, as specified in section 3 of this document. This includes an understanding of the reliability impact of wafer fab process-induced defects. It is expected that considerable dialogue will occur between a manufacturer and the qualifying activity, resulting in mutually agreeable defect control procedures. This document is deliberately non-specific regarding metrics such as defect sizes, defect densities, correlation and risks to allow adaptability for different process technologies, different manufacturing control methods and continuous improvement. The procedures are specified in this document with the intent that metrics and their values will be made more specific via dialogue between a manufacturer and its qualifying activity.

Defect characterization is addressed in section 4 of this document. A key element in this section is understanding the effects of process defects on final product reliability. This understanding can be achieved in many ways, including: experimentation, review of pertinent literature and certain semiconductor traditions. The depth and scope of any characterization will be determined by a manufacturer and its qualifying activity.

The concept of demonstration is discussed in many sections of this document. The methods for demonstrating defect understanding have been made as diverse as possible to allow flexibility.

As described in section 9 of this document, results of defect characterization must be documented as well as the methods for monitoring and controlling defect levels. The effectiveness of any screens that are used (in-line or end-of-line) must also be documented. The ultimate requirements for demonstration and documentation will be determined between a manufacturer and its qualifying activity. The qualifying activity will be concerned with maintenance of institutional knowledge and the level to which a manufacturer understands: defect generation, control, reduction, prevention and the effects of defects on product reliability.

This document makes the underlying assumption that a manufacturer will undertake efforts to continuously improve defect levels (i.e. reduce these levels) in its wafer fabrication processes. As part of this assumption, it is expected that the inspections, as outlined in section 5 of this document, will be used to acquire information for defect level reduction. The intent is not to create inspections which "inspect in" quality, though screens of this nature may be a part of a manufacturer's integrated defect control system. Rather, it is intended to provide an effective means of defect prevention, control and reducing defects generated by the wafer process. Ideally, the manufacturer is striving to continually improve its control systems.

Sections 6, 7 and 8 of this document deal with excursion containment, yield analysis and a system for unexpected failure.

This document makes extensive use of examples and attachments to illustrate key points and ways in which these points could be implemented. The examples are intended to be no more than examples, illustrating how the items in this procedure might be performed in a given instance. They are not intended to specify the way items must be done. A glossary of terms is provided in section 100. of this document.

APPENDIX A

Introduction:

The evolution and progress in semiconductor fabrication technology require that new quality assurance methodologies be employed which are applicable to small geometry and multiple metallization microcircuits. Removal of ineffective visual inspections require an effective foreign material and defect control program early in the manufacturing process. It is the intent of this procedure to define the key elements of such a program. It is the responsibility of each manufacturer to define and document his approach to manufacturing defect reduction and control. This program shall be approved by the qualifying activity.

The goal of this procedure is to assure that defects induced during the wafer fabrication process shall be minimized to such an extent as to avoid non-conformance of product to device specifications or premature termination of its useful life. It is expected that killer defects (as defined by the manufacturer) will not be found in the delivered product. It is expected that critical defects (as defined by the manufacturer) will be controlled to meet the intended product life.

10. Scope:

10.1 This procedure may be conducted for complex technology microcircuits when any of the following conditions exist:

a. Minimum horizontal geometries are equal to or less than 1.5 μm final dimension of any current carrying conductors on the wafer, or

b. Interconnects (eg. metal, polysilicon) conducting current consist of three or more levels and the number of logical gates exceeds 4000.

c. Opaque materials mask design features and either or both conditions A or B apply.

10.2 This procedure may be subject to review by the acquiring activity.

10.3 Any manufacturer required to be compliant with this procedure for complex microcircuits may extend it to other devices (optional devices) that do not meet the conditions as specified in 10.1, conditions a through c herein. Extension applies only if those optional devices are manufactured primarily on the same wafer process line to most of the same process baseline (the majority of the fab equipment and process baseline used to fabricate required product as defined in 10.1, conditions a through c, is also used on extension product). All elements of the processes that are different for the extension products must meet the requirements herein.

10.4 This procedure allows for the removal, modification or reduction of inspections and screens, as a result of process improvements. For such changes, the process (and/or sub-process) must be sufficiently characterized to permit such action. Data supporting these changes must be made available to the qualifying activity upon request.

10.5 This procedure is applicable only to wafer fabrication related defects. When using this procedure the manufacturer is exempt from sections 3.1.1 (except as noted below), 3.1.2, 3.1.4, 3.1.5, 3.1.6 and 3.1.7 of conditions A and B of test method 2010. Assembly induced defects (ie: scribe damage, probe damage, bond integrity, die surface scratches and foreign material) shall be inspected at low power (30X to 60X) only, in accordance with sections 3.1.1.1, 3.1.1.6, 3.1.3 and 3.2.5 of test method 2010, conditions A and B as applicable.

10.6 This procedure does not override the requirements of any other government specifications, unless otherwise specified herein.

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20. APPLICABLE DOCUMENTS (This section is not applicable to this document.)

30. Qualifying activity approval:

30.1 The manufacturer's implementation of this procedure shall be validated (audited) by the qualifying activity. The qualifying activity will issue a letter of suitability to the supplier, prior to delivery of compliant product. The letter of suitability shall specify exactly what is covered (eg: description of wafer fab line, including: location, process baseline, optional devices and technologies, etc.)

30.2 The qualifying activity shall recognize the need for auditor expertise in semiconductor wafer fabrication in order to validate a line to the requirements herein. Expertise in semiconductor wafer fabrication consists of: an understanding of wafer fabrication process flow, wafer fabrication process and measurement tools, wafer fabrication process chemistry and physics, reliability physics and defect generation and control.

40. Characterization of defects and screening effectiveness:

40.1 Products built using this procedure must have the process characterized to determine "non-critical" defects, "critical" defects and "killer" defects and to understand their impact on reliability. The characterization must consider interactive effects to the extent they have a reasonable probability of occurrence (eg: contact resistance change as affected by contact critical dimension variations interacting with dielectric film thickness variations). Defect characterization must identify categories of known defects (see 40.3), the source of each defect type (to the extent necessary to insure adequate defect control) and their population (ie: random, variation from die to die within a wafer, variation from wafer to wafer within a lot, variation from lot to lot, variation with date of manufacturer).

40.2 Methods and techniques for evaluating defect impact on reliability may include but are not limited to: designed experimentation, failure modes and effects analysis (FMEA), characterization data, analysis of field failures, analysis of unexpected failures at a manufacturer, historically available data such as public literature and proprietary information, existing reliability data, device/ process modeling, etc. It is not necessary to understand the reliability impact of each and every defect or defect combination(s); rather, the repeatable reliability performance of the delivered product must be understood in the context of defects likely to be present in the wafer process line at the time of fabrication.

40.3 Categories of defects must include the following, as a minimum (unless these defects do not occur because of process capability or other fundamental reasons):

DEFECTS:	EXAMPLES/TYPES/CONSIDERATIONS:
- Particles:	Size and composition of particles for affected mask levels and source(s) of variation.
- Conductive Traces:	Size, incidence and impact of imperfections (ie: scratches, voids, cracks, etc.). Shorting potential (ie: extrusions, hillocks, stringers, bridging, etc.). Most vulnerable areas where current carrying density violations may occur.
- Metal Corrosion:	Corrosion or corrosive elements present in metallization.
- Film Delam:	Delamination, poor adherence, excessive stress or coefficient of thermal expansion mismatches.
- Misalign:	Contact, via, poly/diff. alignment. Acceptable versus unacceptable alignment matching.

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- Diffusion Pattern Violation:	Bridging between wells, width reduction (resistors) and enlargement.
- Dielectric Film Faults:	Blown contacts/via's, holes, cracking, active junction line exposure, excessive thickness variations.
- Die Surface Protection Faults:	Cracks, pinholes, scratches, voids, cornerholes, peeling/lifting, blistering, bond pad clearance.
- Diffusion, isolation defects, trenches, guard rings, other techniques:	Voids, notches in pattern diffusion, overlaps of diffusion, contact windows tub-to-tub connections (except by design), etc.

DEFECTS:	EXAMPLES/TYPES/CONSIDERATIONS:
- Film Resistor Flaws:	Scratches, voids, potential bridging, non-adherence, corrosion, alignment, overlap between resistors and conductive traces, step coverage thinning, composition (color) changes.
- Laser Trimmed Film Resistor Flaws:	Kerf width, detritus, current carrying violations (resistor width).
- Foreign Material:	Foreign to process step/ structure (chemical stains, photoresist, ink, stains, liquid droplets).

Note: See appropriate category figures in TM 2010 Conditions A and B

40.3.1 The following metallization concerns need to be addressed by the manufacturer in the process control procedures used to demonstrate metal integrity.

a. Silicon consumption

b. Junction spiking

c. Silicon precipitates (nodules)

d. Copper nucleation

e. Nonplanarity

f. Undercutting

g. Notching

h. Tunneling

i. Cusping

40.4 Defect characterization must identify and quantify non-critical defects, critical defects, and killer defects at each mask level and establish action limits at the appropriate inspection steps. If 100% in-line or end-of-line production screens are used to remove a specific defect, action limits and inspections may not be required at the affected mask level. Characterization must determine the major sources of variations and the impact of defect attributes (ie: size, mass, composition and quantity). Characterization must comprehend the effects of defects on the mask level being characterized and their impact on subsequent mask levels, up to and including the final product. Characterization must encompass defect behavior at worse case allowable processing locations (eg: worse case physical location for critical defect generation), at worse case boundary conditions (ie: thickness, temperature, gas flow, etc.) and to worse case design rules. See Attachment #1: Example of Defect Characterization.

40.5 In accordance with the results of defect characterization, the action limits for defects must be less than the level at which the defects are known to adversely affect the reliability and performance of the device (the use of process "safety margins" must be invoked, eg: if an aluminum line with a 25% notch is known to shorten the life of the device, then margin limits for the notching must be accounted for, that is, the allowable notch limit must be less than 25%). By definition, any observation of a killer defect (one or more) exceeds its action limit.

40.6 The results of the defect characterization shall be used to establish inspection sampling requirements (ie: sample sizes and sampling frequency) and analytical techniques for in-line and end-of-line process inspections (see section 50).

40.7 The manufacturer shall establish a process baseline and put the process under formal change control after defect characterization has been completed and in-line and end-of-line inspection steps are implemented. Any changes that adversely affect the defects require re-characterization of the defects (eg #1: changing fabrication gowns may affect particulate generation and must be determined if they are equivalent or better than gowns used when the original defect characterization was completed, if better no further action, if worse, re-characterization of the line. eg #2: a change in HCl (hydrochloric acid) chemical supplier requires comparative analysis of new supplier to old supplier, relative to trace impurities, followed by an engineering evaluation to validate the impact on product. Discovery of excessive, new impurities that could not be proven benign would require re-characterization before the new supplier could be used).

40.8 Any manufacturers' imposed in-line or end-of-line screens must demonstrate their effectiveness in eliminating killer and critical defects in excess of their allowable action limit(s).

40.9 Any new defects that surface as a result of excursion containment, yield analysis, customer returns, inspection procedures, (etc.) must be characterized in accordance with specifications in section 40.

50. Inspection and test system:

50.1 Control and reduction of defects will result from an inspection and test system, employing process and product monitors and screens. The inspection and test system is incorporated throughout the wafer fab process flow (in-line and/or end-of-line). It is expected that an inspection and test system will prevent killer defects from appearing in the delivered product. See Attachment #2: Example of an Inspection and Test System.

50.2 Inspection and test procedures shall form an integrated approach that in total controls and reduces defects. The procedure shall consider the following criteria where applicable:

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50.2.1 The supplier shall define and implement inspection and test procedures at appropriate points to monitor killer and critical defects (as identified in section 40).

50.2.2 The inspection and test procedures shall consist of sampling plans which recognize the sources of defects and their variance (ie: random, variation from die to die within a wafer, variation from wafer to wafer within a lot, variation from lot to lot, variation with date of manufacturer). Sample plans shall be consistent with statistical practices (distributional form and alpha/beta risks). The population to be sampled must be homogeneous.

Examples of homogeneity considerations include:

Lots that have been split or otherwise altered for rework are not considered homogeneous, unless otherwise demonstrated, and therefore require independent sampling of the non-homogeneous (reworked) population. If different pieces of processing equipment are used at the same process step (mask level), for the same purpose (eg: use of multiple wafer steppers on the same wafer lot), these tools must demonstrate the killer and critical defect characteristics are statistically comparable, for a given wafer lot to be considered a homogeneous population.

50.2.3 Inspections and tests must consider, but are not limited to worst case locations (as identified in Section 40). Examples Include: 1) At an LPCVD operation, the defect characterization might determine particles to be consistently higher on wafers at, or near, the door end of the tube, sampling at LPCVD must comprehend inspection at this location. While characterizing metal bridging, one location on the die might appear consistently more prone to bridging than other die locations, sampling criteria should include inspections at this location.

50.2.4 Inspection and test procedures must make use of "look backs". A look back inspection examines the current process step and one or more preceding process steps. This procedure allows for inspection/test of telescoping effects (magnifies or enhances the defect) and/or defects decorated by subsequent processing. This technique allows for additional opportunities to inspect/test for killer and critical defects in preceding layers.

Examples Include: 1) While inspecting field oxidation it is possible to look back at pattern definitions in previous levels. 2) A defect is known to be more obvious after a subsequent LTO deposition (the defect size telescopes), therefore an inspection at LTO could effectively look back at the previous operation which generate a defect.

50.2.5 Inspection and test procedures must define action limits and the appropriate data to be recorded. Data recording shall recognize the need for wafer, lot, or product disposition and corrective action (eg: data may need to be classified by machine number, tool, wafer lot, operator, etc.). These types of data and action limits are derived from the defect characterization (as identified in section 40) and shall take into account relevant attributes of defects (ie: size, color, mass, composition, density). Action limits shall comprehend safety margins (as specified in section 40).

50.2.6 As a result of defect characterization (see section 40), non-critical defects shall be monitored, unless the non-critical defect has been proven not to have any influence on the finished product, regardless of incidence or defect density. This is required to address situations when:

a. Non-critical defects may mask detection of killer and critical defects (eg: a change in color obscures visual observation of a killer or critical defect).

b. A non-critical defect becomes critical as a result of increased defect density (eg: due to an increase of non-critical defects, a chain is formed, creating a critical defect).

c. An inconsistency between the incidence of non-critical and critical defects, signaling a change in the process that must be explained.

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50.3 Any in-line or end-of-line screens shall be defined, implemented and documented when used in lieu of, or to supplement inspections/tests for killer and critical defects. The population to be screened must also be defined and documented (eg: wafers, die, portions of wafers, wafer lots, etc.). These procedures shall only include those screens proven to be effective, per requirements in section 40. Records of screening results must be maintained (accept/ reject data).

50.4 The Analytical tools and product, process reliability and equipment monitors must have sufficient capability to measure defect attributes as defined in section 40. This includes changes in critical defect density (eg: if defect characterization indicates a 0.1 μm particle is a critical defect at a given mask level, the inspection procedure must be capable of detecting and quantifying the incidence of particles this size and larger). See attachment #3: Analytical tools.

60. Excursion Containment for Material Exceeding Action Limits:

60.1 The manufacturer shall confirm that the action limit has been exceeded. This may be accomplished by: record review, reinspection, increased sampling, higher magnification visual, etc.

60.2 If the condition is confirmed, the manufacturer shall identify and act upon affected material (ie: single wafer, multiple wafers, whole lot, batches of lots, whole line).

60.3 The manufacturer shall perform analysis on affected material and establish a disposition strategy (ie: root cause analysis, scrap, screen, rework, etc.).

60.4 The manufacturer shall implement appropriate short term/long term corrective action (ie: screens, process change, equipment change, design rule change, etc.)

70. Yield analysis:

70.1 The manufacturer shall establish a yield analysis system as a monitor point to confirm effectiveness of inspections and tests. Particular attention should be given to those lots that exhibit abnormal variation from expected yields, as defined by the manufacturer.

70.2 Yield analysis should include root cause analysis to determine and drive process improvements.

70.3 The manufacturer shall coordinate the yield analysis system with a formal material review board (MRB), or other approved disposition authority, to drive corrective action for "excursion" material (killer or critical defect escapes).

80. System for unexpected failure:

80.1 The manufacturer shall establish a system to analyze field returns. Determine root cause of failure and drive action for: identification, containment, disposition, notification and corrective action.

80.2 The manufacturer shall implement a system to capture and contain killer or critical defect escapes originating in wafer fabrication but found elsewhere in the factory (ie: sort, assembly, test, etc.) and implement corrective action.

80.3 The manufacturer shall review unexpected failures through a formal material review board (MRB), or other approved disposition authority, that brings together the expertise to identify and contain the discrepant product (killer or critical defects), to notify internal and external customers, as needed and to implement corrective action. The circumstances for convening an MRB must be defined.

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90. Documentation and data requirements:

90.1 The results of defect characterization, assessment of effectiveness of screening methods, sampling and inspection methodologies, procedures and systems for controlling changes shall be made available to the qualifying activity, upon request.

90.2 Inspection and screening procedures must be placed under formal document and change control. Data records must be maintained and made available to the qualifying activity, upon request. Data retention must be maintained in accordance with the procurement specifications.

90.3 Excursion containment procedures must be documented and placed under document control. When appropriate, records of root cause analysis, containment, disposition and corrective action (via an MRB or other approved disposition authority) must be maintained and made available to the qualifying activity, upon request. Varying degrees of formality are essential to any manufacturer's line; therefore, disposition authority may range from the responsible individual to a formal MRB and documentation may range from initialing a lot traveler to a formal MRB report. The manufacturer shall have prescribed guidelines for the various methods allowable for disposition action and documentation (eg: if product deviation is within certain spec or action limits, the line engineer may have disposition authority; if these limits are exceeded, some higher disposition authority may be required). Records must be retained in accordance with the procurement specifications.

100. Definitions:

(Note: The definitions herein are applicable to this procedure only)

Action limits -Numerical limits for defect densities, counts, or other metrics used to trigger a response. This response may involve: investigation, root cause analysis, disposition and corrective action.

Alignment - Also known as "overlay" or "registration". The proper placement of one photolithography layer atop a preceding layer.

Blown contact - A phenomena most often associated with the wet etching of contacts. The etch proceeds laterally at a rate much greater than is expected or desirable. Typically, the lateral etching is non-uniform with respect to the desired contact profile.

Cornerholes - A process phenomena associated with narrow gaps between lines of topography. In particular, where those lines form an angle of approximately 90 degrees (form a "corner"). A cornerhole is formed when photoresist cannot cover the severe topography generated by structures like these, allowing a subsequent etch to remove film in the gap between the lines.

Critical Defects - Defects known or suspected to cause premature failure but only under certain conditions that have a small probability of occurrence or any defect that cannot be proven as non-critical.

Defect escapes - Lots, wafers or die which contain defects that unintentionally get through a manufacturer's inspection and test system.

DI (DI water) - De-ionized water. Used for wafer cleaning.

Discrepant material - any material determined to be unsuitable for its destined form, fit or function, as specified by the MRB or other disposition authority.

Elements of the process - Any fundamental piece (building block) of the wafer fab process or process step (eg: thermal ramp rates, etch rates, recipe' steps, incoming raw materials, etc.). This includes quantifiable/ measurable chemical and physical phenomena of the wafer fab process.

End-of-line - The steps after wafer fabrication and initial testing (electrical test, wafer sort). This includes most of what is commonly referred to as "assembly/test".

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Excursion containment - Efforts undertaken to find, limit and segregate discrepant material.

* Homogeneous - The state in which every wafer in a lot has received the exact same processing, including: correlated equipment (as specified in appendix A of MIL-PRF-38535), same recipes, same operations and same materials. This does not include metrology or inspection steps.

ILD - Inter-layer dielectric. Typically refers to the layer separating different conductor material layers but is occasionally used to describe the layer between first metal and the underlying layers.

In-line - The process steps that comprise wafer fabrication from initial starting material through and including initial test (electrical test and sort).

Inspection - Any procedure designed to detect or measure defects. Depending on the equipment or procedure, the quantity or types of defects may or may not be measurable; depending on the inspection, defects may or may not be removed. These procedures may utilize visual detection (human or automated), laser surface scatter, in-situ particle detectors, etc.

Interconnects - Any structures on the wafer surface used for electrical connection from one device (or portion of a device) to another. These structures are typically made of polysilicon or metal.

Killer defect - A defect that has a high probability of causing failure, under any condition, at some given point in a products intended life.

Letter of suitability - A formal written document from the qualifying activity stating the manufacturer has sufficient capability and competency to implement/execute the subject procedure.

Look-back inspection - An inspection that is capable of detecting defects not only at the current process layer but also at some number of preceding process layers. Ideally, this inspection allows for differentiation between defects at the current process layer and those of preceding ones.

LPCVD - Low-pressure chemical vapor deposition.

LTO - Low-temperature oxidation or low-temperature oxide.

LYA - Low-yield analysis. A method for determining the reason for yield loss by analyzing low-yielding material.

Mask level - A structure (electrical, physical and/or chemical) on, in, above or below a wafer substrate, achieved or modified by various sequential physical or chemical processes, such as: oxidation, diffusion, etch, film deposition, implant, etc.

Material review board (MRB) - A group of individuals who have sufficient expertise and are duly authorized by the facility to disposition discrepant or non-conforming material.

Monitor - Inspections or tests performed on a sampled population.

Non-critical defect - A defect that has been demonstrated not to cause premature failure, regardless of defect density, defect placement on the die or defect size.

PM - Preventive maintenance procedure.

Poly - Polycrystalline silicon.

Process baseline - An approved set of instructions, conditions and procedures for wafer fabrication.

Product - Material resulting from the output of a wafer fab process that is ultimately destined for delivery to a customer.

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Screens - 100% of a population (dice or wafers) is inspected or tested and all material containing targeted defects are rejected.

Sub-process - Any number of related process steps leading to an outcome on the wafer. Examples would include poly interconnect formation (comprised of poly deposition, poly layer lithography, poly etch and resist strip) and contact formation (dielectric deposition, contact layer lithography, contact etch and resist strip).

Telescoping defects - Defects which increase in visibility, due to an apparent increase in size, as wafers are processed through subsequent operations. The increase is a function of the defect being decorated by etches or films, the defect acting as a nucleation site for subsequent depositions or by the defect creating non-uniform regions in a film or oxide.

Test - 1) Evaluate (ie: stress and measure) reliability, quality and performance; 2) ensure the defects present do not affect reliability, quality or performance.

Unexpected failures - Failures that are not detected, or cannot be predicted, using the manufacturer's standard in-line inspection and containment plans.

Wafer process - The materials, equipment, operations and environment necessary to manufacture a product or family of products. This includes all potential sources of defect generation.

Yield analysis - The analysis of die yields to determine failure modes and defect mechanisms. This can entail analyzing low yielding material, average yielding material or high yielding material or combinations of these items. This type of analysis can be used to validate in-line monitors.

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ATTACHMENT 1

Example 1 - Quality Scenario:

A defect characterization has been performed on an LPCVD operation. The primary defect mechanism was found to be particles. These particles were quantified using a laser surface-scanning tool. The results show that the particles fell into three size distributions: 1) <0.3 microns randomly distributed from wafer to wafer and within a wafer, 2) about 1.0 microns with a higher density near the pump end of the deposition tube, and 3) greater than 6.0 microns that appeared heavily on some wafers but did not appear at all on others. The defects in the 1.0 micron or less categories were found to be relatively small, dark particles when viewed with an optical microscope. The larger particles (>6 microns) appeared as large, black particles that appeared to be on the wafer surface. A compositional analysis of particles from the three distributions showed that the first two types (<0.3 microns and about 1.0 microns) were composed of Si and O, essentially the same composition as the deposited film. The large particles were composed of primarily Fe and Ni.

Wafers containing defects from the smaller size distributions were processed through the subsequent patterning operations. The 1.0 micron particles were observed to have an affect on the subsequent pattern when they occurred adjacent to the patterned lines. The <0.3 micron particles had no observable effect. Both defects were characterized using optical microscopes and an automated pattern inspection system. After resist strip, the 1.0 micron particles were gone, with only their effects on the patterning operation being visible. The <0.3 micron defects were still observable after resist strip. After a subsequent LTO deposition, the <0.3 micron particles appeared to "telescope" in size to about 1 micron due to the conformal nature of the LTO film. The "telescoped" particles had a noticeable effect on the next patterning operation. Observation of both particle types using an SEM (scanning electron microscope) showed that the 1.0 micron particles appeared to be incorporated into the film, whereas the <0.3 micron particles appeared to be under the film. This was consistent with the defect behavior observed during subsequent processing.

The signal from the large particles suggested contamination from a stainless steel source. Observation of the defect with an SEM showed that the defects were on top of the deposited film. The defects were found to be coming from the unload arm of the LPCVD system. The unload arm was occasionally striking another piece of the load/unload assembly, generating metal particles each time it did this.

The characterization of particle defects from this LPCVD operation resulted in the following monitoring plan: 1) The alignment of the unload arm was found to be most affected by the preventive maintenance procedure performed on the load/unload assembly once each week. As a result, a bare silicon particle monitor is run after each PM, before any product wafers can be run on the system. The monitor is set to look for 6 micron and larger particles with the expectation that no such particles should be present if the unloader is working properly. 2) The source of the 1.0 micron particles is unknown. What is known is that these defects are always worse near the pump-end of the tube. As a result, the monitor for this particle source is run at the pump end of the tube, with a door end monitor run simultaneously as a "control". Different action limits exist for each monitor. 3) The small particles were found to be very difficult to monitor at the LPCVD operation since they fell into the "noise" caused by limitations in the particle detection equipment. However, they are easily monitored in a "look-back" fashion after the subsequent patterning operation using the automated pattern inspection system. As a result, this defect is monitored at the post-patterning inspection step with action limits initiating feedback to the LPCVD operation.

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Example 2 - Reliability Scenario:

Characterization of particles at a gate oxide preclean operation showed that the particles contributed by the operation tend to be small (0.2 microns) and vary in concentration from 0.02 d/cm^2 to 0.8 d/cm^2 depending on how heavily the station is utilized. Defect density increased as the number of wafers processed through the station increased.

Wafers from this operation were selected such that some of them had low defect densities (approximately 0.3 d/cm^2) and the remainder had high defect densities (approximately 0.8 d/cm^2). These wafers were processed through the line and the die from these wafers subjected to high voltage stress testing. The results of the tests were that the low and moderate defect density groups showed levels of gate leakage consistent with the historical process baseline. The high defect density die show gate leakage that was 3 times that of the historical baseline and resulted in barely acceptable failure rates.

As a result of this characterization, a particle monitor was implemented at gate oxide preclean with an upper limit of 0.6 d/cm^2 to allow some safety margin from the gate leakage problems seen at 0.8 d/cm^2. However, due to resource limitations, this monitor can only be run once every shift (approximately every 12 hours). It is likely that the movement of material in the line will lead to the station occasionally exceeding its control limits between monitors. A second preclean station is scheduled to be installed in about three months. This station will provide enough capacity to prevent wafer-volume related out-of-control particle conditions at the gate preclean operation. In order to ensure that no material with bad gate oxide is shipped during the interim period (before the new station comes on-line), a manufacturer imposed screen (high-voltage stress test) is used on all material processed between a failing monitor and the last known good monitor at this operation.

In order to show that the screen is effective, particle monitors are processed through the station with every lot of wafers. This test is done for a period of time sufficient to yield multiple lots at various defect densities. Die from each of these lots are processed through the high-voltage screen. The results show that the screen is 100 percent effective at detecting the lots with defect densities greater that 0.6 d/cm^2. The results show a solid correlation between gate oxide preclean defect densities and gate oxide leakage levels. The screen is then used to augment station particle level data and remains in place until the second station is installed and qualified.

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ATTACHMENT 2

EXAMPLE OF DEFECT DETECTION FOR KEY PROCESS STEPS:

PROCESS STEP MONITOR	PRODUCT MONITOR	EQUIPMENT MONITOR	RELIABILITY
Wafer start	Incoming Si QA	NA	NA
EPI	Laser surface particle scan.	Gas flow/pressure, chamber temp	NA
Start Oxide	Oxide thickness, laser surface particle scan.	Tube temp profile, CV, thermocouple cal, gas flows, tube particle checks using laser surface scan.	Oxide integrity test wafers
Patterning/Well Implant	UV light particle insp, optical pattern insp, e-test parametrics.	Exposure dose, reticle/ pellicle inspection, stepper stage checks implant dose processor and voltage calibration, DI water resistivity. Particle checks of stepper, implanter, coat/develop tracks using laser surface particle scan.	LYA
Active Region Patterning/Gate Oxide (no 2010 equiv.)	Alignment check, optical inspection, automated pattern inspection, UV light and laser surface particle inspections, in-line SEM CD measurement, e-test parametrics.	Exposure dose, reticle/ pellicle inspections, stepper stage checks, tube temp profile, CV thermo-couple cal, gas flows, DI water resistivity. Particle checks of stepper, diffusion tube, coat/develop tracks using laser surface particle scan.	Oxide integrity test wafers, comb/serpentine test structures, LYA.
Poly Dep/Patterning	Alignment check, optical and automated pattern inspection, laser surface particle inspections, in-line SEM CD measurement, e-test parametrics.	Dep tube pump/vent speed, MFC calibration, gas flows, pressures, temperature. Expose dose, reticle/pellicle checks, stepper stage checks. DI water resistivity. Particle checks on poly tube, stepper and coat/develop tracks using laser surface particle scan.	Comb/serpentine test structures, buried contact check, LYA.

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Patterning/ S/D Implant	Alignment check, optical pattern inspection, UV light or laser surface particle inspections. E-test parametrics.	Exposure dose, reticle/ pellicle inspection, stepper stage checks. implant dose processor and voltage calibration, DI water resistivity. Particle checks of stepper, implanter, coat/develop tracks using laser surface particle scan.	LYA.
ILD 1/Patterning	Alignment check, automated pattern inspection, UV light and laser surface particle inspection, e-test parametrics. In-line SEM CD measure.	Exposure dose, reticle/ pellicle inspection, stepper stage checks. ILD deposition system temp/pressure. MFC calibration, gas flows. DI water resistivity. Particle checks on stepper, coat/develop tracks and ILD deposition system.	Refractive index. % phosphorus. Film integrity tests (breakdown, etc.). LYA.
Metal 1/Patterning	Alignment check, automated pattern inspection, laser surface particle inspection, metal resistivity/specularity, In-line SEM CD measurement and electrical CD measure, e-test parametrics.	Expose dose, reticle/ pellicle inspection, stepper stage checks. Metal dep thickness, RGA of dep system, gas flows, pressures, pump/vent rate checks, metal resistivity/ specularity. Particle checks on metal dep system, stepper and coat/develop tracks using laser surface scan.	Contact chains, Metal-to-poly contact, Metal-to-diff contacts, electromigration monitors, metal CDs (at end of line), step coverage. LYA.
ILD 2/Patterning.	Similar to ILD1.	Similar to ILD1.	Similar to ILD1.
Metal 2/Patterning	Similar to Metal 1	Similar to Metal 1	Similar to Metal 1 with addition of Via chains, Metal 2-to-Metal 1 contact.
Glassivation/ Bond pads	Coarse alignment check, optical inspection of bond pads to ensure clearing and of passivation for cornerholes.	Glassivation thickness, phos content, temp, pressure and flows. Exposure dose, stepper stage parameters. Particle checks on all equip.	Acid bath for glass integrity. Acoustic microscopy.
Backside prep/ Chrome/Gold Dep/ E-test/Sort	Post-tape visual, post-grind visual, post-detape visual (all optical). Warpage check, thickness check. Chrome/gold thickness checks, visual for backside appearance post-dep. Post-sort visual (optical).	Grind rate check, grind pressure check. Evaporator pressure/leak rate checks, RGA, power and gas flows. Warpage and thickness checks on test wafers.	Warpage and thickness checks. Die cracking and adhesion monitors at assembly.

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ATTACHMENT 3

ANALYTICAL TOOLS/MONITORS AND SCREENS

Analytical tools may include, but are not limited to the following:

a. Oblique light, very low magnification

b. Optical microscope

c. Laser scattering (or equivalent)

d. Automated pattern inspection

e. Alignment measurement tool (automated, high-resolution)

f. Non-destructive S.E.M.

g. Wafer mapping

Broad Use of Tools for Inspections (tools may include but are not limited to):

Oblique Light, visual inspection: A quick and gross visual inspection at very low mag (1X to 20X) using a light source projected onto the wafer and tilting the wafer to detect large particles. This is an inspection step used in-line at various key process steps.

Optical microscope: Looks for defects that are detectable optically (eg: metal stringers, large particles, visible foreign material, visible resist imperfections such as drips, visible voids and cracks, visible misalignment, etc.). This tool is used at different magnifications, at beginning and/or end of key process steps (200X optical sampling in-line for a selected key process step and 800X optical check at the end of a key process step and before proceeding to the next key process step).

Laser scanning (or equivalent): Used to detect any anomalous surface defects (eg: very fine particles that may not be detected by optical microscopy). May be used in numerous process steps and is particularly important early in the process to control telescoping defects.

Automated Pattern recognition: Used to verify integrity of two dimensional geometries (detects anomalies such as: voids and cracks in the metal, metal bridging, diffusion and poly faults or any other abnormalities in an expected pattern).

Automated high resolution alignment measurement tool: Used for inter-level registration at very fine tolerances (on the order of 0.1 μm). This tool is used to align very fine critical geometries undetectable by conventional high power optical registration tools.

Non-destructive S.E.M.: In-line product monitor used for very high power visual examination of critical process steps (critical dimension, step coverage, metal thinning, etc.).

wafer mapping: An analytical technique using data from various inspection tools (eg: automated pattern recognition tools, laser scanning tools, e-test results) for defect characterization and partitioning.

Product, Process and Reliability Monitors/Screens

These monitors/screens incorporate inspections/tests which may include but are not limited to):

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In-line electrical test (E-test): This monitor is used to measure electrical characteristics of transistor elements (sheet resistance, doping levels and other transistor parametrics), contact chains, metallization structures (line width, thickness, resistance) and via structures. Parametric failures detectable by e-test may be indicative of an unacceptable incidence of killer or critical defects.

Test structures: Special structures used to detect killer or critical defects (eg: serpentine structures used to detect metal continuity such as voids, comb structures for bridge detection and to verify field oxide isolation integrity, electromigration structures to verify metal integrity and step coverage and inter-layer dielectric structures to verify e-field integrity).

Periodic reliability studies: Intended to verify design life margins of the technology.

Yield Analysis: Used to validate effectiveness of in-line monitors by a closed loop feedback system that detects the effects of killer or critical defect escapes not caught in-line. Actions may include: scrapping lot, root cause analysis and correction, lot screening, etc. (see section 70).

Other monitors: Used to measure key process elements. Examples may include but are not limited to:

a. Metal reflectivity and resistivity (to check metal irregularities such as: hillocks formations, step thinning, changes in granularity, voiding, etc.).

b. Ionic contamination.

c. Refractive index for interlayer dielectric thickness measurements.

d. Post wafer probe visual inspection. A monitor performed on randomly selected post probe wafer(s) beginning with visual high power inspection and may be followed by subsequent detailed analysis (S.E.M., EDX, layer strip-back, etc.). This is used to confirm the effectiveness of in-line monitors.

e. Acid bath (used for quick detection/ decoration of glassivation defects, cracks and holes) or acoustic microscopy (to measure glassivation integrity).

Equipment Monitors (equipment monitors may include but are not limited to):

Particle checks: Performed on process equipment such as: etch, metal deposition, implant, diffusion, dielectric deposition, photoresist material and application. Particles of sufficient size and density may lead to killer or critical defects (metal bites, dielectric holes, poly/ diffusion geometry changes, etc.).

Residual Gas Analysis: Used to monitor gas integrity of key process equipment (eg: metal deposition equipment to control corrosion).

Photolithography exposure equipment: Used to verify critical parameters and controls for photolithography operation (pre-alignment checks, stage accuracy, machine alignment accuracy using reference patterns, lens distortion check, alignment accuracy, wafer chuck flatness measurement, lens focus check, reticle rotation, etc.)

METHOD 5005.13

QUALIFICATION AND QUALITY CONFORMANCE PROCEDURES

* 1. PURPOSE. This method establishes qualification and quality conformance inspection procedures for microelectronics to assure that the device and lot quality conforms with the requirements of the applicable acquisition document. The full requirements of groups A, B, C, D, and E tests and inspections are intended for use in initial device qualification, requalification in the event of product or process change, and periodic testing for retention of qualification. Groups A and B tests and inspections are required for quality conformance inspection on individual inspection lots as a condition for acceptance for delivery. Groups C and D tests are required for quality conformance inspection on a periodic basis as a condition for acceptance for delivery. Group E tests are qualification and quality conformance procedures to be utilized only for radiation hardness assurance levels as specified in table V. In general, it is intended that the device class level to which qualification or quality conformance inspection is conducted would be the same device class level to which screening procedures (in accordance with method 5004) are conducted. However, it is permissible for qualification or quality conformance procedures to be specified at a higher quality level (in no case shall a lower level be permitted) to reduce the potential percent-defective. It is also permissible to specify tightened inspection criteria for individual subgroups where experience indicates justifiable concern for specific quality problems.

* NOTE: Reference to method 5005 on a stand alone basis (not indicating compliance or noncompliance to 883) requires full compliance to 1.2.1 of this standard (see 1.2.2 of this standard).

2. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with the requirements of the applicable acquisition document and other apparatus as required in the referenced test methods.

* 3. PROCEDURE. The procedure contained in 3.1, 3.2, or 3.3, as applicable to the microcircuit type and class, shall apply for all qualifications and quality conformance inspection requirements. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests. Where end-point electrical measurements are required for subgroups in groups B, C, D, and E testing, they shall be as specified in the applicable device specification or drawing. Where end-point measurements are required but no parameters have been identified in the acquisition document for that purpose, the final electrical parameters specified for 100 percent screening shall be used as end-point measurements. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be treated in accordance with the optional provisions below, where applicable.

* Constant acceleration. Delete test condition E and replace with test condition as specified in the applicable device specification or drawing. Unless otherwise specified, the stress level for large monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

* Qualification and quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal classes level S and level B requirements. Those requirements for each of the specified radiation levels (M, D, L, R, F, G and H) are detailed in table V.

* Qualified manufacturers list (QML) manufacturers' who are certified and qualified to MIL-PRF-38535 or who have been grated transitional certification to MIL-PRF-38535 may modify the class level B tables (tables I, IIb, III, and IV) as specified in the applicable device specification or Standard Microcircuit Drawing and as permitted in 1.2 of MIL-STD-883 provided the modification is contained in the manufacturer's Quality Management (QM) plan and the "Q" or "QML" certification mark is marked on the devices. For contractor prepared drawings with specific references to individual test methods of MIL-STD-883 (e.g., method 1010, method 2002, etc.), these test methods may not be modified by a QML manufacturer without the knowledge and approval of the acquiring activity.

* 3.1 Qualification procedure for class level S microcircuits.

* 3.1.1 Qualification for class level S QML-38535 listing. Qualification testing for class level S microcircuits shall be in accordance with appendix A of MIL-PRF-38535.

* 3.1.2 Steady-state life test. In the case of multiple sublots contained in the class level S inspection lot, the sample size number shall be selected from the sublots in the nearest whole number of devices proportionately to the number of devices in each sublot. Where this results in less than 10 samples from any sublot, additional samples shall be selected from that sublot(s) to provide a minimum of 10 samples from each sublot. Any sublot which exhibits more than one failure shall be rejected from the inspection lot.

* 3.2 Quality conformance inspection procedures for class level S microcircuits. Each class level S quality conformance inspection lot shall be assembled in accordance with the class level S requirements of appendix A of MIL-PRF-38535. Quality conformance testing shall be in accordance with tables I, IIa, and IV.

3.2.1 Notification of nonconformance. Whenever any of the following occurs, the qualifying activity shall be immediately notified:

a. The number of failures in a single subgroup of table IIa exceeds the acceptance number on two successive lots (applicable to subgroups 2b, 2c, 2d, 5, and 6).

* b. The number of failures for the resubmitted sample in accordance with 40.3.3.1 of appendix A of MIL-PRF-38535 exceeds the acceptance number on two successive lots on the following subgroups: 1, 2a, 2b, 2d, and 4.

c. For a given device type withdrawal from quality conformance testing for any reason on two successive lots.

d. Following initial notification, the manufacturer shall provide the qualifying agency or its designated representative with data which indicates the reason(s) for the reported nonconformance, contributing factors, and proposed corrective action.

e. Two successive lots failing group E testing, or 10 percent or more of the lots requiring the add-on sampling procedure.

* In the absence of timely compliance with the above, or corrective action acceptable to the qualifying activity, action may be taken to remove the product from the class level S QML-38535.

* 3.3 Qualification and quality conformance inspection procedures for class level B microcircuits. Qualification or quality conformance inspection for microcircuits shall be conducted as described in the groups A, B, C, D, and E tests of tables I, II, III, IV, and V herein and as specified in the applicable device specification. For quality conformance inspection, each inspection lot (sublot) shall pass groups A, B and (when applicable) E test (or be accepted in accordance with 3.5 herein), and the periodic group C and D tests shall be in accordance with appendix A of MIL-PRF-38535.

* 3.4 Acceptance procedure. Acceptance numbers, provisions for resubmission, and criteria for acceptance or rejection of lots shall be as specified herein and in the applicable device specification or drawing.

* 3.5 Sample selection. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix A of MIL-PRF-38535 (and in accordance with table V herein for group E) after the specified screen requirements of method 5004 have been satisfactorily completed. Where use of electrical rejects is permitted, unless otherwise specified, they need not have been subjected to the temperature/ time exposure of burn-in.

3.5.1 Alternate group A testing. Alternate procedures for performing group A inspection on each inspection lot or sublot may be used at the manufacturer's option provided that the qualifying activity has previously approved the alternate procedure and flow being used by the manufacturer. A different operator shall check the entire test setup and verify the use of the correct test program prior to testing the group A sample.

3.5.1.1 Inspection lot sample selection. When this option is used, test samples for each individual group A subgroup shall be randomly selected from the inspection lot after 100 percent screening of that subgroup (or subgroups, in the event that multiple subgroups are tested at the same temperature in sequence with the same test program). All devices in the inspection lot or sublot shall be available for selection as a test sample and a fully random sample shall be selected from the total population of devices.

3.5.1.2 Concurrent sample selection. When this option is used, test samples from each individual group A subgroup(s) shall be randomly selected concurrent with the 100 percent screening of that subgroup(s) and tested subsequent to screening each individual device of that subgroup(s). When this option is used, the following requirements apply:

a. A documented verification methodology and operating procedure shall be set up to assure the integrity of the total test system, that the product is being tested with correct test conditions and that all required screening and group A testing is being performed.

b. The group A samples shall be sorted out separately from the balance of the lot and the sample size verified. If because of higher than expected yield loss, the number of samples tested are less than the required sample size, (116 units), then additional samples shall be randomly selected and tested.

c. Each group A reject shall be sorted out separately.

d. All screening rejects shall be segregated from the acceptable product and the physical count verified against the test system attribute data.

e. When sorting (e.g., speed or power) is completed during the final electrical screening, each individual device type screened shall have a full group A sample selected and tested.

f. For small lots, where the lot size is less than the required sample size (116 units) each device in the lot shall be double tested (i.e., 100 percent screening and 100 percent group A).

TABLE I. Group A electrical tests for classes level S and level B devices. 1/

Subgroups 2/ Quality/accept no. = 116/0 3/ 4/ 5/
Subgroup 1
Static tests at 25°C
Subgroup 2
Static tests at maximum rated operating temperature
Subgroup 3
Static tests at minimum rated operating temperature
Subgroup 4
Dynamic tests at 25°C
Subgroup 5
Dynamic tests at maximum rated operating temperature
Subgroup 6
Dynamic tests at minimum rated operating temperature
Subgroup 7
Functional tests at 25°C
Subgroup 8A
Functional tests at maximum rated operating temperatures
Subgroup 8B
Functional tests at minimum rated operating temperatures
Subgroup 9
Switching tests at 25°C
Subgroup 10
Switching tests at maximum rated operating temperature
Subgroup 11
Switching tests at minimum rated operating temperature

See footnotes at top of next page.

TABLE I. Group A electrical tests for classes level S and level B devices - Continued. 1/

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table I), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in 2/, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE IIa. Group B tests for class level S devices. 1/

Test	MIL-STD-883		Quantity (accept no.) Sample size no. accept no.
	Method	Condition	
Subgroup 1			
a. Physical dimensions 2/	2016	5,000 ppm maximum water content at 100°C	2(0)
b. Internal water-vapor content 2/ 3/	1018		3(0) or 5(1) 4/
Subgroup 2 5/			
a. Resistance to solvents	2015		3(0)
b. Internal visual and mechanical	2013, 2014	Failure criteria from design and construction requirements of applicable acquisition document	2(0)
c. Bond strength	2011		Sample size 6/ number = 22, c = 0
(1) Thermocompression		1. Test condition C or D	
(2) Ultrasonic		2. Test condition C or D	
(3) Flip-chip		3. Test condition F	
(4) Beam lead		4. Test condition H	
d. Die shear or substrate attach strength test		In accordance with method 2019 or 2027 for the applicable die size	3(0)
Subgroup 3			
Solderability 7/	2003	Soldering temperature of 245°C ±5°C	Sample size number = 22, c = 0
Subgroup 4 2/			
a. Lead integrity 8/	2004	Test condition B2, lead fatigue	Sample size number = 45, c = 0
b. Seal	1014	As applicable	
(a) Fine			
(b) Gross			
c. Lid torque 9/	2024	As applicable	
Subgroup 5 10/			
a. End-point electrical parameters 11/		As specified in the applicable device specification	Sample size number = 45, c = 0
b. Steady state life 12/	1005	Test condition C, D, or E	
c. End-point electrical parameter 11/		As specified in the applicable device specification	

See footnotes at end of table.

TABLE IIa. Group B tests for class level S devices - Continued. 1/

Test	MIL-STD-883		Quantity (accept no.) Sample size no. Accept number
	Method	Condition	
Subgroup 6			Sample size Number = 15, c = 0
a. End-point electrical parameters		As specified in the applicable device specification	
b. Temperature cycling	1010	Condition C, 100 cycles minimum	
c. Constant acceleration	2001	Test condition E: Y_1 orientation only	
d. Seal (a) Fine (b) Gross	1014	As specified in the applicable device specification	
e. End-point electrical parameters			
Subgroup 7 13/			

1/ Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in.

2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.

3/ This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See 6/ of table IV.

4/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

5/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

6/ Unless otherwise specified, the sample size number for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).

7/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

8/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 9/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need be performed only on packages having leads exiting through a glass seal.

9/ Lid torque test shall apply only to glass-frit-sealed packages.

10/ The alternate removal-of-bias provisions of 3.3.1 of method 1005 shall not apply for test temperature above 125°C.

11/ Read and record group A subgroups 1, 2, and 3.

12/ The same test temperature that was used for burn-in shall be used for the steady-state life test.

* 13/ Subgroup 7 has been deleted from table IIa. The requirements for ESD testing are specified in appendix A of MIL-PRF-38535.

TABLE IIb. Group B tests for level class B. 1/ 2/

Test	MIL-STD-883		Quantity/(accept no.) or sample size number, accept number
	Method	Condition	
Subgroup 2 3/ a. Resistance to solvents	2015		3(0)
Subgroup 3 a. Solderability 4/	2003	Soldering temperature of 245°C ±5°C	Sample size number = 22, c = 0
Subgroup 5 a. Bond strength 5/ (1) Thermocompression (2) Ultrasonic or wedge (3) Flip-chip (4) Beam lead	2011	(1) Test condition C or D (2) Test condition C or D (3) Test condition F (4) Test condition H	Sample size number = 15, c = 0

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in.

2/ Subgroups 1, 4, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.

3/ Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.

4/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

5/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

TABLE III. Group C (die-related tests) (for class level B only).

Test	MIL-STD-883		Quantity/(accept no.) or sample size number accept number
	Method	Condition	
Subgroup 1			
a. Steady-state life test	1005	Test condition to be specified (1,000 hours at 125°C or equivalent in accordance with table I)	Sample size number = 45, C = 0
b. End-point electrical parameters		As specified in the applicable device specification	

TABLE IV. Group D (package related tests) (for class levels B and S).

Test 1/	MIL-STD-883		Quantity/(accept no.) or sample size number accept number
	Method	Condition	
Subgroup 1 2/			
a. Physical dimensions	2016		Sample size number = 15, C = 0
Subgroup 2 2/			
a. Lead integrity 3/	2004	Test condition B_2 (lead fatigue)	Sample size number = 45, C = 0
b. Seal 4/			
(1) Fine	1014	As applicable	
(2) Gross			
Subgroup 3 5/			
a. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum.	Sample size number = 15, C = 0
b. Temperature cycling	1010	Test condition C, 100 cycles minimum.	
c. Moisture resistance 6/	1004		
d. Visual examination		In accordance with visual criteria of method 1004 and 1010	
e. Seal	1014	As applicable	
(1) Fine			
(2) Gross 7/			
f. End-point electrical parameters 8/		As specified in the applicable device specification	

See footnotes at end of table.

TABLE IV. Group D (package related tests) (for class levels B and S) - Continued.

Test 1/	MIL-STD-883		Quantity/(accept no.) or sample size number accept number
	Method	Condition	
Subgroup 4 5/			
a. Mechanical shock	2002	Test condition B minimum	Sample size number = 15, C = 0
b. Vibration, variable frequency	2007	Test condition A minimum	
c. Constant acceleration	2001	Test condition E minimum (see 3), Y_1 orientation only	
d. Seal	1014	As applicable	
(1) Fine			
(2) Gross			
e. Visual examination	9/		
f. End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5 2/			
a. Salt atmosphere 6/	1009	Test condition A minimum in accordance with visual criteria of method 1009	Sample size number = 15, C = 0
b. Visual examination			
c. Seal	1014	as applicable	
(1) Fine 7/			
(2) Gross			
Subgroup 6 2/			
a. Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1) 10/
Subgroup 7 2/			
a. Adhesion of lead finish 11/ 12/	2025		Sample size number = 15, C = 0
Subgroup 8 2/ 13/			
a. Lid torque	2024		5(0)

1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

2/ Electrical reject devices from that same inspection lot may be used for samples.

TABLE IV. Group D (package related tests) (for class levels B and S) - Continued.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use method 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

6/ Lead bend stress initial conditioning is not required for leadless chip carrier packages. For fine pitch packages (≤ 25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

7/ After completion of the required visual examinations and prior to submittal to method 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

8/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

9/ Visual examination shall be in accordance with method 1010 or 1011.

10/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot.

11/ The adhesion of lead finish test shall not apply for leadless chip carrier packages.

12/ Sample size number based on number of leads.

13/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

* TABLE V. Group E (radiation hardness assurance tests). 1/

Test	MIL-STD-883		Class level S		Class level B	
	Method	Condition	Quantity/ accept number	Notes	Quantity/ accept number	Notes
Subgroup 1 2/						
Neutron irradiation	1017	25°C				
a. Qualification			(a) 11(0)	3/	(a) 11(0)	4/
b. QCI			(b) 11(0)	3/	(b) 11(0)	4/
Endpoint electrical parameters		As specified in accordance with device specification				
Subgroup 2 5/						
Steady-state total dose irradiation	1019	25°C Maximum supply voltage				
a. Qualification			(a) 4(0) 2(0)	(a) 6/ 8/	(a) 22(0)	7/
b. QCI			(b) 4(0) 2(0)	(b) 6/ 8/	(b) 22(0)	7/
Endpoint electrical parameters		As specified in accordance with device specification				
Subgroup 3 9/						
Transient ionizing irradiation	1021 1023	25°C 25°C	11(0)	3/	11(0)	4/
Endpoint electrical parameters		As specified in accordance with device specification				

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening (see 3.5.3).

* 2/ Waive neutron tests for MOS IC devices where neutron susceptibility is less than 10^{13} neutrons/cm^2 (e.g., charge coupled devices, BICMOS, etc.). Unless otherwise specified, the limit for neutron fluence shall be 2×10^{12} neutrons/cm^2.

3/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

4/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

* 5/ Class level B devices shall be inspected using either the class level B quantity/accept number criteria as specified, or by using the class level S criteria on each wafer.

* 6/ In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures.

TABLE V. Group E (radiation hardness assurance tests) - Continued. 1/

7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

* 8/ In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures.

9/ Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup.

* 3.5.2 Alternate group B inspection for class level B. At the manufacturer's option, (class level B only), group B inspection shall be performed on any inspection lot of each qualified package type and lead finish from each different week of sealing. Different inspection lots may be used for each subgroup. After this alternate group B inspection is successfully completed, all other device types manufactured on the same assembly line using the same package type and lead finish sealed in the same week may be accepted without further group B testing. A manufacturer shall not accept inspection lots containing devices of a particular package type and lead finish until after the successful completion of group B testing for that package type and lead finish for each week of seal.

3.5.2.1 Nonconformance for the alternate group B inspection. When a failure has occurred in group B using the alternate group B procedure, samples from three additional inspection lots of the same package type, lead finish, and week of seal as the failed package shall be tested to the failed subgroup(s). If all three inspection lots pass, then all devices manufactured on the same assembly line using the same package type and lead finish and sealed in the same week may be accepted for group B inspection. If one or more of the three additional inspection lot fail, then no inspection lot containing devices manufactured on the same assembly line using the same package type and lead finish sealed in the same week shall be accepted for group B inspection until each inspection lot has been subjected to and passed the failed subgroup(s).

* 3.5.3 Group E samples. At the manufacturer's option (but subject to the criteria defined by 3.5.3.1, 3.5.3.2, and 3.5.3.3), group E samples need not be subjected to all the screening tests of method 5004, but shall be assembled in a group D qualified package and, as a minimum, pass group A, subgroups 1 and 7, electrical tests at 25°C prior to irradiation.

* 3.5.3.1 Group E tests shall be performed on samples that have been exposed to burn-in or

* 3.5.3.2 as an alternative, the requirement of 3.5.3.1 can be waived if previous testing has shown that burn-in produces negligible changes in the device total dose response or

* 3.5.3.3 as an alternative, the Group E tests can be performed on samples which have not received burn-in if the results of the Group E tests are corrected for the changes in total dose response which would have been caused by burn-in. This correction shall be carried out in a manner acceptable to the parties to the test.

3.6 Disposition of samples. Disposition of sample devices used in groups A, B, C, D, and E testing shall be in accordance with the applicable device specification.

3.7 Substitution of test methods and sequence.

* 3.7.1 Accelerated qualification or quality conformance testing for class level B. When the accelerated temperature/time test conditions of condition F of method 1005 are used for any operating life or steady state reverse bias subgroups on a given sample for purposes of qualification or quality conformance inspection, the accelerated temperature/time test conditions shall be used for all of those named subgroups. When these accelerated test conditions are used for burn-in screening test (test condition F of method 1015) or stabilization bake (any test temperature above the specified maximum rated junction temperature for devices with aluminum/ gold metallurgical systems) for any inspection lot, it shall be mandatory that they also be used for the operating life, and steady-state reverse bias tests of method 5005, as applicable, or qualification or quality conformance inspection. Qualification and quality conformance inspection may be performed using accelerated conditions on inspection lots that have been screened using normal test conditions.

3.8 Data reporting. When required by the applicable acquisition document, the following data shall be made available for each lot submitted for qualification or quality conformance inspection:

a. Results of each subgroup test conducted, initial, and any resubmission.

b. Number of devices rejected.

c. Failure mode of each rejected device and, for class S, the associated mechanism for catastrophic failures of each rejected device.

d. Number of additional samples added, when applicable.

e. Resubmitted lots, identification and history.

f. Read and record variables data on all specified electrical parameter measurements in group B.

4. SUMMARY. The following details shall be specified in the applicable device specification:

a. Device class and procedure paragraph if other than 3.

b. Sequence of test, sample size, test method, and test condition where not specified, or if other than specified.

c. Test condition, cycles, temperatures, axis, etc., where not specified, or if other than specified (see 3).

d. Acceptance procedure (see 3.3) and quantity (accept number) or sample size number and acceptance number, if other than specified (see 3).

e. Electrical parameters for group A.

f. Electrical parameters for groups B, C, D, and E end point measurements, where applicable.

g. Requirements for failure analysis (see 3.8).

h. Requirements for data recording and reporting if other than specified in 3.8.

i. Restriction on resubmission of failed lots (see 3.4), where applicable.

j. Steady-state life test circuits, where not specified or if other than specified (see subgroup 1 of table III and subgroup 5 of table IIa).

k. Parameters on which delta measurements are required.

METHOD 5006

LIMIT TESTING

1. PURPOSE. This method provides means for establishing or evaluating the maximum capabilities of microelectronic devices, including such capabilities as absolute maximum ratings (from which safe design limits may be derived), maximum stresses which may be applied in screening or testing without causing degradation, and sensitivity to particular screening or testing without causing degradation, and sensitivity to particular screening or testing stresses and the associated modes or mechanisms of failure. Since this is a relatively expensive and time consuming procedure, it is not intended for general application to all device acquisitions. It should however be extremely useful in evaluating the capabilities of new device types or devices which have experienced significant modifications in design, materials or processes which might be expected to alter their stress tolerance or primary modes and mechanisms of failure. It should also be useful in providing information vital to quality and reliability assurance in high reliability programs or in acquisition extending over significant periods of time where test results can be used to provide corrective action in device design, processing or testing.

1.1 Destructive testing. All limit testing accomplished in accordance with this method is considered destructive and devices shall be removed from their respective lot.

1.2 Parameter measurements. Electrical measurement shall be performed to remove defective devices after each stress step unless otherwise specified herein or in the applicable acquisition document. These measurements need not include all device parameters, but shall include sufficient measurements to detect all electrically defective devices. When delta parameter measurements are required they shall be specified in the applicable acquisition document.

2. APPARATUS. The apparatus for this test shall include equipment specified in the referenced test methods as applicable and electrical measurement equipment necessary to determine device performance.

3. PROCEDURE. Limit testing shall be conducted in accordance with the procedure contained in 3.1 and 3.2 using samples sizes as designated in table I.

TABLE I. Sample sizes for limit testing.

Limit test	Sample size
Thermal evaluation	5
Extended thermal shock	10
Step-stress mechanical shock	10
Step-stress constant acceleration	10
Step-stress operational life	10
Constant high stress operational life	10
Step-stress storage life	10
Total devices	65

3.1 Test condition A. Procedure for monolithic and multichip microcircuits. Limit testing shall be conducted as described in 3.1.1 through 3.1.7 in the sequence shown, unless otherwise specified (see 4.). Failure analysis of all devices failing limit tests shall be performed in accordance with method 5003, test condition B, unless otherwise specified in the applicable acquisition document. Limit testing may be discontinued prior to completing the test when 50 percent of the test sample has failed that specific test.

3.1.1 Thermal evaluation. This test shall be performed in accordance with method 1012, test condition B. With maximum power applied, the complete temperature gradient of the active chip area shall be recorded. This data shall be analyzed to determine that no areas of abnormally high operating temperatures are present as a result of improper design or processing. The thermal resistance at the maximum operating temperature of the device shall be determined using test condition C or method 1012.

3.1.2 Extended thermal shock. The purpose of this testing is to establish the resistance of the device to thermal fatigue effects. The device shall be subjected to a minimum of 100 cycles of thermal shock, in accordance with method 1011. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	15	C
2	15	D
3	70	F

Parameter measurements (see 1.2) shall be made at the completion of 15, 30, 40, 70, and 100 cycles, and the number of failures after each of these cycles shall be recorded.

3.1.2.1 Temperature cycling. When specified in the applicable acquisition document, temperature cycling method 1010 may be substituted for the thermal shock test in 3.1.2. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	20	B
2	20	C
3	20	D

Parameter measurements (see 1.2) shall be made at the completion of each step, and the number of failures for each of these steps shall be recorded.

3.1.3 Step-stress mechanical shock. The purpose of this test is to establish the mechanical integrity of the device. The device shall be subjected to mechanical shock in accordance with method 2002 and the following step-stress sequence:

Step	Test condition	Plane	No. of shocks
1	B	Y_1	5
2	C	Y_1	5
3	E	Y_1	5
4	F	Y_1	5
5	G	Y_1	5

Electrical parameter measurements (see 1.2) shall be made after each step, and the number of failures incurred at each step shall be recorded.

3.1.4 Step-stress constant acceleration. The purpose of this testing is to establish the mechanical integrity of the device. The device shall be subjected to a constant acceleration in accordance with method 2001 and the following step-stress sequence:

Step	Test condition	Plane
1	E	Y_2, X_1, Z_1, Y_1
2	F	Y_2, X_1, Z_1, Y_1
3	G	Y_2, X_1, Z_1, Y_1
4	H	Y_2, X_1, Z_1, Y_1

Electrical parameter measurements (see 1.2) shall be made after each plane, and the number of failures incurred shall be recorded.

3.1.5 Step-stress operational life. The purpose of this test is to establish the operational stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The results of the testing will also be utilized to evaluate the safety factors built into the device, to establish the safe constant operational stress conditions, and to improve through corrective action(s) the reliability of the device. Electrical parameter measurements shall be made after each stress level and the number of failures incurred in each step shall be recorded.

3.1.6 Constant high-stress operational life. The purpose of this test is to induce meaningful operational failures in a relatively short period of time and to compare the results of this testing with the results obtained from the step-stress operational life. The stress level to be applied and intervals to intermediate electrical measurements shall be determined on the basis of the results obtained in the step-stress tests (see 3.1.5). Electrical parameter measurements shall be made after each specified time interval and the number of failures shall be recorded.

3.1.7 Step-stress storage life. The purpose of this test is to establish the storage stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The storage temperatures and the step duration shall be established prior to initiation of testing. The results of the testing will be utilized to evaluate the maximum limits of device resistance to failure at high temperature. Electrical parameter measurements shall be made after each stress level and the number of failures incurred at each level shall be recorded.

3.2 Test condition B. Procedure for film and hybrid microcircuits. Limit test shall be conducted in accordance with table I and as described in 3.1.1 through 3.1.7 except that the specified test condition may be changed. When test condition or stress levels are changed, they shall be established prior to the initiation of test. Failure analysis of all devices failing limit tests shall be performed in accordance with method 5003, test condition B, unless otherwise specified in the applicable acquisition document. Unless otherwise specified in the applicable acquisition document, limit testing in any test may be discontinued after 50 percent of test sample has failed that specific test.

3.3 Test plan. When required by the applicable acquisition document, the specific procedures for conducting limit testing shall be submitted as a "Limit Test Plan" for approval by the acquiring activity prior to the initiation of testing. This plan shall include the following as a minimum:

a. Activity responsible for performing the test.

b. Device types to be subjected to limit testing and criteria for their selection.

c. Failure criteria including electrical parameters to be measured.

d. Testing schedule.

e. Description of testing equipment.

f. Test condition if other than specified.

g. Data recording and reporting formats.

h. Data analysis procedures.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test condition letter (see 3.1 and 3.2).

   b. Test sequence and sample quantities if other than specified (see 3.1 and 3.2).

   c. Failure analysis procedures and test condition, if other than specified (see 3.1 and 3.2).

   d. For test condition B, the test conditions and stress levels, where applicable (see 3.2).

   e. Percent failure for test termination, if other than specified (see 3.1 and 3.2).

   f. Requirements for Limit Test Plan and data reporting (see 3.3).

METHOD 5007.6

WAFER LOT ACCEPTANCE

1. PURPOSE. This method establishes the requirements for the lot acceptance testing of microcircuit wafers intended for class level S use.

2. APPARATUS. The apparatus used shall be in accordance with the apparatus requirements of the methods specified in the conditions column of table I.

3. PROCEDURE. The performance of the wafer lot acceptance tests shall be in accordance with the conditions specified in table I. If a lot fails a test under the sampling plan, as an alternative to rejecting the entire lot, the manufacturer may elect to test each wafer in the lot for that parameter(s). All wafers successfully passing the test(s) shall be considered the lot for the remainder of the tests. All wafers failing any test shall be removed from the lot. Data obtained from all tests shall be recorded. The sequence of the tests in table I does not have to be adhered to, however, the tests must be performed at the point in the processing (if specified) required in the conditions column of table I. Where limits are based on tolerances about an "approved design nominal", the nominal shall be stated in the maintenance plan submitted for approval to the qualifying or acquiring activity. Where table I limits are based on tolerances about the "mean", the mean shall be determined initially on measurements from a minimum of five lots and the mean shall be stated in the maintenance plan submitted for approval to the qualifying or acquiring activity. In no case shall the "design nominal" or "mean" exceed the absolute limits specified in table I.

4. SUMMARY. The following detail shall be specified in the applicable device specification:

Requirements or limits if other than those on table I.

TABLE I. Wafer lot acceptance tests.

Test	Conditions 1/	Limits 3/	Sampling plan
1. Wafer thickness	Measurement shall be performed after final lap or polish. All readings shall be recorded. 2/	Maximum deviation of ±2 mil from approved design nominal 6 mil minimum.	Two wafers per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
2. Metallization thickness	All readings shall be recorded.	a. Conductor: 8 kÅ minimum for single level metal and for the top level of multi-level metal; 5 kÅ minimum for lower levels, with a maximum deviation of ±20 percent from the approved design nominal. b. Barrier: Maximum deviation of ±30 percent from the approved design nominal.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10 V or more)	Record V_{FB} or V_T.	a. ΔV_{FB} or ΔV_T $\leq$0.75, normalized to an oxide thickness of 1000Å for bipolar digital devices operating at 10 volts or greater and all bipolar linear devices not containing MOS transistor(s). The monitor shall have an oxide and shall be metallized with the lot.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.

See footnotes at end of table.

TABLE I. Wafer lot acceptance tests - Continued.

Test	Conditions 1/	Limits 3/	Sampling plan
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10 V or more)	Record VFB or V_T.	b. ΔV_{FB} or Δ_{VT} $\leq$1.0 V,normalized to an oxide thickness of 1,000Å for bipolar linear devices that operate above 5 V and containing MOS transistor(s), and digital devices that operate above 10 V and containing MOS structures. The V_{FB} limit shall not be exceeded by the sum of the absolute values of the MOS oxide transistors and the metallization Δ. The monitor(s) shall be oxidized and metallized with the lot. Separate monitors may be used for this test. c. ΔV_{FB} or V_T $\leq$0.4 V, normalized to an oxide thickness of 1,000Å for MOS devices. A monitor consisting of a gate oxide metallized with the lot shall be used.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
4. SEM	MIL-STD-883, method 2018.	MIL-STD-883, method 2018.	MIL-STD-883, method 2018. Lot acceptance basis.
5. Glassivation thickness	All readings shall be recorded.	6 kÅ minimum for SiO_2 and 2 kÅ for Si_3N_4 with maximum deviation of ±20 percent from approved design nominal.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

See footnotes at end of table.

TABLE I. Wafer lot acceptance tests - Continued.

Test	Conditions 1/	Limits 3/	Sampling plan
6. Gold backing thickness (when applicable)	All readings shall be recorded.	In accordance with approved design nominal thickness and tolerance.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

1/ The manufacturer shall have documented procedures for performing each required test. These procedures shall be made available to the qualifying activity or acquiring activity upon request.

2/ This test is not required when the finished wafer design thickness is greater than 10 mil.

* 3/ Approved design nominal values or tolerances shall be submitted to the qualifying activity for line certification in accordance with DESC-EQM-42 or equivalent.

METHOD 5008.8

TEST PROCEDURES FOR HYBRID AND MULTICHIP MICROCIRCUITS

* Method 5008 is canceled effective 1 June 1993. It is superseded by MIL-PRF-38534. For Federal Stock classes other than 5962, the following paragraphs of MIL-PRF-38534 are provided to replace method 5008.

* Superseded method 5008	MIL-PRF-38534	Requirement
3.2 Element evaluation	4.3 Element evaluation	Element evaluation
3.3 Process control	4.4 Process control	Process control
3.4 Device screening	4.5 Device screening	Screening
3.5 Quality conformance evaluation	4.7 QCI	QCI

METHOD 5009.1

DESTRUCTIVE PHYSICAL ANALYSIS

1. PURPOSE. The purpose of this test is to describe requirements for performance of destructive physical analysis (DPA) for the applicable device class, for sampling, preparation, procedures, accept/reject criteria, disposition of rejected lots and documentation. While this test method may be used by a microcircuit manufacturer, it is intended that these procedures be actually performed by the contractor, subcontractor, or independent testing lab.

1.1 Definitions.

a. Defects. Any nonconformance from specified requirements for form, fit, function, or workmanship.

b. Destructive physical analysis. The process of disassembling, testing, and inspecting a device for the purpose of determining conformance with applicable design and process requirements.

c. Lot related defect. A defect, attributable to a variance in design or the manufacturing, test or inspection process, that may be repetitive (e.g., mask defects, metallization thickness, bond strength insulation resistance and separation between metallization runs, wires or wires and die edge).

d. Screenable defects. A defect for which an effective nondestructive screening test or inspection is available or can be developed.

2. APPARATUS. The apparatus shall consist of suitable equipment to perform each specified DPA test.

* 3. PROCEDURE. The organization (contractor, subcontractor, or independent test lab) conducting the DPA test should contact the manufacturer of the product and supply a list of test methods that are to be used during the DPA test. The manufacturer can then advice the DPA test organization if there are any significant changes to those test methods that are allowed as modification options within MIL-STD-883, MIL-PRF-38535 or under the manufacturer's approved program plan.

3.1 Sample selection. A random sample shall be selected from the inspection lot in accordance with table I, unless otherwise specified.

TABLE I. Sample selection.

Monolithic microcircuits	Two devices or 1 percent of the inspection lot, whichever is greater, to a maximum of 5 total devices, unless otherwise specified, (see 3.1.1 and 4a).
Hybrid or multichip microcircuits	Two devices or 1 percent of the inspection lot, whichever is greater, to a maximum of 5 total devices, unless otherwise specified, (see 3.1.1 and 4a).

* 3.1.1 Combining sample. Where an inspection lot is comprised of more than one device type covered by a single device specification or drawing, the sample selected shall be proportionately divided from the device types in order to assure a representative sampling, and not less than one, of each device type in the DPA sample.

3.2 DPA report. A DPA report shall be prepared for each inspection lot tested and submitted to the acquiring or qualifying activity. The report shall consist of the following:

a. DPA summary sheet.

b. DPA checklist.

c. DPA test data sheet.

d. Photographs.

e. Other data or analysis supporting findings.

3.2.1 DPA checklist. A checklist shall be used to record all attribute data from the applicable test.

3.2.2 DPA test data sheet. A test data sheet shall be used to record the variable data from the applicable test and any electrical test specified.

NOTE: No provisions have been included herein for electrical testing since all devices shall have already passed the specified electrical tests; however, electrical tests may be required for follow-up analysis of a physical discrepancy.

3.2.3 DPA summary sheet. A summary sheet shall be used to summarize the DPA test results, analysis supporting findings, provide other essential data and indicate disposition of lot.

3.3 General requirements.

3.3.1 DPA evaluation. The results of all tests and examinations performed on DPA sample items shall be analyzed by qualified technical personnel to determine disposition and corrective action, as applicable, of the lot from which the samples were taken.

3.3.2 Photographs. Photographs shall be made at sufficient magnification and with enough views to clearly document significant details of the parts construction. When SEM or optical microscopes are used to evaluate a device, photographs shall be made to document discrepant or worst case features.

3.3.2.1 Photograph requirements. A minimum of two photographs will normally be required to document baseline characteristics of an opened part prior to performance of any destructive tests. These shall be supplemented with other photographs as required to record observed defects or anomalies. Microscopy techniques such as color, dark field, phase contrast, interference contrast, etc., shall be used as necessary to enhance image clarity. When SEM examination is performed the DPA report shall include, as a minimum, view(s) of significant features of the die, a photograph of the worst case oxide step and a photograph of the worst case metallization. Each photograph shall be labeled or otherwise identified with the DPA report number, and, if applicable, the part number, serial number, lot date code, and the magnification (and viewing angle for SEM photographs) used.

3.3.3 Retention of DPA reports. The original copy of all DPA reports shall be retained by the performing organization and a copy submitted to the acquiring or qualifying activity.

3.3.4 Sectioned samples. When performed techniques similar to those used to prepare sectioned metallurgical and mineralogical specimens for optical examination are generally applicable to the preparation of DPA samples. The device to be examined is first potted in a suitable plastic (or mounting by other suitable means). It is then cut or rough ground to the desired section plane. This is followed by fine grinding, polish and sometimes an etch to bring out the necessary detail. Care shall be taken to ensure that damage is not introduced during any of these operations (in particular, during potting cure, cutting, and rough grinding).

3.3.5 SEM samples. The microcircuits shall be prepared for SEM examination in accordance with method 2018 of MIL-STD-883, "Notes on SEM examination of Microelectronic Parts". Other types of parts shall be prepared for SEM by using standard laboratory techniques for mounting and coating, taking care that anomalies are not introduced by the coating.

3.3.6 Baseline design documentation. Each DPA procedure should be referenced to a baseline photograph, sketch, or drawing showing the general configurations of the device to be examined, which includes critical dimensions, location of constituent parts and details of any pertinent materials or processes. The baseline documentation shall be current so as to show any approved changes in the configuration.

3.4 Microcircuits (monolithic) procedure. The purpose is to verify external and internal physical configuration and that the devices were not damaged during sealing or any other processing step(s). To verify that the devices have met the requirements for radiography, seal, external visual, internal water vapor analysis, internal visual, baseline, bond strength, and contamination control.

3.4.1 External visual. Record identification marking. Examine parts, at 10X minimum magnification for configuration and defects in seal, plating, or glass feed through in accordance with method 2009 of MIL-STD-883.

3.4.2 Radiography. When specified, radiography shall be in accordance with MIL-STD-883, method 2012. Radiograph shall be required before delidding to examine cavity devices for loose particles, die attach, and to determine internal clearances. It is also useful as an aid in locating delidding and sectioning cuts and to nondestructively investigate suspected defects.

3.4.3 Seal. A fine and gross leak seal test shall be performed on all DPA samples in accordance with MIL-STD-883, method 1014. Record both fine and gross leak rates.

3.4.4 Internal water vapor analysis. When specified, internal water vapor analysis shall be performed in accordance with method 1018.

3.4.5 Internal visual. De-cap all samples using appropriate method (see 3.6) taking care not to introduce contamination during the de-cap process. Examine all devices in accordance with MIL-STD-883, method 2010, test condition A or B or appendix A of method 5004 (alternate 2) as applicable, and methods 2013 and 2014.

3.4.6 Baseline configuration. During external and internal visual all devices shall be evaluated for conformance with the baseline design documentation (see 3.3.6) and other specified requirements. Variance from requirements shall be reported as defects.

3.4.7 Bond strength. Perform bond strength tests in accordance with MIL-STD-883, method 2011, test condition D. Pull all wires on at least two devices. Record the force at which the wire breaks or bond lifts and the location of the break.

3.4.8 SEM. Prepare the samples for SEM evaluation and conduct this inspection in accordance with MIL-STD-883, method 2018. If any of the wire bonds lifted during the bond strength tests, these shall be included in the SEM inspection to determine the nature of the bond to chip interface at the point of rupture.

3.4.9 Die shear. Die shear tests shall be performed on at least two samples in accordance with MIL-STD-883, method 2019. Record the die force required to separate the die from substrate and the interface appearance in terms of areas affected in the break.

3.4.10 Evaluation criteria. The inspection lot shall be considered suspect if devices exhibit any defects when inspected or tested to the criteria listed below. Each defect shall be photographed (when applicable), measured, and described in the DPA report. In the absence of defects or based on a decision by the responsible parts authority that any observed anomalies do not constitute rejectable defects, the lot may be considered acceptable for use (see 3.7.1 for disposition of suspect lots).

INSPECTION REQUIREMENT	MIL-STD-883 EVALUATION CRITERIA
External visual	Method 2009
Radiography	Method 2012
Seal	Method 1014
Internal water vapor	Method 1018
Internal visual	Method 2010 test condition A or B or alternate 2 of Method 5004 as applicable, 2013 and 2014
Bond strength	Method 2011
SEM	Method 2018
Die shear	Method 2019
Configuration	Baseline design documentation

3.5 Microcircuits hybrid and multichip procedure. The purpose is to verify external and internal physical configuration. To verify that devices met the requirements for radiography, PIND, seal, external Visual, gas analysis, internal visual, baseline, bond strength, and contamination control. These devices are normally custom and will depend on contractor drawings, therefore, the DPA procedure for a hybrid or multichip microcircuit shall be tailored to evaluate the features specified and the overall configuration as defined by the applicable hybrid or multichip drawing.

3.5.1 External visual. Conduct external visual examination on all samples to determine conformance with MIL-STD-883, method 2009, and the applicable device specification.

3.5.2 Radiography. When specified, radiography shall be in accordance with MIL-STD-883, method 2012. Radiography shall be required before delidding to examine cavity devices for loose particles, die attach, improper interconnecting wires, and to determine internal clearances. It is also useful as an aid in locating delidding and sectioning cuts and to nondestructively investigate suspected defects.

3.5.3 Particle impact noise detection test (PIND). A PIND test shall be performed on all DPA samples in accordance with MIL-STD-883, method 2020, condition A or B.

3.5.4 Seal. A fine and gross leak seal test shall be performed on all DPA samples in accordance with MIL-STD-883, method 1014. Record both fine and gross leak rates.

3.5.5 Internal water vapor analysis. When specified, internal water vapor analysis shall be performed in accordance with method 1018.

3.5.6 Internal visual. De-cap all devices (see 3.6) and perform internal visual inspection in accordance with MIL-STD-883, method 2017, and the applicable device design data.

3.5.7 Baseline configuration. Evaluate configuration and workmanship of each sample for compliance with the requirements of the applicable device specifications and drawings or baseline design documentations (see 3.3.6). Report variances as defects.

3.5.8 Bond strength. Perform bond strength tests in accordance with MIL-STD-883, method 2011. Pull all wires on at least two devices. Record the force at which the wire breaks or bond lifts and location of the break.

3.5.9 SEM. Prepare the samples for SEM evaluation and conduct this inspection on the microcircuits and other expanded contact chips in accordance with MIL-STD-883, method 2018. If any of the wire bonds lifted during the bond strength test, these shall be included in the SEM inspection to determine the nature of the bond to chip interface at the point of rupture.

3.5.10 Die shear. Die shear tests shall be performed on at least two samples in accordance with MIL-STD-883, method 2019. Record the die force required to separate the die from substrate and the interface appearance in terms of area affected in the break. Test a representative sample of each chip type in each package under test. Samples of each other chip type such as resistors and capacitors shall also be tested for shear strength in accordance with the requirements of the applicable specification, and the force required to separate the active and passive components from the substrate shall be recorded.

3.5.11 Evaluation criteria. The lot shall be considered suspect if parts exhibit any defects when inspected or tested to the criteria listed below. Each defect shall be photographed, measured, and described in the DPA report. In the absence of defects or based on a decision by the responsible parts authority that any observed anomalies do not constitute rejectable defects, the lot may be considered acceptable for use (see 3.7.1 for disposition of suspect lots).

INSPECTION REQUIREMENT	MIL-STD-883 EVALUATION CRITERIA, Sample Size
External visual	Method 2009
Radiography	Method 2012
PIND	Method 2020
Seal	Method 1014
Internal water vapor	Method 1018
Internal visual	Methods 2017, 2010 test condition A or B or alternate 2 of Method 5004 as applicable; 2013 and 2014
Bond strength	Method 2011
SEM	Method 2018
Die shear	Method 2019
Configuration	Baseline design documentation

3.6 Delidding procedures. The devices shall be delidded using one of the procedures below or other suitable means. Caution should be exercised to preclude damage to the device or the generation of internal contamination as the result of delidding.

3.6.1 Solder seals. Do not reflow the solder. After these cans are opened, the interior shall be examined for excess solder or flux. Reflowing the solder seal will destroy the evidence. To open, grind can just above the header until it is thin enough to be cut with a sharp instrument.

3.6.2 TO-5 type enclosures. Semiconductors, microcircuits, and other devices are often packaged on TO-5 type enclosure that can be quickly opened using a commercial device known as a "Head Remover, Silicon" or, more commonly, as a TO-5 can opener. This device can be modified to accept various lid heights and a metal guide bar may be added over the cutting wheel to maintain minimum clearance between the TO-5 flange and the cutting wheel.

3.6.3 Flange welded enclosures. Grind off flange until can is thin enough to be cut with a sharp instrument.

3.6.4 Tubulated enclosures. Before opening, file or dry grind into the crimp to ensure that it has properly engaged the conductor. Note whether the number and placement of the crimps are normal and check for over crimping. Free the center conductor from the crimp before removing the device cover by using a can opener or grinder.

3.6.5 Solder sealed flat-pack or DIP. Hold the sample flat against a dry Buehler grinding wheel (180 grit paper) until the lid becomes thin enough to make the cavity indentation visible. Clean the sample, then puncture the lid with a sharp instrument and peel it off.

3.6.6 Ceramic flat-pack.

a. Preferred method. Pass an oxygen/butane flame over the lid of the sample while the part is under light pressure from the blades of a delidding vise. Each pass of the torch should last two or three seconds and the vise should be tightened slightly between passes. Two or four passes are normally required. The blades of the delidding vise should be positioned above the leads and not at the ends of the sample.

b. Alternate method. Hold the sample firmly by its lower body (this may require careful bending of the leads). Place the point of a sharp blade on the seal line above the lead frame and strike the blade lightly with a small hammer. Continue this process around the package circumference until the seal fractures to release the lid.

NOTE: The "flat-pack delidding vise" referred to in 3.6.6 is a special fixture which can be assembled or may be acquired from a commercial source.

3.6.7 Dual-in-line package.

a. Preferred method. This technique is suitable for all types of ceramic packages, including those types where the lid seal is formed at the lead frame interface. Position the package between the knife blades of a delidding vise contacting the seal region. The physical condition of the seal regions (i.e., the determination of the optimum package sides exhibiting the maximum seal glass dimensional length) to be clamped between the parallel cutters, will generally dictate the orientation. Apply sufficient pressure to just hold the package in place. Heat the package lid for approximately 5 seconds with a oxygen/butane microflame torch, remove the heat and slowly increase pressure on the package seal. Repeat the heat/pressure sequence until the entire lid, intact, is sheared off at the seal.

b. Alternate method. Place abrasive paper (e.g., Buehler emery paper or equivalent) on a flat surface. Abrade the package lid by repeated strokes across the paper. The sample may optionally be placed in a fixture containing a mounted dual-in-line socket for ease in handling. Continue abrading, with frequent visual checks, until the lid is almost completely gone. Remove the remainder of the lid over the cavity by attaching a piece of tape and lifting off.

3.7 Failure criteria. The inspection lot shall be considered suspect if the devices exhibit any defect when inspected or tested to the criteria in 3.4 or 3.5. Each defect shall be photographed, measured, and described in the DPA report.

3.7.1 Disposition of suspect lots. Inspection lots which are found to have one or more defects as the result of evaluation of a DPA sample shall be: a. subjected to resampling if the results of the first sample were inconclusive, b. screened, c. scrapped, or d. returned to supplier, as applicable.

3.7.2 Resampling. In the event that results of the initial DPA sample are inconclusive, a second DPA sample may be selected in accordance with 3.1 except that the sample size shall be determined by the cognizant authority for the parts and approved by the acquiring or qualifying activity on the basis of the type of defect that is being investigated and the number of devices remaining in the inspection lot. Final disposition shall be made of the inspection lot after completion of the evaluation of the second sample.

3.7.3 Rescreened lots. Inspection lots which are found to have parts with screenable defects may be subjected to 100 percent nondestructive screening tests to eliminate the nonconforming items. After completion of screening the remaining devices may be accepted for shipment.

3.7.4 Retention of samples. When requested, all DPA samples shall be submitted to the acquiring activity or qualifying activity along with the DPA report.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

   a. DPA sample size if different than specified in 3.1.

   b. Radiography requirement (see 3.4.2 and 3.5.2).

   c. Disposition of suspect lots and DPA samples if different than specified (see 3).

   d. Any additional requirements for tests or for documentation in DPA report (see 3.2)

   e. Electrical test requirement, if applicable.

   f. Die shear strength for resistor and capacitor chips (see 3.5.10).

   g. Internal water vapor requirement (see 3.4.4 and 3.5.5).

   h. A manufacturer listing of defects, if applicable (see 3.4.5).

METHOD 5010.3

TEST PROCEDURES FOR COMPLEX MONOLITHIC MICROCIRCUITS

* 1. PURPOSE. This method establishes screening, qualification, and quality conformance requirements for the testing of complex monolithic microcircuits to assist in achieving the following levels of quality (class level B and S) and reliability commensurate with the intended application. Complex monolithic microcircuits are defined as monolithic devices that contain a minimum of 4,500 transistors. It shall be used in conjunction with other documentation such as appendix A of MIL-PRF-38535 and an applicable device specification or drawing to establish the design, material, performance, control, and documentation requirements which are needed to achieve prescribed levels of device quality and reliability.

2. APPARATUS. Suitable measurement equipments necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

3. PROCEDURE. The procedures defined herein, including appendix I and II, outline the requirements and testing necessary to certify and qualify a complex microcircuit design, fabrication, assembly and testing facility. It illustrates the concept of generic qualification through the use of standard evaluation circuits and process monitors.

* 3.1 Test procedures for complex monolithic microcircuits. Complex monolithic microcircuits shall be tested as described herein, and in the device specification or drawing.

* 3.1.1 Precedence. Unless otherwise specified in the device specification or drawing, the test requirements and conditions shall be given herein.

* 3.1.2 Electrostatic discharge sensitivity. Electrostatic discharge sensitivity testing, marking, and handling shall be in accordance with appendix A of MIL-PRF-38535.

3.1.3 Failure analysis. When required by the applicable device specification failure analysis of devices rejected during any test in the screening sequence shall be accomplished in accordance with method 5003, test condition A.

* 3.1.4 Failure analysis class level S. Class level S devices shall be analyzed in accordance with method 5003, test condition B to identify the cause for failed lots and burn-in failures in accordance with appendix A of MIL-PRF-38535, 40.3.3.1, and 40.6.1.2.1. The documented results shall only be reported to the qualifying or acquiring activity when specifically requested.

* 3.1.5 Class requirements. Within tables having a class column, only those test and inspections or subgroups identified with "B" are applicable to class level B. All apply to class level S.

* 3.1.6 Radiation. When required by the applicable device specification or drawing, qualification, and quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal class level S and B requirements. These requirements for each specified radiation levels (M, D, L, R, F, G and H) are detailed in table VIII herein.

3.2 Element evaluation.

3.2.1 General.

3.2.1.1 Element. Herein "element" refers to materials for device assembly. Before device assembly, element characteristics shall be evaluated and verified to assure their compatibility with element specifications, device requirements, and manufacturing procedures (see table I). Also, characteristics which cannot be verified after manufacturing but could cause function failure shall be evaluated and verified before assembly.

TABLE I. Element evaluation summary.

Element	Paragraph	Requirement
Microcircuit wafer	3.2.2	Appendix II (herein)
Package	3.2.3	Table II (herein)

3.2.1.2 Element evaluation requirements. Element evaluation may be performed at either the element supplier or device manufacturing facility up to the point where the element must undergo processing or assembly prior to testing. If element evaluation is performed by the supplier, then the device manufacturer must obtain a summary of the results for verification, and record retention.

3.2.2 Microcircuit wafer evaluation.

3.2.2.1 Definition. Diffused wafers used and evaluated shall, as a minimum, be complete with interconnect layers and glassivation from material that was homogeneously processed through wafer fabrication.

3.2.2.2 General. For the purpose of microcircuit wafer evaluation and wafer lot acceptance, measurement of the process monitor (PM), verifying that the identified parameters are within process limits, will be required from each wafer lot in accordance with appendix II wafer lot acceptance herein. Each die from each diffused wafer lot shall be electrically tested prior to assembly in accordance with the manufacturer's in-house documentation.

3.2.3 Package evaluation. Each package type shall be evaluated and characterized in accordance with table II herein prior to use. Finite element analyses techniques may be used. Packages used for complex monolithic microcircuits and fabricated to this test method shall be tested as follows:

3.2.3.1 Definition. Package used and evaluated shall consist of the same element specifications, materials, and finish; and homogeneously processed through device assembly.

3.2.3.2 Incoming inspection.

a. From the initial package inspection lot, a randomly selected sample shall be subjected to package evaluation (see table II). Additionally, subgroup 3 testing shall be accomplished using sealed packages. A die may be attached. Subgroups 2, 3, and 4 apply to cases only.

b. Additionally, subgroups 1, 2, and 3 of table II shall be accomplished for each subsequent acquisition.

c. For solderability (subgroup 2), lead integrity (subgroup 3), and metal package isolation (subgroup 4) defined within table II, a quantity (accept number) of 15 (0) shall apply to the number of terminals or leads tested. The leads shall be randomly selected from the three packages.

* TABLE II. Package evaluation requirements.

Subgroup	Class levels		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	S	B		Method	Condition		
1	X	X	Physical dimensions	2016		15 (0)	3.2.3.3
2	X	X	Solderability	2003	Solderability temperature 245 ±5°C	3 (0) 1/	
3	X	X	Thermal shock or Temperature cycle	1011 1010	C C (20 cycles)	3 (0)	
	X	X	High temperature bake	1008	2 hours at 150°C	3 (0)	
	X	X	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carriers) B1 (leaded chip carrier packages) (Pin grid array leads and rigid leads)	3 (0) 1/	
	X	X	Seal	1014	D Sealed cases	3 (0)	
4	X	X	Metal package isolation	1003	600 V dc, 100 nA maximum	3 (0) 1/	3.2.3.4
5	X	X	Insulation	1003	2/	3 (0)	
6	X	X	Conductor	MIL-STD-202 method 307	2/	3 (0)	
7	X	X	Thermal characterization	1012		3/	

1/ A quantity (accept number) of 15 (0) shall apply to the number of terminals or leads to be tested. The leads shall be randomly selected from three packages minimum.

* 2/ Selected from three packages minimum. Conditions as specified by acquisition document and Appendix A of MIL-PRF-38535.

3/ Required on all package types prior to initial use.

* 3.2.3.3 Subgroup 1. Separately verify case and cover dimensional compliance with the device specification or drawing.

3.2.3.4 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to nonmetallic cases.

3.3 Manufacturing control.

3.3.1 Process control requirements. Line control as detailed below is required.

3.1 Wafer fabrication controls. Wafer fabrication shall be controlled in accordance with the manufacturer's fabrication baseline and documented procedures of the fabrication process.

* 3.3.1.2 Assembly controls. Assembly controls shall be in accordance with the manufacturer's assembly baseline and documented assembly procedures and additions herein

3.3.2 Design/layout system control. Design/layout controls shall be implemented using appendix I as a guide.

* 3.3.3 Testing controls. Documentation of testing controls shall meet the requirements of MIL-PRF-38535, appendix A.

* 3.3.3.1 Test vectors. The manufacturing-level logic test vectors shall be graded for fault coverage using a fault simulator. The resulting fault coverage shall be reported in the device specification or drawing. Fault coverage shall be based on the detectable equivalence classes of single, permanent, stuck at zero, and stuck at one faults on all logic lines of a structural logic model. The logic model shall be expressed in terms of gate-level primitives or simple atomic functions (such as flip-flops). Large, regular structures such as RAMs and ROMs shall not be modeled at the gate level; rather, documentation shall be provided to show that these structures are tested using appropriate procedures (such as, galloping patterns for a RAM).

* 3.3.3.2 Built-in-test/build-in-redundancy. When specified in the device specification or drawing, the following shall apply.

* 3.3.3.2.1 Probe/bond sites. The device shall contain probe/bond sites to allow testing using the full set of test vectors specified in the device specification or drawing.

3.3.3.2.2 Built-in redundancy for yield enhancement. Where built-in redundancy is used to provide yield enhancement, testing shall be included to provide a statistic which represents the amount of alternate element selection utilized.

3.3.3.2.3 Built-in redundancy using self test and fix. Where built-in redundancy is provided in the form of self test and fix, the circuitry will be capable of interrogation to determine the level of redundancy remaining on the device.

* 3.3.4 Quality controls. The product assurance program plan shall be in accordance with MIL-PRF-38535, appendix A.

3.3.4.1 Process monitor. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's process monitor (PM). The PM is to be designed so that the dc process parameters may be measured in wafer form. The PM may also be packaged so as to permit biasing of those circuits for measurement. The PM design must be submitted to the qualifying activity for approval prior to qualification and must contain as a minimum the structures outlined in table I of appendix II herein.

3.3.4.1.1 Process monitors for other technology devices. An adequate set of PM's applicable for other technology devices shall be generated to assure that applicable failure mechanisms are detected and submitted for approval by the qualifying activity.

3.3.4.2 Qualification device. A qualification device shall be used to demonstrate process stability and reliability. The qualification device, either a standard evaluation circuit (SEC) or an actual device (worst case design) shall be submitted to the qualifying activity for approval and as such contain the basic information as detailed herein. The qualification device shall be fabricated with the same process and designed to the same design rules that will produce any device in the technology to be qualified. The qualification device design shall be configured in such a manner so as to evaluate the reliability of the underlayer designs (e.g., diffusion) and evaluate the worst case design rule conditions on the personalization layers. The design should utilize cell libraries as well as test structures which will detect metal to metal shorting or opening, high via resistance and dielectric pinholes during reliability life testing, where applicable. The following structures are suggested:

Parameter	Structure
Functionality and performance	Large functional block (ALU), ring oscillator
Contact resistance/electromigration	Contact strings
Hot electrons/holes	Short channel devices
Oxide breakdown voltage	Capacitors
Resistance (electromigration test)	Metal stripes

3.4 Screening procedures for microcircuits. Screening of microcircuits shall be conducted as described in 3.4 through 3.4.13 and table III herein. This provision does not preclude the performance of additional tests or inspection which may be required for specific devices or which may be desirable to optimize results of screening; however, any such special test inspection shall be subjected to the requirements of appendix A of MIL-PRF-38535, 40.3.4 and 40.3.7. Sampling inspections shall not be an acceptable substitute for any specified screening test. Any burn-in, in addition to that specified, is only permitted when documented in the lot records, and any failures shall be counted in applicable PDA calculations. Where end point or post test measurements are required as part of any given test method used in the screening procedure and where such post-test measurements are duplicated in the interim (post burn-in) or final electrical tests that follow, such measurements need not be duplicated and need to be performed only as part of the interim (post burn-in) or final electrical tests. Devices which pass screening requirements of a higher reliability level shall be considered to meet the screening requirements of all lower levels. In no case shall screening to a lower level than that specified be permitted.

3.4.1 General.

a. Devices that fail any test or inspection criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no device may be retested for acceptance. Unless otherwise specified in the device specification or drawings, electrical rejects may be used to satisfy sample selection requirements for qualification and quality conformance inspection in accordance with 3.5.

b. Device screening shall be performed in the sequence shown in table III except where variations in sequence are specifically allowed herein.

TABLE III. Device screening.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt	Method	Reqmt	
Wafer lot acceptance	5010 appendix II and 5007	All lots	5010 appendix II	All lots	
Nondestructive bond pull	2023	100%			
Internal visual	2010, test condition A	100%	2010, test condition B	100%	3.4.2
Stabilization bake. No end point measurements required					3.4.3
Temperature cycling or thermal shock	1010, test condition C	100%	1010, test condition C 1011, test condition A	100% 100%	3.4.5
Constant acceleration	2001, test condition E (min) Y1 orientation only	100%	2001, test condition E (min) Y1 orientation only	100%	3.4.6
Visual inspection		100%		100%	
Particle impact noise detection (PIND)	2020, test condition A	100%			3.4.7
Serialization		100%			
Interim (pre-burn-in) electrical parameters	In accordance with applicable device specification	100%	In accordance with applicable device specification	100%	3.4.9.1
Burn-in test	1015 240 hours at 125°C minimum	100%	1015 160 hours at 125°C minimum	100%	3.4.10
Interim (post-burn-in) electrical parameters	In accordance with applicable device specification	100%		Optional	3.4.9.1
Reverse bias burn-in	1015; test condition A or C, 72 hours at 150° minimum.	100%			

TABLE III. Device screening -Continued.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt.	Method	Reqmt.	
Interim (post-burn-in) electrical parameters	In accordance with applicable device specification	100%	In accordance with applicable device specification	100%	3.4.9.1
Percent defective allowable (PDA) calculation	5 percent (subgroup 1, table IV) 3 percent functional parameters at 25°C (subgroup 7 table IV)	All lots	5 percent (subgroup 1, table IV)	All lots	3.4.9.1
Final electrical test	In accordance with applicable device specification		In accordance with applicable device specification		3.4.11
a. Static tests					
(1) 25°C (subgroup 1, table IV)		100%		100%	
(2) Maximum and minimum rated operating temp. (subgroup 2, 3, (table IV)		100%		100%	
b. Dynamic or functional tests					
(1) 25°C (subgroup 4, or 7, table IV)		100%		100%	
(2) Minimum and maximum rated operating temp. (subgroup 5 and 6, or 8, table IV)		100%		100%	
c. Switching tests at 25°C (subgroup 9,) table IV)		100%		100%	

TABLE III. Device screening - Continued.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt.	Method	Reqmt.	
Seal Fine Gross	1014	100%	1014	100%	3.4.8
Radiographic	2012 two views	100%			3.4.12
Qualification or quality conformance inspection test sample selection	See 3.5		See 3.5		
External visual	2009	100%	2009	100%	3.4.13

* 3.4.2 Internal visual inspection. Internal visual inspection shall be performed to the requirements of method 2010, condition A for class level S devices and condition B for class level B devices. Devices awaiting preseal inspection, or other accepted, unsealed devices awaiting further processing shall be stored in a dry, inert, controlled environment until sealed.

Unless otherwise specified, at the manufacturer's option, test samples for group B, bond strength may be randomly selected prior to or following internal visual, prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam).

The alternate procedure of 3.4.2.1 shall be used when any of the following criteria are met:

a. Minimum horizontal geometry is less than three microns.

b. Metallization consists of two or more levels.

c. Opaque materials mask design features.

* 3.4.2.1 Alternate procedures for class level B microcircuits. Alternate procedures may be used on an optional basis on any microcircuit, provided that the conditions and limits of the alternate procedures are submitted to, and approved by the preparing activity, or the acquiring activity.

* 3.4.2.1.1 Alternate procedures. The deletions and the changes stated herein are allowable only if the requirements of alternate 1 or alternate 2 are met.

* Alternate 1: The deletions and the changes stated in 3.4.2.1.1a. are allowable for complex monolithic microcircuits for class level B product only if the requirements of 3.4.2.1.1.b and 3.4.2.1.1.c are imposed and any of the following conditions exists.

1. Minimum horizontal geometry is less than 3 micrometers (μm).
2. Interconnects consisting of two or more levels.
3. Opaque materials mask design features.

a. For inspection of each microcircuit die, delete the inspection criteria of 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.1.5, 3.1.6, 3.1.7, and 3.2.5 of condition B of method 2010 and for use in conjunction with alternate procedures, add 3.1.1.1, 3.1.1.2, 3.1.1.6, 3.1.3, 3.1.4, and 3.2.5 to the low magnification inspection of method 2010.

b. Temperature cycling (3.4.5). The minimum total number of temperature cycles shall be 50. The manufacturer may reduce the number of temperature cycles from 50 to the 10 required as part of normal screening based upon data justifying the reduction in temperature cycles approved by the preparing activity and an approved plan which shall include the following criteria:

(1) Reduction of test must be considered separately for each wafer fabrication line and each die family.

(2) The manufacturer shall demonstrate that the wafer fabrication line that produces product which will involve reduction of temperature cycles is capable and in process control.

(3) The manufacturer shall perform a high magnification visual inspection on a small sample of devices (e.g., 5(0)) to monitor the process. This inspection may be performed at wafer level.

c. Special electrical screening tests shall be applied to each microcircuit die at the wafer, individual die (chip) and packaged, or both, microcircuit level in accordance with the requirements of MIL-STD-883, method 5004, 3.3.2. The conditions and limits of the electrical tests (in table III format) shall be submitted to the preparing activity for approval and subsequently maintained on file with the qualifying activity. These special screens are in addition to the required electrical parametric tests which the device must pass and shall be designed to screen out devices with defects that were not inspected to the full criteria of 3.4.3 (internal visual). Due to the nature of these tests, they are not to be repeated as part of the qualification and quality conformance procedures.

* Alternate 2: The requirements and conditions for use of this alternate are contained in appendix A of method 5004. This option applies to both class level B and class level S microcircuits.

* 3.4.3 Stabilization bake. Stabilization bake is not required for class level S or class level B product unless specified in the device specification or drawing.

3.4.4 Visual inspection for damage. The manufacturer may inspect for damage after each screening step. Damaged devices shall be removed from the lot.

* 3.4.5 Temperature cycling or thermal shock. All devices shall be subjected to the requirements of temperature cycling or thermal shock. The device specifications or drawing shall specify which screen shall be employed. Temperature cycling shall be in accordance with MIL-STD-883, method 1010, condition C minimum. For class level B, this test may be replaced with thermal shock in accordance with MIL-STD- 883, method 1011, condition A minimum.

3.4.6 Constant acceleration. All devices shall be subjected to constant acceleration, in the Y_1 axis only, in accordance with MIL-STD-883, method 2001, condition E (minimum). Microcircuits which are contained in packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of five grams or more may be treated in accordance with provisions below as an alternate to this procedure. Delete test condition E and replace with test condition D. Unless otherwise specified, the stress level for large, monolithic microcircuit packages shall not be reduced below condition D. If the stress level specified is below condition D, the manufacture shall have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

* 3.4.7 Particle impact noise detection test (PIND). Testing to be performed in accordance with appendix A of MIL-PRF-8535, 40.6.3. The PIND test may be performed in any sequence after temperature cycling and prior to final electrical test.

* 3.4.8 Seal (fine and gross leak) testing. For class level S devices seal testing may be performed in any sequence between the final electrical test and external visual, but it shall be performed after all shearing and forming operations on the terminals. For class level B devices, fine and gross seal test shall be performed separate or together in any sequence and order between 3.4.7 and 3.4.13 and they shall be performed after all shearing and forming operations on the terminals. When the 100 percent seal screen cannot be performed following all shearing or forming operations (i.e., flat packs, brazed lead packages, and chip carriers) the seal screen shall be done 100 percent prior to those shearing and forming operations and a sample test using sample size number of 45 (C = 0) shall be performed on each inspection lot following these operations to verify integrity. For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15 (0). If sample fails the sample acceptance criteria, all devices in the inspection lot represented by the sample tested shall be subjected to and pass 100 percent fine and gross leak seal screens.

3.4.9 Electrical measurements.

* 3.4.9.1 Interim (pre- and post-burn-in) electrical parameters. Interim (pre- and post-burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in cases where delta parameters are specified) with the parameters, deltas, and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening, where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA, or 20 percent, whichever is greater.

* 3.4.9.2 Pattern failures. Pattern failure criteria may be used as an option for class level B, provided that:

a. Inspection lot size is less than 500 devices.

b. Pre burn-in electrical testing is done.

3.4.9.2.1 Pattern failures criteria. A maximum number of pattern failures (failures of the same part type when the failures are caused by the same basic failure mechanism) shall apply as specified in the acquisition document. If not otherwise specified, the maximum allowable pattern failures shall be five. Accountability shall include burn-in through final electrical test.

3.4.9.2.2 Pattern failure resubmission. When the number of pattern failures exceeds the specified limits, the inspection lot shall be rejected. At the manufacturer's option, the rejected lot may be resubmitted to burn-in one time provided:

a. The cause of the failure has been evaluated and determined.

b. Appropriate and effective corrective action has been completed to reject all devices affected by the failure cause.

c. Appropriate preventive action has been initiated.

* 3.4.10 Burn-in. Device burn-in shall be performed in accordance with the requirements of method 1015 conditions A, B, C, D, or E. Regardless of power level, devices shall be able to be burned-in at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I of method 1015 applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C, and where the ambient temperature would cause T_J to exceed 200°C for class level B or 175°C for class level S, the ambient operating temperature may be reduced during burn-in from 125°C to a value that will demonstrate a T_J between 175°C and 200°C (for both class levels S and B) and T_C equal to or greater than 125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

3.4.11 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the applicable device specification or drawing and shall include, as a minimum, the tests of group A, subgroups 1, 2, 3, 4 or 7, 5 and 6, or 8, and 9.

3.4.12 Radiographic. The radiographic screen may be performed in any sequence after PIND test and before external visual inspection. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

3.4.13 External visual inspection. All devices shall be inspected in accordance with MIL-STD-883, method 2009, prior to acceptance for shipment

* 3.5 Qualification and quality conformance procedures. Qualification and quality conformance shall be performed in accordance with 40.4 qualification procedures and 40.5 quality conformance inspection of appendix A of MIL-PRF-38535 except as modified herein. The qualification device shall be used for QCI testing in accordance with 3.5.3 herein, as well as for qualifying the process line. Life testing requirements shall follow the same criteria as burn-in (3.4.10 herein) for reduced temperature.

* 3.5.1 Qualification testing. Initial product process qualification shall be in accordance with MIL-STD-883 method 5005. Change to qualified product shall be addressed in accordance with MIL-STD-883, method 5005 and appendix A of MIL-PRF-38535, 30.4.2. The SEC shall be used for group D inspection whenever practical; where the SEC cannot be used, another die may be used (for gate arrays, 60 percent or greater utilization required). Utilizing the qualification device the process monitor, the manufacturer shall demonstrate:

a. Process control and stability.

b. Process/device reliability.

c. Design and simulation control.

3.5.1.1 Detailed qualification test plan. The manufacturer shall submit to the qualifying activity for approval a detailed qualification test plan to assure conformance to 3.5.1 herein. The test plan shall, as a minimum, define test groups, subgroups, conditions, and sampling plans in accordance with method 5005, as well as the tests to carry out 3.5.1.2, 3.5.1.3, and 3.5.1.4.

3.5.1.2 Database test. For qualification, at least five PM's per wafer (located in accordance with appendix II) shall be measured to ensure the establishment of a statistically valid database on which a decision can be made as to whether the manufacturer's process is stable and under control.

3.5.1.3 Qualification device design and test plan. Qualification device design and test plan to be used to qualify the manufacturing line shall be submitted to the qualifying activity for approval. The design must meet the minimum requirements of 3.3.4.2 herein. The test plan must include life test requirements. If a SEC is used as the qualification device, data demonstrating process reliability from lots processed within 12 months of qualification and that an on-going SEC program is in effect shall be submitted for qualifying activity review.

3.5.1.4 Design and simulation verification. Design and simulation verification shall be accomplished as follows:

a. Design rule check (DRC) verification. DRC software shall be run on a design which contains known design rule violations.

b. Electrical rule check (ERC) verification. ERC software shall be run on a design which contains known electrical rule violations (e.g., fan-out violations).

c. Layout versus schematic (LVS) check.

d. Correct by construction. If the manufacturers' design methodology is based on a "correct by construction" approach, distinct DRC, ERC, and LVS software is unnecessary and a, b, and c above do not apply. However, the manufacturer shall provide suitable data to demonstrate the correct performance of "correct by construction" software.

e. Computer aided design (CAD) system control shall be in accordance with appendix I herein.

* 3.5.2 Quality conformance inspection. This procedure, as applicable to the microcircuit type and class, shall apply for all quality conformance inspection requirements. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests herein. Where end-point electrical measurements are required for subgroups in groups B, C, D, and E testing herein, they shall be as specified in the applicable device specification or drawing. Where end-point measurements are required but no parameters have been identified in the acquisition document for this purpose, the final electrical parameters specified for 100 percent screening shall be used as end-point measurements. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.

* 3.5.2.1 Radiation hardness. Quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal class level S and B requirements. Those requirements are detailed in table VIII (group E) herein. The radiation levels (M, D, L, R, F, G and H) are defined in appendix A of MIL-PRF-38535.

* 3.5.2.2 Quality conformance inspection. For class level B quality conformance inspection, each inspection lot (sublot) shall pass groups A, B, and E (when applicable) tests or be accepted in accordance with 3.5.3 herein and the periodic group C and D tests shall be in accordance with appendix A of MIL-PRF-38535. End point electrical parameters shall be as specified in 3.5.2.3 herein. For class level S, each QCI inspection lot shall be assembled in accordance with the class level S requirements of appendix A of MIL-PRF-38535. Quality conformance testing for class level S shall be in accordance with tables IV, V, VI, and VII herein.

* 3.5.2.3 End point electrical parameters. Where intermediate and end point electrical measurements are required for subgroups B, C, D, and E testing, they shall be as specified in the applicable device specification or drawing where required and when end point parameters have not been identified, group A, subgroup 1, 2, 3, 4 or 7, and 9 shall be used for end point measurements.

3.5.2.4 Constant acceleration. Constant acceleration shall be performed in accordance with method 2001, test condition E for all applicable subgroups except as allowed in accordance with 3.4.6, herein.

3.5.3 Quality conformance testing. Conformance testing shall be performed through the use of the identified quality conformance vehicles.

Quality conformance test		Quality conformance vehicle	Frequency
Table IV	Group A	Actual device	Each inspection lot
Table V	Group B	Actual device	Each inspection lot
Table VI	Group C	SEC or actual device	3 months
Table VII	Group D	SEC or actual device	6 months
* Table VIII	Group E	Actual device	See MIL-PRF-38535. appendix A

3.5.3.1 Alternate group A method. The alternate group A method below may be used provided that:

a. Inspection lot size is less than 500 devices.

* b. Final electrical test shall assure that the electrical requirements of the device specification or drawing are met and shall include the tests of group A, subgroups 1, 2, 3, 4 or 7, 5 and 6 or 8, 9, as a minimum.

c. All test software and procedures are under document control.

3.5.3.1.1 In-line verification testing.

a. For each test set up (and operator for manual testing), production runs correlation unit to assure that the accuracy requirements of MIL-STD-883 4.5.2 are being met.

b. Testing is performed using the verified set up.

c. At the completion of testing utilizing the verified set up (not to exceed 8 hours and at the change of operators) a separate party (QA or QA designate) then verifies the production testing by:

(1) Checking visually to verify that the correct fixture, equipment, software, and procedure(s) were used.

(2) Actual testing of controlled known good device utilizing the fixtures, set ups, software and procedures that were used by production. Variables data for all required group A tests shall be read and recorded for the controlled unit. This data shall be maintained with the lot.

TABLE IV. Group A electrical test. 1/

Subgroup	Parameters 2/ 3/ 4/ 5/	Quantity/ acceptance number
1	Static test at +25°C	116/0
2	Static tests at maximum rated operating temperature	116/0
3	Static tests at minimum rated operating temperature	116/0
4	Dynamic test at +25°C	116/0
5	Dynamic tests at maximum rated operating temperature	116/0
6	Dynamic tests at minimum rated operating temperature	116/0
7	Functional test at +25°C	116/0
8	Functional tests at maximum and minimum rated operating temperatures	116/0
9	Switching tests at +25°C	116/0
10	Switching tests at maximum rated operating temperature	116/0
11	Switching tests at minimum rated operating temperature	116/0

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table I), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in 2/ above, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

* 5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE V. Group B testing.

Subgroup	Class level		Test	MIL-STD-883		quantity/(accept number) or sample size number, accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	Physical dimensions	2016		2 (0)	
2	X		Particle impact noise detection test	2020	A or B	15 (0)	3.4.7
3	X	X	Resistance to solvents	2015		3 (0)	
4	X	X	Internal visual and mechanical	2014		1 (0)	3.4.2
5	X	X	Bond strength a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2 (0)	
6	X	X	Die shear strength or substrate attach strength	2019 or 2027		2 (0)	
7	X	X	Solderability	2003	Solder temperature 245°C ±5°C	1 (0)	
8	X	X	Seal a. Fine b. Gross	1014		Sample size number = 15 C = 0	3.4.8

TABLE VI. Group C testing.

Subgroup	Class levels		Test	MIL-STD-883		Sample size number, accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	External	2009		Sample size number = 15 C = 0	3.4.13
	X	X	Temperature cycling	1010	C 100 cycles minimum		3.4.5
	X	X	Mechanical shock or constant acceleration	2002 2001	B, Y1 axis E, Y1 axis		3.4.6
	X	X	Seal (fine and gross)	1014			3.4.8
	X		Radiographic	2012	Y axis		3.4.12
	X	X	Visual examination		In accordance with visual criteria of method 1010.		
	X	X	End point electrical		As specified in accordance with device specification		3.5.2.3
2	X	X	Steady-state life test	1005	1,000 hours at +125°C minimum	Sample size number = 22 C = 0	3.5.2.3
			End point electrical		As specified in accordance with device specification		

TABLE VII. Group D testing.

Subgroup	Class		Test	MIL-STD-883		Quantity/ accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	Internal water vapor content 5000 PPM maximum water content at +100°C	1018		3 devices (0 failures) or 5 devices (1 failure)	
2	X	X	Moisture resistance	1004		5 (0)	
3	X	X	Salt atmosphere	1009		5 (0)	

TABLE VIII. Group E (radiation hardness assurance tests). 1/

Test	MIL-STD-883		Class level S		Class level B	
	Method	Condition	Quantity/ accept number	Notes	Quantity/ accept number	Notes
Subgroup 1 2/						
Neutron irradiation	1017	+25°C				
a. Qualification			a. 11 (0)	3/	a. 11 (0)	4/
b. QCI			b. 11 (0)	3/	b. 11 (0)	4/
Endpoint electrical parameters		As specified in accordance with device specification				
Subgroup 2 5/						
Steady-state total dose irradiation	1019	+25°C Maximum supply voltage				
a. Qualification			a. 4 (0) 2 (0)	a. 6/ 8/	a. 22 (0)	7/
b. QCI			b. 4 (0) 2 (0)	b. 6/ 8/	b. 22 (0)	7/
Endpoint electrical parameters		As specified in accordance with device specification				

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

2/ Waive neutron test for MOS IC devices except where neutron susceptibility is less than 10^{13} neutrons/cm^2 (e.g., charge coupled devices, BICMOS, ect.). Where testing is required, the limit for neutron fluence shall be 2×10^{12} neutrons/cm^2.

3/ Per wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

4/ Per inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

5/ Class level B devices shall be inspected using either the class level B quantity/accept number criteria as specified, or by using the class level S criteria on each wafer.

6/ Per wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.

7/ Per inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

8/ Per wafer for device types with greater than 4,000 equivalent transistor/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

(3) The verifying party shall stamp or sign the lot traveler to attest that the above data meets the test requirements and that all of the above items were performed and were found to be acceptable.

(4) Failure of the verification test shall require, as a minimum, engineering to perform a detailed review of hardware/software/set up and parts. If engineering locates the problem, a one time only 100 percent retest to all group A requirements for all devices that were under consideration for acceptance shall be required. If the engineering review does not locate the problem, the verification unit shall undergo failure analysis before retesting the lot.

(a) If failure analysis locates the problem, the entire group of devices being considered for acceptance at the time of the failure may be retested for appropriate subgroup(s) acceptance one time only by repeating this group A method.

(b) If the failure analysis does not specifically locate the problem, the lot may be considered for acceptance one time only by 100 percent retesting of all the devices of the group A requirements and by repeating this group A method.

3.6 Disposition of samples. Disposition of sample devices in groups A, B, C, D, and E testing shall be in accordance with the applicable device specification.

3.7 Substitution of test methods and sequence.

* 3.7.1 Accelerated qualification or quality conformance testing for class level B. When the accelerated temperature/time test conditions of condition F of method 1005 are used for any operating life or steady-state reverse bias subgroups on a given sample for purposes of qualification or quality conformance inspection, the accelerated temperature/time test conditions shall be used for all those named subgroups. When these accelerated test conditions are used for burn-in screening test (test condition F of method 1015) or stabilization bake for devices with aluminum/gold metallurgical systems (any test temperature above the specified maximum rated junction temperature) for any inspection lot, it shall be mandatory that they also be used for the operating life, and steady-state reverse bias tests of method 5005, or herein as applicable, or qualification or quality conformance inspection. Qualification and quality conformance inspection may be performed using accelerated conditions on inspection lots that have been screened using normal test conditions.

* 3.8 Test results. Unless otherwise specified, test results that are required by the applicable acquisition document shall be reported in accordance with the general requirements of appendix A of MIL-PRF-38535 (see 40.7).

4. SUMMARY. The following details shall be specified in the applicable device specification:

a. Procedure paragraph if other than 3.1, and device class.

b. Sequence of test, sample size, test method, and test condition where not specified, or if other than specified.

c. Test condition, limit, cycles, temperatures, axis, etc., where not specified, or if other than specified (see 3).

* d. Acceptance procedure or sample size and acceptance number, if other than specified.

e. Initial and interim (pre and post burn-in) electrical parameters for group A.

f. Electrical parameters for groups B, C, D, and E end point measurements, where applicable.

g. Burn-in test conditions (see table III) and burn-in test circuit.

h. Delta parameter measurements or provisions for PDA including procedures for traceability or provisions for pattern failure limits including accountable parameters, test conditions, and procedures for traceability, where applicable.

i. Final electrical measurements.

j. Constant acceleration level.

k. Requirements for failure analysis.

l. Requirements for data recording and reporting if other than specified in 3.8.

m. Restriction or resubmission of failed lots where applicable.

n. Steady-state life test circuits, where not specified or if other than specified.

o. Parameters on which delta measurements are required.

p. Wafer travelers shall be used to record completion of each requirement of 3.4.2.1.1.

APPENDIX I

COMPUTER AIDED DESIGN (CAD)
CERTIFICATION REQUIREMENTS

10. SCOPE.

10.1 Scope. Additional line certification requirements. This appendix defines additional line certification requirements. The answers to the questions in this appendix shall be provided to the qualifying activity for approval. The manufacturer shall have the following additional information on file and available for review.

a. Design/layout rules as a manufacturer's controlled document.

b. A list of the cells in the manufacturer's cell library, cell performance data, and simulation verification data, if applicable.

c. Process monitor design used by the manufacturer.

d. Standard evaluation circuit implementation used by the manufacturer for qualification and qualification conformance inspection (QCI).

e. JEDEC benchmark macro set (see JEDEC standards 12, 12-1, 12-2, and 12-3), delay simulation data, if applicable.

f. A list of the software packages (including names and current version) used by the manufacturer in the circuit design process.

g. Design rule check (DRC) verification. DRC software shall be run on a design which contains known design rule violations.

h. Electrical rule check (ERC) verification. ERC software shall be run on a design which contains known electrical rule violations.

i. Layout versus schematic (LVS) checker.

j. If the manufacturer's design methodology is based on the "correct by construction" approach, distinct DRC, ERC, and LVS software is unnecessary and may not exist. In this case, the provisions of g., h., and i. do not apply. Instead, the manufacturer will provide suitable example data to demonstrate the correct performance of "correct by construction" software.

10.2 Functional delay simulation. To be retained by manufacturer; simulation to be derived from each final application specific electrical design and layout (i.e., post-routed design). Simulation will be done using actual delays and parasitics computed from the placement and layout of the device as it will be fabricated. Actual delays shall include the contribution associated with the delay through the gate, as well as the contribution due to actual metal capacitance and device loading on the output(s). Using these actual delays, the application specific integrated circuit (ASIC) designer shall insure that there are no timing violations remaining in the circuit. Such timing violations shall include, but not be limited to, setup, hold, critical delay path, and circuit race conditions due to variations in process, temperature and supply voltage. Simulation at the two worst case extremes (temperature, process, radiation (if applicable) and supply voltage) shall be identical with respect to circuit operation (final state of each signal in each clock cycle must be identical).

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10.3 Layout verification. The manufacturer shall retain the results of full mask level design rule checks, electrical rule checks, and connectivity checks (see 10.1) for each application specific design. Rule checking will encompass the rules set provided under 10.1 herein. The manufacturer will explain any rules not checked and all error reports produced by the checker. The LVS checker will ensure that the layout matches exactly the schematic simulated by the ASIC designer. Final layout verification results will not be required if the manufacturer's design methodology is "correct by construction." In this case, the manufacturer will explain the methodology and rules used, as well as any rules not checked and all error reports which were not corrected during construction of design.

10.4 Power routing simulation. To be retained by manufacturer; derived from each final application specific electrical design and layout. The worst case simulation of power buses shall show that at no time shall the localized bus current density exceed specification for allowable current density of the power bus material. In addition, at no point in the power bus shall voltage levels exceed design goals for IR drop values from the respective supply. Power routing simulation must be based upon actual placement of cells within the array. Such a simulation may be driven by Monte Carlo methods, or in conjunction with a digital simulator using the selected set of test vectors.

10.5 Cell design and simulation qualification. Cell design and simulation qualification shall be accomplished in a two step procedure consisting of:

a. Parameter verification/simulation verification, and

b. Functional verification.

A chip or set of chips, called the cell test chip set, shall be designed to provide access to a set of cells to test performance characteristics. The cell test chip set design must be submitted to the qualifying activity for approval prior to use. The cell test chip shall include as a minimum:

Description

Inverter

4-input NAND

2-input AND into 3-input NOR

D latch with active low reset

JK flip-flop with active low reset

TTL input buffer

CMOS input buffer

Output buffer

Three-state I/O buffer with pull-up

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The intent is to get a representative cross section of cell types (i.e., combinational, sequential, input, output). Chains shall be formed (when necessary to avoid rise and fall time measurement problems) and actual performance data over the full operating range shall be taken (a provision to extract for multiplexing and I/O buffer delay shall be included). Delay versus metal wire length and fanout for the above cells shall be determined. The actual performance data shall be submitted to the qualifying activity along with computer program simulation results. The actual performance data must be within the limits predicted by the simulation. If multipliers are used to extrapolate performance at the temperature extremes, such multipliers shall be verified as well.

In addition, for the above cells, a set of pins shall be provided on the test chip for observability. This will enable verification of functionality of the cells. (Note: Inputs and outputs may be multiplexed).

10.6 CAD routing and post routing simulation. A chip or set of chips shall be submitted for approval and used to qualify the manufacturer's ability to perform routing and to accurately predict post routing performance. The manufacturer must submit to the qualifying activity:

a. The actual measured performance data for each function over temperature and voltage.

b. The computer simulation performance prediction.

The two results will remain on file and the actual measured performances must fall between the simulation extremes.

20. APPLICABLE DOCUMENTS (This section is not applicable to this document.)

30. CERTIFICATION QUESTIONS

30.1 Cell libraries.

a. Who is the source for your cell libraries?

Own organization?

Work station vendors?

Outside commercial vendors?

Universities?

b. What verification or certification is done for cell libraries, including those obtained from outside organizations? Are macrocells implemented in silicon and verified for functionality and performance limits via actual hardware test? Is only software simulation performed?

c. How are cell libraries controlled (e.g., level of documentation, maintenance and revisions, specifications, additions)?

d. Provide company-approved cell library.

e. Identify those implemented and tested in silicon.

f. Is a designer allowed to tailor a macrocell or "roll his own" for a certain application? If so, how is the resulting macro tested to insure there are no problems?

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30.2 Design process.

a. Who does and who approves the various levels of design?

Requirements definition? Detail function definition? Detail design (e.g., gate level design)? Layout and mask generation?

b. What automatic aids are used for refinement from each design level to the next?

c. What automatic aids are used for verifying the refinement at each level (e.g., automatic checking of layout versus schematic)?

d. How is automatic placement and routing software verified and certified for use?

30.3 Simulation.

a. What simulators are used for:

Process simulation (e.g., SUPREME-II)?

Circuit simulation (e.g., SPICE, SCEPTRE)?

Gate level simulation (e.g., LASAR HITS)?

Switch level simulation?

Behavior/function simulation?

Dynamic timing analysis (to include actual delays due to placement and routing?

b. How are the above simulators verified? Are benchmarks used, and if so, what are these benchmarks?

c. Are the simulation results periodically checked against actual silicon test data (to complete the loop)?

30.4. Test.

a. What test tools are used for:

Automatic test vector generation?

Fault simulation?

Insertion of design-for-testability/built-in-test features? (And are they integrated with the design process?)

b. Who is responsible for test generation:

Foundry?

Customer?

Designer?

c. If test vectors are not generated by the foundry, are the submitted vectors evaluated by the foundry to determine the percentage of faults detected?

30.5. Design rule checking.

a. Are design constraints enforced by the customers or management, such as:

Synchronous designs only?

Use of an approved set of cells/macrocells only?

Conservative use of electrical and switching limits?

Is the designer able to obtain waivers?

b. What design rule checkers (DRCs) are used for:

Physical rule checks (e.g., minimum spacing)?

Electrical rule checks (e.g., max current density, fanout restrictions)? Timing rule checks (e.g., worst-case timing paths)? Logical rule checks (e.g., unclocked feedback paths)?

c. Is each design subjected to the above DRCs?

d. How can the DRC software be shown to "work as advertised?"

e. If "correct by construction" techniques are used, what procedure is used, how is "correctness" assured?

30.6. Software control.

a. What are the sources of design and test software?

Own organization?

Workstation vendors?

Outside commercial vendors?

Universities?

b. How is design and test software approved and controlled:

Frequency of major/minor revision?

Trouble reports?

Regression testing?

c. What commercial CAD/CAE work stations or packages are used (e.g., MENTOR, Daisy, Silvar-Lisco)? Are modifications to any of the software packages permitted?

30.7. How is interface with foundries and customers, or both done?

Data formats?

Media (e.g., magtapes, modems, DDN/Arpanet)?

Qualification of foundry via test chips?

Are evaluation chips available for customers to assess performance?

30.8. Who tests the chips?

At wafer level?

After packaging?

Burn-in?

Life testing?

What automatic test equipment types are used?

30.9. Masks.

a. What are the procedures for mask making, inspection, verification, and repair?

b. Is the design transferred to the fab house via an actual mask set or via software?

c. If design transfer is via software, what are the procedures used to verify the mask design?

30.10. Wafer acceptance.

a. What wafer inspection/accept-reject criteria are currently used (i.e., how is process control/stability demonstrated)?

b. Which of the following process control indicators are used?

Kerf test structure measurements? (What structures are in the kerf; how many kerf sites are measured; what data are taken; tolerances allowed?)

Drop-ins: (What does the drop-in design consist of? How many drop-ins per wafer? Allowed parameter tolerances?)

Visual test structures?

c. How is high magnification inspection being accomplished? Are voltage stress tests used in lieu of some of the high mag inspections?

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30.11. Reliability evaluation.

a. How is the reliability of the process proven? It is done via:

Standard evaluation chips (SECs) or reliability evaluation chips?

Test dice with specialized/optimized test structures?

b. If such vehicles do not exist, how is the processing shown to be free of reliability hazards?

c. How can the power buses be guaranteed to be within current density specifications at all times and under all conditions?

d. For CMOS technology, how is a latch-up free process assured?

e. For bipolar technology, is any radiation hardness characterization done?

30.12. Documentation.

a. What are the procedures for certifying and controlling the configuration of software?

b. What are the procedures outlining in detail the process flows for computer-aided design/manufacture/engineering/test (CAD/M/E/T)?

c. If neither of above is available, when will they be available?

APPENDIX II

WAFER LOT ACCEPTANCE

10. SCOPE

* 10.1 Scope. This appendix establishes the requirement for wafer lot acceptance of microcircuit wafers intended for class level B and level S use. The performance of each wafer shall be evaluated individually and independently of the performance of other wafers in the lot. This wafer lot acceptance procedure is based on fabrication specification adherence (in accordance with appendix A of MIL-PRF-38535 and the manufacturer's documented fabrication procedures), physical testing, and electrical testing of suitable process monitors (PM's).

This method can be used only on a fabrication line that has Appendix A of MIL-PRF-38535 certification or control and has successfully instituted the required checks. Wafers failing any process specification (with the exception of acceptable rework instances) shall be removed from further processing.

This method is restricted to a well characterized and baselined process. By characterized, it is meant that a fabrication line has been adequately described in relation to the capabilities of the process. Baselined refers to the existence of a well defined process parameter target value with associated variances (based on characterization data) against which the actual wafer to wafer process data is measured to determine acceptability.

A collection of test structures which can provide the parametric data as well as additional yield indicators is referred to as a "process monitor" (PM). A statistically valid number of PM's shall be provided on each wafer. The PM may be either stepped onto every wafer in dedicated drop-in die locations, incorporated into kerf locations, or located on each die, such that they can be probed at the conclusion of processing up to and including final metallization and passivation (glassivation). Table I presents a minimum listing of structures which make up a PM. The manufacturer shall see PM parametric limits as called for by design rules and process rules, or both. Probe pads shall be designed to conform to the 2 x N (NIST) dimensions.

20. APPLICABLE DOCUMENTS. (This section is not applicable to this document.)

30. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

40. PROCEDURE. There are three phases to wafer acceptance:

a. Processing to the manufacturer's fabrication baseline and documented fabrication procedures.

b. Visual/SEM inspection.

c. PM evaluation.

* Wafers failing any test (with the exception of acceptable rework instances in accordance with appendix A of MIL-PRF-38535) shall be removed from the lot.

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TABLE I. Minimum suggested set of structures used in a PM. 1/

N-channel transistors for measuring threshold voltages (minimum and maximum geometries)
P-channel transistors for measuring threshold voltages (minimum and maximum geometries)
Field threshold device(s)
Leakage current structures
Sheet resistance measurement structures
N-channel gain structures (KN)
P-channel gain structures (Kp)
Oxide breakdown structures (gates, intermetal, and field)
Contact chains (to be sufficient length to allow accurate measurement of the contact resistance typically found on a device, with diagnostic procedures to isolate failures)
Metal to poly
Metal 1 to metal 2 via resistance (where applicable)
Metal to diffusion
SEM step coverage checking structures for metal step coverage analysis
Alignment verniers
Functional circuits (e.g., ring oscillator, delay chains, etc.

1/ Appropriate structures for other technologies shall be developed.

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40.1 Processing. Table II presents a minimum checkpoint list for wafer processing. If certain parameter values are proprietary, they may be presented in normalized or other specialized form.

TABLE II. In-process check points.

Process step	Inspection
Incoming material inspection	Water, wafers, chemicals, gasses
Photolithography	Spin speed, thickness, critical dimension measurements, alignment, post development visual inspection (100X)
Oxidation	Index of refraction, flatband, and threshold voltage shifts, thicknesses
Diffusion	Resistivity
Ion implant	Resistivity, range, species
Deposition	Thickness, resistivity, index of refraction
Etching	Critical dimension measurements, etch rates, end point detection
SEM	Step coverage (all metallization layers)

40.2 Visual/SEM inspection. Visual inspection of photo resist (PR) patterns, alignment verniers, and critical dimension measurements shall be made after each PR develop/bake operation. Following every etch and every ion implant, PR mask stripped wafers shall be inspected for proper PR removal, damage, or other defects, and defective wafers removed from the lot for scrap or for rework.

In-line nondestructive SEM inspection in accordance with MIL-STD-883, method 2018, shall be performed on each wafer lot. One wafer from each metallization level shall be randomly selected for inspection. SEM inspection for each level may be reduced to a weekly basis for each fabrication process when five consecutive lots pass inspection for the given level. If a metallization level fails the weekly inspection, then lot by lot inspection shall be required until five consecutive lots again pass. Wafers failing to meet the requirements of the test method shall be removed from processing. Wafer lot acceptance shall be in accordance with table IV herein.

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40.3 PM evaluation. PM structures shall be submitted for approval. Wafer acceptance will be made on a wafer by wafer basis depending upon the information derived from PM room temperature testing in accordance with table III. If drop-in PM's are utilized, each wafer shall have at least 5 PM's; one shall be stepped in the center and the others in each of the quadrants. For kerf PM's and PM's on individual die, the five probed PM's shall be located in the center and in each of the quadrants. Quadrant PM's shall lie at least two-thirds of a radius away from the wafer center. Wafer acceptance will be governed by table III.

TABLE III. PM evaluation.

PM type	Number within PM specification limits	Less than 3 out of 5
Drop-in		Reject
Kerf		Reject
Each die		Reject

40.4 Lot acceptance. Acceptance requirements are as defined in table IV.

TABLE IV. Wafer lot acceptance requirements.

Requirement	Condition	Acceptance
Line certified	MIL-PRF-38535 Appendix A	Control to specification
Lot traveler check points	MIL-PRF-38535 Appendix A	100 percent in specification for lot acceptance
PM test data	Every wafer	75 percent of wafers in lot pass PM evaluation, otherwise reject.
Visual inspection	Every wafer	Wafer by wafer
SEM inspection	MIL-STD-883 Method 2018	Method 2018 criteria

APPENDIX II

* 40.5 Test results. When required by the applicable document, the following test results shall be made available for each lot submitted for qualification or quality conformance.

a. Results of each test conducted; initial and any resubmission.

b. Number of wafers rejected.

c. Failure analysis data and failure mode of each rejected SEC and the associated mechanism for catastrophic failures for each rejected device.

d. Number of reworked wafers and reason for rework.

e. Read and record data of PM electric parameter measurements.

40.6 Defective devices. All wafers that fail any test criteria shall be removed at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a failure, no wafer may be retested for acceptance.

METHOD 5011.4

EVALUATION AND ACCEPTANCE PROCEDURES FOR POLYMERIC MATERIALS

1. Purpose. This method establishes the minimum inspection procedures and acceptance criteria for polymeric materials used in microcircuit applications. These materials shall be classified in two types as follows:

a. Type I being electrically conductive.

b. Type II being electrically insulative.

1.1 The user may elect to supplement Quality Conformance Inspection (QCI) test data or Qualification Testing data as a substitute where applicable for user Certification Testing.

2. Apparatus. Suitable measurement equipment necessary to determine compliance with the requirements of the applicable acquisition document and other apparatus as required in the referenced test methods.

3. Procedures.

3.1 Material acquisition specification. The microcircuit manufacturer shall prepare an acquisition specification describing the detailed electrical, mechanical, chemical, and thermal requirements for the polymeric material to be acquired. The requirements shall not be less than those imposed by this method, but may be increased to reflect the specific parameters of a particular material or the requirements of a particular application.

3.2 Certificate of compliance. The material supplier shall provide upon the users request a certificate of compliance for each polymeric material order. This certificate shall contain the actual test data for the supplier's testing as prescribed in this document.

3.3 Evaluation procedures. Evaluation procedures for polymeric materials shall be performed as specified in 3.4.1 through 3.5.13 for the type of material being tested.

3.4 Properties of uncured materials.

3.4.1 Materials. The components of a polymeric material and/or system shall be examined in accordance with table I and 3.8.1 and shall be uniform in consistency and free of lumps or foreign matter when examined in film, liquid or other acceptable form. Any filler shall remain uniformly dispersed and suspended during the required pot life (see 3.8.3). The electrically conductive fillers used in type I materials shall be gold, silver, alloys of gold or silver, or other precious metals.

3.4.1.1 Encapsulating compounds Encapsulating compounds are liquidous material and are to be tested in accordance with the requirements in Table I.

3.4.1.2 Molding compounds. Molding compounds as used in microelectronic devices are normally solidous material and are to be tested in accordance with MIL-PRF-38535, Appendix H Tables H-IB and H-IIB.

3.4.2 Viscosity. The viscosity of paste materials shall be determined in accordance with 3.8.2. The viscosity, including an acceptable range, shall be specified in the material acquisition document.

3.4.3 Pot life. The pot life when required shall be determined in accordance with 3.8.3 and shall be a minimum of 1 hour. The polymeric material shall be used within the pot life period after removal from the container, after mixing, or after thawing to room temperature in the case of premixed frozen polymers.

3.4.4 Shelf life. The shelf life, defined as the time that the polymeric material continues to meet the requirements of this specification shall be determined in accordance with 3.8.4. This shelf life shall be a minimum of 12 months at -40°C or below for one component system and a minimum of 12 months at room temperature (32°C maximum) for two component systems unless the supplier certifies for some other period of time. For class K devices, no polymeric material shall be used after the expiration date. Materials in class H devices may be requalified once, with acquiring activity and qualifying activity approval. Encapsulants shall have a minimum shelf life of 6 months.

TABLE I. Requirements.

Test or condition	Test method paragraph	Adhesive	α-Absorbers	Film 6/ dielectrics	Particle getters	Desiccants	Junction coatings	T-Wave absorbers	Encap-sulating compound
Materials (3.4.1)	3.8.1	4/	4/	4/	4/	4/	4/	4/	4/
Viscosity (3.4.2)	3.8.2	1/,2/	1/,2/	1/,2/	—	—	—	—	1/
Pot life (3.4.3)	3.8.3	1/,2/	1/,2/	1/,2/	—	—	—	—	—
Shelf life (3.4.4)	3.8.4	1/	1/	1/	1/	1/	1/	—	1/
Thermogravimetric analysis (3.5.2)	3.8.5	1/,2/	1/,2/	1/	1/,2/	1/,2/	1/,2/	—	1/
Outgassed materials (3.5.3)	3.8.6	3/	3/	3/	3/	3/	3/	3/	—
Ionic impurities (3.5.4)	3.8.7	1/2/	1/,2/	1/	1/	1/,2/	1/	—	1/,2/
Bond strength (3.5.5)	3.8.8	1/,5/	1/	—	—	—	—	—	1/,2/
Coefficient of linear thermal expansion (3.5.6)	3.8.9	1/	—	—	—	—	—	—	1/
Thermal conductivity (3.5.7)	3.8.10	1/	—	—	—	—	—	—	1/
Volume resistivity (3.5.8)	3.8.11	1/	—	—	—	—	—	—	1/
Type I materials		1/,5/	—	—	—	—	—	—	—
Type II materials		1/	1/,2/	1/,2/	—	—	1/,2/	—	1/
Dielectric constant (3.5.9)	3.8.12	1/	—	1/	—	—	—	—	1/
Dissipation factor (3.5.10)	3.8.13	1/	—	1/	—	—	—	—	1/
Sequential test environment (see 3.5.11)	3.8.14	3/	3/	3/	—	3/	3/	—	—
Density (3.5.12)	3.8.15	—	—	—	—	—	—	1/,4/	—
Mechanical integrity (see 3.5.13)	3.8.16	—	—	—	3/	—	—	—	—
Operating life test (see 3.5.14)	3.8.17	—	—	—	3/	3/	—	—	3/

1/ Responsibility of the supplier at certification.
2/ Responsibility of the supplier at acceptance.
3/ Responsibility of the user at certification.
4/ Responsibility of the user and supplier at certification and acceptance.
5/ Responsibility of the supplier at acceptance. Required at 25°C test condition only (no high temperature storage required).
6/ Film dielectrics are defined as polymeric materials that are used in film form to act as either interlayer dielectrics, passivation layers, and/or circuit support films.

3.5 Properties of cured polymer materials.

3.5.1 Curing of polymer materials. The material must be capable of meeting the requirements of this document when cured according to the supplier's instructions. The cure schedule for supplier tests shall be identical for all tests and shall be reported. The cure schedule for the user tests shall be the minimum cure schedule plus, as a minimum, the pre-seal bake specified in the user's assembly document and shall be reported. Deviation from the suppliers recommended cure schedule will require verification by the user of the materials performance.

3.5.2 Thermogravimetric analysis (TGA).

3.5.2.1 Thermal stability. The thermal stability of the cured material shall be determined in accordance with 3.8.5. Unless otherwise noted, the weight loss at 200°C shall be less than or equal to 1.0 percent of the cured material weight. Equivalent standard, i.e., "classical analytical techniques" are acceptable.

3.5.2.2 Filler content. Polymeric materials using a filler to promote properties such as electrical and thermal conductivity shall be tested in accordance with 3.8.5 to determine the inorganic filler content. For acceptance testing, the percent filler content shall not differ from the filler content in the certified materials by more than ±2 percent.

3.5.3 Outgassed materials. Outgassing of the cured material shall be determined in accordance with 3.8.6. Outgassed moisture, as determined in 3.8.6.1, shall be less than or equal to 5,000 ppmv (0.5 percent V/V) for 3 packages (0 failures) or 5 packages (1 failure). Other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V. The data obtained in 3.8.6.2 shall also be reported in the same manner but for information only. The outgassing of the cured getter shall be determined in accordance with 3.8.6. The vapor content of the package with getter shall not exceed 2000 ppmv after 24 hours at 150°C and 3000 ppmv after 1000 hours at 150°C.

3.5.4 Ionic impurities. The ionic impurity content shall be determined in accordance with 3.8.7 and shall meet the requirements specified in table II. Ionic content analysis shall be in triplicate for certification and single analysis for acceptance testing. Failure at acceptance shall require the passing of two additional samples.

TABLE II. Ionic impurity requirements.

Total ionic content specific electrical conductance)	≤ 4.50 millisiemens/meter
Hydrogen (pH)	4.0 ≤ pH ≤ 9.0
Chloride	≤ 200 ppm
Sodium	≤ 50 ppm
Potassium	≤ 50 ppm
Flouride	≤ 50 ppm

Other ions present in quantities > 5 ppm shall be reported in ppm.

3.5.5 Bond strength. The bond strength of a polymeric material shall be determined in accordance with 3.8.8 at 25°C, and 25°C after 1,000 hours at 150°C. The bond strength shall meet as a minimum the 1.0X requirement specified in figure 2019-4 of method 2019 of MIL-STD-883 at each test condition. The manufacturer should test to shear or until twice the minimum 1.0X shear force is reached.

3.5.6 Coefficient of linear thermal expansion. The coefficient of linear thermal expansion shall be determined from -65°C to 150°C in accordance with 3.8.9. The coefficient of linear thermal expansion shall be ±10% of the value required in the users material specification or purchase order. This requirement shall apply to the material as it is configured for actual use. This requirement shall not apply to glass supported polymeric films.

3.5.7 Thermal conductivity. The thermal conductivity shall be determined at 121°C ±5°C in accordance with 3.8.10. The thermal conductivity shall be greater than or equal to 1.5 watt/meter-K for type I polymers and greater than or equal to .15 watt/meter-K for type II polymers.

3.5.8 Volume resistivity. The volume resistivity shall be determined in accordance with 3.8.11. The volume resistivity of conductive materials at 25°C, at 60°C, at 150°C, and at 25°C after 1,000 hours at 150°C shall be less than or equal to 5.0 microhm-meter for silver-filled polymers and less than or equal to 15.0 microhm-meter for gold-filled polymers. The volume resistivity of insulative materials shall be greater than or equal to 0.1 teraohm-meter at 25°C and greater than or equal to 1.0 megohm-meter at 125°C.

3.5.9 Dielectric constant. The dielectric constant of insulative polymeric materials shall be determined in accordance with 3.8.12 and shall be less than or equal to 6.0 at both 1 kHz and 1 MHz for this type of polymer but shall be less than or equal to 3.5 at 1 kHz and 1 MHz for materials used for dielectric layers.

3.5.10 Dissipation factor. The dissipation factor of insulative polymers shall be determined in accordance with 3.8.13 and shall be less than or equal to 0.03 at 1 kHz and less than or equal to 0.05 at 1 MHz.

3.5.11 Sequential test environment. The polymeric material shall withstand exposure to the test conditions specified in 3.8.14. After exposure to the complete sequence of environmental conditions, the test specimens shall show no evidence of mechanical degradation. For adhesives the measured bond strength of components shall meet as a minimum the 1.0X requirement specified on figure 2019-4 of method 2019 of MIL-STD-883.

3.5.12 Density. The density of microwave or RF absorbing materials shall be tested in accordance with 3.8.15. The acceptable value shall be that which is within ±10% of the value required on the user's material specification or purchase order.

3.5.13 Mechanical integrity. Particle getter integrity shall be verified after different levels of environmental stress.

3.5.13.1 Getter integrity (short term). When tested in accordance with 3.8.14.1 all samples shall pass the criteria for PIND as defined in MIL-STD-883 method 2020.

3.5.13.2 Getter integrity (long term). When tested in accordance with 3.8.14.2 all samples shall pass the criteria for PIND as defined in MIL-STD-883, method 2020, both initially and after storage at 150°C for 1,000 hours. The salted particles shall remain attached to the getter material in the original position with no attachment and reattachment when viewed at 30X to 60X magnification.

3.5.13.3 Getter integrity (vibration). When tested in accordance with 3.8.14.3 the sample shall pass PIND as defined in MIL-STD-883, method 2020, the salted particles shall remain attached to the getter material in the original position, with no detachment and re-attachment when viewed at 30X to 60X.

3.5.14 Operating life. When tested in accordance with 3.8.15, the comparison between initial and post test electrical data shall not indicate parametric shifts, which are unique to the test group containing getter material.

3.6 Responsibility for testing. The manufacturer and user are responsible for the performance of all tests as specified in table I herein.

NOTE: The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

3.6.1 Test equipment and testing facilities. Test and measuring equipment and testing facilities of sufficient accuracy, quality and quantity to permit performance of the required testing shall be established and maintained by the manufacturer and user. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with ANSI/NCSL Z540-1 or equivalent. The supplier and user may utilize a commercial laboratory acceptable to the qualifying activity for performing the required certification and acceptance testing.

3.6.2 Testing conditions. Unless otherwise specified herein, all testing shall be performed in accordance with the test conditions specified in the "general requirements" of the MIL-STD-883.

3.7 Classification of testing. The test requirements specified herein are classified as certification testing and acceptance testing.

3.7.1 Certification testing. Certification testing shall be performed on the initial lot of material and for any major changes to the material thereafter and consist of all tests to determine conformance with all requirements specified herein. To insure that both the polymeric material and the processes employing the material are controlled, both the supplier and the user of the material shall be responsible for performance of the tests as designated in table I.

3.7.1.1 Sample size. The number of samples to be subjected to each testing procedure shall be as specified in the individual test methods.

3.7.1.2 Failures. Failure of any polymeric material to meet the testing requirements shall be cause for refusal to grant certification approval.

3.7.1.3 Retention of data. The data generated for certification shall be retained for a period of 5 years or until a recertification is performed, whichever is greater.

3.7.2 Acceptance testing. Acceptance tests shall be performed on each lot and shall consist of tests as specified in table I.

3.7.2.1 Test lot. A test lot shall consist of all polymeric material manufactured under the same batch number, i.e., a batch number identifies those materials whose constituents can be traced to a single lot of raw materials.

3.7.2.2 Sample size. The number of samples to be subjected to each testing procedure shall be as specified in the individual test methods.

3.7.2.3 Failures. Failure of the samples to meet the testing requirements of a specific test shall be cause for rejection of the lot.

3.7.2.4 Retention of data. The data generated for acceptance testing shall be retained for a period of 5 years.

3.8 Methods of examination and test. The following test criteria and analytical protocols shall be documented and approved by the qualifying activity prior to material certification.

3.8.1 Materials. The polymeric components or system or both shall be examined visually at a minimum magnification of 30X to ensure conformance with the requirements of 3.4.1.

3.8.2 Viscosity. The material user and supplier shall define a mutually acceptable method for verifying the viscosity of fluid or paste materials. The supplier shall use the same method in performing the required certification and acceptance testing.

3.8.3 Pot life. The parameters to be used in the measurement of pot life (e.g., viscosity change, skin-over, loss of bond strength, etc.) are generally material dependent. The material supplier and user shall select the procedure to be used in establishing and testing the pot life.

3.8.4 Shelf life. Where applicable, an unopened container of material shall be stored under the condition specified in 3.4.4. As a minimum, the test methods and requirements specified in table III shall be used to establish the shelf life.

TABLE III. Shelf Life Determination.

Property	Requirement	Test method	Application/condition
Materials	3.4.1	3.8.1	All polymeric materials
Pot life	3.4.3	3.8.3	Adhesives; α Absorbers; Junction coatings; Dielectrics
Bond strength	3.5.5	3.8.8	Adhesives; α Absorbers; Junction coatings; 25°C only
Volume resistivity 1/	3.5.8	3.8.11	Adhesives, type I, 25°C only

1/ To be determined for materials where electrical conductivity is a design parameter.

3.8.5 Thermogravimetric analysis (TGA). The thermal stability of the polymeric system and it's filler content (if any) shall be determined by testing samples of the cured system (see 3.5.1) in nitrogen using suitable TGA equipment or in accordance with ASTM D3850. Single point analyses are acceptable, however if the first sample fails, then two additional analyses must be performed. The average value of the three samples must then meet or exceed the minimum requirements.

3.8.5.1 Thermal stability. The thermal stability of the polymeric material shall be determined by heating the specimens from room temperature to not less than 210°C, at a heating rate between 10°C/minute and 20°C/minute, in a nitrogen atmosphere with 20-30 milliliter/minute nitrogen flow. The weight loss at 200°C shall be determined.

3.8.5.2 Filler content. The filler content of polymeric materials using a filler to promote properties such as electrical or thermal conductivity shall be determined by heating the specimen from room temperature to 600°C, at a heating rate between 10°C/minute and 20°C/minute, in an air atmosphere with 20-30 milliliter/minute air flow. The temperature shall be maintained at 600°C until constant weight is obtained. It is permitted to perform 3.8.5.1, followed by heating from 210°C to 600°C as detailed above. The filler content shall be reported as weight percent of the cured specimen.

3.8.6 Outgassed materials. Ten test specimens shall be prepared using gold- or nickel-plated Kovar or ceramic packages, (dielectric materials may be prepared using aluminum coated silicon as the substrate). (The use of "leadless" packages is permitted to reduce moisture contributions due to package construction). The material shall be cured using the minimum cure schedule and shall receive the minimum pre-seal bake specified in the assembly document(s) (see 3.5.1). After a pre-seal bake, the packages shall be hermetically sealed. Only those packages that meet the fine and gross leak test requirements of test method 1014 shall be submitted for moisture content analysis. If less than 10 test specimens remain after hermetically testing, the failed packages shall be replaced by additional hermetical packages processed and tested in the same manner as the original group.

3.8.6.1 Testing for short term outgassing of moisture and other gaseous species. Five packages containing polymer prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008, 24 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V.

All polymeric materials tested shall have quantities of material equivalent in mass and exposed surface area to that of the intended application. Gold plated Kovar tabs and alumina blanks may be used as facsimile device elements. Several polymeric materials of different application may be tested in combination with each other in this test, however their combined moisture content shall not exceed 5,000 ppmv.

3.8.6.2 Testing for long term outgassing of moisture and other gaseous species. Provided that the moisture requirement of 3.5.3 has been met by packages tested in 3.8.6.1, the remaining five devices containing polymer from the group prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008 for 1,000 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V.

3.8.7 Ionic impurities. A water-extract analysis shall be performed to determine the level of ionic contamination in the cured polymeric material. The total ion content (specific electrical conductance) and the specific ionic content for the hydrogen (pH), chloride, sodium, fluoride and potassium ions shall be measured. Other ions present in quantities > 5 ppm shall also be reported in ppm. The methods of analysis submitted in the following paragraphs are suggested techniques. Alternate methods of analysis may be selected where it can be shown that the techniques are equivalent and the method of analysis is approved by the qualifying activity.

3.8.7.1 Sample preparation. Adequate material shall be cured to obtain 3 gram samples of polymer following grinding, for final preparation. The material shall be cured on teflon or other inert surface in a forced draft oven. When possible the cured specimen shall be removed from the curing substrate and ground to 60-100 mesh particles; polymeric film samples less than or equal to 0.025 cm thick shall be cured and cut into less than or equal to 0.25 cm^2 samples; gels or low modulus materials may be cast directly into the flat bottom of the sample flask for the extraction. Smaller sample sizes may be selected where it can be shown that the accuracy of the test method has not changed.

3.8.7.2 Extraction procedure. 3 grams (equivalent resin) of the ground or cut equivalent polymer shall be added to a cleaned; tarred, 250-ml flasks made of pyrex, or equivalent. The weight of the cured material in each flask shall be recorded to the nearest milligram. 150.0 grams of deionized water with a measured specific conductance less than or equal to 0.1 millisiemens/meter (specific resistivity greater than or equal to 1.0 megohm-centimeter) shall be added to the flask. A blank shall be prepared by adding 150.0 grams of the deionized water and a boiling chip to a second 250-ml flask. The flasks shall be refluxed for 20 hours.

NOTE: 1.0 mho = 1.0 siemens; 1.0 mho/cm = 100.0 siemens/meter.

3.8.7.3 Measurement of ionic content.

3.8.7.3.1 Total ionic content. The total extractable ionic content shall be determined by measuring the specific electrical conductance of the water-extract samples and the blank using a conductivity meter with an immersion conductivity cell having a cell constant of 0.01/centimeter (alternatively 0.1 cm^{-1} to adjust for proper analysis of the solution). The total ionic content, in millisiemens/meter, shall be obtained by subtracting the specific conductance of the blank from the specific conductance of the samples.

3.8.7.3.2 Hydrogen ion content (pH). The pH of the water extract shall be determined using a pH meter with a standard combination electrode.

3.8.7.3.3 Specific ion analysis. Specific ion analysis of the water extract shall be conducted using ion chromatography or a demonstrated equivalent. The ion concentrations in the extract shall be converted to the sample extractable concentrations by multiplying the ratio of the deionized water weight (W) to polymer sample weight (S); that is, by (W/S). The chloride, sodium, fluoride and potassium ion levels and all other ions detected in quantities > 5 ppm shall be reported in ppm.

3.8.8 Bond strength. The bond strength of the polymeric material shall be determined in accordance with 3.8.8.1, 3.8.8.2 or 3.8.8.3 below. As a minimum, five elements shall be tested to failure at the following conditions:

a. At 25°C.

b. At 25°C after 1,000 hours at 150°C in an air or nitrogen ambient.

The average bond strength at each test condition shall be determined in kilograms (force).

3.8.8.1 Bond strength. The bond strength shall be determined in accordance with method 2019 of MIL-STD-883. A gold-metallized substrate or a gold- or nickel-plated package shall be used as the bonding surface for bond strength testing.

3.8.8.1.1 Type I materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) gold-plated Kovar tabs.

3.8.8.1.2 Type II materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) alumina chips.

3.8.8.2 Bond strength. The bond strength may be determined in accordance with ASTM D1002 as an alternative to test method 2019.

3.8.8.3 Molding compounds or encapsulants. Molding compounds or encapsulants shall be tested in accordance with MIL-STD-883, test method 1034.

3.8.9 Coefficient of linear thermal expansion. The coefficient of linear thermal expansion shall be determined in accordance with ASTM D3386 over the temperature range of -65°C to 150°C. The glass transition temperature, coefficients, and temperature ranges corresponding to different slopes of the curve shall be noted.

3.8.10 Thermal conductivity. The thermal conductivity, in watt/meter-K, shall be determined at 121°C ±5°C in accordance with ASTM C177 or ASTM C518.

NOTE: 1 cal/cm-s-k = 418.4 W/m-K.

3.8.11 Volume resistivity.

3.8.11.1 Type I polymers.

3.8.11.1.1 Paste materials. Test specimens shall be prepared using a standard 1 inch x 3 inch glass slide. A jig capable of holding this slide, with two scribed lines 100 mil apart and parallel to the length, shall be the guide for applying two strips of transparent tape. There shall be no wrinkles or bubbles in the tape. The slide shall be cleaned with alcohol and air dried. A drop of the type I material shall be placed between the two strips of tape. Using a single edge razor blade maintaining a 30° angle between the slide surface and the razor blade, the material shall be squeezed between the tape strips. The length of the applied strip shall be at least 2.5 inches. The tape shall be removed, and the material shall be cured according to 3.5.1. After cure, the test specimens shall be allowed to cool to room temperature.

3.8.11.1.2 Film materials. Test specimens shall be prepared using a standard 1 inch x 3 inch glass slide. The slide shall be cleaned with alcohol and air dried. A thin strip of the uncured film approximately 100 mil wide and at least 2.5 inches long shall be placed on the glass slide. The film shall be covered with a strip of copper foil or Teflon film and a second 1 inch x 3 inch glass slide shall be placed over the foil or Teflon film. Sufficient force (weight, clip, etc.), shall be applied to the assembly to compress the material during cure. The material shall be cured according to 3.5.1. After cure, the test specimen shall be allowed to cool to room temperature, and the top slide and foil or Teflon shall be removed. The exact width and thickness of each polymer strip shall be measured with a precision caliper and micrometer respectively. These measurements, after conversion to the appropriate units, shall be used to calculate the volume resistivity using the formula given in 3.8.11.1.3.

3.8.11.1.3 Resistance measurements. Resistance measurements shall be made using a milliohm meter in conjunction with a special four-point probe test fixture. (This fixture can be made of an acrylic material with four spring-loaded contacts. The contacts must be set into the acrylic so that the current contacts are 2 inches apart, the voltage contacts are between the two current contacts, and the voltage contacts are separated from each current contact by 0.5 inch.) The four-point probe fixture shall be placed on the strip of conductive polymer and contact between each probe and the material shall be ensured. The measured resistance shall be recorded in ohms, and the resistivity shall be determined from the following formula:

$$P = \frac{R\,(w \times t)}{l}$$

Where:

P = resistivity, ohm-m

R = measured resistance, ohms

w = width, (100 mil = 2.54 mm)

t = thickness, (micrometer reading of the material plus glass side) minus (micrometer reading of the glass slide)

l = length between inner pair of probes, (1 inch = 25.4 mm)

A minimum of three specimens shall be tested at 25°C, at 60°C, at 150°C, and at 25°C after 1,000 hours at 150°C in an air or nitrogen ambient. The same specimens may be used for each test.

3.8.11.2 Type II polymer materials. Type II materials shall be tested in accordance with ASTM D257 at temperatures of 25°C and 125°C.

3.8.12 Dielectric constant. The dielectric constant of type II materials shall be determined as required in the user's material specification in accordance with ASTM D150 at frequencies of 1 kHz and 1 MHz at room temperature.

3.8.13 Dissipation factor. The dissipation factor of type II materials shall be determined as required in the user's material specification in accordance with ASTM D150 at frequencies of 1 kHz and 1 MHz at room temperature.

3.8.14 Sequential test environment. Testing shall be performed using either 3.8.14.1 or 3.8.14.2.

3.8.14.1 Sequential test environment. A minimum of five test specimens shall be subjected to the environmental conditions specified below. Specimens shall be prepared using the largest component/substrate/package combinations representative of end-use applications in backing material, attach surface, and size. Component types include resistor, capacitor, integrated circuit, and discrete semiconductor elements. Two components of each type shall be attached to the substrate with the adhesive (type I or II) proposed for use with that component type. The test specimens shall be subjected to the following environmental conditions in the sequence given:

a. Thermal shock (MIL-STD-883, method 1011, condition C, 15 cycles).

b. Temperature cycling (MIL-STD-883, method 1010, condition C, 100 cycles).

c. Mechanical shock (MIL-STD-883, method 2002, condition B, Y1 only).

d. Variable frequency vibration (MIL-STD-883, method 2007, condition A, Y1 only).

e. Constant acceleration (MIL-STD-883, method 2001, condition B, Y1 only).

3.8.14.2 Alternate sequential testing. Alternatively, testing in accordance with Qualification Testing (QML sequences in accordance with MIL-PRF-38534, using maximum baseline limits may be performed. The user is still required to satisfy the requirements of 3.8.14.1 by completing the necessary supplemental testing, i.e., thermal shock and vibration.

Following the environmental exposures of 3.8.14.1 or 3.8.14.2, the test specimens shall be examined for possible degradation in accordance with MIL-STD-883, method 2017. For adhesives, one of each type of component from each sample shall be evaluated for die shear strength in accordance with MIL-STD-883, method 2019 and shall meet the strength requirements of figure 2019-4.

3.8.15 Density. The density of materials used as RF or microwave absorbers shall be determine in accordance with principles outlined in ASTM D1564, paragraphs 69-74. Those RF absorbers that are foamed in-place are to be foamed, cured, and cut to form the free standing material for this analysis.

3.8.16 Mechanical integrity.

3.8.16.1 Getter integrity - short term. Samples shall be prepared using hermetically sealed packages representative of the maximum size and type which will incorporate the use of getter material. These samples will contain only "salted" particles and getter material. The getter material shall be applied to the package in the location and approximate volume as specified for a normal production part. The getter material coverage area shall be measured and recorded. The particles to be salted shall consist of the following unless otherwise agreed upon by the user and the qualifying activity.

(1) Solder balls: 3-6 mils in diameter - 2 pieces required.

(2) Aluminum ribbon: Approximate dimensions of 2 mil thick by 5 mil wide by 10 mils long - 1 required. A piece of aluminum wire 2-6 mils in diameter may be substituted for the ribbon.

(3) Gold wire: 1 mil diameter by 15-20 mils in length - 1 piece required. Getter material application and cure shall take place in the sequence normally followed for production parts. The samples shall be processed through the same environmental conditioning steps as a qualified production part. The samples shall be subjected to PIND test in accordance with MIL-STD-883, method 2020, condition A or B, which shall be repeated three time for a total of five cycles to verify the integrity of the getter material. During all PIND testing the samples shall be mounted on the tester such that the shock pulses integral with the test shall be in the direction most likely to dislodge the particles from the getter material. A minimum of three samples shall be evaluated and all shall pass the defined PIND criteria.

3.8.16.2 Getter integrity - long term. All of the conditions and requirements of 3.8.16.1 apply, except that the samples either newly prepared or as received from the short term test, shall be stored at 150°C for 1,000 hours.

The samples shall then be subjected to mechanical shock in accordance with MIL-STD-883, method 2002, condition B, in the Y_2 direction. Following mechanical shock the samples shall be PIND tested as specified above.

Following PIND, the samples shall be delidded and a visual inspection shall be performed to verify the following:

a. Determine if particles have separated from the getter material or have fallen into the package.

b. Determine if getter coverage has spread or bled out.

c. Check for any evidence of peeling from inside and/or getter becoming separated from package.

3.8.16.3 Vibration. Samples shall be prepared as in 3.8.16.1 except that the lid shall be attached in such a manner that it may be removed for visual inspection. After particle salting and immobilization as in 3.8.16.1, visual inspection shall be done to verify entrapment of the salted particles. Location of the particles in the getter material shall be recorded for future reference.

The lid shall then be reattached to the package securely enough to withstand the testing that follows. After PIND testing in accordance with MIL-STD-883, method 2020, the samples shall be subjected to vibration in accordance with MIL-STD-883, method 2007, condition A or B. At the end of this test, the lids shall be removed from the package by whatever method is required. Location of the "salted" particles in the getter material shall be noted and compared with the location prior to vibration. Particles other than the original "salted" particles shall be ignored. A minimum of three samples shall be submitted for evaluation and all shall pass the defined PIND criteria initially and after vibration.

3.8.17 Operating life test. Ten electrically functioning samples shall be fabricated using hermetically sealed devices which have been processed through the same steps as a normally qualified production part as specified by the user's assembly drawing. If agreed upon by the user and the qualifying activity, standard evaluation circuits may be substituted. All the samples shall meet the PIND test requirements in accordance with MIL-STD-883, method 2020, condition A or B. The samples shall be subjected to the life test in accordance with MIL-STD-883, method 1005, condition A, for 1,000 hours at 125°C. Electrical parameters shall be measured and recorded for the units initially and at the completion of the life test. Data taken from the samples shall be reviewed for evidence of device degradation due to the presence of getter material.

NOTE: Qualification test data may be used to satisfy this requirement with qualifying activity approval.

* 3.9 Test deviation. Additional, reduced or alternate testing, as may be dictated by the uniqueness of particular material and manufacturing construction techniques can be required or authorized by the qualifying activity provided the manufacturer submits data to support test deviation.

4. SUMMARY. As a minimum, acquisition documents shall specify the following information:

a. Title, number, and revision letter of acquisition specification.

b. Size and number of containers required.

c. Manufacturer's product designation.

d. Request for test data.

METHOD 5012.1

FAULT COVERAGE MEASUREMENT FOR DIGITAL MICROCIRCUITS

1. PURPOSE. This test procedure specifies the methods by which fault coverage is reported for a test program applied to a microcircuit herein referred to as the device under test (DUT). This procedure describes requirements governing the development of the logic model of the DUT, the assumed fault model and fault universe, fault classing, fault simulation, and fault coverage reporting. This procedure provides a consistent means of reporting fault coverage regardless of the specific logic and fault simulator used. Three procedures for fault simulation are described in this procedure: Full fault simulation and two fault sampling procedures. The applicable acquisition document shall specify a minimum required level of fault coverage and, optionally, specify the procedure to be used to determine the fault coverage. A fault simulation report shall be provided that states the fault coverage obtained, as well as documenting assumptions, approximations, and procedures used. Where any technique detailed in this procedure is inapplicable to some aspect of the logic model, or inconsistent with the functionality of the available fault simulator and simulation postprocessing tools, it is sufficient that the user of this procedure employ an equivalent or comparable technique and note the discrepancy in the fault simulation report. Microcircuits may be tested by nontraditional methods of control or observation, such as power supply current monitoring or the addition of test points that are available by means of special test modes. Fault coverage based on such techniques shall be considered valid if substantiating analysis or references are provided in the fault simulation report.

1.1 Terms. Terms and abbreviations not defined elsewhere in the text of this test procedure are defined in this section.

a. Automatic test equipment (ATE). The apparatus with which the actual DUT will be tested. ATE includes the ability to apply a test vector sequence (see 1.1l).

b. Broadside application. A method of applying a test vector sequence where input stimuli change only at the beginning of a simulation cycle or ATE cycle and all changes on primary inputs of the DUT are assumed to be simultaneous. Nonbroadside application occurs when test vectors are conditioned by additional timing information such as delay (with respect to other primary inputs), return-to-zero, return-to-one, and surround-by- complement.

c. Detection. An error at an observable primary output of a logic model caused by the existence of a logic fault. A hard detection is where an observable output value in the fault-free logic model is distinctly different from the corresponding output value in the faulty logic model. An example of a hard detection is where the fault-free logic model's output value is 0 and the faulty logic model's output value is 1, or where the fault-free logic model's output value is 1 and the faulty logic model's output value is 0. If the high-impedance state (Z) can be sensed by the ATE, then a hard detection can involve the Z state as well. A potential detection is an error where the fault-free output is 0 or 1 and the faulty output value is unknown (X), or Z if Z cannot be sensed by the ATE.

d. Established test algorithm. An algorithm, procedure, or test vector sequence, that when applied to a logic component or logic partition has a known fault coverage or test effectiveness. This fault coverage or test effectiveness is denoted herein as the established fault coverage or established test effectiveness for the established test algorithm. For example, an established test algorithm for a RAM may be a published memory test algorithm, such as GALPAT, that has been shown by experience to detect essentially all RAM failures and therefore is assessed an established test effectiveness of 100 percent. An ALU may be tested by means of a precomputed test vector sequence for which fault coverage has been previously determined. More than one established test algorithm may exist for a logic component or logic partition, each with a different established fault coverage or test effectiveness.

e. Failure hierarchy: Failure mechanism, physical failure, logical fault, error. The failure hierarchy relates physical defects and their causes to fault simulators and observable effects. A failure mechanism is the actual cause of physical failure; an example is electromigration of aluminum in a microcircuit. A physical failure (or simply failure) is the actual physical defect caused by a failure mechanism; an example is an open metal line. A logical fault (or simply fault) is a logical abstraction of the immediate effect of a failure; an example is "stuck- at-one" behavior of a logic gate input in the presence of an open metal line. An error is a difference between the behavior of a fault-free and faulty DUT at one or more observable primary outputs of the DUT.

f. Fault coverage. For a logic model of a DUT, a fault universe for the logic model of the DUT, and a given test vector sequence, fault coverage is the fraction obtained by dividing the number of faults contained in the fault universe that are detected by the test vector sequence by the total number of faults contained in the fault universe. Fault coverage is also stated as a percentage. In this test procedure, fault coverage is understood to be based on the detectable fault equivalence classes (see 3.3). Rounding of fault coverage fractions or percentages shall be "toward zero," not "to nearest." For example, if 9,499 faults are detected out of 10,000 faults simulated, the fault coverage is 94.99 percent; if this value is to be rounded to two significant digits, the result shall be reported as 94 percent, not 95 percent.

g. Logic line, node. Logic lines are the connections between components in a logic model, through which logic signals flow. Logic lines are the idealized "wires" in a logic model. A set of connected logic lines is a node.

h. Logic: Combinational and sequential. Combinational digital logic contains only components that do not possess memory, and in which there are no feedback paths. Sequential digital logic contains at least one component that contains memory, or at least one feedback path, or both. For example, a flip-flop is a component that contains memory, and cross-coupled logic gates introduce feedback paths.

i. Macro. A logic modeling convention representing a model contained within another model. A macro boundary does not necessarily imply the existence of a physical boundary in the logic model. A main model is a logic model that is not contained within a larger model. Macros may be nested (that is, a macro may contain submacros).

j. Primary inputs, primary outputs. Primary inputs to a logic model represent the logic lines of a DUT that are driven by the ATE's drivers and thus are directly controllable test points. Primary outputs from a logic model represent the logic lines of the DUT that are sensed by the ATE's comparators and thus are directly observable test points. The inputs to the "main model" of the logic model of the DUT are the primary inputs, and the outputs from the main model are the primary outputs. Internal nodes that can be driven or sensed by means of special test modes shall be considered to be control or observation test points.

k. Test effectiveness. A measure similar to fault coverage, but used in lieu of fault coverage in cases where physical failures cannot be modeled accurately as logical faults. For example, many RAM and PLA failures cannot be idealized conveniently in the same way as gate-level failures. However, established test algorithms may be used to detect essentially all likely physical failures in such structures.

l. Test vector sequence. The (ordered) sequence of stimuli (applied to a logic model of a DUT) or stimulus/response values (applied to, and compared for, the actual DUT by the ATE).

m. Undetectable and detectable faults. An undetectable fault is defined herein as a logical fault for which no test vector sequence exists that can cause at least one hard detection or potential detection (see 1.1c). Otherwise (that is, some test vector sequence exists that causes at least one hard detection, or potential detection, or both), the fault is defined herein to be a detectable fault (see 3.3.3).

2. APPARATUS.

2.1 Logic simulator. Implementation of this test procedure requires the use of a facility capable of simulating the behavior of fault-free digital logic in response to a test vector sequence; this capability is herein referred to as logic simulation.

In order to simulate sequential digital logic, the simulator must support simulation of a minimum of four logic states: zero (0), one (1), high-impedance (Z), and unknown (X). In order to simulate combinational digital logic only, the simulator must support simulation of a minimum of two logic states: 0 and 1.

At the start of logic simulation of a logic model of a DUT containing sequential logic, the state of every logic line and component containing memory shall be X; any other initial condition, including explicit initialization of any line or memory element to 0 or 1, shall be documented and justified in the fault simulation report.

In order to simulate wired connections or bus structures, the simulator must be capable of resolving signal conflicts introduced by such structures. Otherwise, modeling workarounds shall be permitted to eliminate such structures from the logic model (see 3.1.2).

In order to simulate sequential digital logic, the simulator must support event- directed simulation. As a minimum, unit-delay logic components must be supported.

Simulation of combinational-only logic, or simulation of sequential logic in special cases (such as combinational logic extracted from a scannable sequential logic model) can be based on nonevent-directed simulation, such as levelized, zero-delay, or compiled-code methods. The fault simulation report shall describe why the selected method is equivalent to the more general event-directed method.

2.2 Fault simulator. In addition to the capability to simulate the fault-free digital logic, the capability is also required to simulate the effect of single, permanent, stuck-at-zero and stuck-at-one faults on the behavior of the logic; this capability is herein referred to as fault simulation. Fault simulation shall reflect the limitations of the target ATE (see 3.4.1). It is not necessary that the fault simulator directly support the requirements of this test procedure in the areas of hard versus potential detections, fault universe selection, and fault classing. However, the capability must exist, at least indirectly, to report fault coverage in accordance with this procedure. Where approximations arise (for example, where fault classing compensates for a different method of fault universe selection) such differences shall be documented in the fault simulation report, and it shall be shown that the approximations do not increase the fault coverage obtained.

3. PROCEDURE.

3.1 Logic model.

3.1.1 Level of modeling. The DUT shall be described in terms of a logic model composed of components and connections between components. Primary inputs to the logic model are assumed to be outputs of an imaginary component (representing the ATE's drivers), and primary outputs of the logic model are assumed to be inputs to an imaginary component (representing the ATE's comparators). Some logic simulators require that the ATE drivers and comparators be modeled explicitly; however, these components shall not be considered to be part of the logic model of the DUT.

3.1.2 Logic lines and nodes (see 1.1g). All fan-out from a node in a logic model is ideal, that is, fan-out branches associated with a node emanate from a single point driven by a fan-out origin. All fan-in to a node in a logic model is ideal; that is, multiple fan-in branches in a node drive a single line. Figure 1 shows a node that includes fan-in branches, a fan-out origin, and fan-out branches. Because fan-in and fan-out generally are not ideal in actual circuit layout, the actual topology of the circuit should be modeled, if it is known, by appropriately adding single-input noninverting buffers to the logic model.

Modeling workarounds may be used to eliminate fan-in to a node. This may be required if the simulator does not directly model wired connections or bus structures. Some simulators may permit internal fan-in, but require that bidirectional pins to a DUT be modeled as separate input and output functions.

3.1.3 G-logic and B-logic partitions. Simple components of the logic model (logic primitives such as AND, OR, NAND, NOR, XOR, buffers, or flip-flops; generally the indivisible primitives understood by a simulator) are herein referred to as gate logic (G-logic). Complex components of the logic model (such as RAM, ROM, or PLA primitive components, and behavioral models - relatively complex functions that are treated as "black boxes" for the purpose of fault simulation) are referred to herein as block logic (B-logic).

For the purpose of fault simulation, the logic model shall be divided into nonoverlapping logic partitions; however, the entire logic model may consist of a single logic partition. The logic partitions contain components and their associated lines; although lines may span partitions, no component is contained in more than one partition. A G-logic partition contains only G-logic; any other logic partition is a B-logic partition.

A logic partition consisting of G-logic, or B-logic, or G-logic and B-logic that, as a unit, is testable using an established testing algorithm, with known fault coverage or test effectiveness, may be treated as a single B-logic partition.

3.1.4 Model hierarchy. The logic model may be hierarchical (that is, consisting of macro building blocks), or flat (that is, a single level of hierarchy with no macro building blocks). Hierarchy does not impose structures on lines; for example, there is no implied fan-out origin at a macro input or output. Macros that correspond to physical partitions in a model shall use additional buffers (or an equivalent method) to enforce adherence to the actual DUT's fan-out.

3.1.5 Fractions of transistors. The fraction of transistors comprising each G-logic and B-logic partition, with respect to the total count of transistors in the DUT, shall be determined or closely estimated; the total sum of the transistor fractions shall equal 1. Where the actual transistor counts are not available, estimates may be made on the basis of gate counts or microcircuit area; the assumptions and calculations supporting such estimates shall be documented in the fault simulation report. The transistor fractions shall be used in order to weight the fault coverage measured for each individual logic partition (see 3.5).

3.2 Fault model.

3.2.1 G-logic. The fault model for G-logic shall be permanent stuck-at-zero and stuck-at-one faults on logic lines. Only single stuck-at faults are considered in calculating fault coverage.

3.2.2 B-logic. No explicit fault model is assumed for B-logic components. However, an established test algorithm shall be applied to each B-logic component or logic partition. If a B-logic partition contains logic lines or G-logic components, or both, justification shall be provided in the fault simulation report as to how the established test algorithm that is applied to the B-logic partition detects faults associated with the logic lines and G-logic components.

3.2.2.1 Built-in self-test. A special case of B-logic is a partition that includes a linear-feedback shift register (LFSR) that performs signature analysis for compression of output error data. Table I lists penalty values for different LFSR degrees. If the LFSR implements a primitive GF(2) polynomial of degree "k", where there is at least one flip-flop stage between inputs to a multiple-input LFSR, then the following procedure shall be used in order to determine a lower bound on the established fault coverage of the logic partition:

Step 1: Excluding the LFSR, but including any stimulus generation logic considered to be part of the logic partition, determine the fault coverage of the logic partition by fault simulation without signature analysis; denote this fault coverage by C.

Step 2: Reference table I. For a given degree "k" obtain the penalty value "p". The established fault coverage of the logic partition using a LFSR of degree "k" shall be reported as (1-p)C. That is, a penalty of (100p) percent is incurred in assessing the effectiveness of signature analysis if the actual effectiveness is not determined.

3.3 Fault universe selection and fault equivalence classing. Fault coverage shall be reported in terms of equivalence classes of the detectable faults. This section describes the selection of the initial fault universe, the partitioning or collapsing of the initial fault universe into fault equivalence classes, and the removal of undetectable faults in order to form the detectable fault universe. These three stages constitute the fault simulation reporting requirements; however, it is generally more efficient to obtain the set of faults that represent the fault equivalence classes directly without explicitly generating the initial fault universe.

3.3.1 Initial fault universe. The initial fault universe shall consist of single, permanent, stuck-at-zero and stuck-at-one faults on every logic line (not simply on every logic node) in the G-logic partitions of the logic model. A bus, which is a node with multiple driving lines, shall be considered, for the purpose of fault universe generation, to be a multiple-input, single-output logic gate. The initial fault universe shall include stuck-at-zero and stuck-at-one faults on each fan-in and fan-out branch and the fan-out origin of the bus (see figure 1).

The fault universe does not explicitly contain any faults within B-logic partitions. However, all faults associated with inputs and outputs of B-logic components either are contained in a G-logic partition or shall be shown to be considered by established test algorithms that are applied to the B-logic partitions.

No faults shall be added or removed by considering or not considering logic model hierarchy. No extra faults shall be associated with any primary input or output line, macro input or output line, or logic line that spans logic partitions where the logic partitions do not correspond to a physical boundary. No more than one stuck-at-zero and one stuck-at-one fault per logic line shall be contained in the initial fault universe.

3.3.2 Fault equivalence classes. The initial fault universe shall be partitioned or collapsed into fault equivalence classes for reporting purposes. The fault equivalence classes shall be chosen such that all faults in a fault equivalence class cause apparently identical erroneous behavior with respect to the observable outputs of the logic model. One fault from each fault equivalence class shall be selected to represent the fault class for reporting purposes; these faults shall be called the representative faults.

For the purpose of implementing this test procedure it is sufficient to apply simple rules to identify structurally-dependent equivalence classes. An acceptable method for selecting the representative faults for the initial fault universe consists of listing all single, permanent, stuck-at faults as specified in table II. Any other fault equivalencing procedure used shall be documented in the fault simulation report. If a bus node exhibits wired-AND or wired-OR behavior in the applicable circuit technology, then faults associated with that bus shall be collapsed in accordance with the AND or OR fault equivalencing rules, respectively. Otherwise, no collapsing of faults associated with a bus shall be performed.

3.3.3 Detectable fault universe. Fault coverage shall be based on the detectable fault universe. Undetectable faults shall be permitted to be dropped from the set of representative faults; the remaining set of representative faults comprises the detectable fault universe. In order for a fault to be declared as undetectable, documentation shall be provided in the fault simulation report as to why there does not exist any test vector sequence capable of guaranteeing that the fault will cause an error at an observable primary output (see 1.1m.). Any fault not documented in the fault simulation report as being undetectable shall be considered detectable for the purpose of calculating fault coverage.

3.4 Fault simulation.

3.4.1 Automatic test equipment limitations. Fault coverage reported for the logic model of a DUT shall reflect the limitations of the target ATE. Two common cases are:

a. Fault detection during fault simulation shall occur only at times where the ATE will be capable of sensing the primary outputs of the DUT; there must be a one-to-one correspondence between simulator compares and ATE compares. For example, if fault coverage for a test vector sequence is obtained using broadside fault simulation (where fault detection occurs after every change of input stimuli, including clock signals), then it is not correct to claim the same fault coverage on the ATE if the test vectors are reformatted into cycles where a clock signal is pulsed during each cycle and compares occur only at the end of each cycle.

b. If the ATE cannot sense the Z output state (either directly or by multiple passes), then the reported fault coverage shall not include detections involving the Z state. That is, an output value of Z shall be considered to be equivalent to an output value of X.

Any differences in format or timing of the test vector sequence, between that used by the fault simulator and that applied by the ATE, shall be documented in the fault simulation report and it shall be shown that fault coverage achieved on the ATE is not lower than the reported fault coverage.

3.4.2 G-logic.

3.4.2.1 Hard detections and potential detections. Fault coverage for G-logic shall include only faults detected by hard detections. Potential detections shall not be considered directly in calculating the fault coverage. No number of potential detections of a fault shall imply that the fault would be detected.

Some potential detections can be converted into hard detections for the purpose of calculating fault coverage. If it can be shown that a fault is only potentially detected by fault simulation but is in fact detectable by the ATE by a difference not involving an X value, then upon documenting those conditions in the fault simulation report that fault shall be considered to be detected as a hard detection and the fault coverage shall be adjusted accordingly.

Faults associated with three-state buffer enable signal lines can cause X states to occur on nodes with fan-in branches, or erroneous Z states to occur on three-state primary outputs that may be untestable on some ATE. These faults may then be detectable only as potential detections, but may be unconvertible into hard detections. In such cases, it is permissible for the fault simulation report to state separately the fraction of the undetected faults that are due to such faults.

3.4.2.2 Fault simulation procedures. The preferred method of fault simulation for G-logic is to simulate the effect of each representative fault in the G-logic. However, this may not be practical in some cases due to the large number of representative faults, or because of limitations of the logic models or simulation tools. In such cases fault sampling procedures may be used. When fault sampling is used, either the acquisition document shall specify the method of obtaining a random sample of faults or the fault simulation report shall describe the method used. In either case, the complete random sample of faults shall be obtained before beginning the fault simulation procedure involving a random sample of faults.

Use of any fault simulation procedure other than fault simulation procedure 1 (see 3.4.2.2.1) shall be documented and justified in the fault simulation report.

In this section, it is assumed that the representative faults declared to be undetectable have been removed from the set of faults to be simulated.

3.4.2.2.1 Fault simulation procedure 1. Simulate each representative fault in a G-logic partition. The procedure used shall be equivalent to the following:

Step 1: Denote by "n" the total number of representative faults in the G-logic partition.

Step 2: Fault simulate each representative fault. Denote by "d" the number of hard detections.

Step 3: Fault coverage for the G-logic partition is given by d/n.

3.4.2.2.2 Fault simulation procedure 2. Obtain lower bound on actual fault coverage in a G-logic partition using fixed sample size (see table III). The procedure used shall be equivalent to the following:

Step 1: Select a value for the penalty parameter "r" (r = 0.01 to 0.05). The corresponding value of "n" in table III is the size of the random sample of representative faults.

Step 2: Fault simulate each of the "n" representative faults. Denote by "d" the number of hard detections.

Step 3: The lower bound on the fault coverage is given by "d/n-r".

3.4.2.2.3 Fault simulation procedure 3. Accept/reject lower bound on fault coverage in a G-logic partition using fixed sample size (see table IV). The procedure used shall be equivalent to the following:

Step 1: Denote by "F" the minimum required value for fault coverage. From table IV obtain the minimum required sample size, denoted by "n".

Step 2: Fault-simulate each of the "n" representative faults, and denote by "d" the number of hard detections.

Step 3: If "d" is less than "n" (that is, any faults are undetected), then conclude that the fault coverage is less than "F." Otherwise (that is, all sampled faults are detected), conclude that the fault coverage is greater than or equal to "F".

3.4.3 B-logic. Fault coverage shall be measured indirectly for each B-logic partition. For a given B-logic partition, the established fault coverage or test effectiveness shall be reported for that B-logic partition only if it is shown that: (a) the test vector sequence applied to the DUT applies the established test algorithm to the B-logic partition, and (b) the resulting critical output values from the B-logic partition are made observable at the primary outputs. Otherwise, the fault coverage for that B-logic partition shall be reported as 0 percent. For each B-logic partition tested in this way, the established test algorithm, proof of its successful application, and the established fault coverage or test effectiveness shall be documented in the fault simulation report.

3.5 Fault coverage calculation. Let "m" denote the number of logic partitions in the logic model for the DUT. For the ith logic partition, let "F_i" denote its fault coverage (measured in accordance with 3.4), and let "T_i" denote its transistor fraction (measured in accordance with 3.1.5). The fault coverage "F" for the logic model for the DUT shall be calculated as:

$$F = F_1T_2 + F_2T_2 + \ldots + F_mT_m$$

If fault simulation procedure 1 is performed for each G-logic partition in the logic model of a DUT, then the fault coverage for the logic model of a DUT shall be reported as:

"F of all detectable equivalence classes of single, permanent, stuck-at-zero and stuck-at-one faults on the logic lines of the logic model as measured by MIL-STD- 883, test method 5012."

If fault simulation procedure 2 or 3 is performed for any G-logic partition, then the fault coverage for the logic model of a DUT shall be reported as:

"No less than F of all detectable equivalence classes of single, permanent, stuck-at-zero and stuck-at-one faults on the logic lines of the logic model, with 95 percent confidence, as measured by MIL-STD-883, test method 5012."

The confidence level of 95 percent shall be identified if any fault simulation procedure other than procedure 1 was performed for any G-logic partition.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Minimum required level of fault coverage and method of obtaining fault coverage.

   b. If a fault sampling method is permitted, guidance on selection of the random sample of faults.

   c. Guidelines, restrictions, or requirements for test algorithms for B-Logic types.

The fault simulation report shall provide:

   a. Statement of the overall fault coverage. If there are undetectable faults due to three-state enable signal lines, then, optionally, fault coverage based on those potential detections may be reported separately.

   b. Description of logic partitions.

   c. Description of test algorithms applied to B-logic. For each B-logic partition tested in this way the established test algorithm, proof of its successful application, and description of its established fault coverage or test effectiveness (including classes of faults detected) shall be documented.

   d. Justification for any initial condition, other than X, for any logic line or memory element.

   e. Justification for any approximations used, including estimates of fault coverages, transistor fractions, and counts of undetectable faults.

   f. Description of any fault equivalencing procedure used in lieu of the procedure defined by table II.

   g. Justification for declaring any fault to be undetectable.

   h. In the event that the test vector sequence is formatted differently between the ATE and the fault simulator, justification that fault coverage achieved on the ATE is not lower than the reported fault coverage.

   i. Justification of the use of fault simulation procedure 2 or 3 rather than fault simulation procedure 1.

   j. When fault sampling is used, description of the method of obtaining a random sample of faults.

   k. In the event that the fault simulation procedure used is not obviously equivalent to fault simulation procedure 1, 2, or 3, justification as to why it yields equivalent results.

   l. In the event that a test technique or design-for-testability approach is used that provides additional control or observation test points beyond those provided by the DUT's primary inputs and primary outputs (see 1.1j), justification that the stated fault coverage is valid.

FIGURE 1. Node consisting of fan-in branches, a fan-out origin, and fan-out branches.

TABLE I. Penalty values, P, for LFSR signature analyzers implementing primitive polynomial of degree k.

K	p
k < 8	1.0
k = (8...15)	0.05
k = (16...23)	0.01
k > 23	0.0

TABLE II. Representative faults for the fault equivalence classes.

Stuck-at faults	Type of logic line in logic model
s-a-1	Every input of multiple-input AND or NAND gates
s-a-0	Every input of multiple-input OR or NOR gates
s-a-0, s-a-1	Every input of multiple-input components that are not AND, OR, NAND, or NOR gates
s-a-0, s-a-1	Every logic line that is a fan-out origin
s-a-0, s-a-1	Every logic line that is a primary output

Note: "s-a-0" is stuck-at-zero and "s-a-1" is stuck-at-one.

TABLE III. Sample sizes used to obtain lower bound on fault coverage using fault simulation procedure 2.

r	n
0.01	6860
0.015	3070
0.02	1740
0.03	790
0.04	450
0.05	290

NOTE: "n" is the minimum sample size required for a chosen penalty "r".

TABLE IV. Sample sizes used to accept/reject lower bound on fault coverage using fault simulation procedure 3.

F	n	F'
50.0%	5	87.1%
55.0%	6	89.1%
60.0%	6	89.1%
65.0%	7	90.6%
70.0%	9	92.6%
75.0%	11	93.9%
76.0%	11	93.9%
77.0%	12	94.4%
78.0%	13	94.8%
79.0%	13	94.8%
80.0%	14	95.2%
81.0%	15	95.5%
82.0%	16	95.8%
83.0%	17	96.0%
84.0%	18	96.2%
85.0%	19	96.4%
86.0%	20	96.6%
87.0%	22	96.9%
88.0%	24	97.2%
89.0%	26	97.4%
90.0%	29	97.6%
91.0%	32	97.9%
92.0%	36	98.1%
93.0%	42	98.4%
94.0%	49	98.6%
95.0%	59	98.8%
96.0%	74	99.1%
97.0%	99	99.3%
98.0%	149	99.5%
99.0%	299	99.8%

NOTE: For a given minimum required fault coverage "F" simulate "n" faults. If all faults are detected, then conclude that the actual fault coverage is greater than or equal to "F". Otherwise, conclude that the actual fault coverage is less than "F." The column labeled "F'" shows the actual fault coverage that has a 50 percent probability of acceptance.

METHOD 5013

WAFER FABRICATION CONTROL AND WAFER ACCEPTANCE PROCEDURES FOR PROCESSED GaAs WAFERS

* 1. PURPOSE. This method specifies wafer fabrication control and wafer acceptance requirements for GaAs monolithic microcircuits for application in class level B or class level S microcircuits. It shall be used in conjunction with other documents such as MIL-PRF-38535, MIL-PRF-38534 and an applicable device specification or drawing to establish the design, material, performance, control, and documentation requirements.

2. APPARATUS. The apparatus required for this test method includes metallurgical microscopes capable of up to 1,000X magnification, a scanning electron microscope (SEM), electrical test equipment suitable for the measurement of process monitor (PM) test structures and other apparatus as required to determine conformance to the requirements of this test method.

3. PROCEDURE. The procedures defined herein specify the wafer fabrication controls and wafer acceptance tests necessary for the production of GaAs wafers compliant to the requirements of this test method.

* 3.1 Precedence. Unless otherwise specified in the device specification or drawing, the test requirements and conditions shall be as given herein.

3.2 Wafer fabrication line controls.

3.2.1 Process baseline. The use of this test method is restricted to a well characterized (controlled) and baselined process. By "characterized" it is meant that the fabrication line has been adequately documented in relation to the capabilities of the process. "Baselined" refers to the existence of a well defined process parameter target value with associated variances (based on characterization data) against which the actual wafer to wafer process data is measured to determine acceptability. The manufacturer shall submit process baseline documentation as specified herein to the acquiring activity for approval.

* 3.2.2 Statistical process control. The manufacturers shall have implemented statistical process control (SPC) for the wafer fabrication line in accordance with the requirements of EIA-557-A.

* 3.2.2.1 Alternate visual inspection procedure for class level B microcircuits. A sample plan for visual inspection in accordance with 3.1 of test method 2010 may be implemented in lieu of 100 percent visual inspection for processes controlled by the SPC program. The sample size for inspection shall be identified in the baseline process documentation.

3.2.3 Incoming material evaluation. Incoming material evaluation shall be performed as documented in the process baseline to assure compatibility with wafer fabrication specifications and manufacturing procedures.

3.2.4 Electrostatic discharge sensitivity. The manufacturer shall develop and implement an ESD control program for the wafer fabrication area.

3.2.5 Failure analysis. When required by the applicable device specification or drawing, failure analysis shall be performed on wafers rejected at in-process or acceptance testing.

3.3 Wafer acceptance tests.

3.3.1 General. This wafer lot acceptance procedure is based on wafer visual inspection and electrical testing of suitable process monitors (PMs), see table I. The performance of each wafer shall be evaluated individually. Process monitor measurements, verifying that the identified baseline parameters are within process limits, will be required from each wafer lot in accordance with 3.3.2 herein.

3.3.1.1 Process monitor (PM). A process monitor (PM) is a collection of test structures which provide data for the purposes of process control and determining wafer acceptability. PMs may be either stepped into every wafer in dedicated drop-in locations, incorporated into kerf locations, located on each die, or combinations of these, such that they can be probed at the conclusion of processing up to and including final front-side metallization and passivation (glassivation) where applicable. PM structures, tests and acceptance limits shall be recorded in the baseline document. A suggested list is shown in table I.

3.3.2 PM evaluation. Wafer acceptance will be made on a wafer by wafer basis upon the information derived from PM room temperature testing, which may be performed at any time during the manufacturing cycle. If drop-in PMs are utilized each wafer shall have a sufficient number of PMs stepped in the center of each of the quadrants to assure the integrity of the wafer acceptance procedure and the baseline SPC program. For kerf PMs and for PMs on individual die, the probed PMs shall be located in the center of the wafer and in each of the quadrants. Quadrant PMs shall lie at least one-half of the distance to the wafer edge away from the wafer center.

3.3.3 Visual/SEM inspection. Inspection via visual microscopy or SEM shall be performed at critical process steps during wafer fabrication. When the process flow includes substrate via processing, the backside features shall be visually inspected to the criteria specified in test method 2010. Inspections may include patterns, alignment verniers, and critical dimension measurements. Defective wafers shall be removed from the lot for scrap or for rework. Inspection operations, sampling plans and acceptance criteria shall be documented in the process baseline.

* 3.3.4 Test results. When required by the device specification or drawing or for qualification, the following test results shall be made available for each wafer lot submitted.

a. Results of each test conducted; initial and any resubmissions.

b. Number of wafers accepted/rejected per lot.

c. Number of reworked wafers and reason for rework.

d. Measurements and records of the data for all specified PM electrical parameters.

3.3.5 Defective wafers. All wafers that fail any test criteria shall be removed at the time of observation or immediately at the conclusion of the test in which the failure was observed. Rejected wafers may be subjected to approved rework operations as detailed in the baseline document. Once rejected and verified as an unreworkable failure, no wafer may be retested for acceptance. Rejected wafers processed in accordance with approved rework procedures shall be resubmitted to all applicable inspections at the point of rejection and must be found acceptable prior to continuing processing.

3.3.6 Element evaluation. When specified, upon completion of wafer acceptance based on the baseline SPC program and PM measurement results, 100 percent static/RF testing at 25°C shall be performed on each individual die. Failures shall be identified and removed from the lot when the die are separated from the wafer.

TABLE I. Test structures for use in a PM.

1.	N-channel transistors for measuring transistor parameters.
2.	P-channel transistors for measuring transistor parameters.
3.	Sheet resistance.
4.	E-mode transistor parameters.
5.	D-mode transistor parameters.
6.	Isolation.
7.	Contact resistance (via/ohmics).
8.	Step coverage.
9.	Alignment verniers.
10.	Line width.
11.	Diode parameters.
12.	Backgating.
13.	Doping profile structure.
14.	FATFET.
15.	Thin film resistor characteristics.
16.	Capacitance value measurements.

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision *letter should be given.*

2. The submitter of this form must complete blocks 4, 5, 6, and 7.

3. The preparing activity must provide a reply within 30 days from receipt of the form.

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I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER	2. DOCUMENT DATE *(YYMMDD)*
	MIL-STD-883E	961231

3. DOCUMENT TITLE

Test Method Standard Microcircuits

4. NATURE OF CHANGE *(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)*

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME *(Last, First, Middle Initial)*	b. ORGANIZATION	
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8. PREPARING ACTIVITY

a. NAME	b. TELEPHONE *(Include Area Code)*	
Mr. Raymond Monnin	(1) Commercial (614) 692-0536	(2) AUTOVON 850-0536
c. ADDRESS *(Include Zip Code)* Defense Supply Center Columbus DSCC-VAS P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340	