



# Flatsat Platform Documentation

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*Flatsat Platform Documentation*

*SpaceLab, Universidade Federal de Santa Catarina, Florianópolis - Brazil*



# Flatsat Platform Documentation

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## Nomenclature

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AWG	<i>American Wire Gauge.</i>
BOM	<i>Bill Of Materials.</i>
DC	<i>Direct Current.</i>
DNP	<i>Do Not Place.</i>
EEPROM	<i>Electrically-Erasable Programmable Read-Only Memory.</i>
EMC	<i>Electromagnetic Compatibility.</i>
EPS	<i>Electric Power System.</i>
IC	<i>Integrated Circuit.</i>
OBDH	<i>On-Board Data Handling.</i>
PCB	<i>Printed Circuit Board.</i>
PC	<i>Personal Computer.</i>
RBF	<i>Remove Before Flight.</i>
SMA	<i>SubMiniature version A.</i>
SPDT	<i>Single Pole, Double Throw.</i>
UART	<i>Universal Asynchronous Receiver/Transmitter.</i>
UHF	<i>Ultra High Frequency.</i>
USB	<i>Universal Serial Bus.</i>
VHF	<i>Very High Frequency.</i>



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# CHAPTER 1

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## Introduction

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The SpaceLab FlatSat Platform is a testbed for CubeSat PCB modules. FlatSats enable easier, faster and a secure method for testing subsystems independently while been integrated in a flat design before going to integration on a CubeSat form factor. The PCB can support up to 7 modules, all PC-104 pins are interligated to flexibilize its use, only the particularity connection between modules need to be taken into account. One PC-104 has inverted pinout, the board also makes it possible to have two seperate power supplies, a UART to USB converter for 4 modules, kill-switches activation though SPDTs, Remove Before Flight (RBF) pin header, connector for charging batteries and SMA connectors for antennas. This project is to be used on the GOLDS-UFSC mission [1] during test phase.

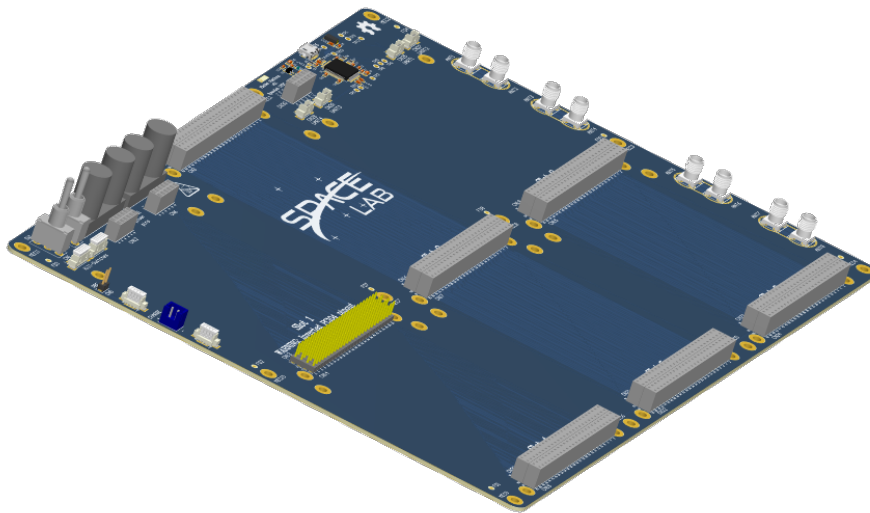


Figure 1.1: 3D view of the FlatSat PCB.

All the project, source and documentation files are available freely on a GitHub repository [2] under its respective licenses.



## CHAPTER 2

### System Overview

The FlatSat form factor choosen for this project is a retangular one piece design. On its current version v0.1 the platform can be purely used hardware wise. The hardware block diagram can be seen on Figure 2.1. The PC-104 slot N°7 is supossed to be used for a extra interface, shield or another FlatSat platform.

### 2.1 Block Diagram

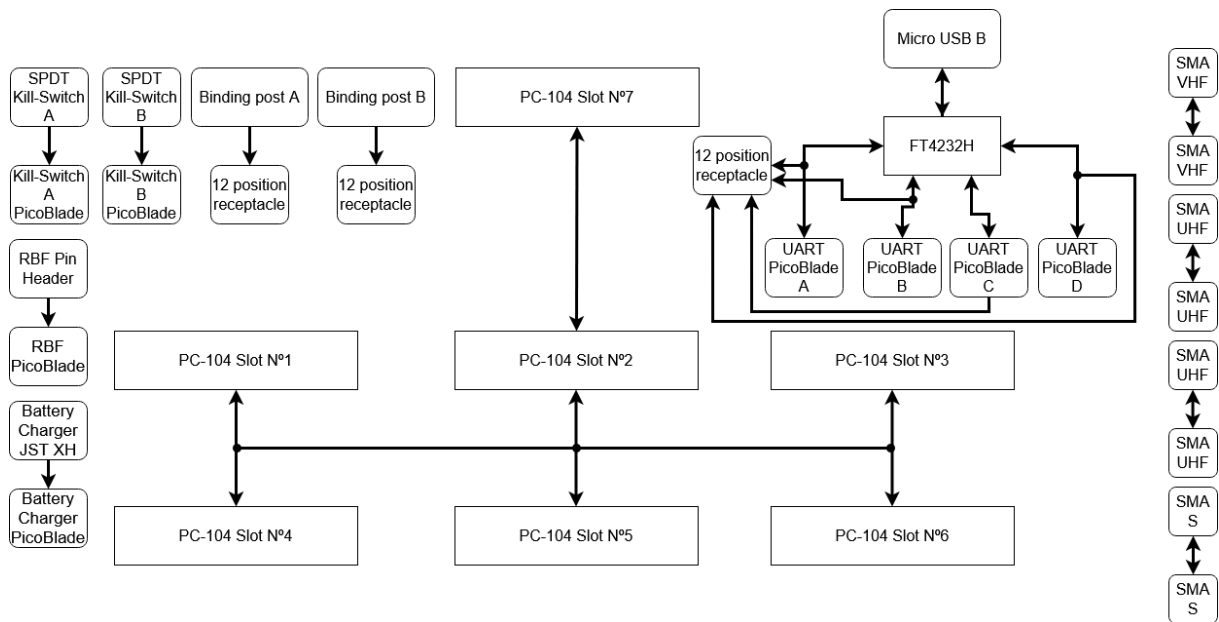


Figure 2.1: FlatSat hardware block diagram.

### 2.2 Board Dimensions

The board is a retangular PCB with linear dimensions of 300×220 mm. The full mechanical specs of the platform can be seen on its draftsman document available at it's GitHub repository [3].





## CHAPTER 3

## Hardware

This chapter describes all the FlatSat's hardware interfaces in detail. On Figures 3.1 and 3.2 are displayed de top and bottom PCB prints.

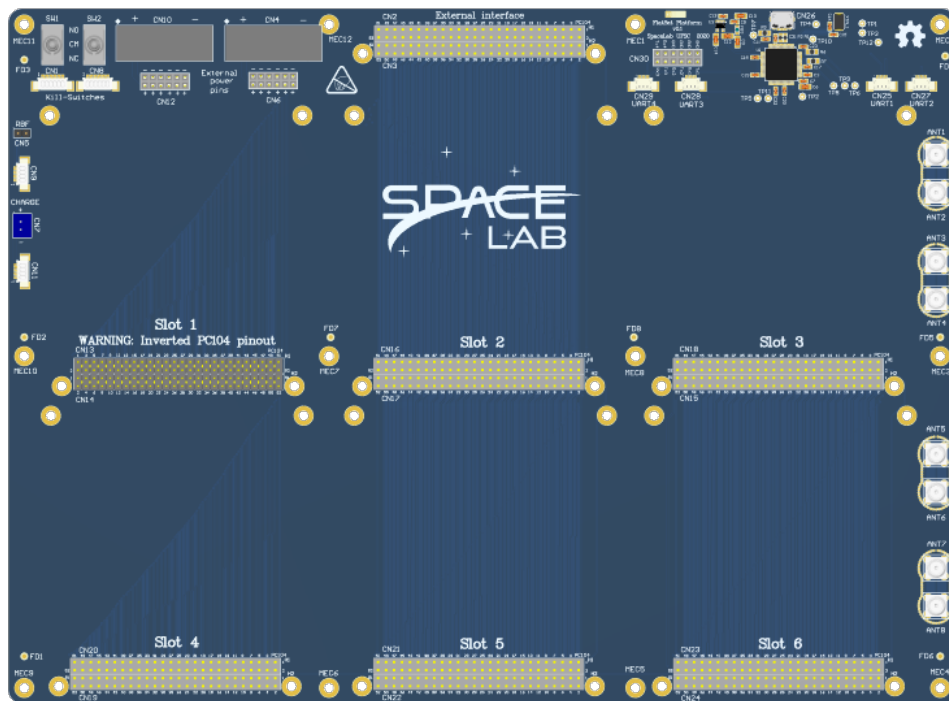


Figure 3.1: FlatSat top PCB print.

### 3.1 PC-104 Interfaces

On SpaceLab's FlatSat Platform the PC-104 interfaces are composed by two 52 pins with 2.54 mm (0.1 inch) pitch connectors. Slots N°2 to N°7 has two *SSW-126-01-G-D* and the slot N°1 uses two *TSW-126-07-G-D* connectors with inverted pinout, see Figures 3.3 and 3.4. All pins are interconnected to flexiblesize the positioning of the modules on the platform. All slots have grounded unlabeled mounting holes for the modules, the labeled MEC1 to MEC12 holes are for the FlatStats stability feet.

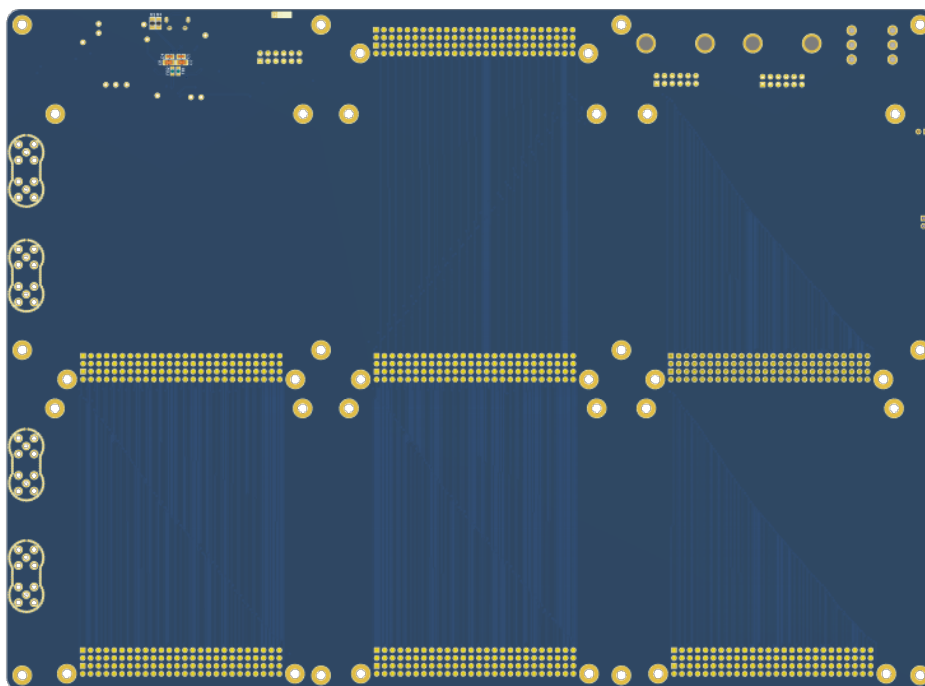


Figure 3.2: FlatSat bottom PCB print.

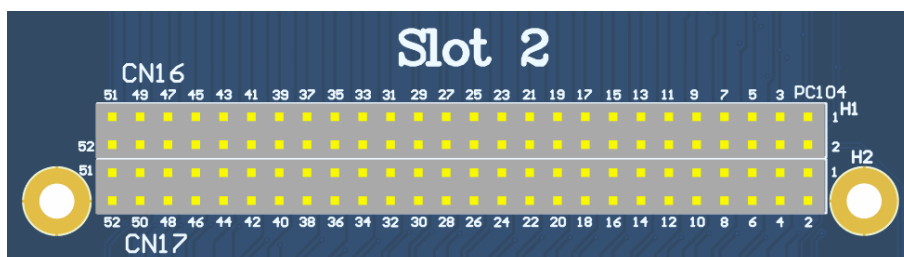


Figure 3.3: FlatSat N°2 PC-104 slot.

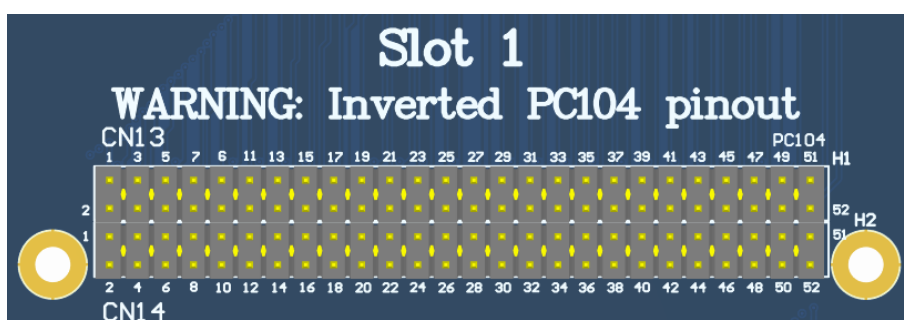


Figure 3.4: FlatSat N°1 PC-104 slot.

## 3.2 Binding Posts and Power Receptacles

Two sets of binding posts (4243-0) can be mouted on the labeled CN4 and CN10 hole pads to be used for two external power supplies, see Figure 3.5. The modules are powered

via external jumper wires to the 12 position receptacle connectors (*BCS-106-L-D-TE*) labeled CN6 and CN12. On the silkscreen the plus (+) signs are the positive power pins while the minus (-) signs are the GND pins.

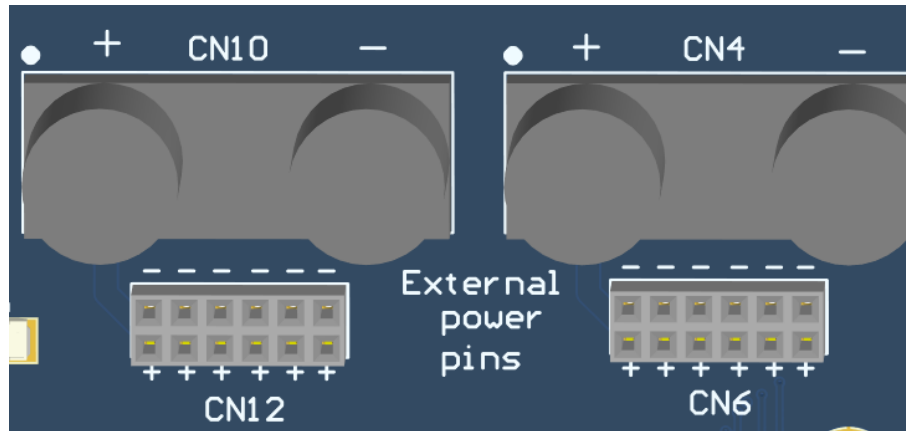


Figure 3.5: FlatSat binding posts and power receptables.

### 3.3 Charge Header

On the board there is a JST XH 2 position header (*B2B-XH-A-M(LF)(SN)*) for charging batteries, it can be seen in Figure 3.6. The component can suport up to 3000 mA of current, but it is advised to be used with less than 1500 mA. The 4 pin PicoBlade is to be connected to the EPS module to make the interconnection for the JST header. The charge header also provides a detent lock for fastening and avoid a mistankenly reverse connection.

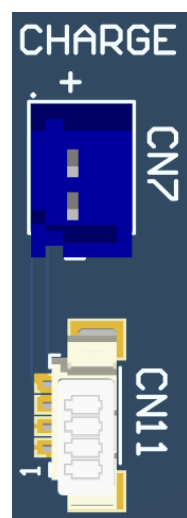


Figure 3.6: FlatSat charge connectors.

### 3.4 RBF Pin Header

The platform has a RBF pin header that can be seen in Figure 3.7. The interconnection between the header and the EPS module is done by a 4 pin PicoBlade.



Figure 3.7: FlatSat RBF connectors.

### 3.5 SPDT Kill-Switches

The kill-switches use SPDT switches (*100SP1T1B4M2QE*) for powering off the EPS module, see Figure 3.8. The power off states are seen on Figure 3.9, they are also present on the hardware schematics. The SPDTs are interconnected to the EPS module via two 6 pin PicoBlade connectors labeled CN1 and CN8.

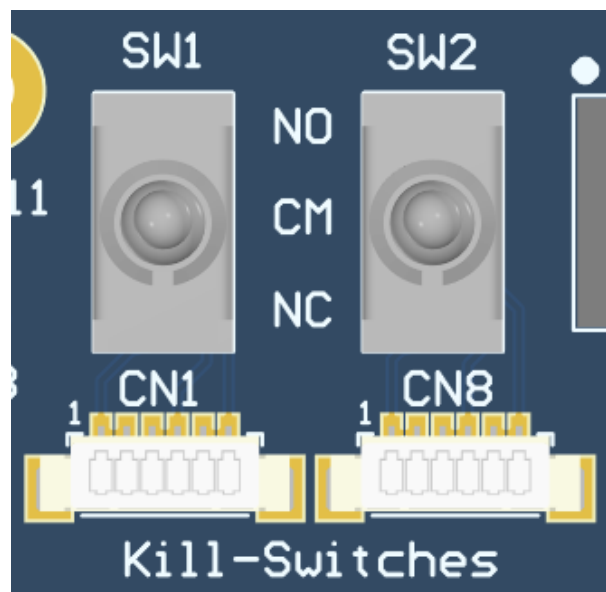


Figure 3.8: FlatSat kill-switches connectors.

RBF	Switch(NC)	Switch(NO)	MOSFET	EPS POWER
1	X	X	OPEN	Cut-off
0	1	0	CLOSE	ON
0	0	1	OPEN	Cut-off (launch moment)

Figure 3.9: FlatSat kill-switches states.

## 3.6 Antenna Interfaces

### 3.6.1 SMA connectors

On the PCB there are SMA connectors (132134-15) labeled ANT1 to ANT8 for connecting VHF, UHF and S-Band antennas, see Figure 3.10. The receiver (RX) antenna is to be connected to one of the SMA, while the transmitter (TX) goes to the other connector and to the CubeSat module. The impedance control (see Figure 3.11) and power dissipation (see Figure 3.12) where approximately calculated for all 3 bands. As the FlatSat platform is to be used in light testing the aproximations where considered acceptable for the project.

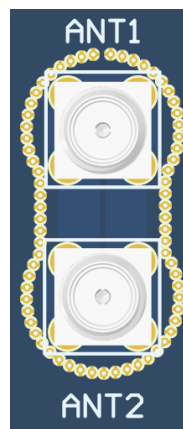
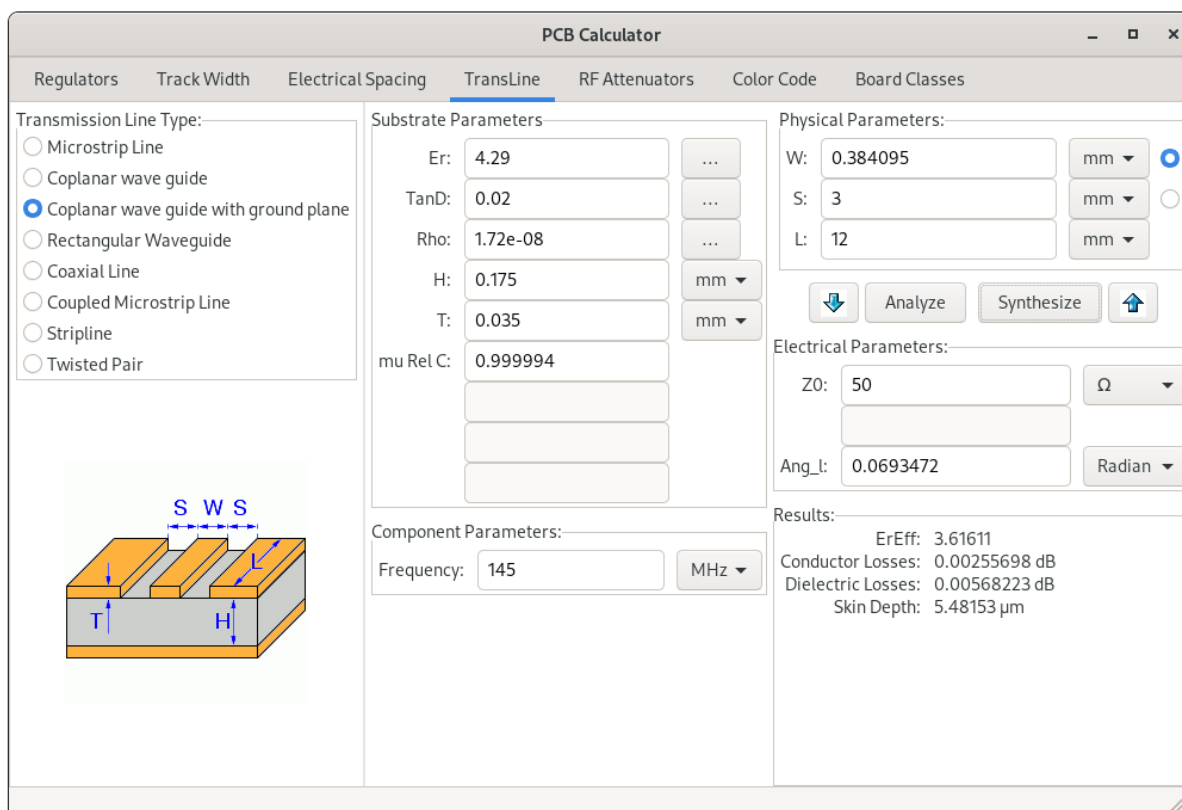


Figure 3.10: FlatSat SMA connectors.

### 3.6.2 Impedance Control of the RF Tracks

## 3.7 UART to USB Converter

There is a UART to USB converter circuit built-in the FlatSat platform for debbuging pourposes for four independent modules, it can be seen on Figure 3.13. The subcircuit is self powered from a USB cable connecting a computer to a micro USB type B port (10118194-0001LF). The USB Bridge converter IC is the *FT4232HL-REEL* from FTDI. PicoBlade connectors are used for connecting the IC to the modules, see Figures 3.14



PCB Calculator

Regulators Track Width Electrical Spacing **TransLine** RF Attenuators Color Code Board Classes

Transmission Line Type:

- ☐ Microstrip Line
- ☐ Coplanar wave guide
- ☒ Coplanar wave guide with ground plane
- ☐ Rectangular Waveguide
- ☐ Coaxial Line
- ☐ Coupled Microstrip Line
- ☐ Stripline
- ☐ Twisted Pair

Substrate Parameters:

Er: 4.29

TanD: 0.02

Rho: 1.72e-08

H: 0.175 mm

T: 0.035 mm

mu Rel C: 0.999994

Physical Parameters:

W: 0.384095 mm

S: 3 mm

L: 12 mm

Analyze Synthesize

Electrical Parameters:

Z0: 50  $\Omega$

Ang\_L: 0.0693472 Radian

Results:

ErEff: 3.61611

Conductor Losses: 0.00255698 dB

Dielectric Losses: 0.00568223 dB

Skin Depth: 5.48153  $\mu\text{m}$

Component Parameters:

Frequency: 145 MHz

Diagram: A 3D perspective view of a coplanar waveguide (CPW) structure. It shows a central signal strip of width 'W' on a substrate of thickness 'H'. Two ground planes of width 'S' are located on either side of the signal strip. The total width of the structure is 'T'.

Figure 3.11: Calculation of the width of the RF tracks.

and 3.15. It is also possible to use jumper wires connecting the 12 Position receptacle connector (*BCS-106-L-D-TE*) labeled CN30 to the modules if PicoBlades are not used.

## 3.8 Test Points

The FlatSat has test points for the UART to USB converter circuit. The Table 3.1 displays their labels and description.

**PCB Calculator**

Regulators   **Track Width**   Electrical Spacing   TransLine   RF Attenuators   Color Code   Board Classes

Parameters:

Current: 1.18584 A

Temperature rise: 10.0 deg C

Conductor length: 12 mm

Resistivity: 1.72e-8 Ohm-meter

If you specify the maximum current, then the trace widths will be calculated to suit.  
 If you specify one of the trace widths, the maximum current it can handle will be calculated. The width for the other trace to also handle this current will then be calculated.  
 The controlling value is shown in bold.

The calculations are valid for currents up to 35A (external) or 17.5A (internal), temperature rises up to 100 deg C, and widths of up to 400mil (10mm).  
 The formula, from IPC 2221, is

$$I = K * dT^{0.44} * (W * H)^{0.725}$$

where:  
**I** = maximum current in amps  
**dT** = temperature rise above ambient in deg C  
**W, H** = width and thickness in mils  
**K** = 0.024 for internal traces or 0.048 for external traces

External layer traces:

**Trace** 0.38 mm

Trace thickness: 0.035 mm

Cross-section area: 0.0133 mm x mm

Resistance: 0.0155188 Ω

Voltage drop: 0.0184028 Volt

Power loss: 0.0218227 Watt

Internal layer traces:

Trace width: 2.03524 mm

Trace thickness: 0.017 mm

Cross-section area: 0.0345991 mm x mm

Resistance: 0.00596546 Ω

Voltage drop: 0.00707407 Volt

Power loss: 0.00838868 Watt

Figure 3.12: Power dissipation of the RF tracks.

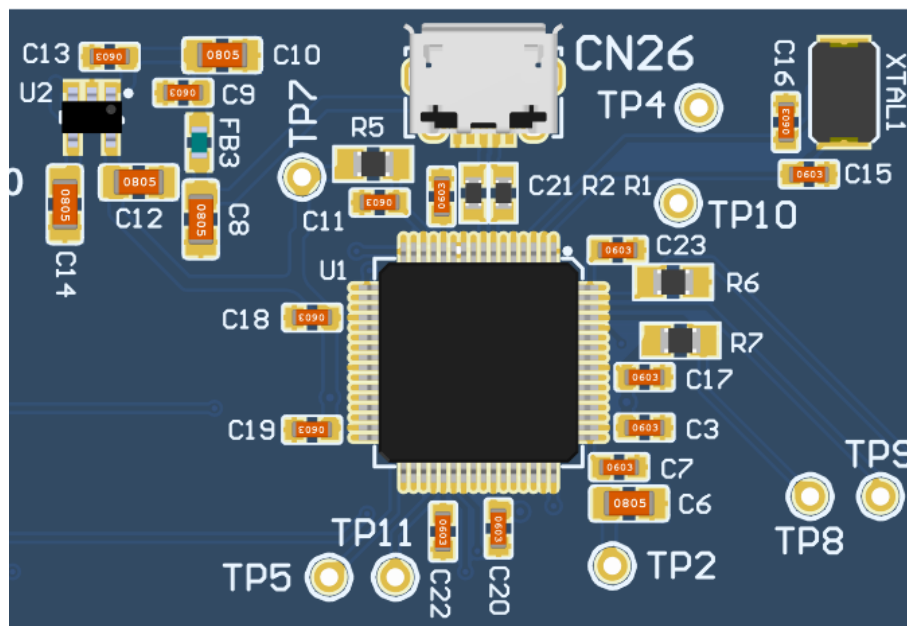


Figure 3.13: Top view of the UART to USB converter circuit.



Figure 3.14: UART PicoBlade N°1 and N°2 connectors.

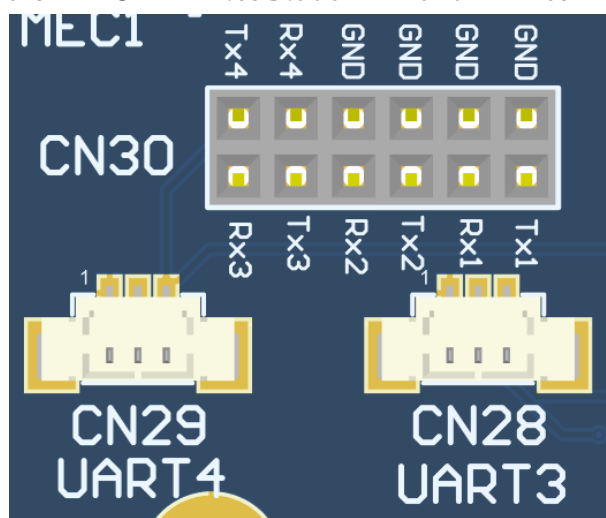


Figure 3.15: UART PicoBlade N°3 and N°4 connectors and receptable.

<i>Label</i>	<i>Description</i>
TP1	(VPLL) 3V3 FT4232H power input.
TP2	(VREGOUT) 1V8 FT4232H internal power output.
TP3	(VPHY) 3V3 FT4232H power input.
TP4	(REF) Current reference for FT4232H.
TP5	(RESET#) Reset input for FT4232H.
TP6	(EECS) EEPROM chip select - pulled down by 10k resistor.
TP7	(VCCIO) I/O interface 3V3 power supply input.
TP8	(EEDATA) EEPROM data I/O - pulled up by 10k resistor.
TP9	(EECLK) Clock signal to EEPROM - not used.
TP10	(PWREN#) Active low power-enable output.
TP11	(SUSPEND#) Active low when USB is in suspend mode.
TP12	(GND) 0V ground input for FT4232H.

Table 3.1: FlatSat test points.



## CHAPTER 4

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### Board Assembly

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The hardware project has the Bill of Material (BOM) available at its GitHub repository in excel spreadsheets format. The PCB can be assembled by a Pick-and-place machine using the .txt file found on the hardware/fabrication folder if desired, fiducials labeled FD# are placed to make this possible.

#### 4.1 FlatSat Stability Feet

On the PCB there are labeled MEC1 to MEC12 mounting holes on the edges and in the middle of the board to be used for stability feet when the board is placed on top of a test bench.

#### 4.2 DNP Components

There is only one Do Not Place (DNP) component present in the USB to UART circuit, it is the labeled R4 pad with 0805 size (2012 metric) available for soldering the micro USB type B chassi to GND for Electromagnetic compatibility (EMC) see Figure 4.1. This can be done soldering a zero-Ohm resistor for a DC path or capacitor for a high-frequency path between shield and signal ground, see Section 2.2.2 of the document [4] for more details.

#### 4.3 Modules Mounting

The PC-104 slots N°2 to N°7 are compatible for CubeSat PCB modules that are stacked in middle or the first on top. The slot N°1 can only be used for the last module on this stack because of the inverted pinout. For the case of the SpaceLab's CubeSat stackup of the core modules, the last module of the stack is the EPS. For this case the EPS needs to be mounted up-side-down on slot N°1 as can be seen on Figure 4.2. For other modules any other PC-104 slots can be used, the OBDH is showed mouted on Figure 4.3.

#### 4.4 Antennas Connection

Since the SMA connectors present on the board are on the right far side, modules placed in the opposite side may not be in reach for the connection. Because of this reason is recommended to use slots N°1 and N°4 for non antenna dependents PCBs.

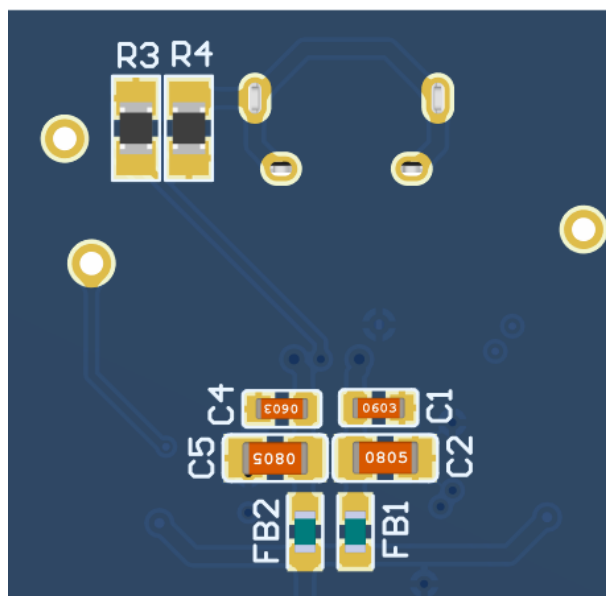


Figure 4.1: Bottom view of the UART to USB converter circuit.

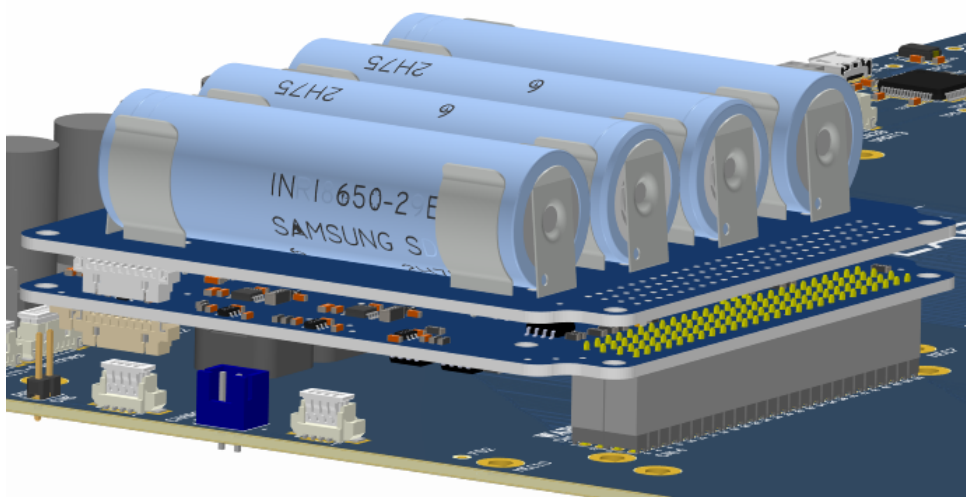


Figure 4.2: EPS mounted on N°1 slot on a EDA tool.

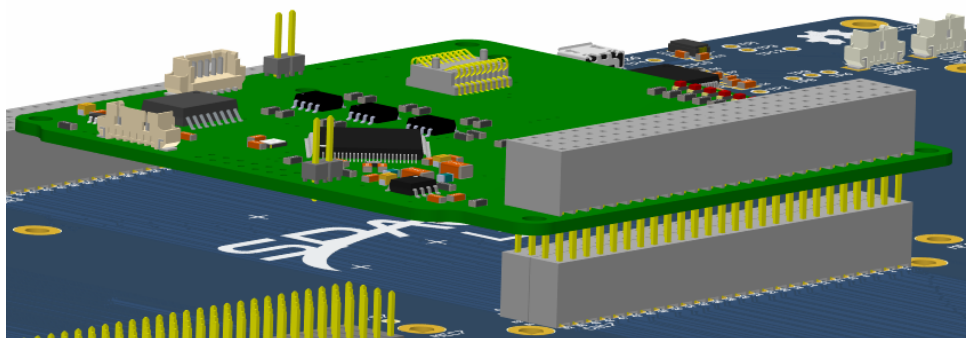


Figure 4.3: OBDH mounted on N°2 slot on a EDA tool.

## CHAPTER 5

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### Usage Instructions

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#### 5.1 Charging Batteries Through Connector

To charge the batteries it will be needed a cable compatible with the JST XH header. The compatible housing is a XHP-2 receptacle, the jumper lead socket to socket to be used can be *ASXHSXH22K305*, or any other with AWG #30 to #22. The only constraint is that the current cannot excel 2000 mA, because the PicoBlades connectors used to interconnect the JST header to the EPS only supports 1000 mA per pin. For safe usage it is recommended to use the header with a maximum of 1500 mA charge current.

#### 5.2 Debugging Though USB

Connecting a type A to micro type B USB cable to a PC and the USB port present on the FlatSat, the four USB to UART channels should be ready to be used. Note that the computer will recognize the port as four different devices. The FT4232H IC present on the platform doesn't have an EEPROM, so it will be already configured to operate as default serial ports. The FT4232H will have the built-in default VID (0403) and PID (6011).

#### 5.3 Debugging Though PC-104

Since all PC-104 interfaces are interconnected any slot can be used for probing and debbuging. Intentionally the slot N°7 or also labeled "external interface" on the PCB was meant to be used for testing all pins. A new board or another FlatSat platform can be connected to this interface if the pinout of the specific project is compatible. The GOLDS-UFSC pinout is avalaible at its github repository [1].



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- [3] SpaceLab. FlatSat draftsman documentation, 2020. Available at <[https://github.com/spacelab-ufsc/flatsat-platform/hardware/outputs/board\\_draftsman/board\\_draftsman.pdf](https://github.com/spacelab-ufsc/flatsat-platform/hardware/outputs/board_draftsman/board_draftsman.pdf)>.
- [4] Future Technology Devices International Ltd. USB Hardware Design Guidelines for FTDI ICs, 2014. Available at [https://www.ftdichip.com/Support/Documents/AppNotes/AN\\_146\\_USB\\_Hardware\\_Design\\_Guidelines\\_for\\_FTDI\\_ICs.pdf](https://www.ftdichip.com/Support/Documents/AppNotes/AN_146_USB_Hardware_Design_Guidelines_for_FTDI_ICs.pdf).