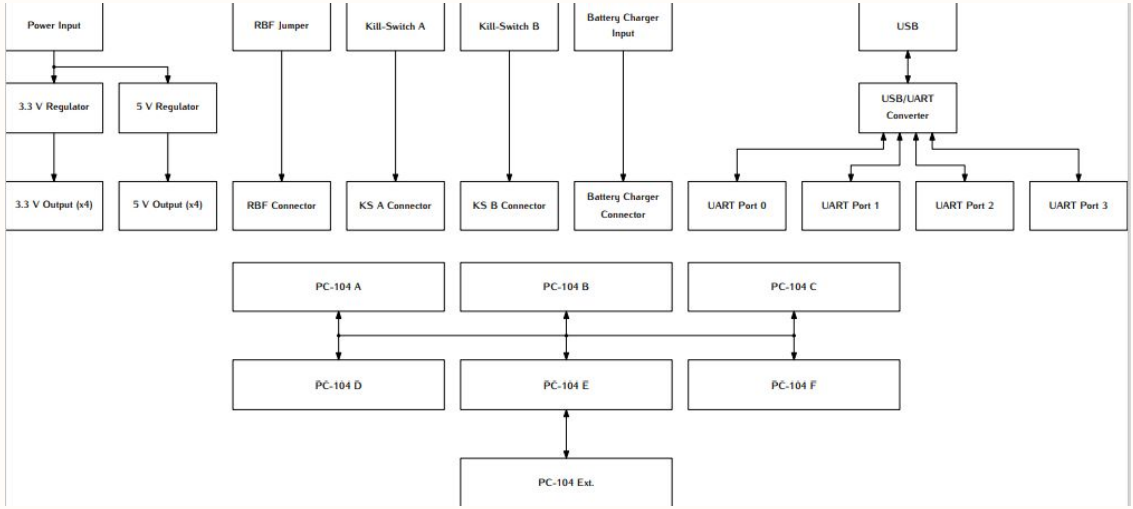
FlatSat Hardware:

- Designed by: Yan C. de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support:

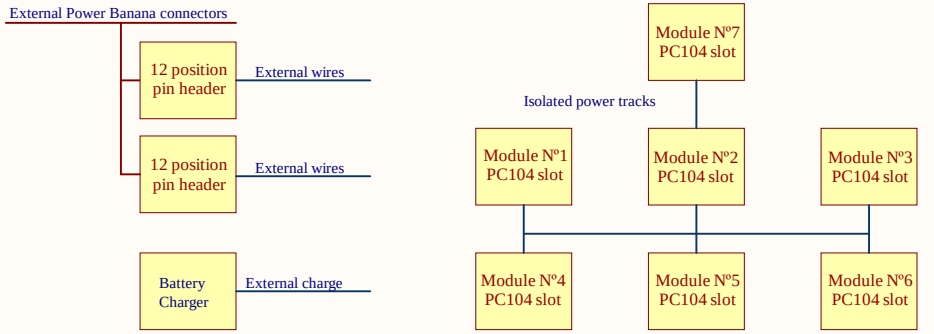
Project Contributions



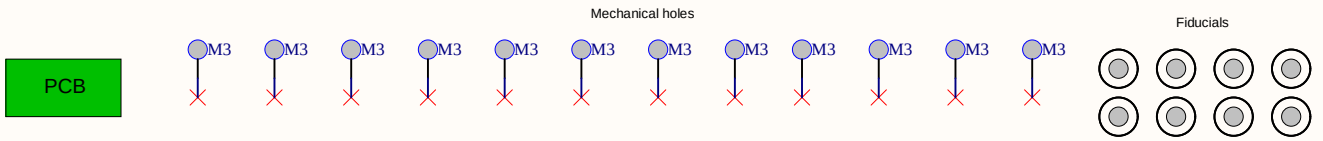
Block Diagram

Rev	Description	Date	Author
1.0	Initial release	dd-mmm-aaaa	Name LastName

Revision History



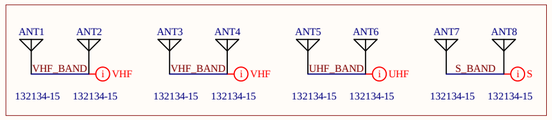
Power Architecture



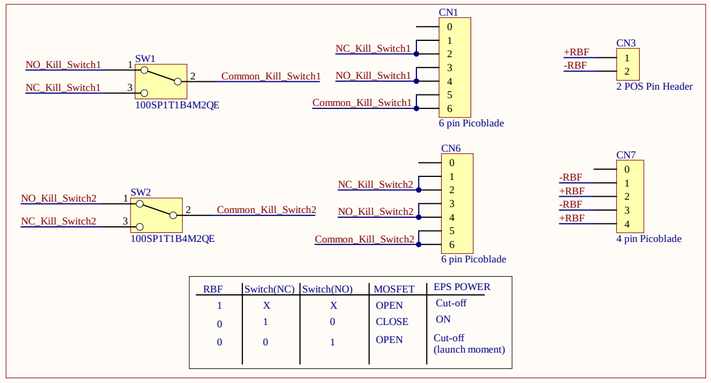
PCB Elements

SpaceLab - Federal University of Santa Catarina			
Project: *flatsat_platform.PrjPcb / [No Variations]*			
Title: *FlatSat Hardware Architecture*			
Designed by: *Yan Castro de Azeredo*			Project Code: *FLATSAT1*
Date: 10/8/2020	Revision: *1.0*	Sheet *1* of *3*	Size: A4

SMA Connectors

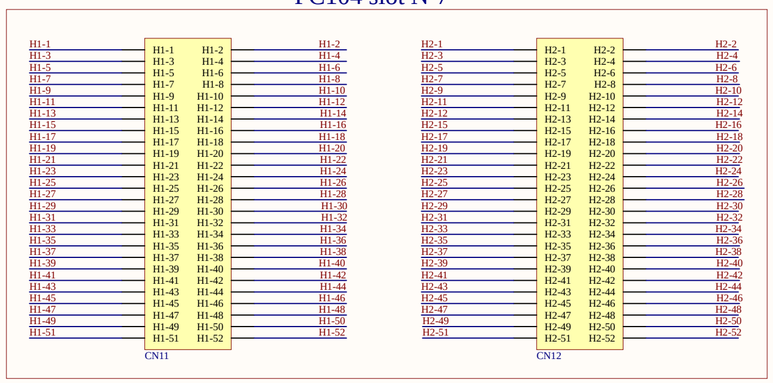


RBF and Kill-Switches

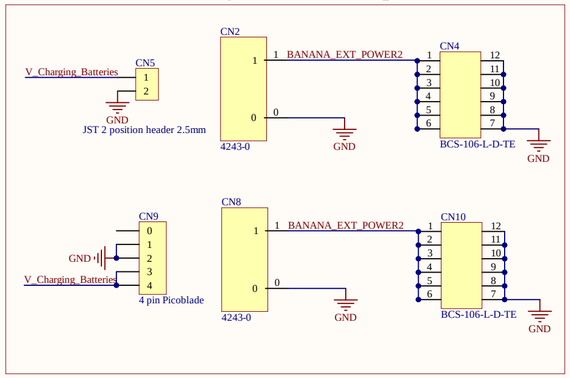


RBF	Switch(NC)	Switch(NO)	MOSFET	EPS POWER
1	X	X	OPEN	Cut-off
0	1	0	CLOSE	ON
0	0	1	OPEN	Cut-off (launch moment)

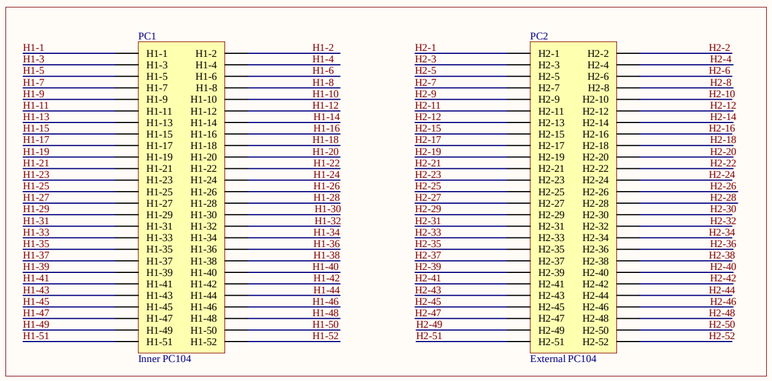
PC104 slot Nº7



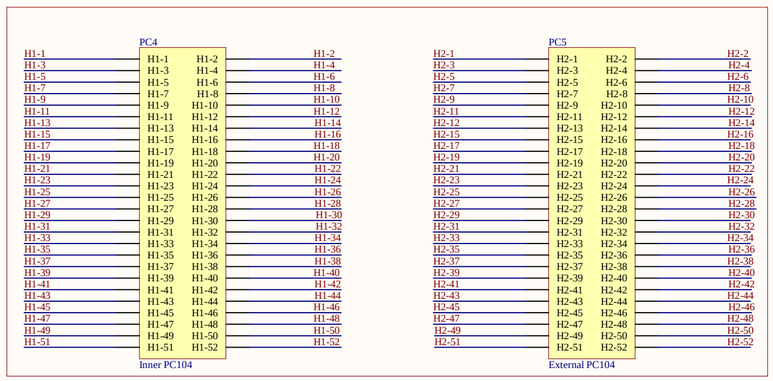
Charge and external power



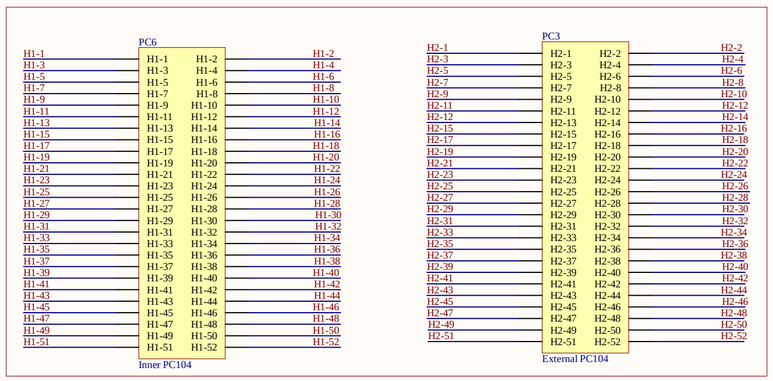
PC104 slot Nº1



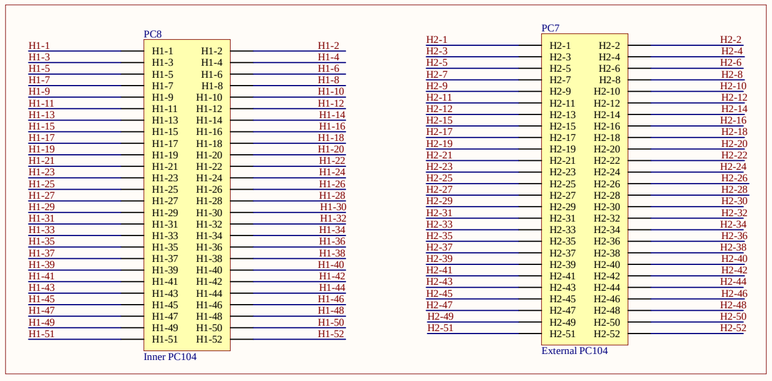
PC104 slot Nº2



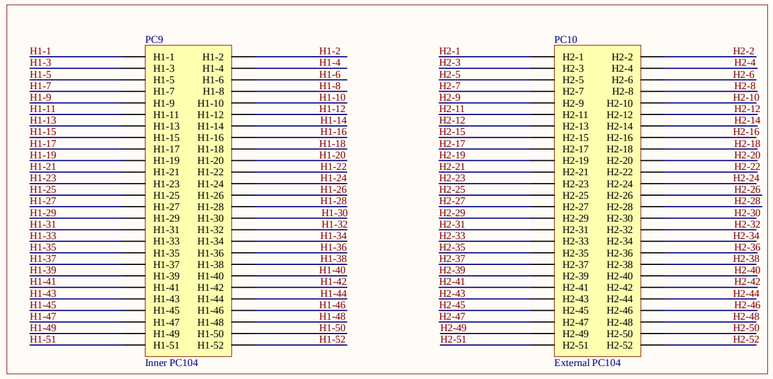
PC104 slot Nº3



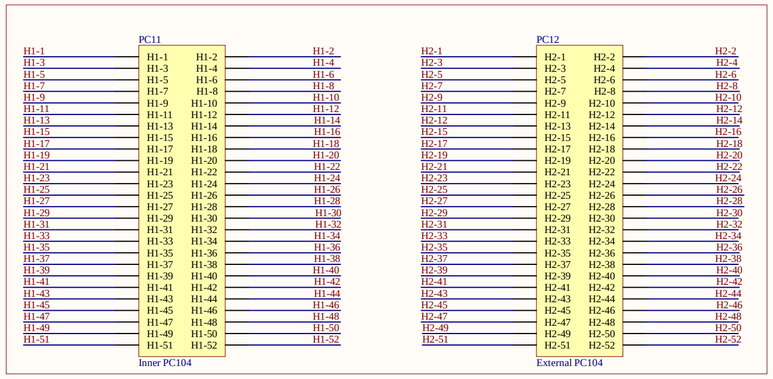
PC104 slot Nº4



PC104 slot Nº5

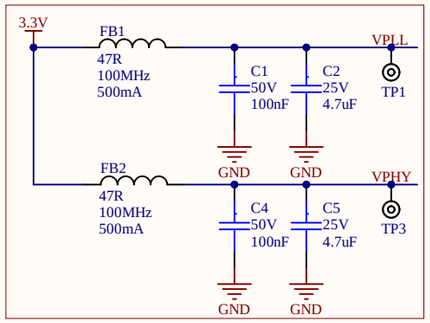


PC104 slot Nº6

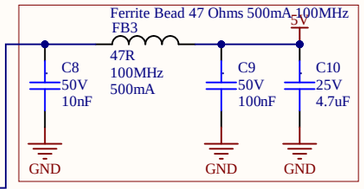


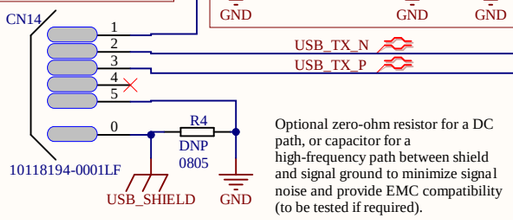
SpaceLab - Federal University of Santa Catarina			
Project: *flatsat_platform.PrjPcb / [No Variations]*			
Title: *FlatSat Main Interfaces and Connectors*			
Engineer: *Yan Castro de Azeredo*			Project Code:*FLATSAT1*
Date: 10/8/2020	Revision: *1.0*	Sheet *2* of *3*	Size: A2

Low pass LC filters for VPLL and VPHY

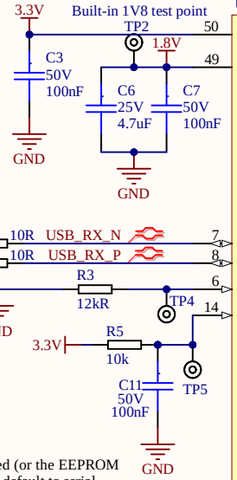


USB VBUS Filter





Optional zero-ohm resistor for a DC path, or capacitor for a high-frequency path between shield and signal ground to minimize signa1 noise and provide EMC compatibility (to be tested if required).

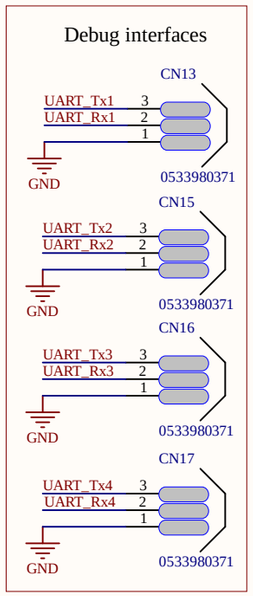


From FT4232H datasheet:
"If no EEPROM is connected (or the EEPROM is blank), the FT4232H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value."

Testpoints for debugging IC

PWREN# = 0: Normal operation.
PWREN# =1: USB SUSPEND mode or device has not been configured.
SUSPEND#: Active low when USB is in suspend mode.

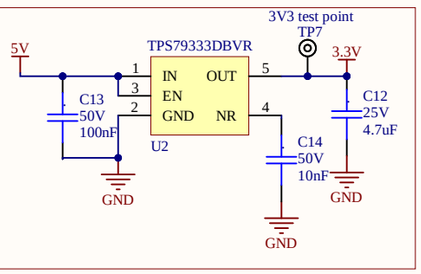
Debug interfaces



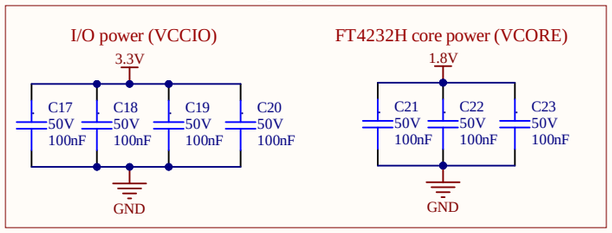
Linear Voltage Regulator for VREGIN (LDO)

LDO specifications:
- DBV Package
- Fixed configuration
- Voltage Input (Min): 2.7 V
- Voltage Input (Max): 5.5V
- Voltage Output (Min): 3.3V
- Current Output: 200mA
- Dropout Voltage 112 mV at 200 mA

Capacitors configuration:
- Cin: 0.1uF (100nF)
- Cinr: 10nF
- Cff: 0F (fixed regulator)
- Cout: 4.7uF (recommended >2.2uF)



Decoupling Capacitors



SpaceLab - Federal University of Santa Catarina			
Project: *flatsat_platform.PrjPcb / [No Variations]*			
Title: *FTDI FT4232 UART Debug Circuit*			
Engineer: *Yan Castro de Azeredo*			Project Code: *FLATSAT1*
Date: 10/8/2020	Revision: *1.0*	Sheet *3* of *3*	Size: A3