	DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE **Regular Summer 2024** **Course: B. Tech. Branch : Electronics and Computer Engineering Semester :VI** **Subject Code & Name: BTECOE604A VLSI Design** **Max Marks: 60 Date:21/06/2024 Duration: 3 Hr.**		
	Instructions to the Students: *1. All the questions are compulsory.* *2. The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.* *3. Use of non-programmable scientific calculators is allowed.* *4. Assume suitable data wherever necessary and mention it clearly.*		
		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	**Explain Ids and Vds characteristics of depletion and enhancement type mosfet.**	**CO1**	**6**
B)	**Explain CMOS Inverter analysis and design. Implement a three-input NOR gate using CMOS logic.**	**CO4**	**6**
C)	**Explain pass transistor logic with neat diagram.Implement NAND and NOR gate using PTL.**	**CO2**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	**Design stick diagram for:** **i) F= $\overline{(A.B)+C}$** **ii) F= $\overline{A+B+C}$**	**CO2**	**6**
B)	**What is Stick Diagram? What are the uses of Stick diagram.Draw the stick diagram and layout for CMOS inverter.**	**CO2**	**6**
C)	**Differentiate between NMOS,CMOS and Bi CMOS inverters.**	**CO1**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	**Explain transmission gate with its symbol.Implement NOR gate using TG.**	**CO2**	**6**
B)	**Explain Pseudo nMOS Logic, Dynamic CMOS LOGIC and clocked CMOS logic.**	**CO1**	**6**
C)	**Explain different alternate gate circuits.**	**CO2**	**6**
Q.4	**Solve Any Two of the following.**		**12**
A)	**Explain twin tub process for CMOS fabrication.**	**CO1**	**6**
B)	**With neat diagram explain different operating regions for a MOS transistor.**	**CO1**	**6**

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C)	**Give the subsystem design considerations of a four-bit adder.**	**CO3/CO4**	**6**
Q. 5	**Solve Any Two of the following.**		**12**
A)	**Explain about different programmable elements in FPGA architectures.**	**CO5**	**6**
B)	**Implement the following functions using PLA.** **A(x,y,z) = ∑m(1,2,4,6) B(x,y,z) = ∑m(0,1,6,7) C(x,y,z) = ∑m(2,6)**	**CO4**	**6**
C)	**Write about the following** **i) Transistor-transistor Logic (TTL)** **ii) Emitter – coupled Logic (ECL)** **iii) CMOS Logic**	**CO4**	**6**
	***** End *****		

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