6T SRAM BASED MEMORY DESIGN

MEL ZG628T: Dissertation

by

SUBODH KANSAL

2020HT80057

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CERTIFICATE

This is to certify that the Dissertation entitled SRAM based memory Design and submitted by SUBODH KANSAL having ID-No. 2020HT80057 for the partial fulfillment of the requirements of M.Tech. <MICROELECTRONICS> degree of BITS, embodies the bona fide work done by him/her under my supervision.

sudhir kumar

Signature of the Supervisor

Place : NOIDA

Date : 15 November

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INTRODUCTION

As microprocessors and other electronic applications become faster, the need for large amounts of data at very high speeds increases, and transmitting data at such high speeds becomes increasingly difficult. To solve this problem, system designers have become more creative in using caching, interleaving, burst mode, and other fast memory access methods as the speed of microprocessors has increased from 10 MHz to 100 MHz, to 500 MHz, and beyond.

Although they can take up a sizable amount of chip space, large SRAM arrays are frequently employed as cache memory in microprocessors and application-specific integrated circuits. When attempting to maximize these chips' performance-to-cost ratio, designers encounter a challenge. Large arrays of high-speed SRAM contribute to improved system performance, but their integration into a chip raises the device's cost. Minimizing the footprint of SRAM cells is the result of balancing these criteria. Thus, SRAM arrays are the densest circuits on a chip because millions of tiny SRAM cells are crammed together. Approximately 33% of the entire semiconductor market is made up of memory chips, which also comprise DRAM, SRAM, ROM, EPROM, EEPROM, and flash memory.

High-performance networking applications will be the main driver of the SRAM memory market. Because of their energy efficiency and bandwidth, Such devices are helpful in electronic equipment including electronic user interfaces, digital cameras, and cell phones.
The IT, communications, consumer electronics, automotive and industrial sectors will experience market trends in a wide range of SRAM applications depending on product type.

Next-generation networks have presented many challenges to telecommunications equipment manufacturers around the world. To ensure high quality of service (QoS), communication devices must now support higher transmission speeds of over 40 Gbps for various types of traffic under peak loadconditions. In addition, you need to use this device to check data destinations and manage data packet traffic. Data complexity such as video, voice and data applications require even greater storage capacity. High-speed SRAM can meet these requirements.

CHAPTER 1

SRAM INTRODUCTION

An essential part of memory design work is Static Random Access Memory (SRAM). It can function in a word-oriented or bit-oriented manner. Data can be accessible in single bits or multiple bits in terms of powers of two when using bit-oriented mode. Compared to bit orientation, word orientation is a little more complicated. In the electronics industry, SRAM is more crucial than ever since consumers seek economical and effective methods for handling and storing data. Low power consumption and little human involvement are important design factors for SRAM cells. SRAM has a fast operating speed, which is essential in the current industry. Its products are a pleasure to work with for designers. For system-on-a-chip designs, which can improve speed and accuracy, SRAM type memory is necessary. The

The SRAM cell is the major application of the system-on-chip in today's market

Importance of SRAM

To ensure reliable and steady SRAM functioning, an SRAM (Static Random Access Memory) cell's design is essential. SRAM designers are forced to raise the packing density as the demand for more on-chip store space persists. As a result, an SRAM cell needs to be as tiny as feasible while yet fulfilling the specifications for yield, speed, power, and endurance. The main element in charge of storing binary data is the SRAM cell. It is a low-power memory that runs without the need for a memory refresh. The quick pace of operation enables versatile application across multiple sectors. Furthermore, the SRAM cell's design minimizes power loss, guaranteeing that other components of the cell remain unaffected while operating.

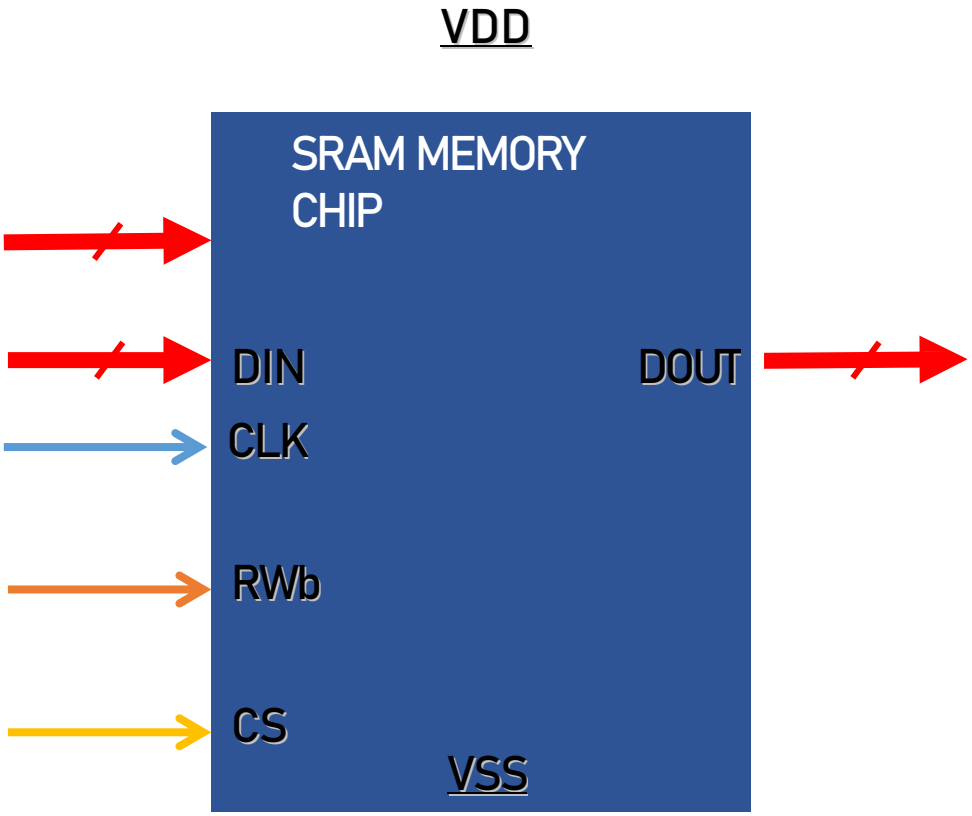


Fig.1 BASIC SYMBOL

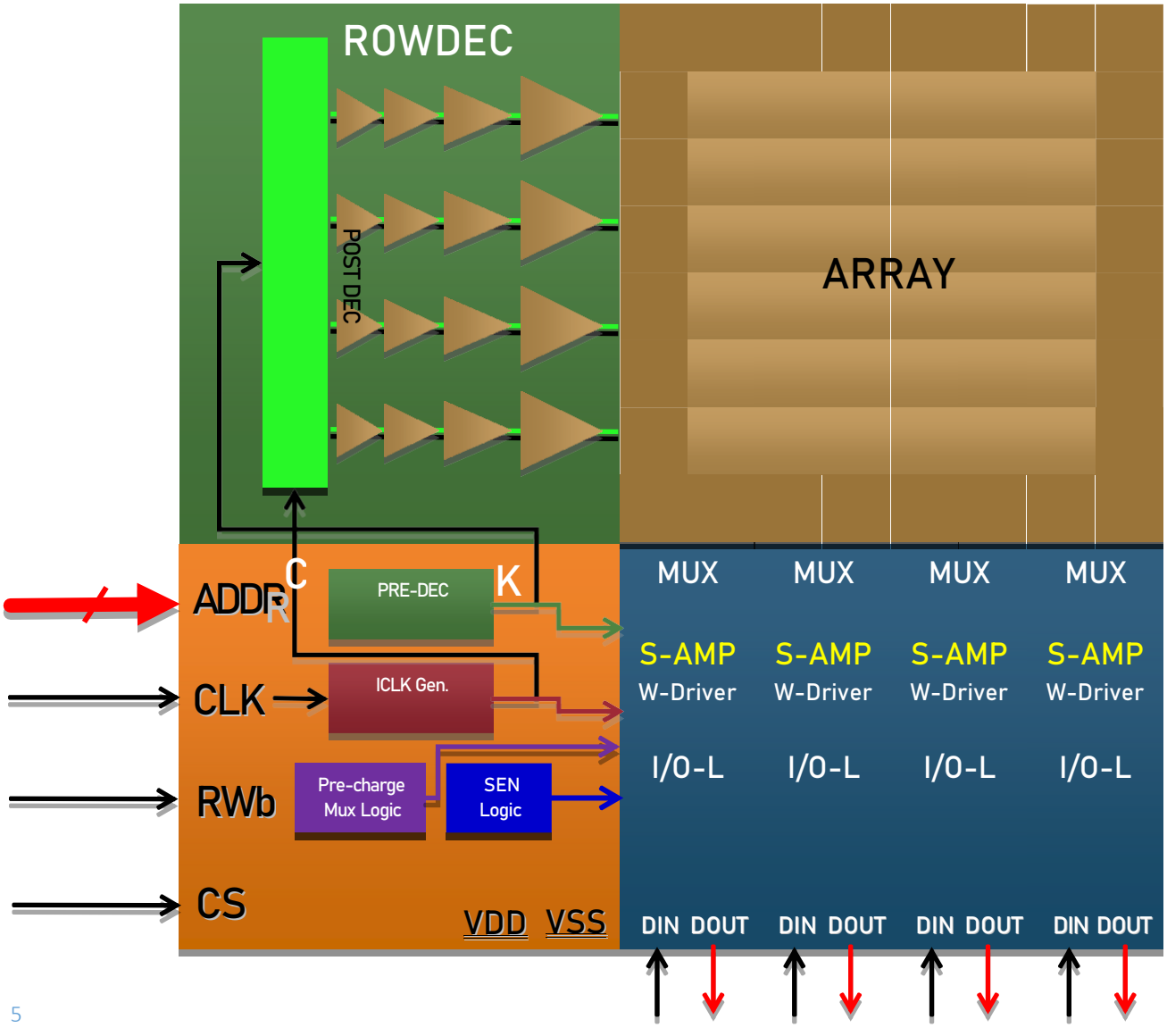
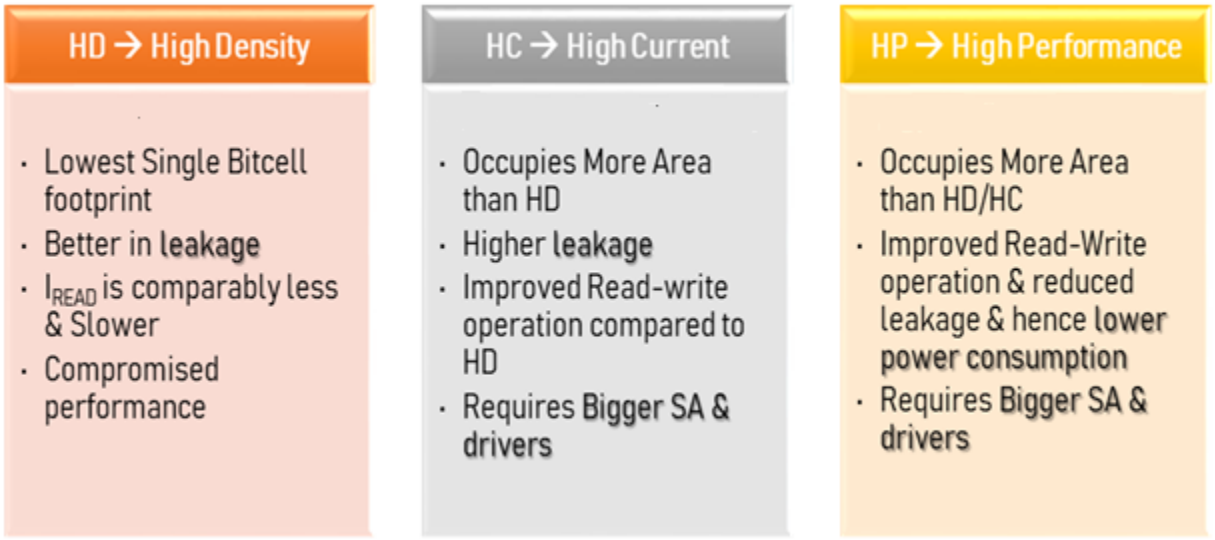


Fig 2. MEMORY ARCHITECTURE

DIFFERENT TYPES OF BITCELL AND THEIR SIZING



BITCELL SIZING INFLUENCE ON PARAMETERS

Access Transistors (AC1 & AC2) : If made bigger

- High I_{READ} → Improves Read access time
- Better Write margin
- High I_{LEAK}

Pull Down Transistors (PD1 & PD2) : If made bigger

- Improved SNM
- Degraded Write margin
- Area Increases

Pull Up Transistors (PU1 & PU2) : If made bigger

- Good SNM
- Degraded Write margin
- Area Increases

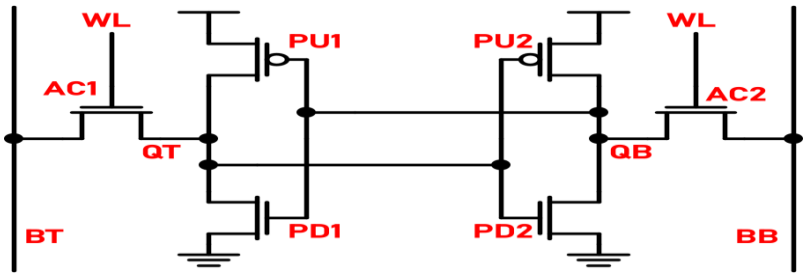


Fig 3 BITCELL

Chapter2

Six-transistor (6T) CMOS SRAM Cell

One of the parts needed to store binary data in SRAM is an SRAM cell. Usually, two cross-coupled inverters are used to make latch and gate transistors. The access transistors serve to effectively isolate the cell when not in use while facilitating admission to the cell during read and write operations. Stable and dependable SRAM operation depends on the SRAM cell's precise design. SRAM designers are also attempting to boost packaging density as a result of the requirement to expand on-chip store capacity.

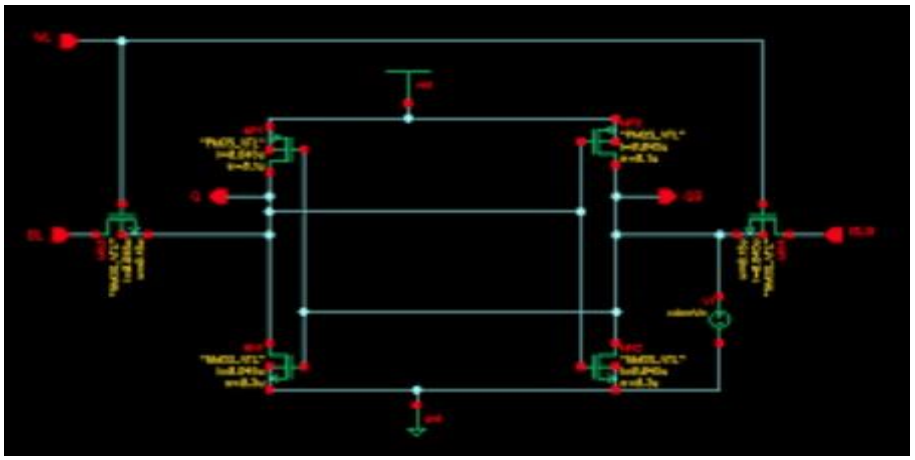
Consequently, it is important to build SRAM cells as tiny as feasible while yet ensuring PPA (power, performance, and area) and stability.

Near-minimal cell transistors are more susceptible to process variations, though. The critical area of the SRAM, which restricts the chip's performance, is determined by the cell arrangement. A key factor in large-scale technologies is cell stability.

Six transistors make up a six-transistor (6T) CMOS SRAM cell, as the following figure illustrates. The SRAM cell is made up of two NMOS transistors (Q5 and Q6) that enable read and write access to the cell, in addition to four transistors (Q1–Q4) arranged in cross-coupled CMOS inverters. When the word line is engaged, access transistors link the two internal nodes of the cell to the true (BL) and complementary (BLB) bit lines. The most widely used cell is the 6-Transistor CMOS SRAM cell because of its outstanding longevity and low power consumption.

low voltage operation. SRAM cells need to be built for dependable reads and writes as well as non-destructive reads. The size of the transistors in SRAM cells must meet these two requirements, which are incompatible.

Figure4: Six-transistor (6T) CMOS SRAM cell Schematic



Read Operation

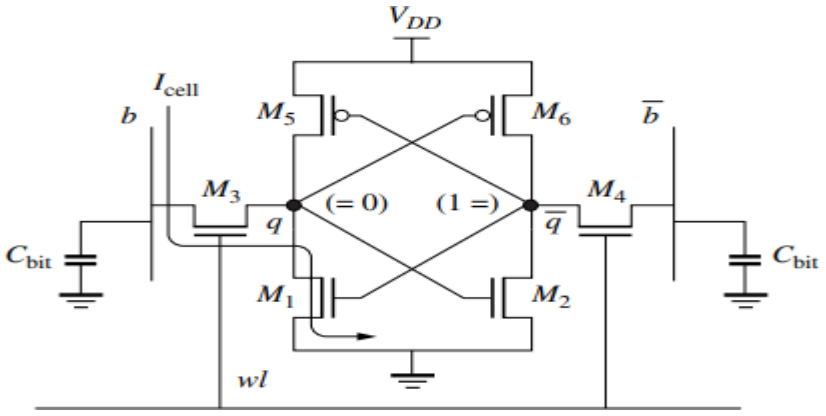


Fig 5 : Read operation

The design of a 6T RAM cell for read operations is described below. Access to transistors M3 and M4 is enabled when the selected line is elevated to VDD. Transistor M3 and transistor M1 allow current to flow to ground while the voltage across the cell stays high. The rectified low output signal from the sense amplifier is subsequently saved in a data buffer. By choosing the magnitude of either transistor M1 or transistor M3, the

voltage at node q is determined. To improve reading stability, transistor M1's conductivity is roughly three to four times higher than transistor M3's. Making sure there is enough current to discharge the bitline in 20–30% of the cycle time is another factor to take into account.

WRITE OPERATION

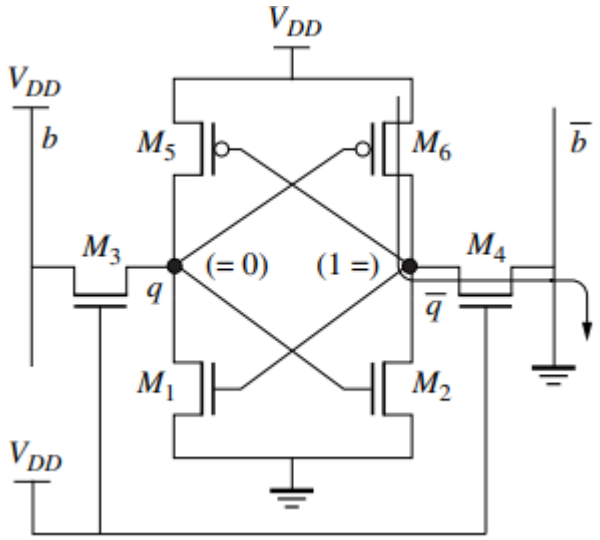


Fig 6 : Write Operation

One of the two bit lines is driven low while the other stays at roughly VDD in order to write a value of zero or one in an SRAM cell. In order to draw the M2 transistor's drain below VSS, the design necessitates that the M4 transistor's conductance be greater than the M6 transistor's. The cell might change into a different condition thanks to its regenerative function.
As a result, transistor M1 will turn off and the drain voltage will increase to VDD due to transistors M5 and M3 pulling up.
Transitor M2 will switch on during the same interval and help transistor M4 drag the output bar to a low value.

Two M6-M4 transistors are used in the design of the SRAM cell to produce a pseudo-NMOS inverter. The above figure depicts the switching procedure.
In conclusion, the general rule of thumb for constructing sizes M6–M4 for an SRAM cell is to make sure that the M4 transistor's conductance is greater than the M6 transistor's in order to create a regenerating effect and transition to a new state. As a result, the Write operation will occur by exceeding the threshold value.

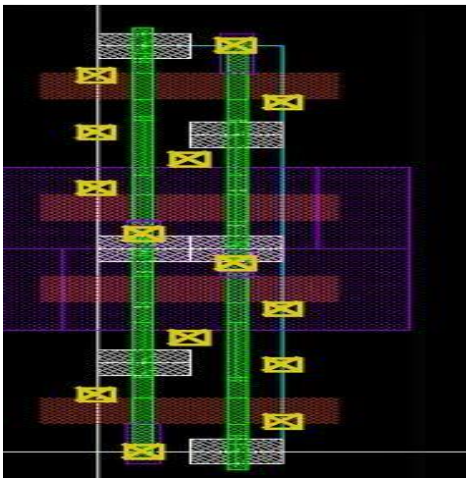


Fig 7 : 6T BITCELL LAYOUT

CHAPTER 3

ARRAY

- ARRAY → Group of Bitcells arranged in ROWS & COLUMNS
- Word-Lines(WL) are shared by all Bitcells present in any single row
- Bit-Line Pairs (BT/BB) are shared by all Bitcells present in any single column
- Number of Physical Rows(PR) = Number of Word-Lines
- Number of Physical Columns(PC) = Number of Bit-Line Pairs
- Total Number of Bitcells in an Array = NW x NB

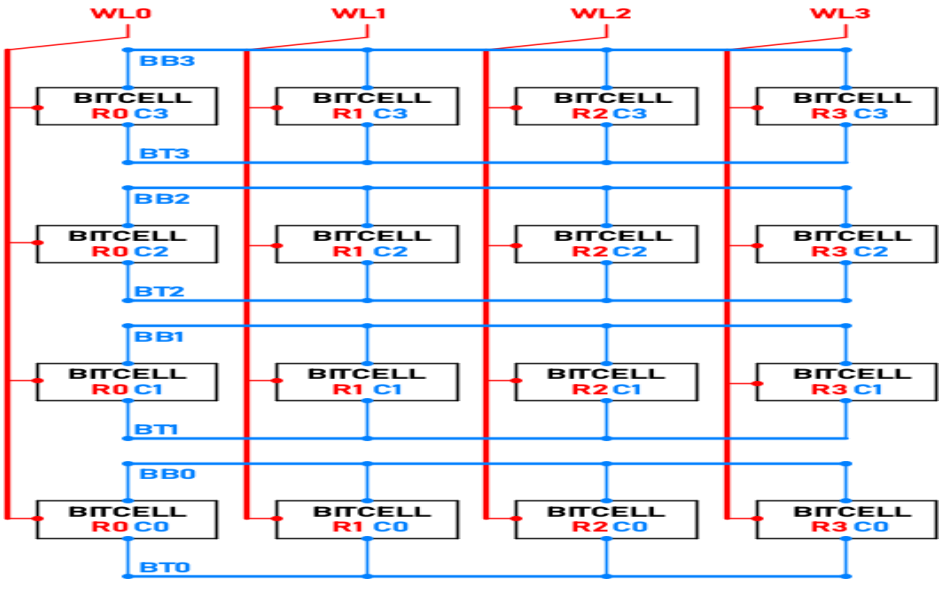


Fig 8 : 4X4 BITCELL

- Sharing of WL across columns
- Sharing of BL across rows

ARRAY EXAMPLES

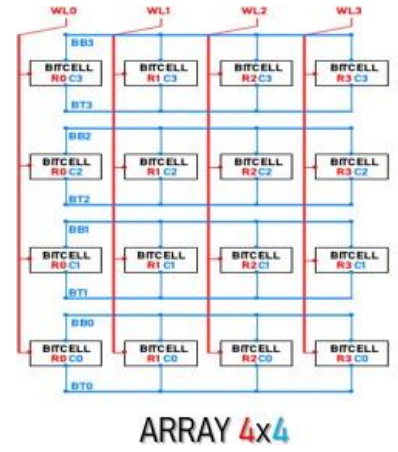


FIG 9 : 4X4 Array

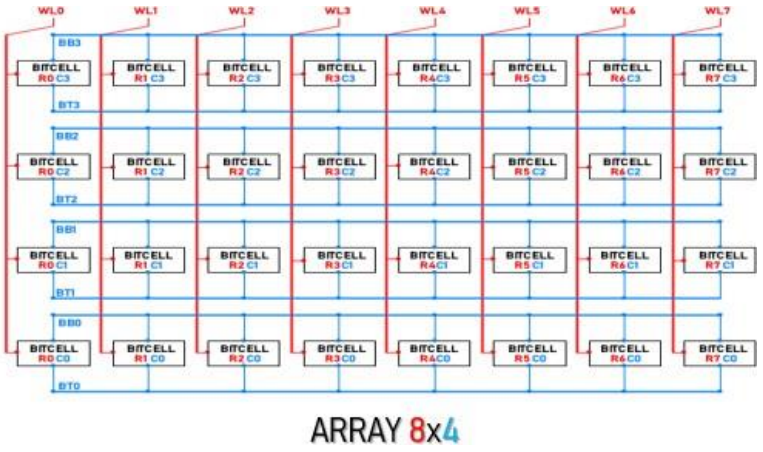
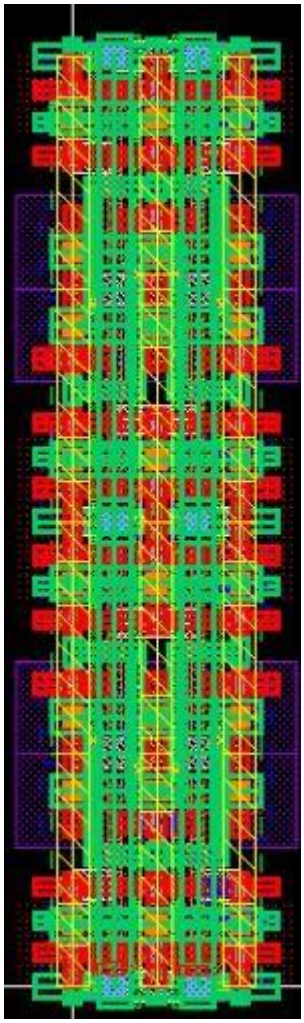
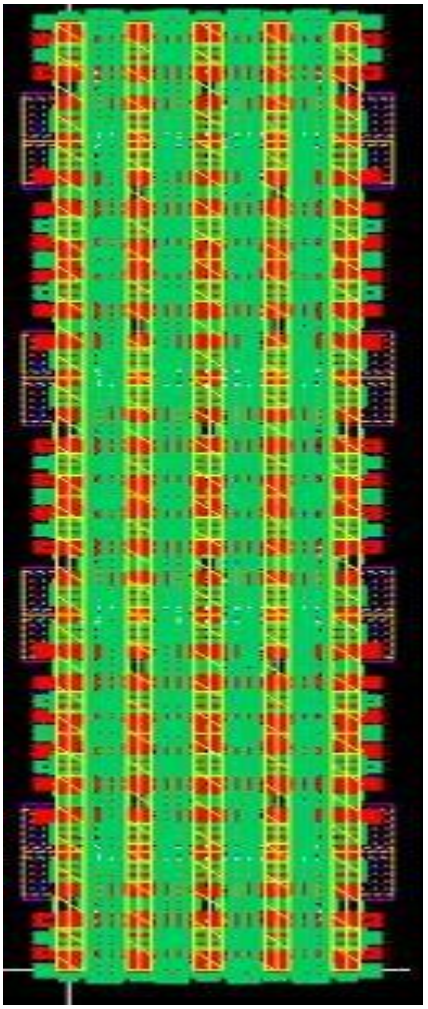


FIG 10 " 8X4 Array



2x2 BITCELL ARRAY



4x4 BITCELL ARRAY

Fig 11 : BITCELL ARRAY LAYOUT

EDGE CELLS

- Edge cells serve to complete end connections and fulfill DRC requirements within a block.
- They enhance reliability and yield by maintaining an identical RC environment for the Bitcells at the perimeter.
- Typically, edge cells consist of tap cells and/or dummy bitcells.
- Dummy bitcells, created by shorting all transistor terminals to supply rails, don't store data and aren't involved in read/write operations. They solely mimic the RC environment for boundary bitcells.
- Separate schematics and symbols are generated for each edge cell to ensure LVS cleanliness.
- In lower technology nodes, device formation can be hindered by CUT layers, there is no need for schematic creation for edge cells to clean LVS.
- Various types of edge cells include left/right, top/bottom, corner, and mid-tap cells.
- Mid-tap cells are utilized to provide tap connections within a larger array, preventing latch-up.

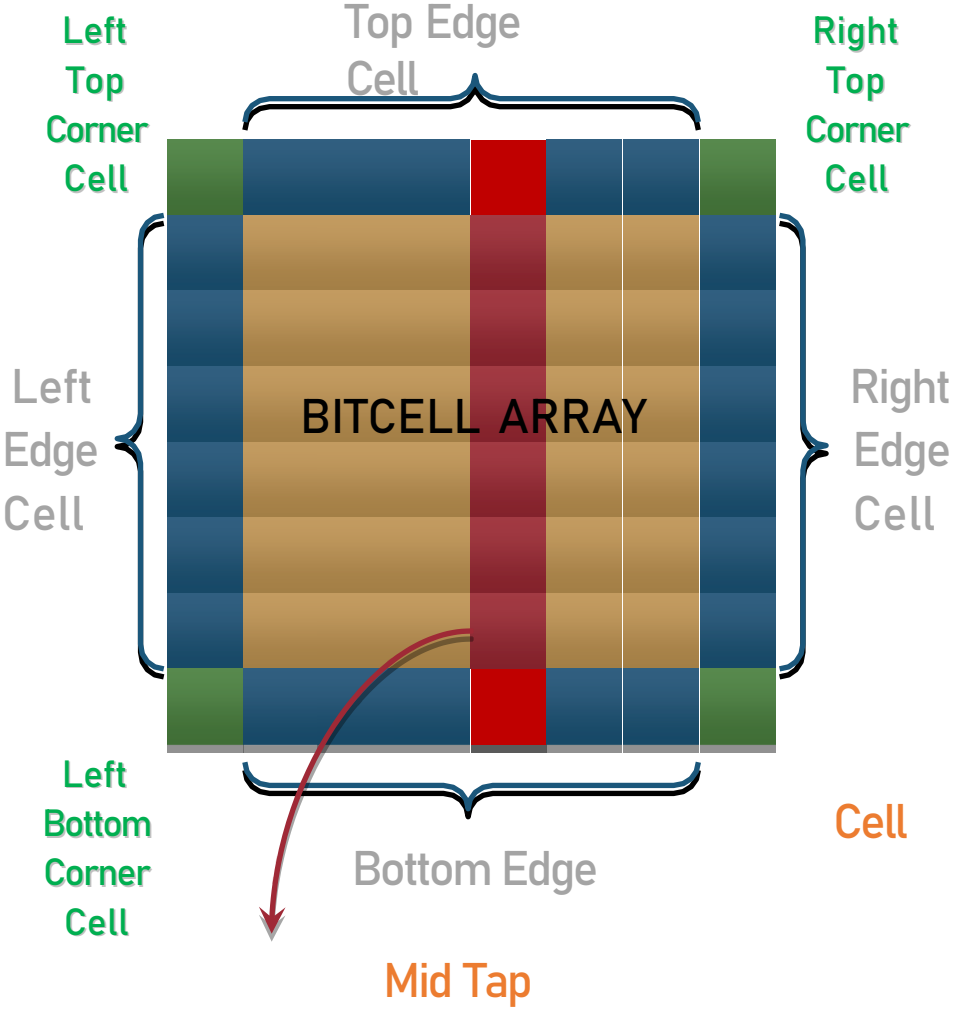


FIG 12 : BITECELL ARRAY WITH EDGE CELLS

LEFT EDGE CELL / BOTTOM EDGE CELL

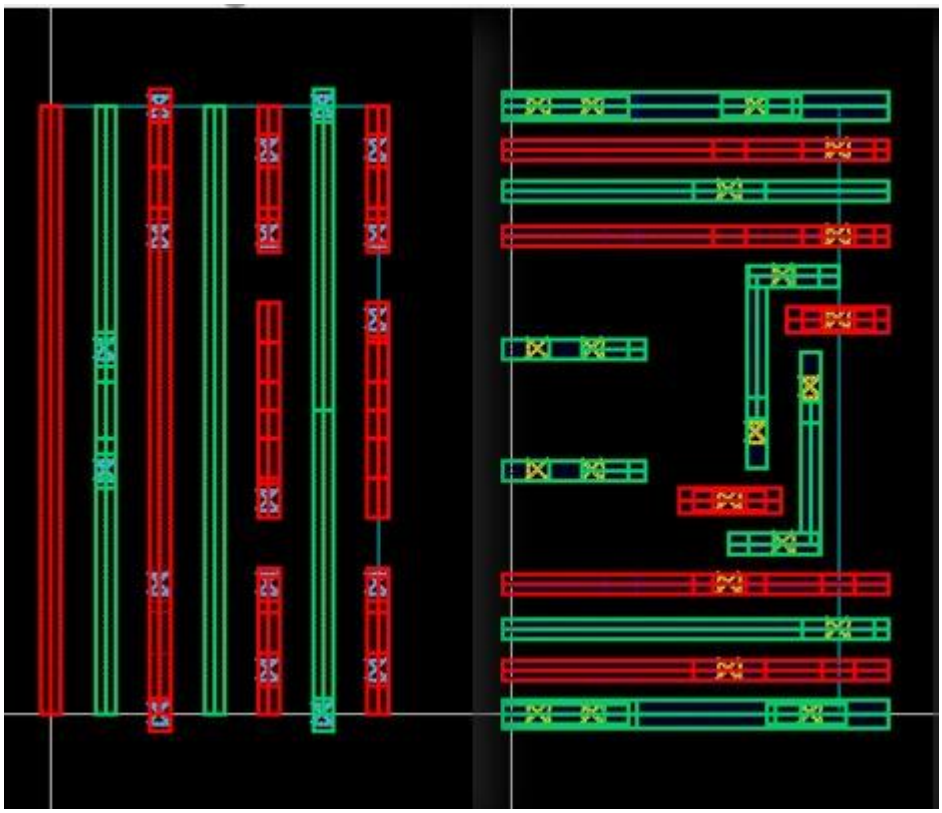
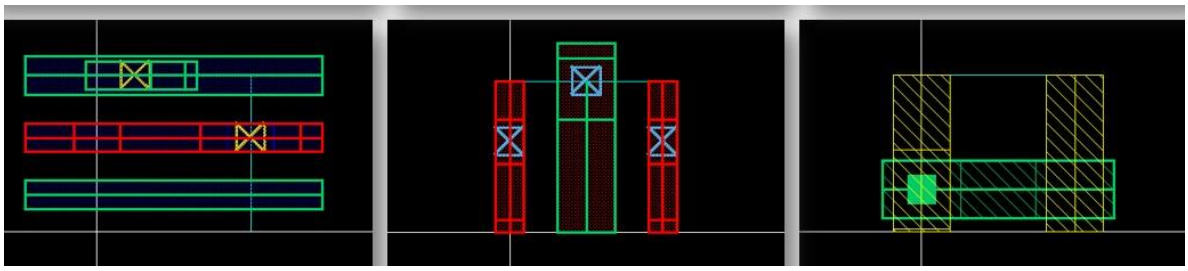


Fig 13 : EDGE CELLS



CHAPTER 4

ROW DECODER

Row decoders are essential components in memory systems that are used to generate WL selection signal to access one row at a time. The need for row decoders arises when working with an N-word memory where each word is M bits wide. In such cases, a general approach is to arrange the memory words in a linear fashion.

The SRAM employs two different kinds of decoders: row and column decoders. There is a significant influence of these decoders' design on the power consumption and SRAM performance. While column decoders choose specific bitline pairs from the sets of bitline pairs in the selected row, row decoders are required to select one row of WL from a set of rows in the array based on address bits.

In all random-access memories, the row and column decoders are necessary components. Decoder design may play a major role on memory access time and power consumption. Both read-only and read-write applications use similar designs. Using an n-bit address, row decoders generate twon outputs, one of which is active. Naturally, the address that is applied to the memory directly determines which one is enabled. AND gates can be used to implement the decoder, or NOR gates that accept inputs in every possible combination. In this case, there are two address bits, and we need the true and complement of each address bit. The figure displays the output line that each input combination activates. Observe that all but one of the outputs are typically low.

PRE DECODER & POST DECODER

A two-stage decoding scheme is used in which a pre and post-decoder are employed. The pre-decoder is placed in the control block while the post-decoder is placed in the RowDec block. Based on the size of the Column Mux, the lower LSB of the Address bits are used as select lines while the remaining address bits are directed towards the pre-decoders.

For instance, consider a compiler with a maximum of 512Byte memory, where the total number of bits is 512 x 8 = 4096 with 1 word size being 8 bits. The number of address bits is log2(512) = 9. Let the c-mux size be 4, then the number of physical rows is 2^(9-2) = 2^7 = 128.

Since there are 9 address bits (A8-A0) and the column mux size is 4, A1 and A0 bits will be fed to the column mux as select lines while A8 to A2 will be fed to pre-decoders. The pre-decoders used are a two:four Decoder, two:four Decoder, and three:eight Decoder. The post-decoder consists of multiple segments of 4:16 decoder.

If a two-stage decoding scheme is not used, the size of the decoder will be very huge (7:128 Decoder). As a result, the circuit becomes more complicated and occupies more chip area.

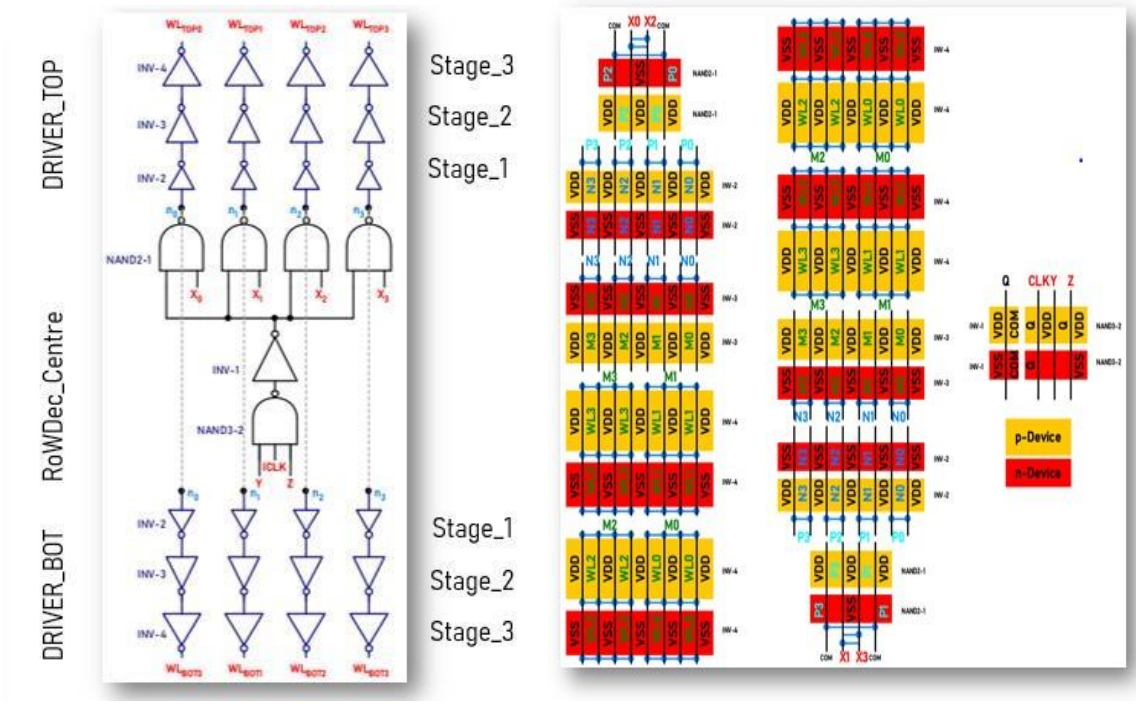
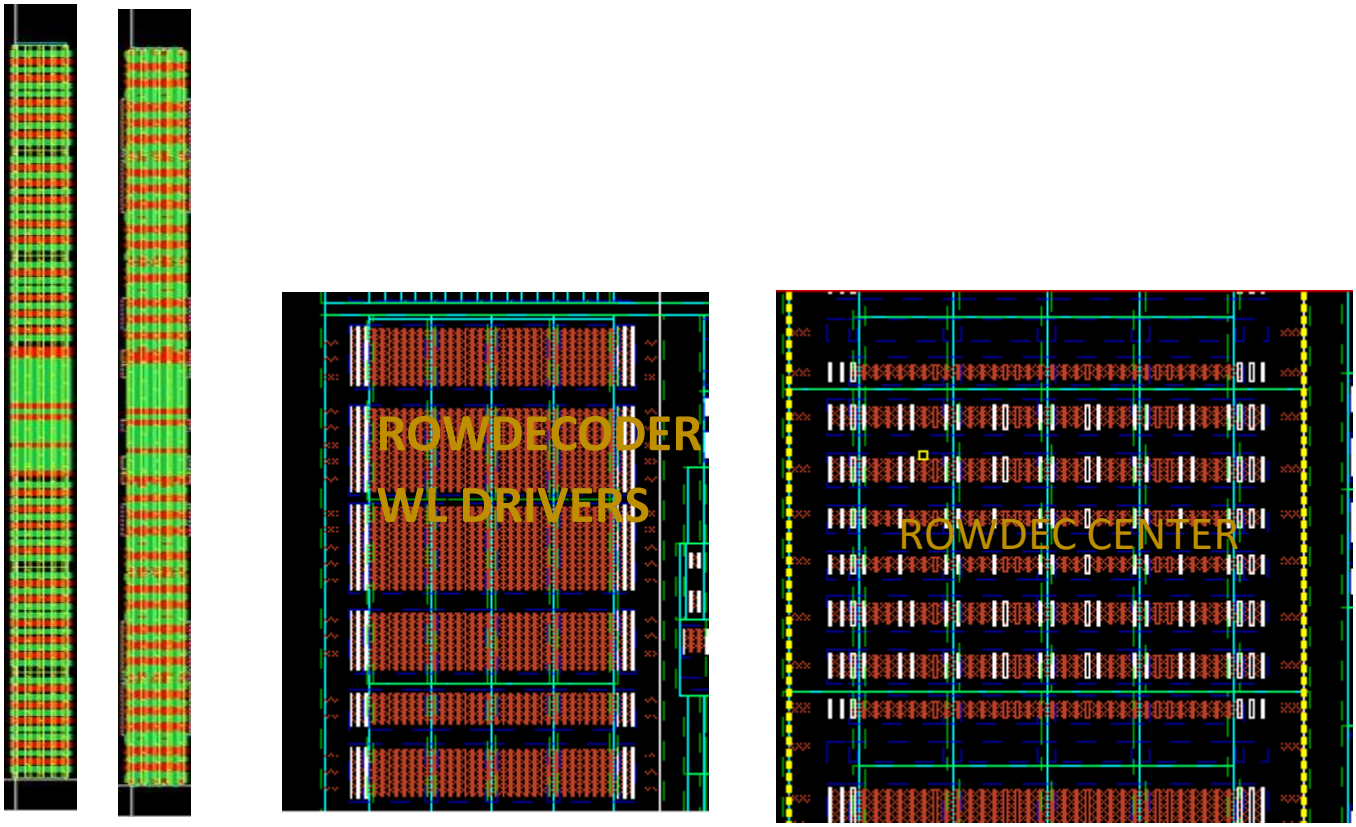


FIG 14 ROW DECODER STICK DIAGRAM (BASIC CIRCUITARY)



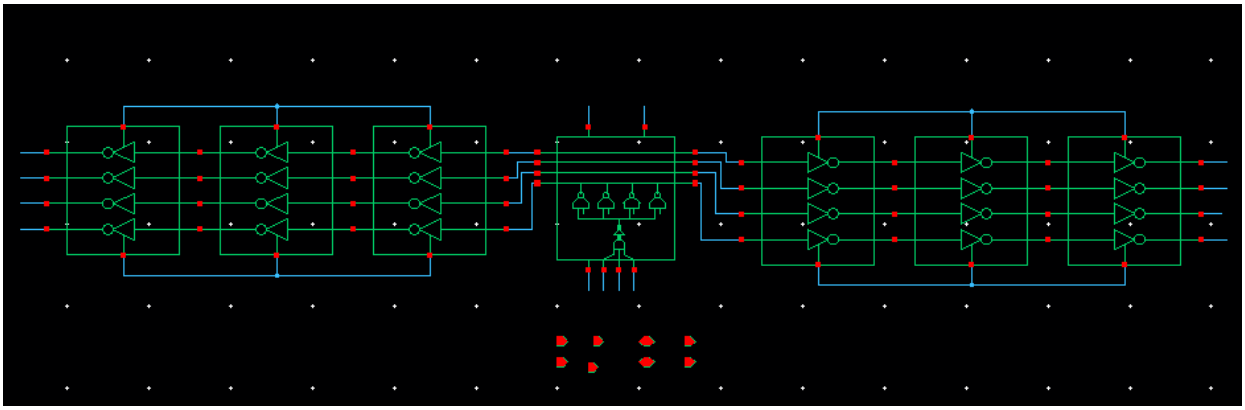


FIG 15 : ROW DECODER SCHEMATIC/ LAYOUT

CHAPTER 5

COLUMN IO

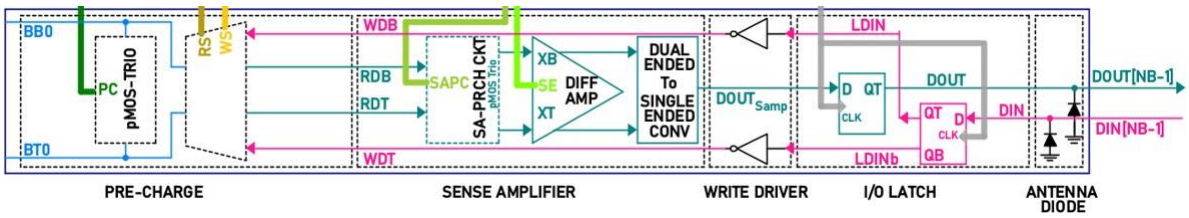


FIG 16 : COLUMN IO

PRECHARGE

A "crowbar" circuit, which consists of three transistors, is commonly used to pre-charge VDD. It is composed of one additional PMOS transistor that is coupled to the two bit lines and equalizes their potentials, and one PMOS transistor that pulls each bit line to VDD. A different strategy would be to pre-charge the bit lines to VDD using just the two PMOS transistors and leave the third PMOS alone.
This circuit is turned off for the particular column being read during a read operation, while the precharge is kept on for the inactive columns. The cell competes with the pre-charge circuit when the precharge is in the active state and the word line is high on the unselected columns. Even so, on a cell level, the small amount of current used by this disagreement is typically quite acceptable.

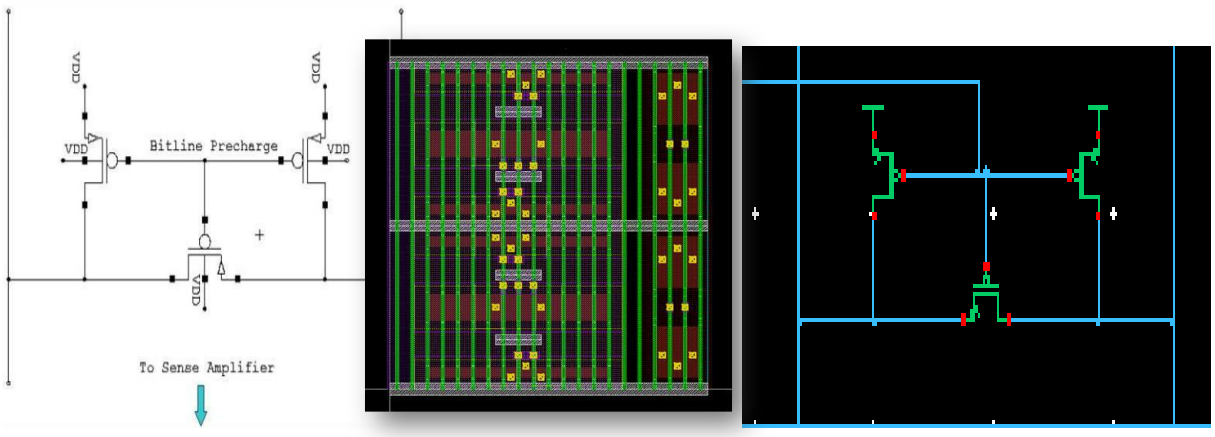


FIG 17 : PRECHARGE

SENSE AMPLIFIER

It is the Memory's sole analog circuit.
To achieve increased density and higher efficiency, a large number of bit-cell are connected to a common bit-line pair.
Due to the increased load (capacitance) on the bit-line pairs, a differential sense amplifier must be used in order to operate at a quicker speed and with less power consumption.

Instead of waiting for a complete rail-to-rail swing, the sense amplifier senses a tiny differential voltage swing on the bit-lines (BT/BB) to identify the data being read. hence reducing the amount of time needed to wait for the bit-line to fully discharge. Consequently, Read Access Time is improved.
After that, the small differential voltage (ΔV) is amplified so that logic operating outside of the memory can correctly comprehend the data.
In order to keep the internal nodes precharged at VDD before sensing operation begins, SA incorporates pMOS Pass transistors controlled by SE (Sense Amp. Enable), which offers separation of SA internal nodes XT/XB from RDT/RDC Precharge and Equalizer circuit controlled by SP (Sense Amp. Precharge Enable).
The VLSA, or latch-based differential amplifier, is in charge of detecting and amplifying small differential offset voltages. It is based on cross-coupled inverters.
Tail MOS (SNT) is managed by SE, allowing SA to increase the differential voltage.
To change the double-ended output to single-ended, two inverters are needed. Dout: This is a clever method of transforming complementary dual-ended signals into full-swing single-ended signals.

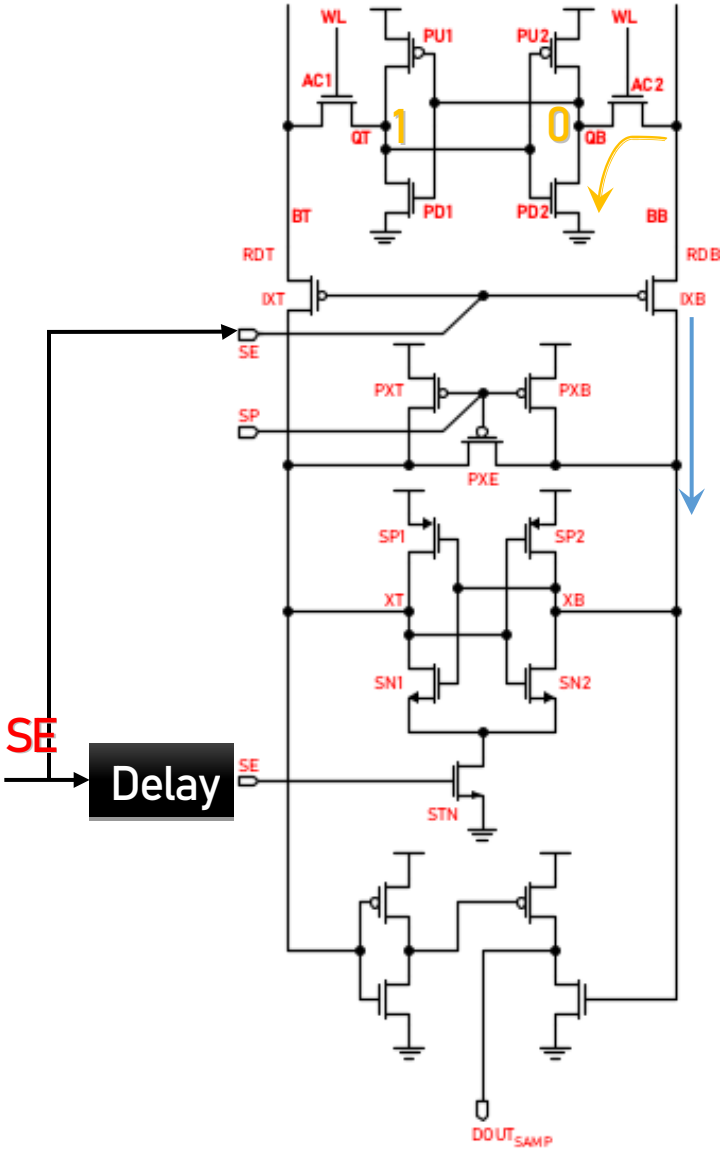


FIG 18 : SENSE AMPLIFIER

Write Driver , I/O Latch, Antenna Diode

- Write driver circuit
  - It is generally an inverter/buffer with proper sizing each driving
  - Proper sizing is very much important for a successful write operation & an optimum flip time
  - Designed to drive maximum RPB
- I/O Latch:
  - This circuit is necessary for the controlled of data in & out of the memory
  - Latches control the movement of data by holding & clocking it
  - Clocked by internal clock
- Antenna Diodes:
  - To avoid antenna effects

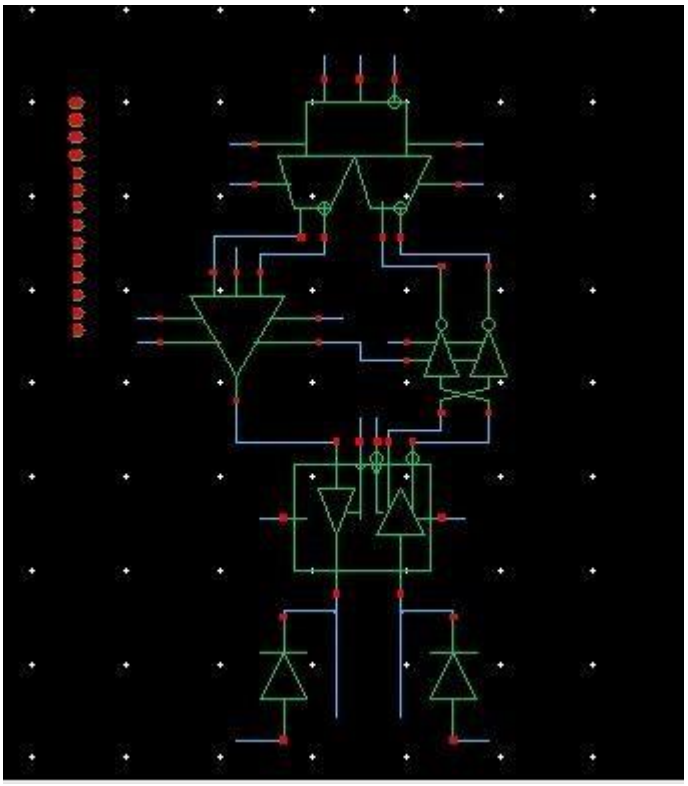


Fig 19 : SCHEMATIC IO

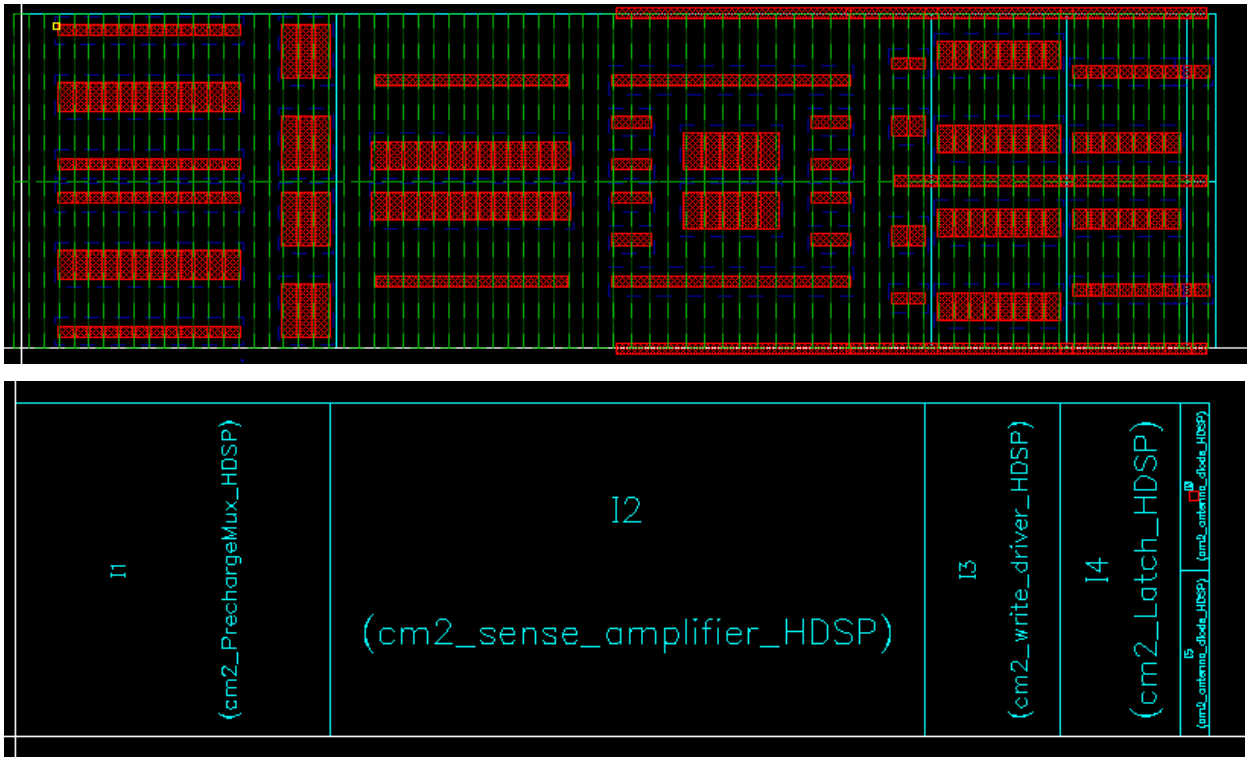


FIG 20 LAYOUT IO

CONTROL UNIT

It is made up of circuits for clock pulse generators, address latches, and pre-decoders. The pre-decoded signals are sent by the control unit to the I/O block's row decoders and column mux in order to access a specific cell for read or write operations. Control generates pre-decoded signals for the word-line decoder.
block for which two, three, or eight decoders were utilized. Eight select lines are provided to the column multiplexer by the 3 to 8 decoder in the column mux control block.

A clock pulse generator circuit produces a horizontal clock pulse for column muxing and a vertical clock pulse for choosing a word line. In order to reduce the dynamic power, the same circuit additionally resets the clock pulses, both horizontally and vertically, whenever the desired memory address is accessed.

Control block Mainly comprises of following sub blocks & pins

1. Pre-decoder logic
2. Address latches
3. Internal clock generator logic
4. Sense enable generator logic
5. Column mux control signal generator logic
6. Precharge control logic
7. I/P pins
    1. CS → Chip Select: Used to enable Memory chip
    2. CLK → Global Clock: Used to generate internal clock & synchronize the memory operations
    3. ADDR[8:0] → Address Bits
    4. RWb → Read Enable (or Write Enable Bar)
        - high → read
        - low → write
    5. Supply → VDD,VSS

Pre-Decoders & Address Latches

- Address latches
    - They are used to latch all the addresses.
    - D latches are used for this purpose
    - The latched address bits are then sent to C-Mux & pre-decoders (X-Dec, Y-Dec, Z-Dec) to generate X,Y,Z pre-decoded signals (totally 16 signals) which is then sent to RowDec

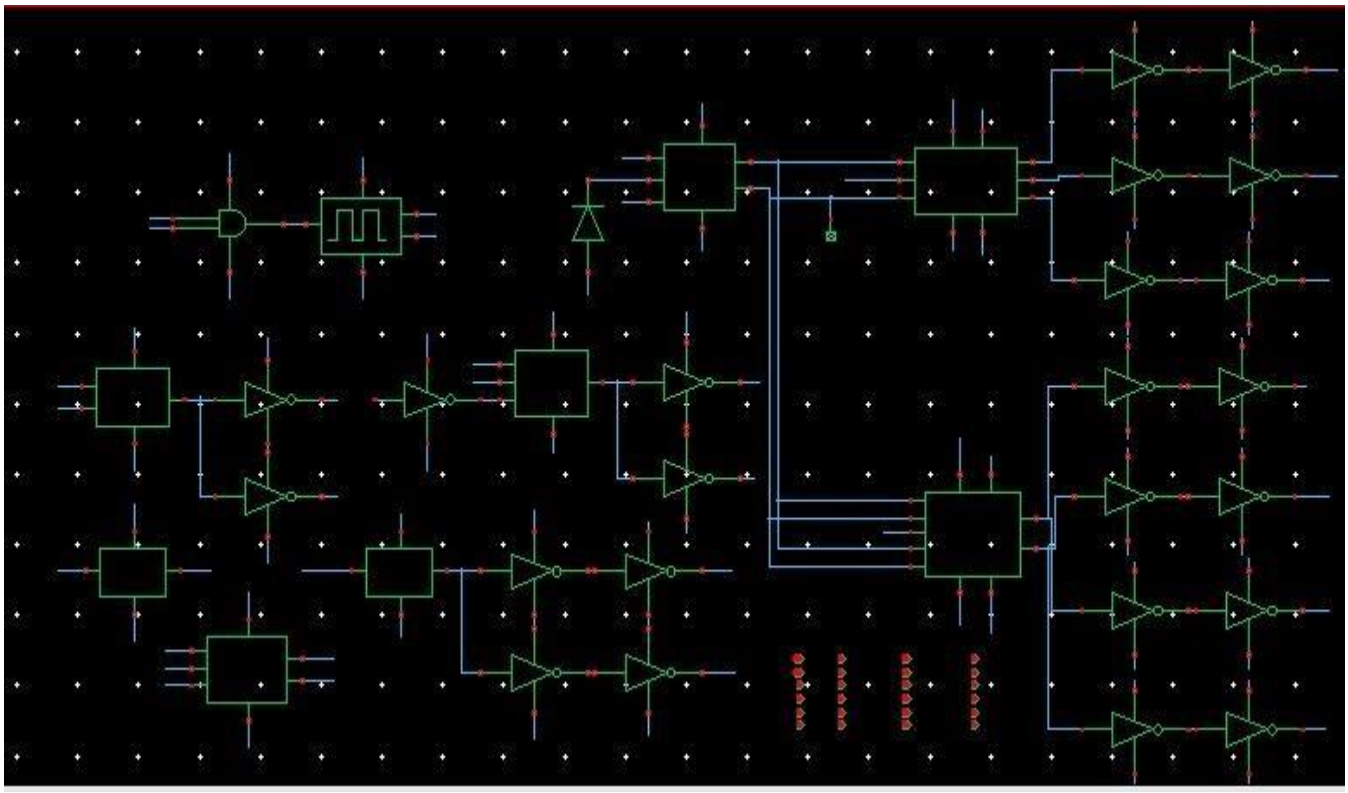


FIG 21 SCHEMATIC CONTROL

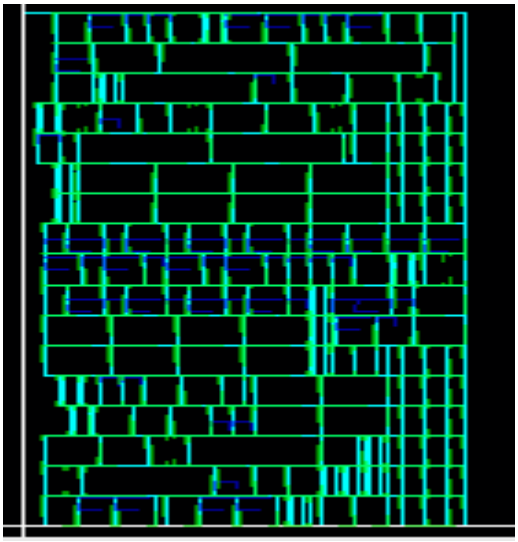


FIG 22 LAYOUT CONTROL

TOP LEVEL 16x32 BK1 MEMORY

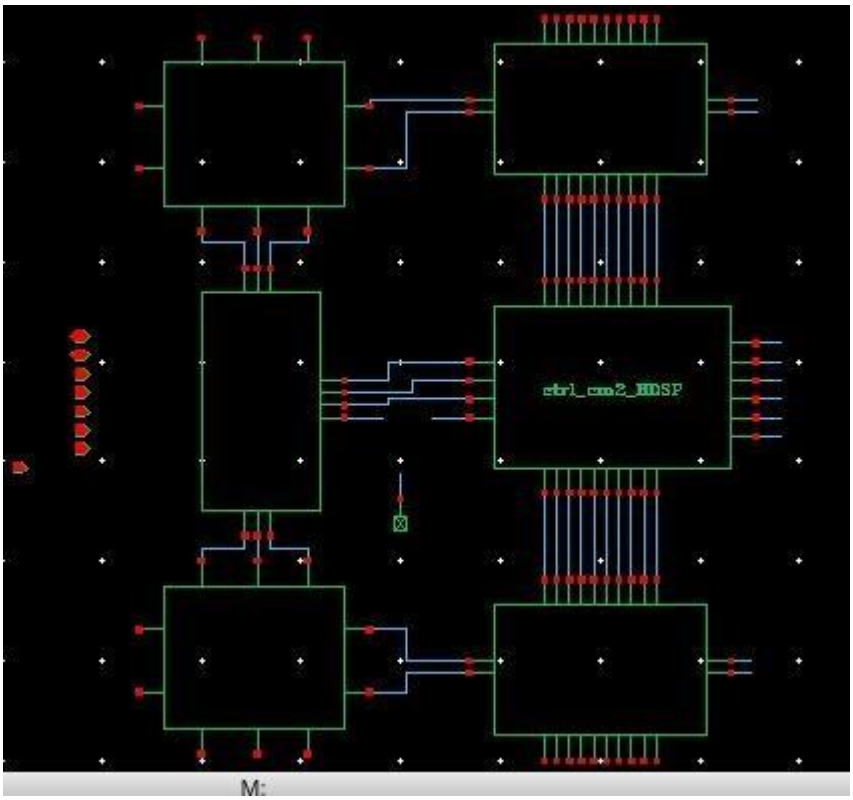


FIG 23 TOP LEVEL SCHEMATIC 16X32

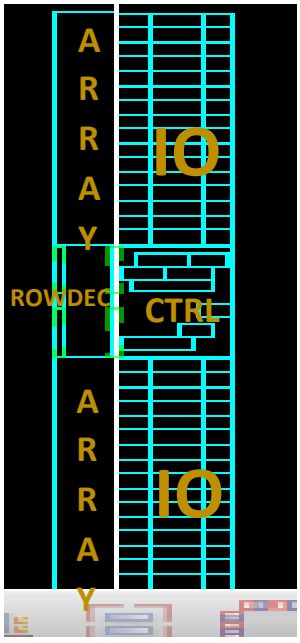


FIG 24 TOP LEVEL LAYOUT 16x32 MEMORY

SUMMARY

Worked on 18nm having poly pitch of 86 and fin pitch of 48nm for the 16x32 memory with Center decoding & Single Bank for both schematic and layout , but major work done on the layout side to achieve the best Area .

Key blocks such as BITCELL, BITCELL ARRAY, and ROW DECODER , IO , CONTROL have been completed with both layout and schematics.

Significant strides have been made in completing essential blocks, laying a strong foundation for further development.

This achieved milestone reflects a substantial accomplishment in the development of the SRAM-based memory design.

Both LVS and DRC is clean for the 16x32 memory that includes all the blocks including Array , Rowdec , Control & IO cells.

The top metal layer is Metal 4

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BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

WORK-INTEGRATED LEARNING PROGRAMMES DIVISION

First Semester 2024-2025

MEL ZG628T: Dissertation

BITS ID No. : **2020HT80057**

NAME OF THE STUDENT : **SUBODH KANSAL**

EMAIL ADDRESS : **2020HT80057@WILP.BITS-PILANI.AC.IN**

STUDENT'S EMPLOYING ORGANIZATION & LOCATION : **SYNOPSYS India PVt Ltd Noida**

SUPERVISOR'S NAME : **Sudhir Kumar**

SUPERVISOR'S EMPLOYING ORGANIZATION & LOCATION : **SYNOPSYS India PVt Ltd Noida**

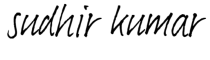
PROPOSED DISSERTATION TITLE: 6T SRAM BASED MEMORY DESIGN

S. No.	Evaluation Component	Excellent	Good	Fair	Poor
1.	Final Project Report		✓		
2.	Final Seminar and Viva-Voce		✓		

S. No.	Evaluation Criteria	Excellent	Good	Fair	Poor
1	Technical/Professional Competence		✓		
2	Work Progress and Achievements	✓			
3	Documentation and expression		✓		
4	Initiative and Originality		✓		
5	Research & Innovation		✓		
6	Relevance to the work environment	✓			

Please ENCIRCLE the Recommended Final Grade: Excellent / Good / Fair / Poor

Remarks of the Supervisor: Report has good and detailed explanation. The memory designed is working as per expectation.

	Supervisor	**Additional Examiner**
Name	Sudhir Kumar	Jaspreet Singh
Qualification	Mtech (20+ Exprerience)	Ph.D (18+ Exprerience)
Designation	Director R &D	Sr Manager R &D
Employing Orgn and Location	Synopsys India Pvt Ltd	Synopsys India Pvt Ltd
Phone No. (with STD code)	9971700386	9999231740
Email Address	sudhirk@synopsys.com	singhj@synopsys.com
Signature		

Checklist of items for the Final Dissertation Report

This checklist is to be attached as the last page of the report.

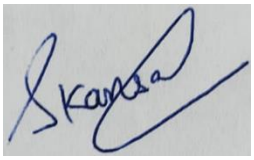
This checklist is to be duly completed, verified and signed by the student.

1.	**Is the final report neatly formatted with all the elements required for a technical Report?**	Yes
2.	Is the Cover page in proper format as given in Annexure A?	Yes
3.	Is the Title page (Inner cover page) in proper format?	Yes
4.	(a) Is the Certificate from the Supervisor in proper format? (b) Has it been signed by the Supervisor?	Yes Yes
5.	Is the Abstract included in the report properly written within one page? Have the technical keywords been specified properly?	Yes Yes
6.	Is the title of your report appropriate? **The title should be adequately descriptive, precise and must reflect scope of the actual work done.** Uncommon abbreviations / Acronyms should not be used in the title	Yes
7.	Have you included the List of abbreviations / Acronyms?	Yes
8.	Does the Report contain a summary of the literature survey?	No
9.	Does the Table of Contents include page numbers? (i). Are the Pages numbered properly? (Ch. 1 should start on Page # 1) (ii). Are the Figures numbered properly? (Figure Numbers and Figure Titles should be at the bottom of the figures) (iii). Are the Tables numbered properly? (Table Numbers and Table Titles should be at the top of the tables) (iv). Are the Captions for the Figures and Tables proper? (v). Are the Appendices numbered properly? Are their titles appropriate	Yes Yes Yes Yes Yes Yes
10.	Is the conclusion of the Report based on discussion of the work?	Yes
11.	Are References or Bibliography given at the end of the Report? Have the References been cited properly inside the text of the Report? Are all the references cited in the body of the report	Yes Yes Yes

12.	Is the report format and content according to the guidelines? The report should not be a mere printout of a Power Point Presentation, or a user manual. Source code of software need not be included in the report.	Yes

Declaration by Student:

I certify that I have properly verified all the items in this checklist and ensure that the report is in proper format as specified in the course handout.



Place: NOIDA **Signature of the Student**

Date: 15 November **Name: SUBODH KANSAL**

ID No.:2020HT80057