

$DB = f^0$

Ex

void writer (void)

{ while (1)

{ down (DB);

Database;

up (DB);

}

W1 : down (DB)

Database;

W2 : down (DB)

↳ Busy
Wait.

}

int $r_c = 0$; || ~~mutex~~

~~void reader (void)~~

~~down (mutex);~~

~~$r_c = r_c + 1$;~~

~~up (mutex);~~

~~down (DB);~~

~~Database;~~

C.S. (fig) 7.5.3 p1

~~up (DB);~~

~~down (mutex);~~

~~$r_c = r_c - 1$;~~

~~up (mutex);~~

void reader (void) { while (1) . . . }

{ down (mutex)

$r_c = r_c + 1$;

if ($r_c == 1$)

down (DB) || No writer usage

up (mutex)

[DB]

|| CS

down (mutex);

$r_c = r_c - 1$;

if ($r_c == 0$) up (DB) || (writer can access)

$$r_c = \emptyset \times \cancel{\emptyset} \quad DB = \emptyset \times \emptyset \quad \text{mutex} = \emptyset \times \emptyset$$

R-W1:

r_1 : not down (mutex)

r_2 : down(mutex) \Rightarrow sleep \rightarrow BW

$$r_1 : r_c = r_c + 1 = 0 + 1 = 1$$

if ($r_c = 1$)

w_1 : down (DB)

Database

r_1 : down (DB) \parallel BW

w_1 : up (DB)

r_1 : down (DB) = $\emptyset \times$

up (mutex)

Database

r_2 down (mutex) $\times \emptyset$

$$r_c = r_c + 1 = 1 + 1 = 2$$

w_2 = down (DB) ($\emptyset \times \emptyset$) \Rightarrow BW

r_2 : Database

up (mutex) $\times \emptyset$

Database

r_1 : down (mutex) $\rightarrow r_c = 0$, $r_w = 0$ (for $r_c < 0$)

$r_c = r_c + 1$ (if writer - avoid race)

→ →

r_2 : down (mutex) \rightarrow $BW(r_c)$ without bias

→ → (writer) with bias

r_1 : if $(r_c == 0)$ \Rightarrow (false).

→ → up (mutex).

r_2 : ~~do~~ down (mutex).

$r_c = (r_c == 0)$ up (DB) ✓

up (mutex)

→ → $r_c = 1$

Ques.) What happens if you interchange down mutex and $r_c = r_c + 1$ in the reader code?

option A

(A) No problem, the solution will work fine.

(B) Multiple readers are not allowed

(C) Reader and writer (both) can access database at the same time.

(D) None of the above. (bias) without bias

→ → $r_c = 0, 1, 2, \dots$

$|r_2| = r_c + 1 \neq \rightarrow$ Not atomic.

→ → (writer) bias

Alternate : Both r_1 & r_2 execute $r_c = 2$ and then got preempted and then writer executed (down (DB)) But readers without checking r_c , directly jump to DB along with writer).

→ → (writer) bias

Ques

`int R=0, W=0;` (initially) and μ = 1
 Semaphore mutex = 1

`void Reader (void)`

- { L₁: down(mutex)
- { if ($W=1$)
- { ① up(mutex)
- go to L₁;
- }
- else
- { R = R+1;
- ② up(mutex)

Database

`void down (mutex)`

~~decrease R = R-1~~

`up (mutex)`

{ }

`void Writer (void)`

{ L₂: down(mutex)

{ if (i \leq 1) { ③ } | W=1 or R \geq 1

{ up(mutex)

goto L₂;

else { } | increase R by 1

W=1;

up(mutex);

Database

down(mutex); W=0 up(mutex); }

OPERATIONS

1

2

3

what should be the values of blanks ① ② ③ in order to synchronize the R/W problem.

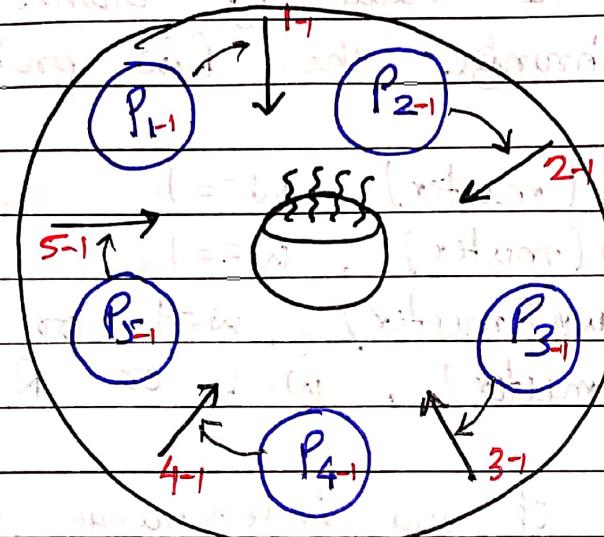
- (A) up(mutex), down(mutex) - $w=1$
- (B) down(mutex), up(mutex), $w=1$
- (C) down(mutex), up(mutex), $w=1$ or $R \geq 1$
- (D) up(mutex), up(mutex), $w=1$ or $R \geq 1$.

Ques 2.) What happen if you interchange $w=1$ and up(mutex) in above problem. in writer code.

- (A) No problem
- (B) Multiple Reader are not allowed
- (C) only Multiple writer are allowed in DB
- (D) Reader and writer access DB at the same time

Dining Philosophers Problem

Deadlock ✓
 (as there
 is no
 progress)



void Philosophers (int i)
 {

while (1)

{ thinking ();
~~left~~ take fork (i); // taken left fork
 take fork ((i+1)%N); take right fork

eat ();

put fork (i);

put fork ((i+1)%N);

}

Solution :

T = 0

H = 1

E = 2.

(Thinking)

(Hungry)

(Eating)

0 1 2 3 4

State

0	0	0	0	0
---	---	---	---	---

- Initially philosophers are in thinking state.
- When they feel hungry, go in eating state.
- When all philosophers get hungry at the same time, all will ~~become~~, try to pick up the left fork first and when they try to attempt to take the right fork, the right fork is not available. Then all the philosophers will wait for each other for the right fork and this results in deadlock position.
- The solution of the above problem is:

```

#define N 5 // No of philosophers
#define LEFT (i+N-1) % N // Left philosopher
#define RIGHT (i+1) % N // Right philosopher
#define THINKING 0
#define HUNGRY 1
#define EATING 2

Semaphore mutex = {value=1, name="Mutex"}; // shared resource
Semaphore S[N] = {value=0, name="S[i]"}; // all initialized to 0
int state[N]; // an array to keep track of states
    
```

void philosopher (int i)

{

 while (1)

 {

 Thinking ();

 take forks (i);

 eat ();

 put forks (i);

 }

}

take forks (int i)

```
{
    down( mutex );
    state[i] = HUNGARY;
    test(i);
    up(mutex);
    down(s[i]);
}
```

put forks (int i)

```
{
    down( mutex );
    state[i] = THINKING;
    test(LEFT);
    test(RIGHT);
    up(mutex);
}
```

void test (int i)

```
{
    if state[i] == HUNGARY && ( state[LEFT] != EATING
        && state[RIGHT] != EATING )
        {
            state[i] = EATING;
            up(s[i]);
        }
}
```

RED

C

D

E

F

G

H

I

J

K

L

M

N

O

P

Q

R

S

T

U

V

W

X

Y

Z

Apoorv Panse, iGate Bhilai

MUTEX : mutex is binary semaphore used by philosopher in mutual exclusion manner.

state[N]: Integer array used to keep track of every philosopher's state. Initially all philosophers will be in thinking state.

S[N]: Array of binary semaphore initially all are assigned to zero.

Ques Assume the philosophers P_1 and P_2 are in the eating state then if the philosopher P_3 is time to go into eating state then which statement in the above code try to go into eating is trying to control the above condition?

(A) if condition

(B) test (i)

(C) down (mutex) taken and swapped

(D) down (S[i])

Ques What happens if you interchange up (mutex) and down S[i] in the take fork function?

(A) No problem, solution will work fine

(B) more than two philosopher will go into eating state.

(C) If is possible for deadlock.

(D) None of the above.

Ques) Let P_0 to P_4 be processes and m_0 to m_4 be binary semaphores. Mutex initialized to 1. Each process execute below code.

P_0 :
 wait ($m[0]$);
 wait ($m[(i+1) \% N]$);

P_1 :
 signal ($m[i]$)

P_2 :
 signal ($m[(i+1) \% N]$);

Consider the following boundary condition
I ME is satisfied

II ME is Not satisfied

III It is possible for Deadlock

- (A) II only
- (B) only I & III
- (C) only I & II
- (D) only II & III

Ques) Suppose we want to synchronize concurrent process P and Q using binary semaphores S_1 and S_2 , the code for the process P and

Q is shown below.

Process P starts with Process Q

```
while (1)
    {
        P(S1);
        P(S2);
    }
```

```
    v(S1);
    v(S2);
```

```
    CS;
    v(S1);
    v(S2);
```

This results in ensure

- (A) ME
- (B) starvation but Not DL
- (C) DL
- (D) None.

Ques.) If $P(s_1)$ and $P(s_2)$ were interchanged, then

- (A) ME
- (B) DL
- (C) Both A & B
- (D) None

Ques.) Three concurrent process executes code segment X Y Z executes, that access a, b, c. Process a b -> X Y execute P operation on semaphores b, c, d.

Process Y : $P(b \ c \ d)$

Process Z : $P(c \ d \ a)$

before entering respective code segment. After

completing the execution of its code segment, each process invoke the v operations on its 3 semaphores. All

semaphores are binary semaphores and initialized to 1. Which one of the

following represent a deadlock free order.

of invoking P operation.

- (a) X : $P(a \ b \ c)$

- ~~(a)~~ (a) $X : a b c \quad Y : b c d \quad Z : c d a$
- ~~(b)~~ $X : b a c \quad Y : b c d \quad Z : a c d$
- ~~(c)~~ $X : b a c \quad Y : c b d \quad Z : a c d$
- (d) $X : a b c \quad Y : b c d \quad Z : c d a$

(a) $X : a b c \rightarrow Y \xrightarrow{DL} Z$
 $Y : b c d$
 $Z : c d a$

~~(b)~~ $X : b a c \quad X \xleftarrow{b} Y \xrightarrow{a} Z$ DL
 $Y : b c d$
 $Z : c d a$ No DL

~~(c)~~ $X : b a c \quad X \xleftarrow{b} Y \xrightarrow{a} Z$ DL
 $Y : c b d$
 $Z : a c d$

Ques.) Suppose we want to synchronize two process

Process P: $\text{while } (1) \text{ do } \dots$ Process Q: $\text{while } (1) \text{ do } \dots$

NA: $\text{read } p \{ \dots \text{ wait } \} \text{ and } \text{read } q \{ \dots \text{ wait } \}$ Y: \dots

both processes print 'o' and condition print 'i';

alt b and P print 'o'; alt condition print 'i';

when off branch X: $\{ \dots \text{ wait } \} \text{ and } \{ \dots \text{ wait } \}$ Z: $\{ \dots \text{ wait } \}$

$\{ \dots \text{ wait } \} \text{ and } \{ \dots \text{ wait } \}$ for

$\{ \dots \text{ wait } \} \text{ and } \{ \dots \text{ wait } \}$ for

Sync statements can be inserted at points w, x, y, z , which of the following will lead to output string: 00 11 00 11 00 ?

	W	X	Y	Z	$P(S) + S$	T	
(A)	$P(S)$	$v(S)$	$P(T)$	$v(T)$	0	1	x
(B)	$P(S)$	$v(T)$	$P(T)$	$v(S)$	1	0	✓
(C)	$P(S)$	$v(T)$	$P(T)$	$v(S)$	1	1	x
(D)	$P(S)$	$v(S)$	$P(T)$	$v(T)$	1	0	x

Ques Consider 6 concurrent processes $S=0$

A: Down(s) CS UP(s)

B: D(s) CS U(s)

C: D(s) CS U(s)

D: U(s) CS D(s)

E: U(s) CS D(s)

F: U(s) CS D(s)

what is maximum value of s. 3 ✓

Ques Consider a schedule with 3 Process

A, B, C binary semaphore are

Process A	Process B	Process C
{ while(1) { $\downarrow P(T)$ $P(S)$ }	$\uparrow P(T)$ $V(Z)$	{ $P(Z)$; $V(S)$; }

$S = X^01$

$T = X^1X^2$

$Z = \emptyset 1$

$V(T)$

** Prints 2 times.

Ques: Consider two processes P_1 and P_2 which share a common
mutex. P_1 has initial state $\{S\}$. P_2 has initial state $\{Q\}$.
while ($S \neq \emptyset$) { while ($Q \neq \emptyset$) {
 } down (mutex); } down (mutex);
 T point '\$'; X point '#';
 X up (mutex); T up (mutex);
 } } } }

Which of the following is possible pattern?

- I \$ # * (A) $\{S\} \rightarrow \{T\}$ & $\{Q\} \rightarrow \{X\}$
- II # * \$ (*) (B) $\{S\} \rightarrow \{T\} \& \{Q\} \rightarrow \{A\}$
- III (# / \$) * (C) $\{S\} \rightarrow \{T\} \& \{Q\} \rightarrow \{A\}$
 (D) None.

Ques: A : $D(S)$
 $D(Q)$

B : $D(C)$
 $D(S)$

print("Akash"); print("Gupta")
 $V(Q)$ $V(Q)$

Initially $Q = \{Q\}$, $S = \{S\}$

In above situation :

- (A) DL may occur (Ans)
- (B) Print "Akash Gupta"
- (C) DL never occurs

Ques. Counting semaphore value $s=10$ in a specific time. $s=10$. $s=15$ down
S up P up

$10 - 15 + P = 35$ If the new value of semaphore is 35 find value of P.

$$P = 40 \quad \checkmark$$

MONITORS

* Monitor is a programming language compiler support to achieve synchronization. It is a collection of variable, procedure combined together, ~~in~~ in a special kind of module or a package.

- The process running outside the monitor cannot directly access the internal variables of monitor. But however they can call the procedure of the monitor.
- The monitors are an important property that only one process can be inside the monitor at any point of time.
- Syntax of the monitors : ~~process~~
Keywords → Monitor Example name of Monitor

Variables; condition variables

and condition variables;

Procedure P₁

Procedure P₂

$\{ \equiv \}$.

Condition Variable : eg. condition X, Y;

- the two different operations are performed on the monitors.

(1) wait () X.wait() or wait(x);
 (2) signal () Y.wait() or signal(y)

Process performing wait operation only on C.Y will be suspended and the suspended process is placed in the block queue of respective condition variable.

Every condition variable have its own waiting queue.

- Signal :

signal (full);

signal (empty);

X.signal() or signal(x);

Y.signal() or signal(y);

- There are two cases :
 - The block Queue of a respective condition variable is empty. (No suspended process on respective block queue). The signal has no effect and the signal will be lost;
 - The block Queue of respective condition variable is not empty. (Already there is some suspended process in block queue) one process will be resumed from the block queue and one process will continue the execution.

Producer-Consumer with monitors

Producer	Consumer	Monitor	Producer-Consumer
1		{ integer count = 0 ;	
2		condition FULL, EMPTY ;	
3	procedure Enter_items		
4	{ if (count == N)		
5	{ wait(FULL); }		
6	Enter(item);		
7		count = count + 1;	
Count =		if (count == 1)	
N = 8		signal (EMPTY);	
	}		

Procedure Remove-item

```

    begin
        if (count == 0) then
            wait (EMPTY);
        else
            Remove (item);
            if (count == N-1)
                signal (FULL);
        end;
    end;
}

```

Procedure Producer

```

begin
    while (true) do
        produce-item (item);
        producer-consumer . enter-item ();
    end;
}

```

Procedure Consumer

```

begin
    while (true) do
        item = producer-consumer . Remove-item ();
        process-item (item);
    end;
}

```

CONCURRENT PROGRAMMING

- Consider following instruction

$$S_1 : a = b + c$$

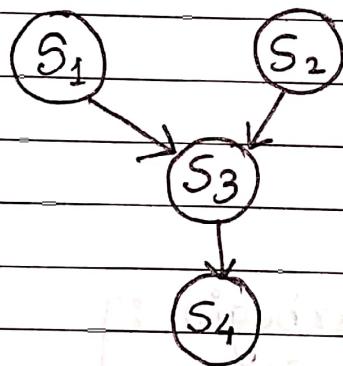
$$S_2 : d = e + f$$

$$S_3 : g = a/d$$

$$S_4 : h = g * i.$$

Read Set = { b, c, e, f, a, d, g, i }

Write Set = { a, d, g, h }



Dependency Graph

$$(i) R(i) \cap W(j) = \emptyset$$

$$(ii) W(i) \cap R(j) = \emptyset$$

$$(iii) W(i) \cap W(j) = \emptyset.$$

} Independent

- S_1 and S_2 execute concurrently because they do not have any common variable.
- Any two statements S_i and S_j can be executed concurrently or parallelly if and only if it satisfies the three rules.

PARALLEL PROGRAMMING

- Concurrent program will be written by using the below statement

begin

$S_1 + S_2 = P$

$S_2 + S_3 = P$

$S_3 + S_1 = P$

end

parbegin/cobegin

S_1

S_2

S_3

coend



For previous example :

begin :

parbegin :

S_1

S_2

parend.

S_3

S_4

end

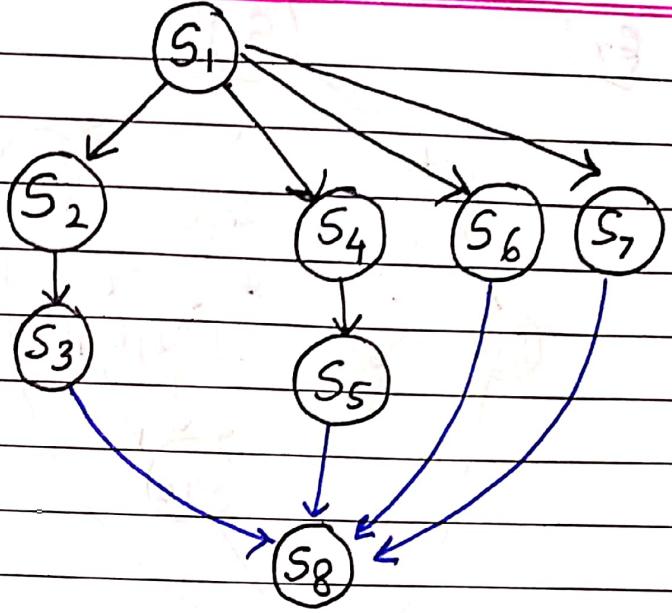
- If nothing is given, by default use begin.

Ques Consider a program:

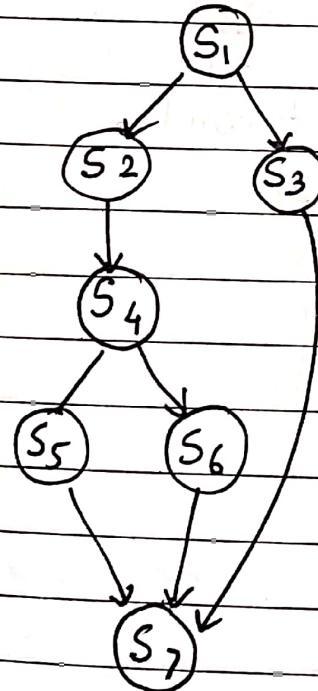
S_1 ;
 parbegin :
 begin S_2
 S_3]
 end
 begin S_4
 S_5]
 end
 S_6
 S_7

Parend

S_8

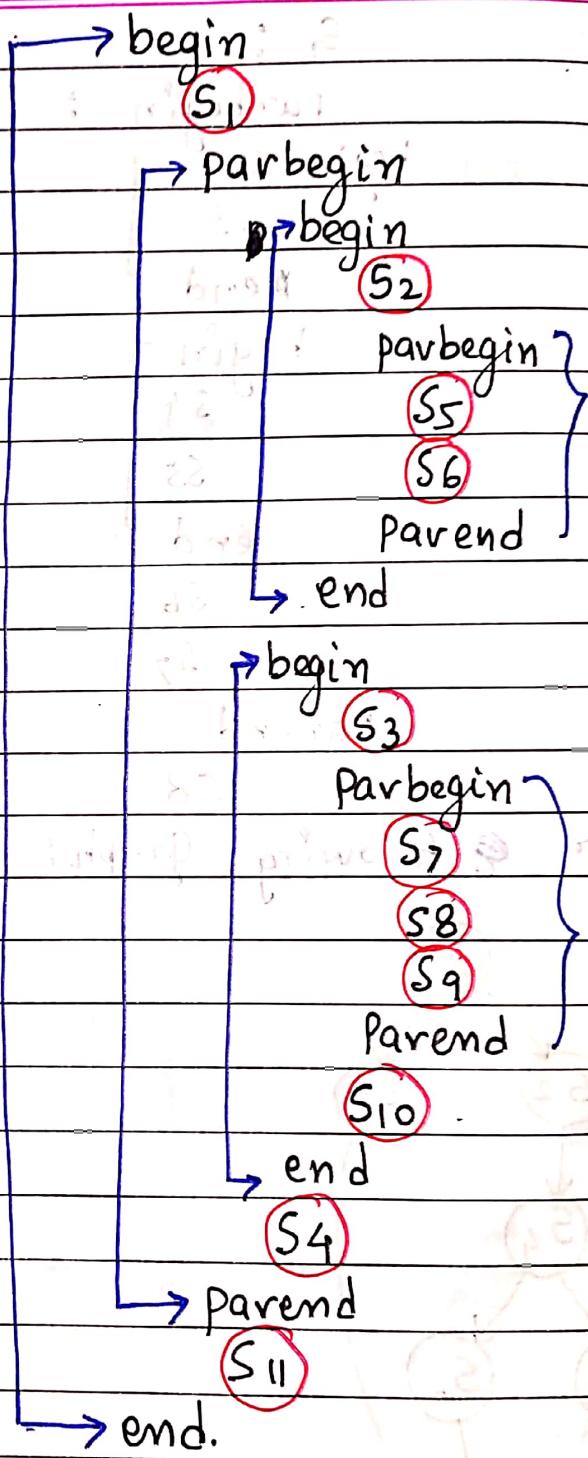
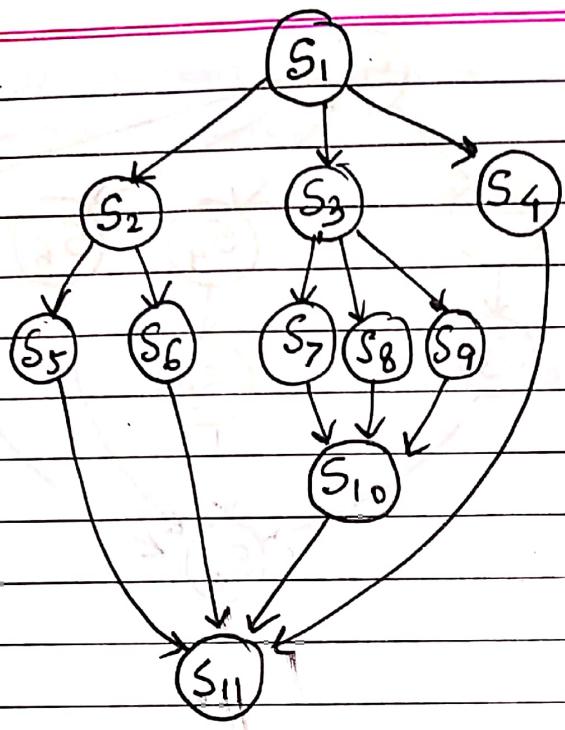


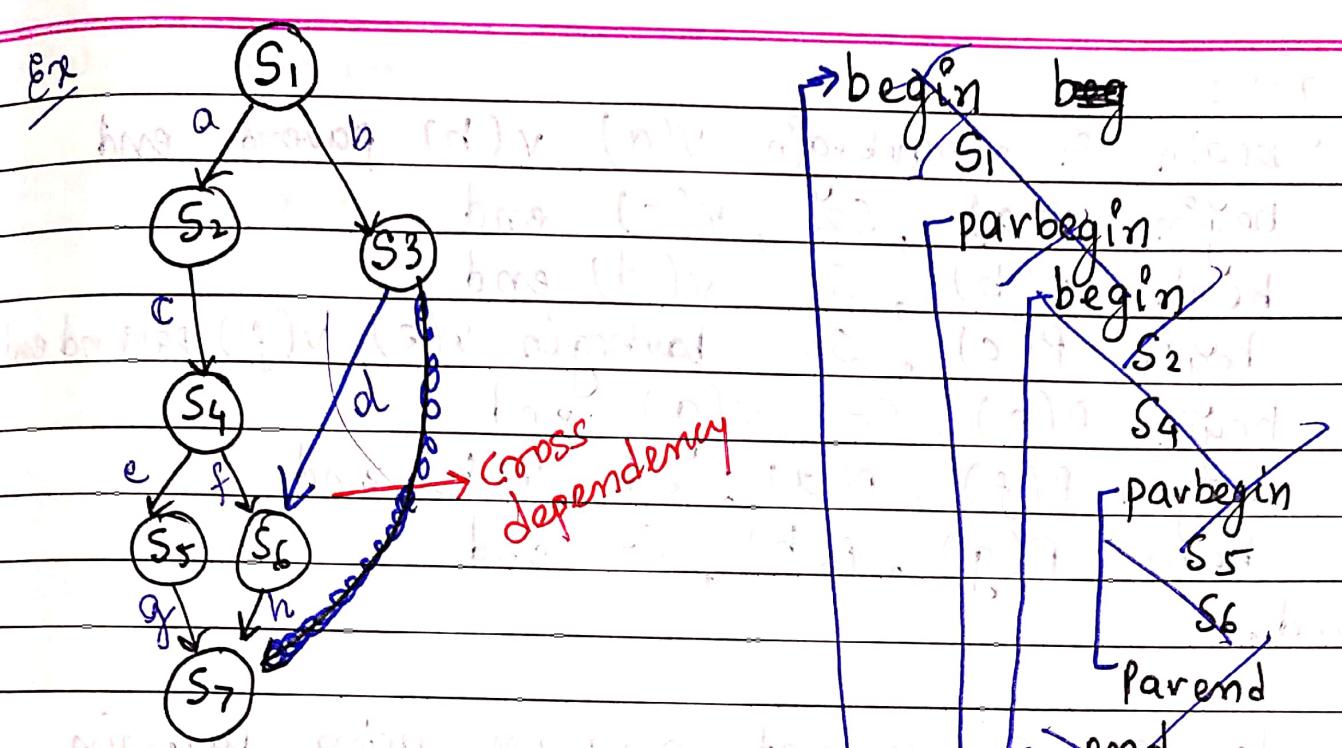
Consider the following graph:



begin S_1 ,
 parbegin
 S_3
 begin
 S_2
 S_4
 parbegin
 S_5
 S_6
 Parend
 end
 Parend
 S_7
 end

Ex





~~begin~~
S₁

~~parbegin~~
S₃

~~begin~~
S₂



~~begin begin~~
S₁

~~parbegin~~
S₃

~~begin~~
S₂

~~parbegin~~
S₄

~~parbegin~~
S₅

~~parbegin~~
S₆

~~Parend~~
S₇

~~end~~
S₃

~~Parend~~
S₇

~~end.~~
S₇

It is not possible to write concurrent programming for all dependency graph using parbegin and parend. But it is very much possible with help of semaphore operation.

~~end~~
S₇

parbegin :

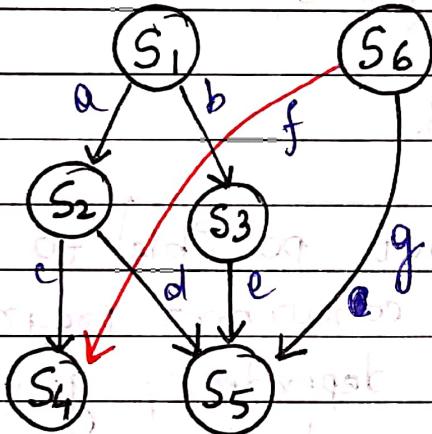
```

begin S1 ; parbegin v(a), v(b) parend end
begin p(a), S2, v(c) end
begin p(b), S3, v(d) end
begin p(c), S4, parbegin v(e), v(f) parend end
begin p(e), S5, v(g) end
begin p(f), p(d), S6, v(h) end
begin p(g), p(h), S7 end

```

parend.

Ques write a concurrent program using parbegin and parend and semaphore.



var

a, b, c, d, e, f, g : Semaphore;

begin

co-begin

Not mandatory to write

begin S1 ; parbegin v(a); v(b); parend

begin P(a); S2 ; parbegin v(c); v(d) end

begin P(b); S3 ; v(e) end

begin P(c); P(f); S4 end

begin P(d), P(e); S5 end

begin S6 , v(f), v(g) end

co-end

end

Ques Consider following concurrent programming.

var

a, b, c, d, e, f, g, h, i, j, k : Semaphore

begin

c begin

begin S1 v(a) v(b) end

begin P(a); S2 v(c) v(d) end

begin P(c) S4 v(e) end

begin P(d) S5 v(f) end

begin P(e) P(f) S7 v(k) end

begin P(b) S3 v(g) v(h) end

begin P(g) S6 v(i) end

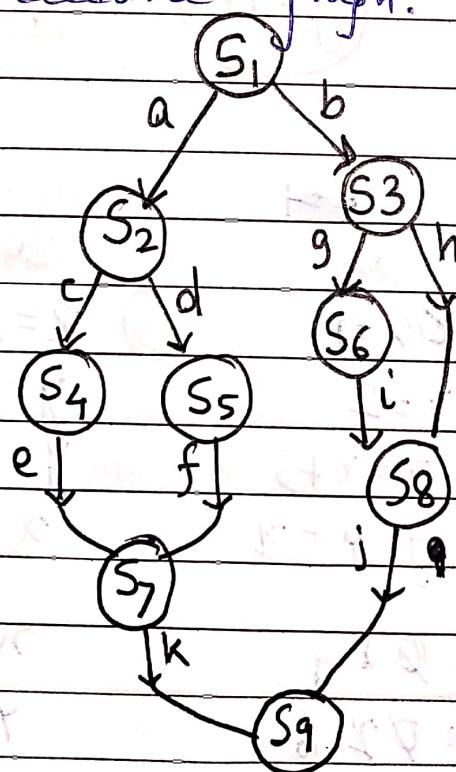
begin P(h) P(i) S8 v(j) end

begin P(j) P(k) S9 end

c end

end.

Draw the precedence graph.



Ques~~int~~~~x=0~~~~,y=0;~~~~parbegin~~~~begin~~~~x=1;~~~~y=y+x;~~~~end~~~~begin~~~~begin~~~~y=2~~~~begin~~~~x=x+3~~~~begin~~~~end~~~~begin~~

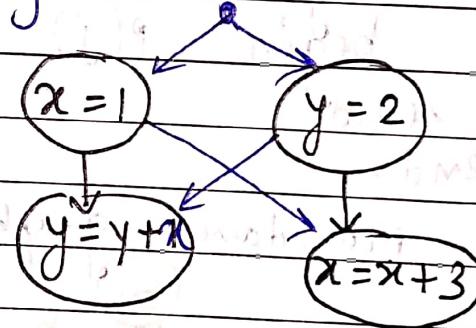
What can be the final values of x, y after running the concurrent program?

$$x = 0 \quad y = 0$$

$$\text{I} : x = 1 \quad y = 2$$

$$\text{II} : x = 1 \quad y = 3 \quad \checkmark$$

$$\text{III} : x = 4 \quad y = 6 \quad \checkmark$$



case 1

$$\textcircled{1} \quad x = 1$$

$$y = y + x$$

$$y = 2$$

$$x = x + 3$$

$$x: \emptyset \times 4$$

$$y: \emptyset \times 2$$

case 2

$$\textcircled{2}$$

$$x = 1$$

$$y = 2$$

$$x = x + 3$$

$$y = y + x$$

$$x = x + 3$$

$$x: \emptyset \times 4$$

$$y: \emptyset \times 6$$

case 3

$$\textcircled{3}$$

$$x = 1$$

$$y = 2$$

$$y = y + x$$

$$x = x + 3$$

$$x: \emptyset \times 4$$

$$y: \emptyset \times 3$$

Case 4Case 5case 6(4) ~~2~~ $y = 2$ $y = 2$ $x = x + 3$ $x = 1$ $y = y + x$ $y = 1$ ~~1~~

<

Ques

Consider the following code

$$x = 0 \quad s = 2$$

Process Z process X

wait(s)

Read(x)

$$X = X - 2;$$

write(x)

Signal(s);

Process X

wait(s)

Read(x)

$$X = X + 1;$$

write(x)

Signal(s);

Process Y

wait(s)

Read(x)

$$X = X - 2;$$

write(x)

Signal(s);

What is maximum possible value of X?

- (A) -2 (B) -1 (C) 1 (D) 2

Minimum value = -4.

Ques The following two processes P_1 and P_2 that share a variable B with an initial value of 2 execute concurrently.

$$X \leftarrow 4 \quad A \leftarrow 1 \quad B \leftarrow 2 \quad C \leftarrow 0 \quad D \leftarrow 0$$

 P_1

$$\begin{aligned} P_1() \\ \{ & C = B - 1; \\ & B = 2 * C; \\ \} \end{aligned}$$

 P_2

$$\begin{aligned} P_2() \\ \{ & D = 2 * B \\ & B = D - 1; \\ \} \end{aligned}$$

what # values B can possibly take after execution (4 distinct).

$$B = 2$$

$$\begin{aligned} 1 & C = B - 1 \\ 2 & B = 2 * C \\ 4 & D = 2 * B \\ 3 & B = D - 1 \end{aligned}$$

$$\begin{aligned} 1 & C = B - 1 \\ 4 & D = 2 * B \\ 2 & B = 2 * C \\ 3 & B = D - 1 \end{aligned}$$

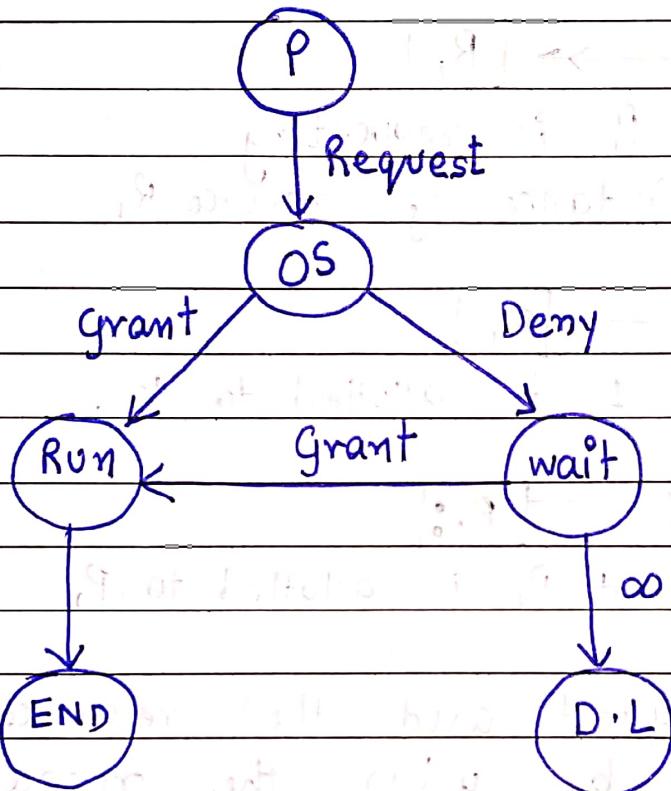
$$\begin{aligned} 1 & D = 2 * B \\ 3 & B = D - 1 \\ 2 & C = B - 1 \\ 4 & B = 2 * C \\ 5 & B = D - 1 \end{aligned}$$

$$\begin{aligned} 4 & D = 2 * B \\ 3 & C = B - 1 \\ 6 & B = 2 * C \\ 5 & B = D - 1 \end{aligned}$$

(3), (3), (4)

3 distinct values.

DEADLOCK

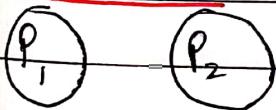


oo wait (permanent Block)

- If two or more processes are waiting on some event to happen which never happened, then those processes are said to be involved in the deadlock.

Basics of deadlock:

Process



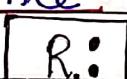
Resource



Resource with instance



Single instances



Multiple instances

Requesting :

(P₁)

R₁

Process P₁ is requesting one instance of resource R₁.

(P₁)

R₁

Process P₁ is requesting two instances of resource R₁.

Allocation :

(P₁)

R₁

Single Resource 1 is allotted to P₁.

(P₁)

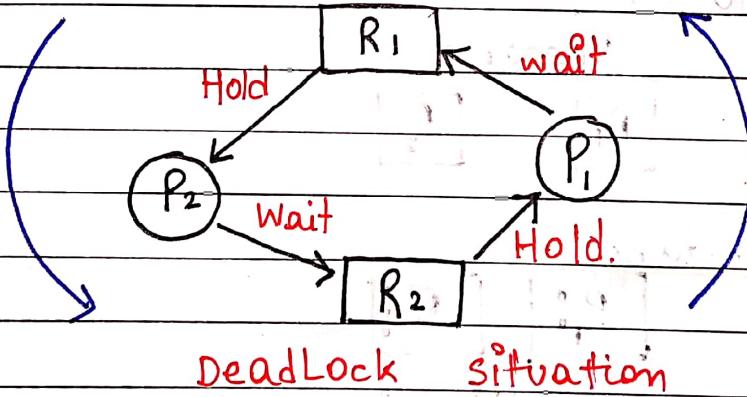
R₁

Two instances of R₁ is allotted to P₁.

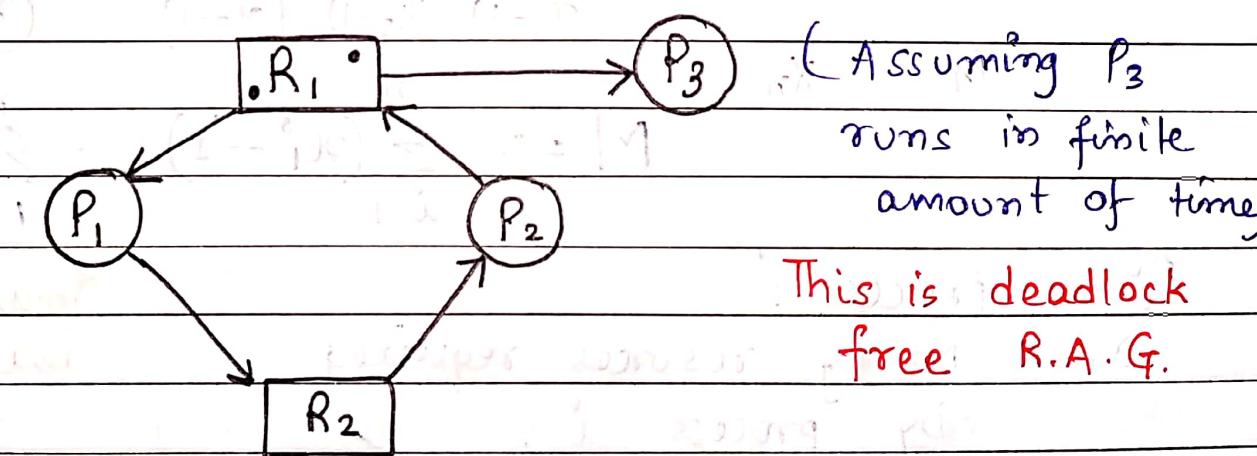
- The resource request and the resource allocation is represented by using the resource allocation graph.

Resource allocation Graph:

- It consists of set of vertices and set of edges.



- The resource request or release life cycle
 - The process will request from resource available in the system.
 - OS clearly validate the request of the process.
 - If the request made by the process is valid then the operating system check for the availability of the resource.
 - If the resource is fairly available then it will be allocated to the process, otherwise the process has to wait.
 - If all the resource requested by the process are allocated, then it will go into execution.
 - Once the execution of the process is completed, then it will release the resource.



Q1) Consider a system with 3 n-processes and 6 tape drives. Each process requires 2 tape drives to complete its execution. Then what is the maximum value of n which ensures deadlock free operation.

P₁, P₂, P₃, P₄, P₅, P₆

| | | | | |

If n=6, chance of deadlock.

if n=5, no deadlock.

Ex. If P₁ needs x_1 unit of resource that

P₂ needs x_2 unit ensures deadlock.

P₃ needs x_3 unit to maintain

P₄ needs x_4 unit if P₁, P₂, P₃, ..., P_n

$(x_1 - 1) (x_2 - 1) (x_3 - 1) \dots (x_n - 1)$.

P_n needs x_n

$$M = \sum_{i=1}^n (x_i^o - i) = \sum_{i=1}^n x_i^o - n$$

P_i^o = Process i^o

R_{max} that ensures deadlock.

x_i^o = No of resources required by process i^o .

Ex Minimum no of unit of resource that ensure no deadlock.

$$m = \sum_{i=1}^n x_i^o - n + 1 \quad m + n > \sum_{i=1}^n x_i^o$$

(Deadlock)

Ex2: Consider a system with 3 processes (P_1, P_2 and P_3). Each requires 2 unit of resource to complete the execution. What is the minimum number of resource required to ensure deadlock free operation.

$P_1 \quad P_2 \quad P_3$

$$1 \quad P_1 + P_2 + P_3 > 1 \times 3P + 3$$

Note :

$$\left[\sum_{i=1}^n x_i < m+n \right] \quad \text{Deadlock Free.}$$

\downarrow
No of No of Processes.

Total
Demand

$$\text{Example 1 : } 2n < 6+n$$

$$\text{Example 2 : } 2 \times 3 < m+3$$

$$m > 3 \quad m \geq 4, \quad m = 4, //$$

Ques.) Consider the system with n process and six tape drive. If each process require 3 tape drive to complete its execution. What is the maximum value of n that ensure DL free.

$$3n < 6+n$$

$$2n < 6$$

$$n < 3$$

$$\boxed{n=2},$$

Ques.) Consider a system with 3 processes P_1 , P_2 and P_3 , if the peak demand for each process for a particular resource type R is 5, 9, 13 then what is the minimum number of resource req to ensure DL free operation.

$$(5+9+13) \leq m + 3$$

$$24 \leq m$$

$$\underline{m=25}$$

Ques.) A system is having 3 user process P_1 , P_2 , P_3 where P_1 require 21, P_2 require 31, P_3 require 41. Minimum number of unit of r ensure ~~No~~ No deadlock. is -

$$21+31+41 \geq 93 \leq m + 3$$

$$\boxed{m = 91}$$

Ques(i)) If there are 100 unit of resource in the system and each process in the system requires 4 unit of resource

$$3n \leq 100$$

$$n \leq 33.3$$

$$\boxed{n = 33}$$

for Deadlock free .

(ii) Min. number of processes that ensure deadlock.

$$n = 33 + 1 = 34 \checkmark$$

Necessary Condition : Deadlock may or may not be possible.

Sufficient condition : Deadlock ~~can~~ never be possible.

Necessary : There are 4 necessary conditions of occurrence of deadlock.

- (i) Mutual Exclusion
- (ii) Hold and wait
- (iii) No preemption (No release)

Sufficient → (iv) Circular wait.

Mutual exclusion : By this condition there must exist at least one resource in the system which can be used by only one process at a time. If there exists no such resource then deadlock will never occur. Resource have been allocated only one process or it is to be freely available. There should be 1-1 relationship between

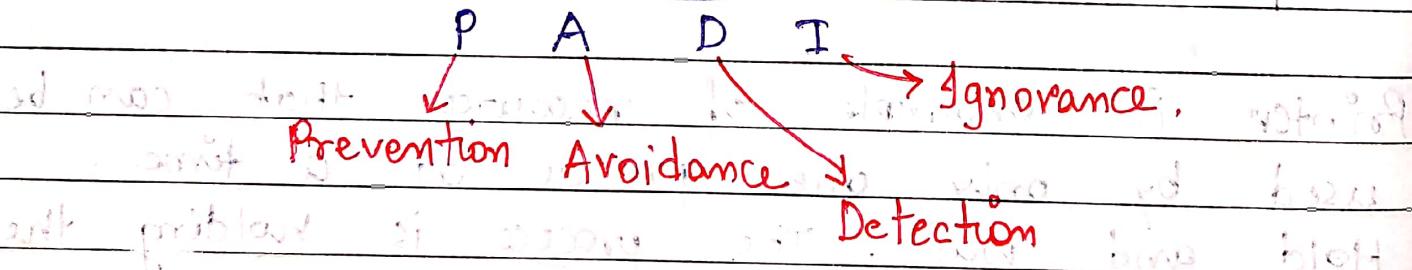
- Printer is example of resource that can be used by only one process at a time.
- Hold and wait. The process is holding the resource and waiting on some other resource simultaneously.

- No preemption: By this condition, once the resource have been "allocated" to the process, it cannot be preempted.
- The resource has to be released, by the process after execution. It is not allowed to forcefully preempt the resource from the process.
- Circular wait: The processes are circularly waiting on each other for the resource.

- If all other 4 conditions exist simultaneously in the system, then definitely there exist a deadlock.

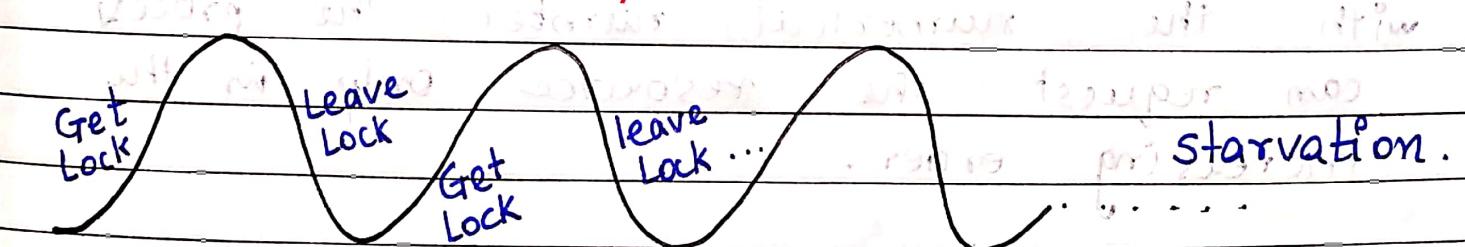
Not only 1, 2, 3, All 4 reasons are must exist for causing deadlock. All 4 conditions are not independent, because the circular wait includes hold and wait.

SOLUTION FOR DEADLOCK



Deadlock prevention

- Mutual exclusion : It is not possible to dissatisfaction mutual exclusion always because of shareable and non-shareable resource. For example, file read by multiple resource. But printer is non-shareable resource. May result data inconsistency.
- Hold and wait : Allocate all the resource required by the process before start of execution. But this results in low utilization of resource. Ex. P_1 is unnecessarily holding a resource which is required only at the end of execution.
- No-preemption : (1) The process should release all the existing resource before making the new request. Ex. the process P_1 requires 100 resource to complete the execution, but $P_1 \leftarrow 85$ only next time $P_1 \rightarrow 100$ but $P_1 \leftarrow 55$
- Partial allocation : $P_1 \rightarrow 100$. but $P_1 \leftarrow 85$ only



• If the above condition is hold to disallow hold and wait then it may go into starvation problem.

No-preemption (2): Let the process P_1 is requesting for resource R_1 , then

Case(i) If R_1 is free then it will be allocated to process P_1 .

Case(ii) If the resource R_1 is not free and if it is allocated to other process P_2

(ii)(a) If Process P_2 is in execution, then the process P_1 has to wait.

(b) If the process P_2 is not in execution and it is requesting some other resource R_2 , preempt the resource R_1 from R_2 and allocate to P_1 .

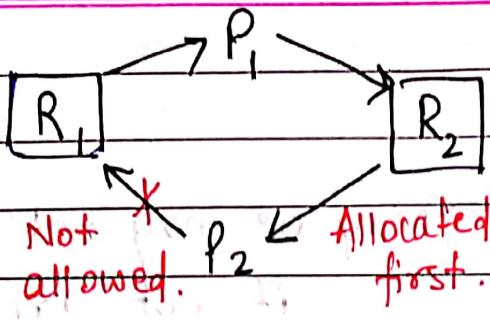
• Resource preemption guarantees the process completion.

Circular wait: The resource will be assigned with the numerical number. The process can request the resource only in the increasing order.

$P_1 \rightarrow R_8$
(allocate)

$P_1 \rightarrow R_6$
(x not allowed)

$P_1 \rightarrow R_{10}$
allowed



DeadLock Avoidance :

- Dead Lock avoidance can be avoided by Bankers' algorithm.

Total Available
A B C

Safe \rightarrow No deadlock
unsafe \rightarrow Deadlock.

Process

Max Need

Current Allocation

Process	A	B	C	A	B	C
P ₀	7	5	3	0	1	0
P ₁	3	2	2	2	0	0
P ₂	9	0	2	3	0	2
P ₃	2	2	2	2	1	0
P ₄	4	3	3	0	0	2

Current Available Current + Need = Available

A B C

A B C

3 3 2 7 4 3 6

A B C

A B C

1 2 2 6 0 0 6

A B C

A B C

0 1 1 5 1 1 5

safe sequence = $\langle P_1, P_3, P_0, P_2, P_4 \rangle$
(Multiple possible) $\langle P_1, P_3, P_0, P_4, P_2 \rangle$
etc.

Deadlock
free.
(Process completion
is guaranteed)



{May or may not be possible,
if not prevented}

- If we can satisfy the remaining need of all the processes with the current available resource then the system is said to be safe state. Otherwise the system is said to be in the unsafe state.
- If the system is in the unsafe state then it is possible for deadlock.
- The order in which we satisfy the remaining need of all the process, is called as safe sequence.
- The safe sequence may not be unique. We can have multiple safe sequence. The unsafe state purely depend on the behaviour of the process. (unpredictable)
- Each and every time when the process is requesting for any resource, the banker algorithm will be used to identify if the system is in the safe state or unsafe state.

- If the system is in the safe state, then the request of the process will be guaranteed.
- If system is in unsafe state, then the request of the process will be denied.

Ques) Consider following table & which Process executes last?

Total Available Current Available.

X	Y	Z
5	5	5

X	Y	Z
3	0	2

Current Allocation

X	Y	Z
P ₀ 1	2	1
P ₁ 2	0	1
P ₂ 2	2	1
5	4	3

Current Need.

X	Y	Z
1	0	3
0	1	2
1	2	0
2	1	0

~~3 2 0~~ + ~~2 2 1~~ = ~~5 4 1~~

~~2 2 1~~ + ~~2 0 1~~ = ~~2 1 3~~

~~0 0 2~~ + ~~1 2 1~~ = ~~1 2 3~~

~~2 2 1~~ + ~~3 3 4~~ = ~~5 5 5~~

~~5 5 5~~ - ~~2 2 1~~ = ~~3 3 4~~

~~3 3 4~~ - ~~1 1 1~~ = ~~2 2 2~~

~~2 2 2~~ - ~~1 1 1~~ = ~~1 1 1~~

~~1 1 1~~ - ~~1 1 1~~ = ~~0 0 0~~

~~0 0 0~~ - ~~0 0 0~~ = ~~0 0 0~~

P₁ P₀ P₂

Current Avail

= Avail + ~~Allocated~~

Allocated.

Current Need = Max Need

- Allocated.

Ques.) Consider following table:

Allocation Max Need current need

	X	Y	Z	X	Y	Z
P ₀	0	0	1	8	4	3
P ₁	3	2	0	6	2	0
P ₂	2	1	1	3	3	3

Current

Available

X	Y	Z
3	2	2

Total Available

8	5	4
---	---	---

Free

3 2 2

• P₁
6/3/2

Extra requests:

Req1: P₀ X Y Z 1 0 current Need.

X	Y	Z
0	0	2

Req2: P₁ X Y Z 1 0 1 2 2

2	0	0	3	0	0
---	---	---	---	---	---

Current Need

X	Y	Z
8	4	4
53	0	0

3 2 2

533

320

853.

current Need $[Q_1, Q_2]$ only (if available) satisfied

X	Y	Z	P
8	4	2	✓
5	0	0	✗
1	2	2	✗

Only Q_2 can be fulfilled.

Ques) A system has 4 processes

Allocated Max Available Need $[2, 0, 0]$

X	Y	Z	P	Q	X	Y	Z	P	Q
0	1	0	2	1	1	1	2	1	3
2	0	1	1	0	1	2	2	2	0
1	1	0	1	1	2	2	0	5	3
1	1	1	1	0	1	1	2	2	0

If Available = X Y Z P Q
0 0 X 1 1

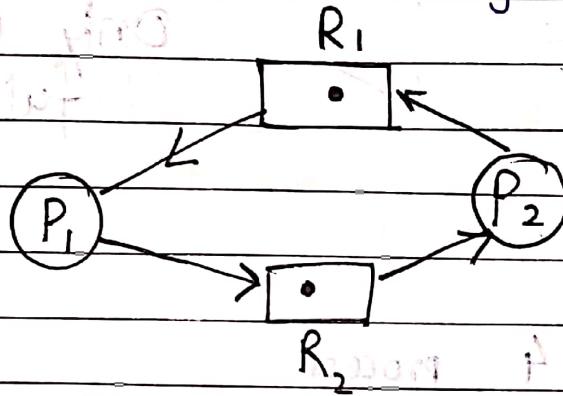
what is smallest value of X for which this is safe state?

silly mistake
~~| X = 3~~

$$\begin{array}{r} 00311 \\ 110101 \\ \hline 11322 \\ 11110 \end{array} \quad \cancel{\text{X=3}}$$

$$\begin{array}{r} X=2 \\ 00211 \\ 11110 \\ \hline 11311 \\ 11011 \\ \hline 22322 \end{array} \quad \checkmark$$

Question.) Consider the following Graph:



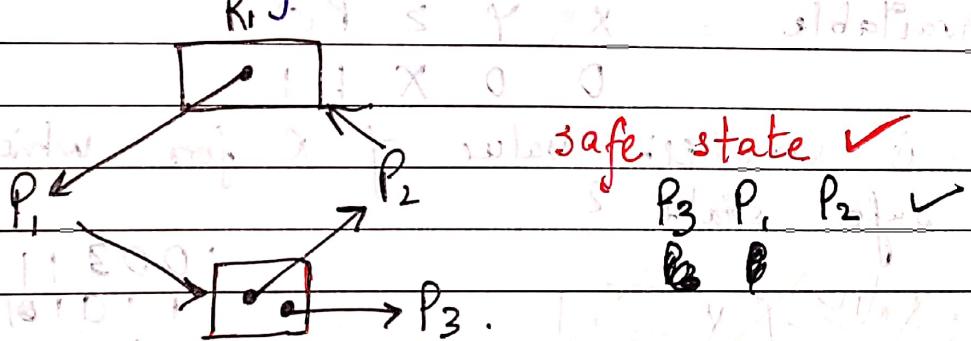
Q) Find if system is in a deadlock state
or else find a safe sequence.

Allocation X Need X Available

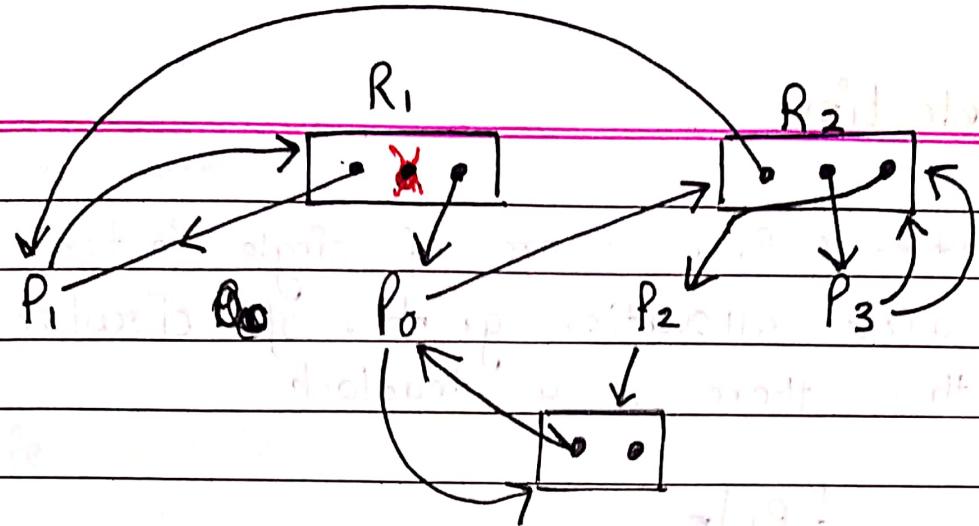
0 0 0 1 0	P ₁	1 1 0 1 1 0 1 1 0 0 0 0
0 0 1 0 0	P ₂	0 0 1 1 0 0 1 0 1 1 0 0

Deadlock. 1 1 0 1 1

Ques) Consider following



Ques) Consider following graph :



$$\langle P_2, P_0, P_1, P_3 \rangle \quad \checkmark$$

Now, start orientation along the same direction. The first two points are P_2 and P_0 . Now, we have to check if P_0 is clockwise from P_2 . If it is, then the orientation is correct. If not, then the orientation is incorrect.

So, calculate the angle between the vectors $\vec{P_2P_0}$ and $\vec{P_2P_3}$. If the angle is less than 180 degrees, then the orientation is correct. Otherwise, it is incorrect.

Now, we have to calculate the angle between the vectors $\vec{P_2P_0}$ and $\vec{P_2P_3}$.

From the diagram, we can see that the angle between $\vec{P_2P_0}$ and $\vec{P_2P_3}$ is 135 degrees.

Now, we have to calculate the angle between the vectors $\vec{P_2P_0}$ and $\vec{P_2P_3}$.

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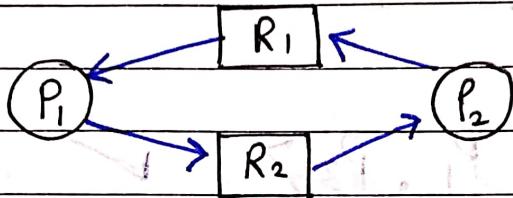
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From the diagram, we can see that the angle between $\vec{P_2P_0}$ and $\vec{P_2P_3}$ is 135 degrees.

DeadLock Detection

- Deadlock Detection : Resource are of single instance type
 - ↳ Draw resource allocation graph . If circular wait cycle exist then there is a deadlock .



- If all resources are of single instance type then the cycle in RAG is necessary and sufficient condition for the occurrence of deadlock.
- If all the resource are not single instance type Then the cycle in the resource allocation graph is just a necessary condition but not a sufficient condition for deadlock.
- The resources are of multiple instance type.

Ex.	Allocate	Need	Available
P ₀	0 1 0	0 0 0	0 0 0
P ₁	2 0 0	2 0 2	3 1 3
P ₂	3 0 3	0 0 0	
P ₃	2 1 1	1 0 0	
P ₄	0 0 2	0 0 2	

$\langle P_0, P_2, P_1, P_3, P_4 \rangle$ No deadlock .

- What happens if the process p_2 is requesting for additional resources? Or what? Then the system will go to deadlock.
- < Unsafe state > : Possibility of Deadlock.
- unsafe state is unpredictable. If it is totally dependent on behaviour of process. Means changing nature of their remaining need, if remaining need is constant (not changing), surely deadlock will occur.

- If the remaining need is changed, it may come again in some state.

Deadlock Recovery :

- Not traditional OS use this deadlock algorithm because it is time consuming and take more space.
- Real time OS use deadlock algorithm, therefore
 - Kill in the process
 - Resource preemption.
- (i) Killing the process : Kill process which are involved in the deadlock. Kill one after the other. Kill one process which is involved in the

deadlock, and again check for deadlock by using deadlock detection. If deadlock exist, then apply again, kill one more process, then again apply deadlock detection and so on.

• on what basis do we delete a process?

(i) Low Priority Process

(ii) Number of resources a process is holding

(iii) % of completion

(iv) Number of resources the process is requesting

(ii) Resource Preemption : Resources will be preempted from the process that are involved in the deadlock, and the preempted resource will be allocated to other process, so that there is a possibility of recovery from deadlock.

• If the resource preemption is followed to recover system from the deadlock. Then it may be possible for the process to go into starvation.

THREADS

- A thread represent an abstract entity that execute in the sequence of instruction.
- It has its own set of CPU registers.
- It has its own stack.
- There is no thread specific heap or data segment.

Code	Data	File	Code	Data	File
Registers	stack		stack	stack	stack
{			{	{	{
x	variables		x	variables	

- Thread is a light weight process (less number of instruction).
- Thread is just like a process having light weight.

THREAD vs PROCESS

- Thread has no data segment or heap.
- Process has everything or heap.
- Thread cannot live on its own. It requires a process.
- There can be more than one thread in a process.
- Process has everything.
- First thread is called main and has process stack.

THREADPROCESS

- Thread within a process share code, data and file but have its own set of stack and register.

Process does not usually share its code, data or file with other processes.

- If a thread die, stack is reclaimed.

If a process die, the resources are reclaimed and all threads also die.

- Each thread can run on a different physical processor.

Each process can run on a different physical processor.

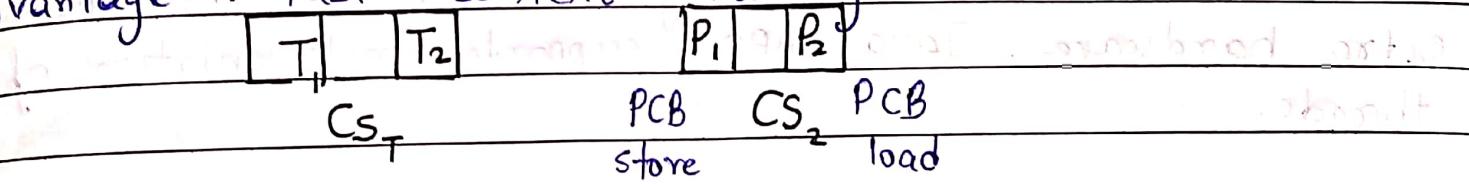
- Inter thread communication is via memory.

Inter Process Communication via data copy.

Advantage of Thread

- Responsiveness : If the process is divided into multiple threads, then if one thread is completed, its execution then the output will respond immediately. This response will be very fast compared to the response of process. Hence the threads will improve the responsiveness.

- Advantage is fast context switching.



- Context switching time between threads is very less than context switching time between the processes. Because in the thread it will have less context compared to the full context of process.

- Effective utilization of multiprocessor system : If the process is divided into multiple threads then the different threads can be scheduled onto the different processor. So that the process execution will be faster.

- Resource sharing : Resource like code, data, file and memory will be shared among all the threads between the process. The stack and register cannot be shared between the thread. Every thread will have its own stack and register.

Thread = stack + set of CPU reg + CPU time

Process = 1 thread + PCB + Code segment + Data + Memory

Multithread Process = n threads + PCB + Code + Data

+ Memory

basically n process = n PCB + n code + n data

• Economical - The implementation of a thread does not require extra hardware. Java API supports implementation of threads.

• Throughput - Enhanced throughput of the system. If the process is divided into multiple threads, if it consider multiple threads and divided into one job, then the number of jobs completed for unit time will increase and hence the throughput of the system will advance.

• Type of threads - There are two level of threads
 (i) user level (ii) Kernel level.

User Level Threads Kernel Level Threads.

- ULT are implemented by user or programmer.
- KLT are implemented by OS
- OS does not know about the ULT. KLT are recognised by ULT or OS views the ULT as part of OS at process only.
- If one ULT is performing blocking system call, then the entire process will be blocked. another thread will continue execution.
- ULT are dependent. KLT are independent.
- Implementation of ULT is easy. Implementation of KLT is complex.
- Has less context. Has more context.
- No H/w support needed. H/w support needed.

Ques: Which of the following is not supported by the thread?

- (A) stack
- (B) file
- (C) Address space
- (D) MQ.

Memory Management

The main functionality of memory management is allocating and deallocated the memory to the process. The main goal of memory management is efficient utilization of memory by minimizing the internal and external fragmentation.

Memory Management Technique:

- (i) Contiguous
- (ii) Non-contiguous.
 - ↳ Fixed partition
 - ↳ variable partition
 - ↳ Paging
 - ↳ Multilevel Paging
 - ↳ Segmentation
 - ↳ Inverted Paging
 - ↳ Segmented Paging.
 - ↳ Demand Paging.

Continuous Memory Allocation Technique:

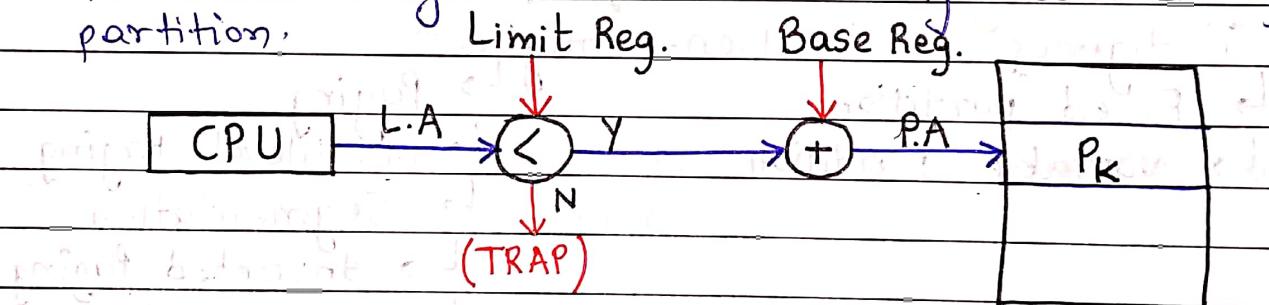
It is of two types: (static) & (Dynamic).

(1) Fixed Partition: Static Partition is a fixed size partition scheme.

→ 1 partition - 1 process.

→ Degree of multiprogramming is fixed.

- | | | |
|---|----|---|
| UB | 3K | • In this technique, main memory is predivided into fixed size partitions. |
| LB | 2K | • Size of each partition is fixed and cannot be changed. |
| | 1K | • Each partition allow only one process at a time. Degree of multiprogramming may not be equal but is restricted by number of partitions. |
| S
E
C
T
U
R
I
T
Y | 2K | • Maximum size of process is restricted by maximum size of partition. |
| | 5K | • Every process is associated with the limit Registers. |
| | | • Lower limit registers contain starting address of partition. |
| | | • Upper limit registers contain ending address of the partition. |



Advantage: Implementation of this scheme is simple.

- Overhead of processing is also low.
- It supports multiprogramming.
- No special hardware is required.
- Only one memory access is required, which reduces access time.

Disadvantage: No single program may be reduced to the size of the largest partition, in a given system.

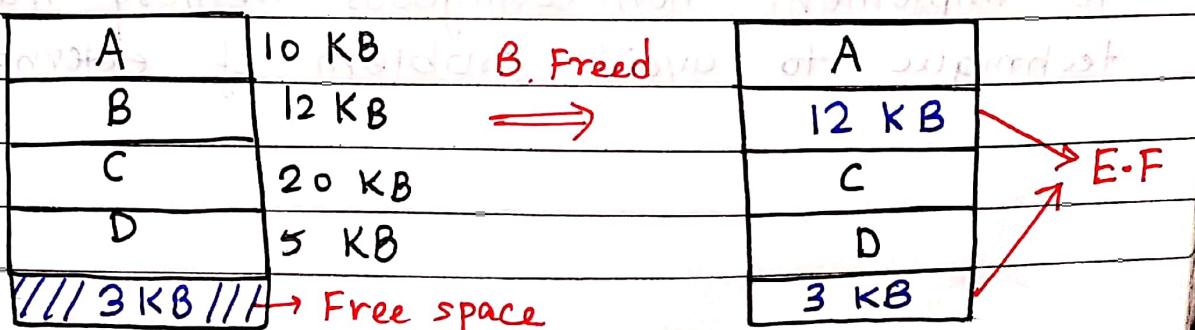
- It does not support dynamic data structures, such as stack, queues, heap.
- It utilizes memory inefficiently.
- The degree of multiprogramming is limited and equal to the number of partitions.
- It suffers from both internal fragmentation and external fragmentation.

Consider below memory allocation:

Process	Allocation	Available
A	10 KB	A - 10 KB
	15 KB	B - 12 KB
C	25 KB	C - 20 KB
D	8 KB	D - 5 KB
B	12 KB	

internal Fragmentation } Free space within partition
} based on contiguous memory allocation system or memory fragmentation scheme

Variable Partition or Dynamic Partition: It is a variable size partitioning scheme. It performs the allocation at runtime when a process arrives, a partition of size equal to the size of process is created. Then that partition is allocated to the process.



External Fragmentation (E.F) may occur because of contiguous allocation to a process. Free partitions are not contiguous.

- In variable partition scheme, initially the main memory will be single continuous free block.
- Whenever the request by the process come, partition will be met.

Advantage : It does not suffer from internal fragmentation.

- Degree of multi programming is Dynamic.
- There is no limitation on the size of process.

Disadvantage: It suffers from external fragmentation, allocation and deallocation of memory is complex.

- Compaction: To avoid the external fragmentation, compaction technique is used. Moving all the process towards the top or towards the bottom to make the free available memory in a same contiguous space.
- The compaction is undesirable to implement because it interrupt all the running process in the memory.
- To implement non-contiguous memory management technique to avoid problem of external fragmentation.

Partition Allocation Methods:

- When more than one partition is freely available to accommodate the request of the process then decision making of selecting a partition will be done by partitioning allocation method.
- First Fit: Allocate the process in a partition which is the first sufficient partition from the top of the memory.
- Best Fit: Allocate the process in a partition which is the smallest sufficient partition in the memory.
- Worst Fit: Allocate the process in a partition which is the largest sufficient among the free available partition. To find out the largest sufficient partition, it is also required to search for free available partition in the memory.
- Next fit: It also works like first fit, but it will be searched for first sufficient partition from the last allocation point.

Difference between Internal and External Fragments

	Internal Fragmentation			External Fragmentation		
Allocation	Process	Allocates	Whole	Process	Allocates	Whole
Basic	p_1	5 KB	{ 10 KB	20 KB	20 KB	10 KB

Wasting of memory occurs when fix size partitions are allocated to a process

Wasting of memory occurs when variable size partitions are allocated to a process

- Solution of internal fragmentation is that memory must be partitioned into variable size.
- Solution is compaction, paging, and segmentation.

Ques A 1000 KB memory is mapped using variable partition but no compaction. It currently has two partitions of size 260 KB and 200 KB. The smallest allocation request in kilobytes that could be denied is for

- (A) 151 (B) 181 (C) 231 (D) 541.



Ques.) Consider six memory locations of size 200, 400, 600, 500, 300, 250 KB. These partitions need to be allocated to 4 processes: 357, 210, 468 on 491 in that order. If the best fit algorithm is used. Which partition are not allocated? Ans. 200 & 300.

Ques.) Given 32 MB for allocation and the following event of memory allocation occurs.

$$P_1 = 2 \text{ MB}$$

$$P_2 = 3 \text{ MB}$$

$$P_3 = 5 \text{ MB} \quad \text{external fragment}$$

$$\text{and later on } P_4 = 1 \text{ MB}$$

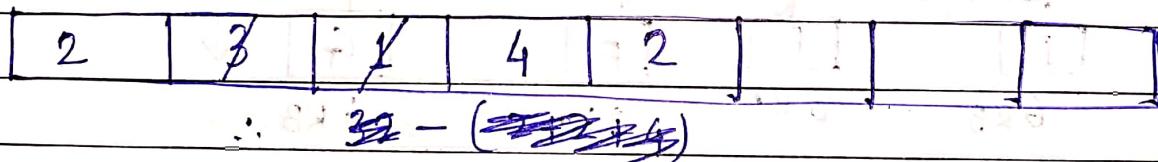
$$P_5 = 4 \text{ MB}$$

$$P_2 - \text{finish - Release.}$$

$$P_6 = 2 \text{ MB}$$

$$P_4 - \text{finish \& Release.}$$

Assume fixed and equal size partitions. Calculate m/o of total 8 partitions. (4 MB each) wasted.



$$\text{Fragments: } 2 + 2 = 4 \text{ MB free.} \quad \text{28 MB wasted.}$$

$$\begin{aligned} \text{Wasted memory} &= \text{Internal Fragments} + \text{External fragment} \\ &= 24 + 4 = 28 \text{ MB} \end{aligned}$$

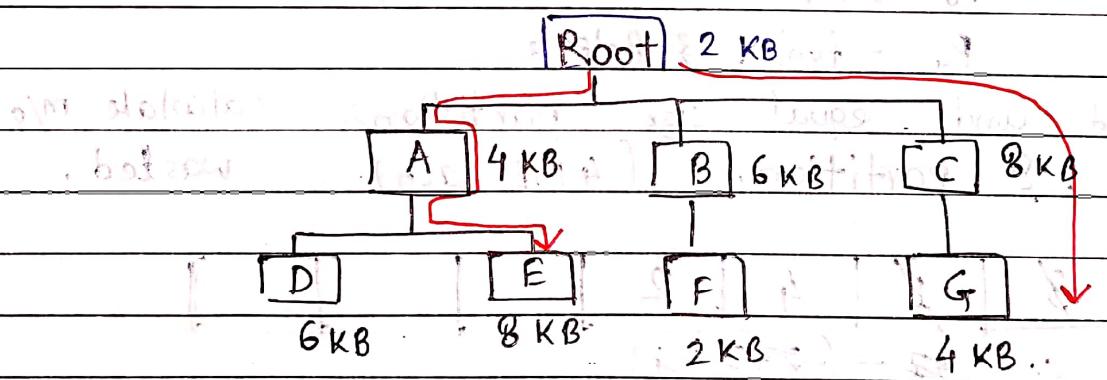
Q.) Let a system has ~~32~~ KB space and subdivided into 8 partitions of fixed size. If the following process reqd. Compute memory wasted if any.

~~P₁~~ - 3 KB ~~P₂~~ - 4 KB ~~P₃~~ - 1 KB ~~P₄~~ - 2 KB ~~P₅~~ - 3 KB ~~P₆~~ - 2 KB ~~P₇~~ - 4 KB ~~P₈~~ - 1 KB

SURGEON

~~P₁~~ - 3 KB ~~P₂~~ - 4 KB ~~P₃~~ - 1 KB ~~P₄~~ - 2 KB ~~P₅~~ - 3 KB ~~P₆~~ - 2 KB ~~P₇~~ - 4 KB ~~P₈~~ - 1 KB → 14 KB wasted due to internal frag.

Ques.) The overlay tree for a program given below.



What will be size of partition in physical memory required to load and run this program?

- (A) 12 KB
- (B) 14 KB
- (C) 10 KB
- (D) 8 KB

$$\begin{aligned}
 & \text{Root} \quad 2 + 4 + 8 = 14 \text{ KB minimum} \\
 & (A) \quad (E) \quad \text{required.} \\
 & (G) \quad (C)
 \end{aligned}$$

- Maximum space that can be needed at any time is 14 KB.
- Non-contiguous memory location.

Non-contiguous memory allocation:

- It is a memory allocation technique. It allows to store parts of a single process in a non-contiguous manner.
- Thus different parts of the same process can be stored at different spaces in the main memory.
- There are two popular techniques used for non-contiguous memory allocation.

(i) Paging

(ii) Segmentation

Memory Address

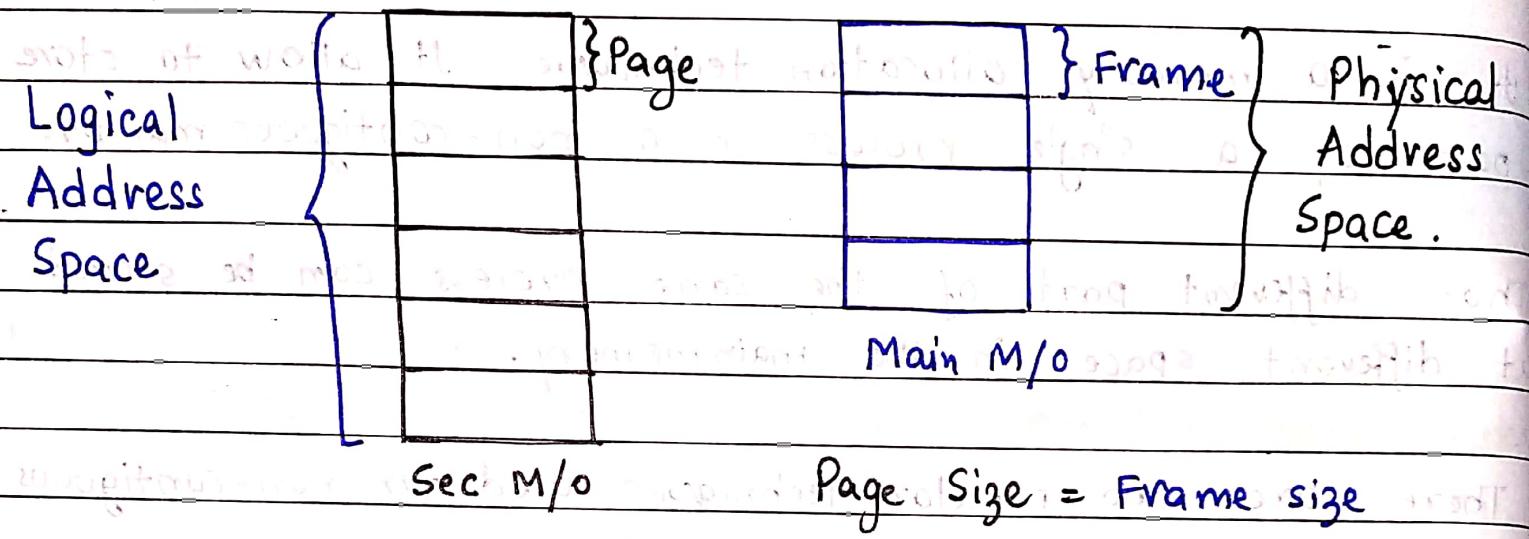
Ex Program - 64 B
Page size = 4 B.
Pages - $\frac{64}{4} \Rightarrow 16$ pages.

0	a	Page 0
1	b	
2	c	
3	d	
4	e	Page 1
5	f	
6	g	
7	h	
8	i	Page 15
9	j	
10	k	
11	l	
12	m	
13	n	
14	o	
15	p	

0	P ₄	Page = Frame size
1	P ₀	
2	P ₃	
3	P ₁	
4		Page table entries
5	P ₂	
6		
7		

Frame No.

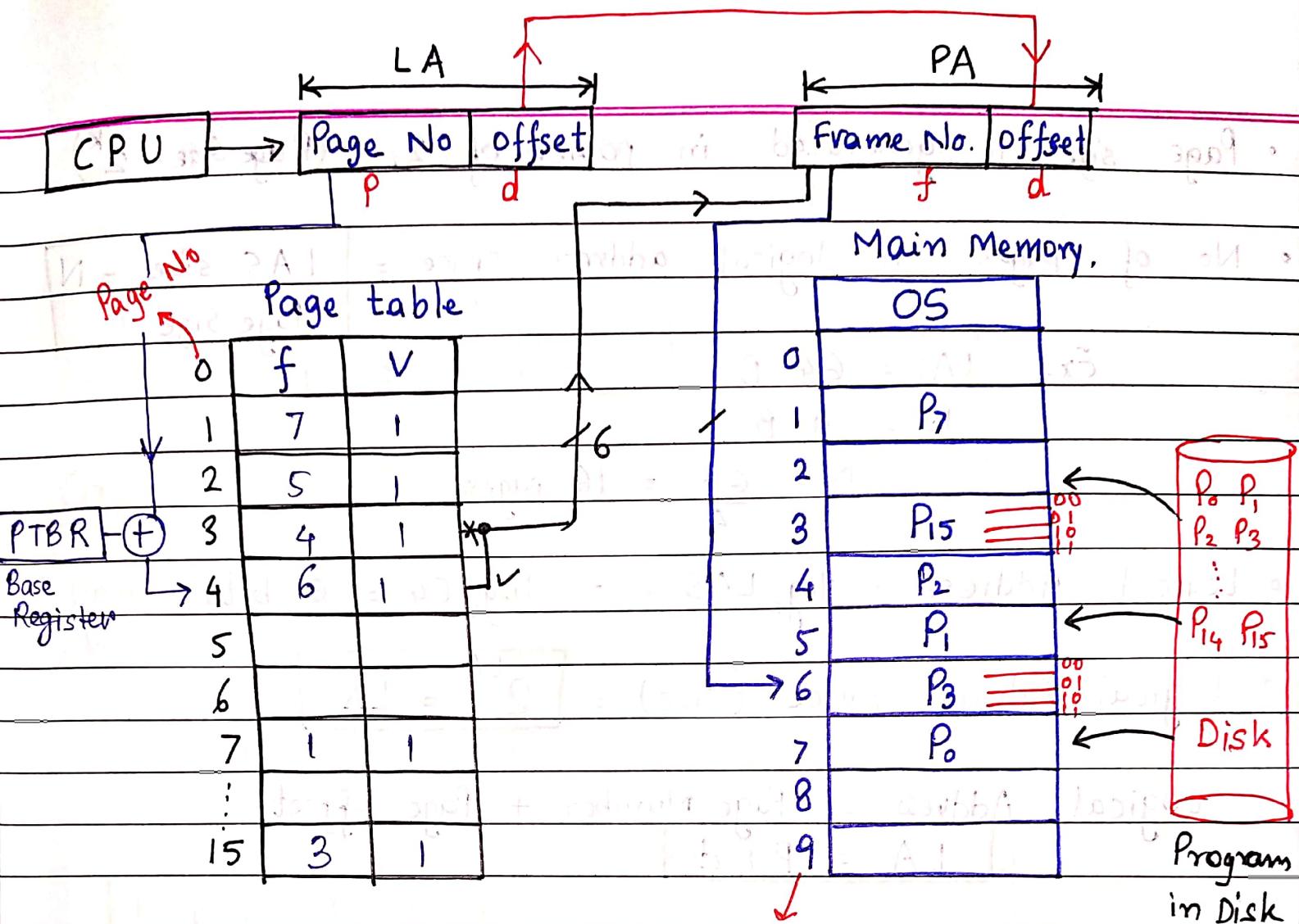
- Paging is a fixed size partitioning scheme. In paging, memory is divided into fixed size partition. The partition of secondary memory are called as pages. The partition of main memory are called as frames.



- Each process is divided in pages, wherein size of each part is same as frame size. The size of the last part may be less than page size.
- The pages of process are stored in the frames of main memory depending upon their availability.

Organization of Logical Address Space.

- CPU always generate logical address for LAS.
- LA = Page No \times Pagesize + Word offset
- LAS is divided into equal size pages.
- Pages are always fixed size units.



Page entry = # Pages in Program / Frame No.

$$\# \text{Pages} = \frac{\text{Program Size}}{\text{Page size}}$$

$$d = \log_2(\text{PageSize}) \quad P = \log_2 \# \text{Pages}$$

Page 3 offset 1

Frame 6th offset 1.

110 01

- Page size is generated in power of 2. ($\text{Page Size} = 2^k$)
- No of pages in logical address space = $\frac{\text{LAS size}}{\text{Page Size}} = N$
- Ex. LAS = 64 B
 $\text{PS} = 4 \text{ B}$
 $\therefore N = \frac{64}{4} = 16 \text{ pages.}$
- Logical Address = $\log_2 \text{LAS} = \log_2 64 = 6 \text{ bits.}$
- Logical Address Space (size) = $2^{\text{LA}} = \text{LAS}$
- Logical Address = Page Number + Page offset.
 $\text{LA} = P + d$
- $P = \log_2 N$ where N is # pages in LAS.
- $d = \log_2 \text{PS}$ where PS is page size.

Organization of Physical Address Space:

- Physical Address space is divided into equal size frame. Frame size is always divided into page size.
- $\text{PA} = \log_2 \text{PAS}$
- $\text{PA} = f + d. \quad (\text{offset})$
 (frame No)

$M = \# \text{ frames in PAS} = \frac{\text{PAS (size)}}{\text{Ps (Page size)}}$

$$f = \log_2 M$$

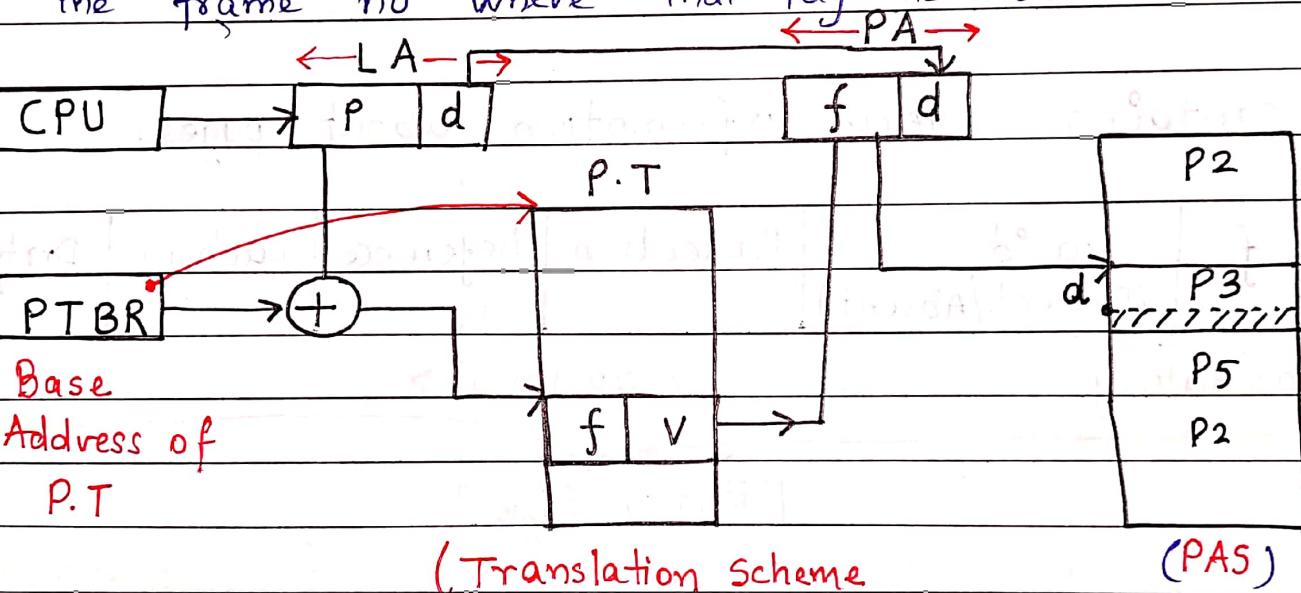
$$d = \log_2 Ps.$$

$$M = 2^f$$

$$Ps = 2^d$$

Organization of Page Table:

- Data structure that maps the Page No referenced by CPU to the frame no where that page is stored.



- Page table is stored in the main memory. Number of entries in the page table is equal to number pages a process is divided into.
- Page table base Register contains the base address of page table.

Page table base Register also contains the position of base address.

- Each process has its own independent page table.

$$\text{Page Table Size} = \# \text{ entries} \times \text{Page Entry Size}$$

$$|PTs| = N \times Es.$$

$$P_{Ts} = \frac{LAS}{Ps} \times Es$$

Page table entry:

- It contains several information about pages.

1 entry	f	valid (Present/Absent)	Protection	Reference	caching	Dirty
		Mandatory	< optional >			

[Entry Size]

- The information contained in the page table entry is changed from OS to OS.
- Most important info is frame number.
- It is also called as valid / invalid and indicate if page is present in the memory or not.
- Protection bit : Also called as read or write bit. If only read operation is allowed to be performed and no writing is allowed, then the

bit is set to zero. It specifies the permission of read or write on pages. If both read/write is allowed to be performed, then this bit is set to 1.

- Reference bit : It specifies whether the page has been referenced in the last clock cycles or not. If the page has been set referenced recently, it is set as 1.
- Caching : Enable or disable information. This bit enables or disable the caching of pages. Whenever freshness in the data is required, then caching is disabled using this bit. If caching of the page is disabled, then it is set one.
- Dirty bit. It is also known as modify bit. This bit specifies if that page is modified or not. If the page has been modified then set 1, otherwise 0.
- Advantages of Paging : It allows to store part of single process in a non-contiguous fashion.
- It solves problem of external fragmentation.

- Disadvantage : suffers from internal fragmentation. on average $P/2$, (last page is half full).
- There is an overhead of maintaining a page table for a process.
- The time taken to fetch the instruction increases.

Since now two memory access are required.

OS	Effective Access time = PTA time + Page Access time = m + m
PT M	EAT = 2m time. (NO TLB)
Po M	

Ques) Consider a system where Number of pages $N = 2^k$

Page size $= 4\text{ KW}$ address bits required $= 12$

PA = 18 bits address bits required $= 18$

logical LA and No of frames in PAS

$$\text{PAS} = 2^{18} \text{ bits} / \frac{\# \text{frames}}{4 \text{ KW}} = 2^{18} / 64 = 64$$

LA = p + d. forward address bits $= 12$

$$p + d = \log_2 N + \log_2 P_s$$

$$p + d = 11 + 12 \text{ bits} = 23 \text{ bits}$$

Ques) Consider a system with logical address space of 128 MW and PA = 24 bits. PAS is divided into 8K frames. Then what is page size and # pages in LAS.

$$\text{LAS} = 2^{27} \text{ word}$$

$$\text{PAS} = 2^{24} \text{ bits}$$

$$2^{24} = 2^{24} / \frac{8K}{P_s} = 2^{24} / 2^{24} = 1 \text{ word}$$

$$2^{24-13} = 2^{11} \text{ word. } \checkmark$$

No of pages in LAS = 2^{27} words = 2^{16} pages.

Ques.) Consider a system with logical address 32 bits and physical address space 64 MB. $P_s = 4 \text{ KB}$. Memory is byte addressable.

$$P_s = 2^B \quad LA = 32 \text{ bits.}$$

what is PTs? $PAS = 64 \text{ MB.}$

$$P_s = 4 \text{ KB.}$$

$$\# \text{ Pages} = \frac{2^{32}}{2^{12}} = 2^{20} \text{ pages.} \times 2 \cancel{\text{bytes}}$$

$$P_s = 2^B.$$

$$\therefore 2 \times 2^{20} \text{ bytes} : PTs.$$

2 MB Page table size.

Ques.) Consider a system with logical address space = PAS = 2^{16} byte. $P_s = 512$ bytes m/o is byte addressible.

$P_s = 2^B$ if Page table entry contain Lv, 1R, 3P, 1d
How many bits are still available in the page table entry, to store paging information?

$$\# \text{ frames} = \frac{2^{16}}{2^9} = 2^7 \text{ frames.}$$

$$16 - (7 + 1 + 1 + 3 + 1) = 3 \text{ bits remaining.}$$

Ques.) Consider a system, $S \text{ LAS} = P \text{ AS} = S$ bytes
 M/O is byte addressable. $P_s = p$ bytes
 $P_{Ts} = e$ bytes.

what is optimal value of page size by minimizing
 memory overhead of main^{tain}ing the page table size
 and internal fragmentation.

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$(A) P = \sqrt{2Se^2}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$(B) P = \sqrt{2Se}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$(C) P = \sqrt{2S^2e}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$(D) P = \sqrt{2(se)^2}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\text{Page size} = \# \text{ Pages} \times P_s \quad \# \text{ pages} = \frac{S}{P}$$

$$\therefore \text{Page size} = \frac{S}{P} \times P_s$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\text{Byte addressable Page size} = \underline{\text{Stes}} \quad \text{or required}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\text{M/O} = \text{P}_{Ts} + \text{Internal frag.}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\text{M/O} = \underline{\text{Stes}} + \underline{\text{P}}.$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\text{M/O} = 2ses + P^2.$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$2P$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\frac{d(\text{M/O})}{dp} = -\underline{\text{ses}} + \frac{1}{2} = 0$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$\frac{d^2(\text{M/O})}{dp^2} = 1 + \frac{1}{2} = \frac{3}{2} > 0$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$-\frac{\text{ses}}{P^2} = -\frac{1}{2}$$

~~S~~ ~~E~~ ~~F~~ ~~C~~ ~~C~~ ~~S~~ ~~D~~ ~~A~~ ~~R~~ ~~E~~ ~~H~~ ~~L~~ ~~I~~ ~~O~~ ~~M~~ ~~N~~ ~~P~~ ~~Q~~ ~~R~~ ~~S~~ ~~T~~ ~~U~~ ~~V~~ ~~W~~ ~~X~~ ~~Y~~ ~~Z~~

$$P^2 = 2ses \quad P = \sqrt{2ses}$$

Ques.) In a paging scheme, virtual address space is 4 KB and $es = 8 \text{ KB}$ what should be the optimal page size?

$$P = \sqrt{2^{12} \times 2^3 \times 2} = \sqrt{2^{26}} = 2^{13} \cancel{KB} \text{ bytes.}$$

$$P = 8 \text{ KB.}$$

Ques.) In a paging scheme, $LAS = 16 \text{ MB}$. $es = 2 \text{ B}$. what is optimal Page size.

$$P = \sqrt{2 \times 2^4 \times 2^{20} \times 2} \text{ Bytes.}$$

$$= 2 \times 2^2 \times 2^{10}$$

$$= 8 \times 2^{10} \text{ Bytes.}$$

$$P = 8 \text{ KB.}$$

Ques.) Consider a single level paging scheme.

$VAS = 4 \text{ MB}$. $P = 4 \text{ KB}$. what is the max Pe size?. Entire PT fits in one Page.

$$8 \text{ KB} = \frac{\cancel{4 \text{ MB}} \times \cancel{2 \times \cancel{8 \text{ B}}}}{4}$$

$$8 \text{ KB} = \frac{4 \text{ MB} \times 8 \text{ KB}}{4}$$

$$8 \text{ KB}$$

$$\text{Pe size} = 8 \text{ KB} \quad // \text{optimal}$$

$$PTs = \# \text{ entries} * es \quad \text{and} \quad PTs \leq Ps.$$

$$\# \text{ entries} * es \leq Ps.$$

$$N * es \leq Ps.$$

$$N \geq 8 \text{ P}$$

$$8 \text{ MB} \text{ has}$$

$e_s \leq P_s$

$\frac{LAS}{P_s} \leq b \Rightarrow$

$e_s \leq \frac{(P_s)^2}{LAS}$

when entire PT fits in one page.

$e_s \leq 4 B$

$e_{max} = 4 B$

Ques.) Consider single level paging scheme.

VAS = 4 GB

$P_s = 128 \text{ KB}$

(128×128)

$e_s \leq 4 \times 128 \times (128)^2 \text{ KB} \times \text{KB}$

$e_s \leq 2^{14} \times 2^{20}$

$2^2 \times 2^{30}$

$e_s = 2^{34-32} = 4 B \checkmark$

Ques.) Consider a single level paging scheme.

VAS = 256 MB. The Page table entry size is 4 B. what is the minimum P_s possible such that entire PT fit in one page.

$$4 B \leq (P_s)^2$$

256 MB.

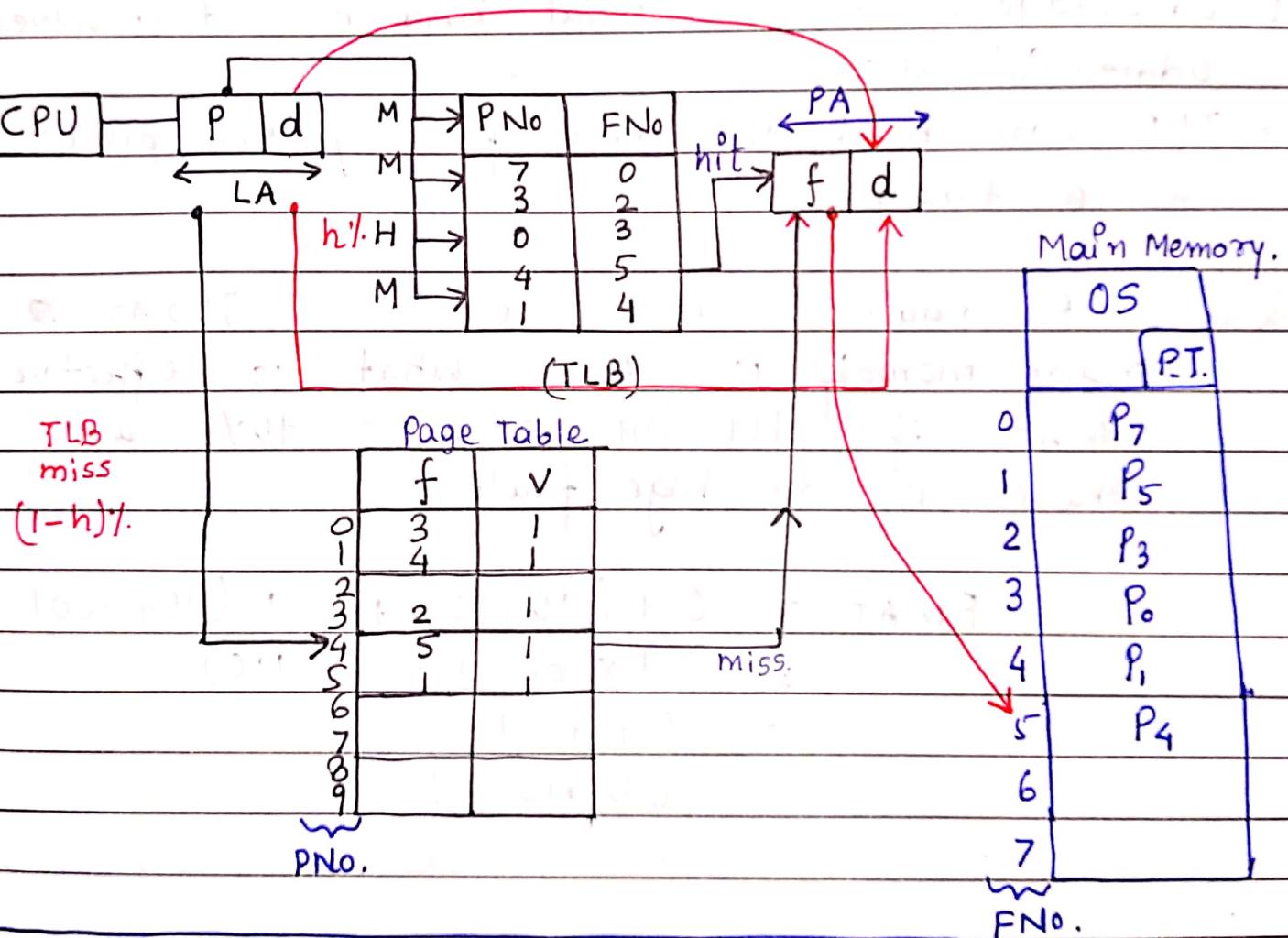
$$2^2 \times 2^{18} B \leq (P_s)^2$$

$$P_s \geq 2^{15}$$

$$|P_s \geq 32 KB|$$

TRANSLATION LOOK ASIDE BUFFER

- By using TLB, we can improve performance of memory access. Means we can reduce Effective Memory access time.



$$EMAT = h \cdot (c + m) + (1 - h) \cdot (c + m + m)$$

hit ratio } miss Ratio. } TLB PT Inst.
 TLB Acc. Inst. Acc. Acc. Acc. Acc.

- TLB contain 2 fields: PNo, Frame No
- Hardware device implemented using associative register. It is faster as compared to main memory.
- TLB will be placed before PT.

Advantage: TLB reduces effective memory access time.

Only one memory access is required.

Disadvantage: It is special hardware, it involves additional cost.

- TLB can hold the data of only one process at a time.

Ques.) A paging scheme uses TLB. TLB AT = 10 ns. Main memory is 50 ns. What is effective EMAT if TLB hit ratio is 90% and there is no page fault?

$$\begin{aligned}
 \text{EMAT} &= 0.9(10+50) + 0.1(10+100) \\
 &= 0.9 \times 60 + 0.1(110) \\
 &= 54 + 11 \\
 &= 65 \text{ ns}.
 \end{aligned}$$

Q.) Consider a paged virtual memory system with 32 bit virtual address. 1 KB pages. Each page table entry requires 32 bits and it is desired to limit page table size to 1 page size.

(i) How many levels of page table are required?

Sol.) ~~$LAS = 2^{32}$~~ # Pages = ~~$\frac{2^{32}}{2^{10} \cdot 2^3} = 2^{22-3} = 2^{19}$~~ ~~$2^{22}$~~
 ~~2^{22} entries $\times 2^2 = 2^{24}$ bits. or 2^{24} Bytes~~
 ~~2^{10} Bytes~~
 ~~2^{21} Bytes = 2^{11} pages. (Level 2).~~

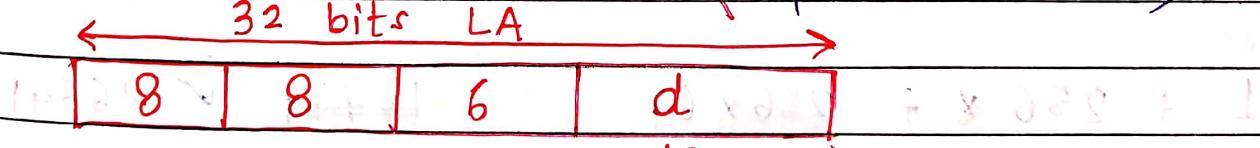
~~Size = $2^4 \times 2^5 = 2^{16}$ Bytes~~

~~$2^{16} = 2^6$ pages. (Level 3)~~

~~Size = $2^{6+5} = 2^{11}$ Bytes.~~

~~2¹⁰ = 2⁴ = 2⁴ pages.~~

~~$2 \times 2^5 = 2^6$ Bytes. (Level 4).~~



~~$\frac{2^{32}}{2^{10}} = 2^{22}$ pages. $\frac{2^{24}}{2^{10}} = 2^{14}$ pages $\rightarrow \frac{2^{16}}{2^{10}} = 2^6$ pages = 2^8 Bytes ✓~~

~~level 1 PTE~~ ~~level 2~~ ~~level 3~~

(address of level 3 stored here) (frames stored here)

(ii) The page table have 2 level have 2^8 entries.
 Table at 1 level 2^6 entries. If top level page table has 2^6 entries then how many pages are possible on page table?

$$P_S = 4 B \quad | L_3 | L_2 | L_1 | 10 B.$$

22.

$$2^8 \times 2^2 = 2^{10}$$



$$1 \text{ page} \times 64 \text{ pages} \times 256 \text{ pages} \times 64$$

$$2^{14} + 2^6 + 1 = 16384 + 64 + 1 \\ = 16449 \quad \checkmark$$

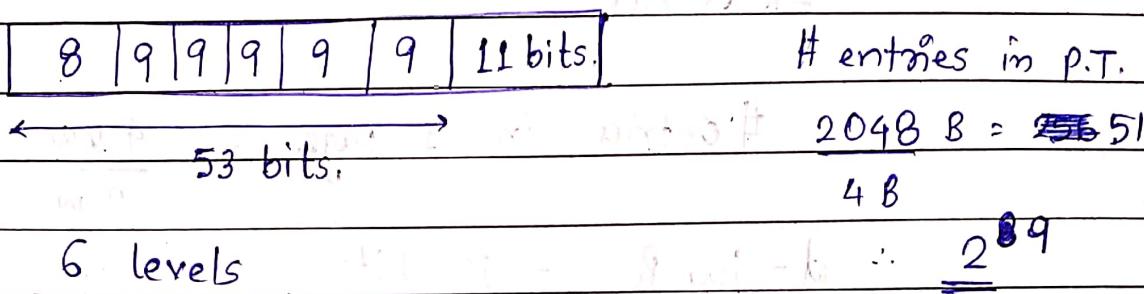
(i) A middle level has 2^6 entries, then how many pages are possible?

$$1 + 256 * + 256 \times 64 = 16449 \quad \checkmark \quad 16641$$

(iii) If bottom level has 2^6 entries how many pages?

$$1 + 256 + 256 * 256 = 65793 \quad \checkmark$$

Question.) A computer has a 64 bit virtual Address and 2048 Bytes (2KB pages). The page table entry size is 4 Byte. A multilevel page table is used and each page table size = 1 page. How many levels are required?



Ques.) Consider a system with 2 level paging. PT is divided into 2K pages. Each of size 4 Kiloword. PT entry size is 2 words. Memory is 49 word addressable. PAS is 64 MW which is divided into 16 K frames.

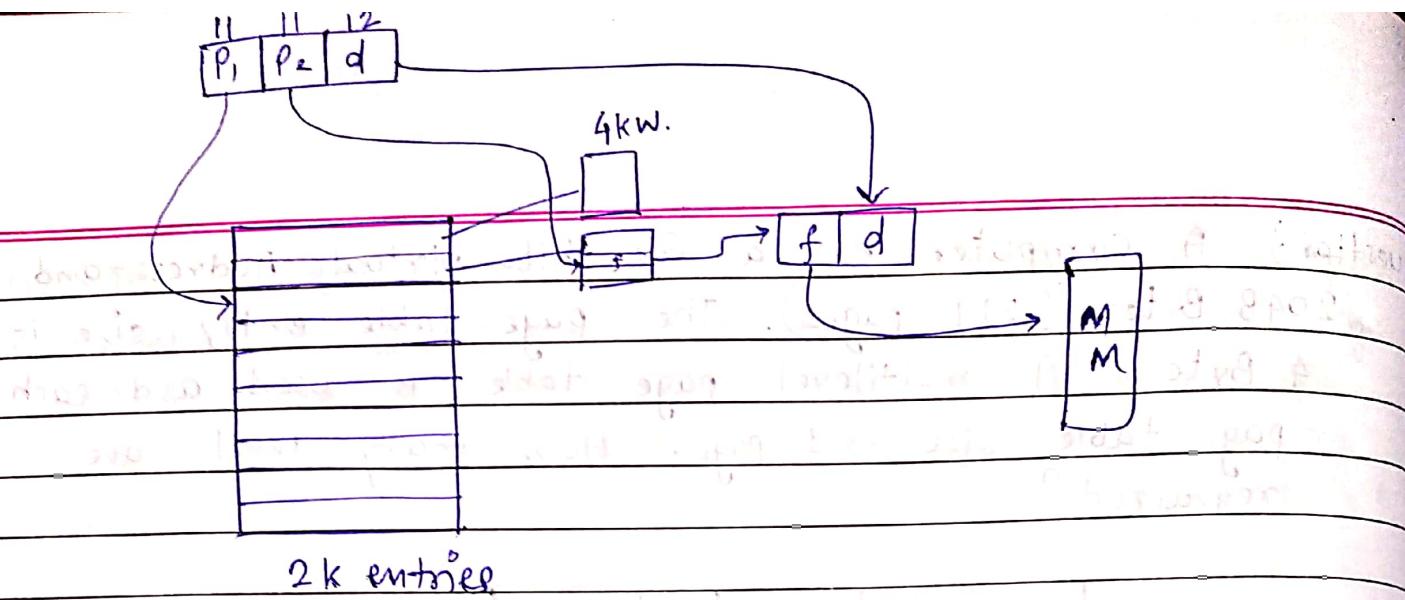
Then calculate :

- (i) length of logical address
- (ii) length of physical address
- (iii) outer page table size.
- (iv) inner page table size.

$$\frac{2^{16}}{2^{14}} = \# \text{ Pages} = 2^{12} \text{ pages. total.}$$

$$\text{size of frames} = \frac{2^{26}}{2^{14}} = 2^{12} = 4K \text{ words.}$$

$$\therefore \text{Page size} = 4 \text{ KW.}$$



$$\text{# entries in 1 page} = \frac{4 \text{ Kw}}{2 \text{ w}} = 2 \text{ K entries.}$$

$$d = \log_2 P_s = 12 \text{ bits.}$$

$$LA = P_1 + P_2 + d = 11 + 11 + 12 = 34 \text{ bits.}$$

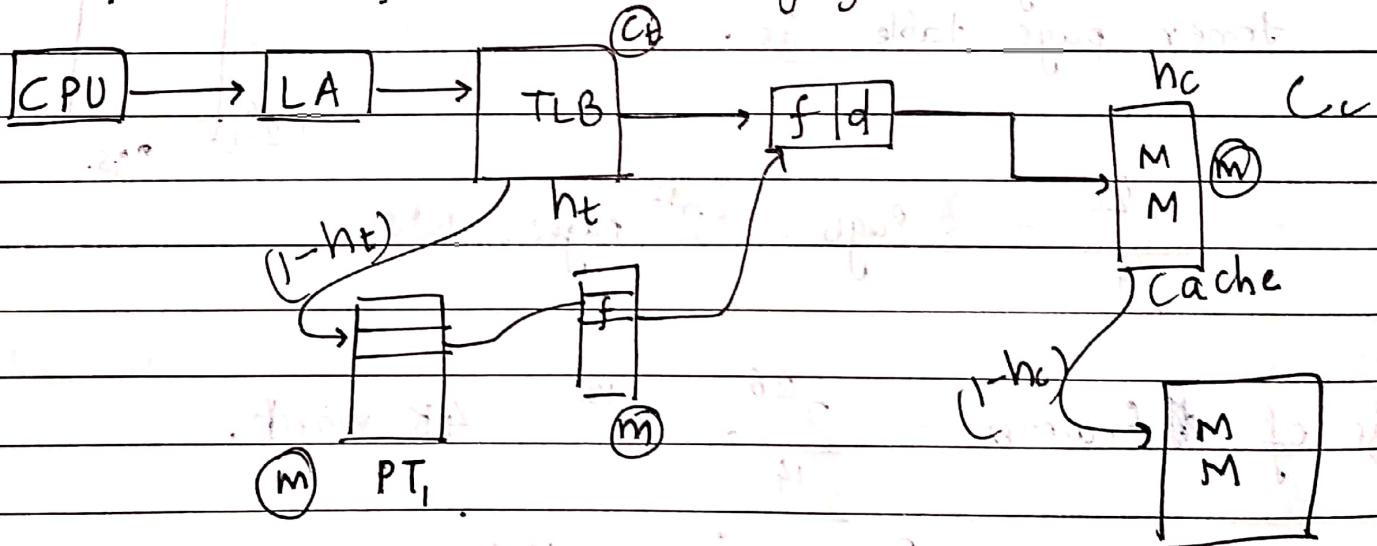
$$PA = f + d = \log_2(16K) + 12$$

$$= 14 + 12 = 26 \text{ bits.}$$

outer page table size = $2 \text{ K} \times 2 \text{ w} = 4 \text{ Kw}$

inner page table size = $2 \text{ K} \times 2 \text{ w} = 4 \text{ Kw}$

Performance of Multilevel paging: For two levels.



$$E_{mat} = h \cdot (c + m) + (1-h) \cdot (c + m + m + m)$$

↓ Hit ↓ TLB ↓ Main Memory ↓ Miss ↓ TLB ↓ PT₁ ↓ PT₂ ↓ P_{Main Memory}

In general,

$$E_{mat} = h(c + m) + (1-h)(c + (n+1)m)$$

where n is number of levels.

Ques.) TLB hit ratio is 0.95. $C = 0$.

cache memory access time 10 ns

MM access time = 100 ns.

CM hit ratio = 90%.

Find effective memory access times for 2 level paging system.

~~$$\begin{aligned}
 E_{mat} &= 0.95(0.9 \times 10 + 0.1 \times 100) + 0.05(0.9 \times 10 + 0.1 \times 100) \\
 &\quad + 0.9 \times 10 + 0.1 \times 100 + 0.9 \times 10 + 0.1 \times 100 \\
 &= 0.95(9 + 10) + 0.05(3 \times 19) \\
 &= 19.05 + 2.95
 \end{aligned}$$~~

~~$$E_{mat} = h_{TLB} (C_t + h_{cache} * C_c + (1 - h_{cache}) * (C_c + m))$$~~

~~$$+ (1 - h_{TLB}) [C_t + m + m + h_{cache} * C_c + (1 - h_{cache})(C_c + m)]$$~~

~~$$E_{mat} = 30 \text{ ns } \checkmark$$~~

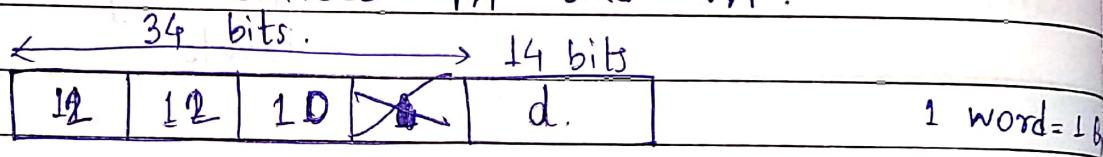
Ques.) Consider a system using multilevel paging scheme. Page size is 16 KB. Memory is byte addressable.

$$P_s = 16 \text{ KB}$$

$$VA = 48 \text{ bits.}$$

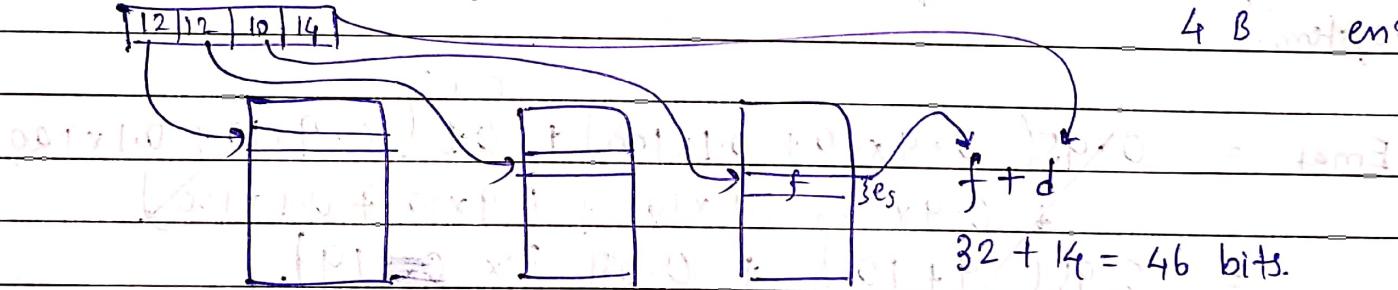
$$e_s = 4 \text{ B.}$$

- (i) How many levels of Page table are required
(ii) Give the divided PA and VA.



$$d = \log_2 P_s = \log_2 2^{14} = 14 \text{ bits}$$

pages \Rightarrow # entries in level L = $\frac{16 \text{ KB}}{4 \text{ B}} = 4096$ entries

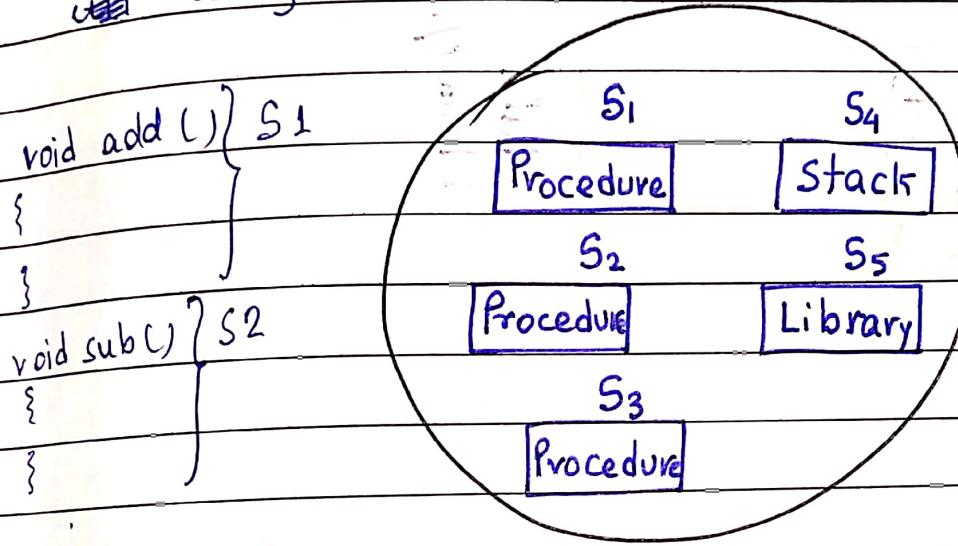


$$\therefore PAS = 2^{46} \text{ B} = 64 \text{ TB}$$

frame bits = e_s .

Segmentation

- Like paging, segmentation is another non-contiguous, memory location technique.
- In segmentation, process is not divided into fixed sized pages. The process is divided into modules for better utilization.

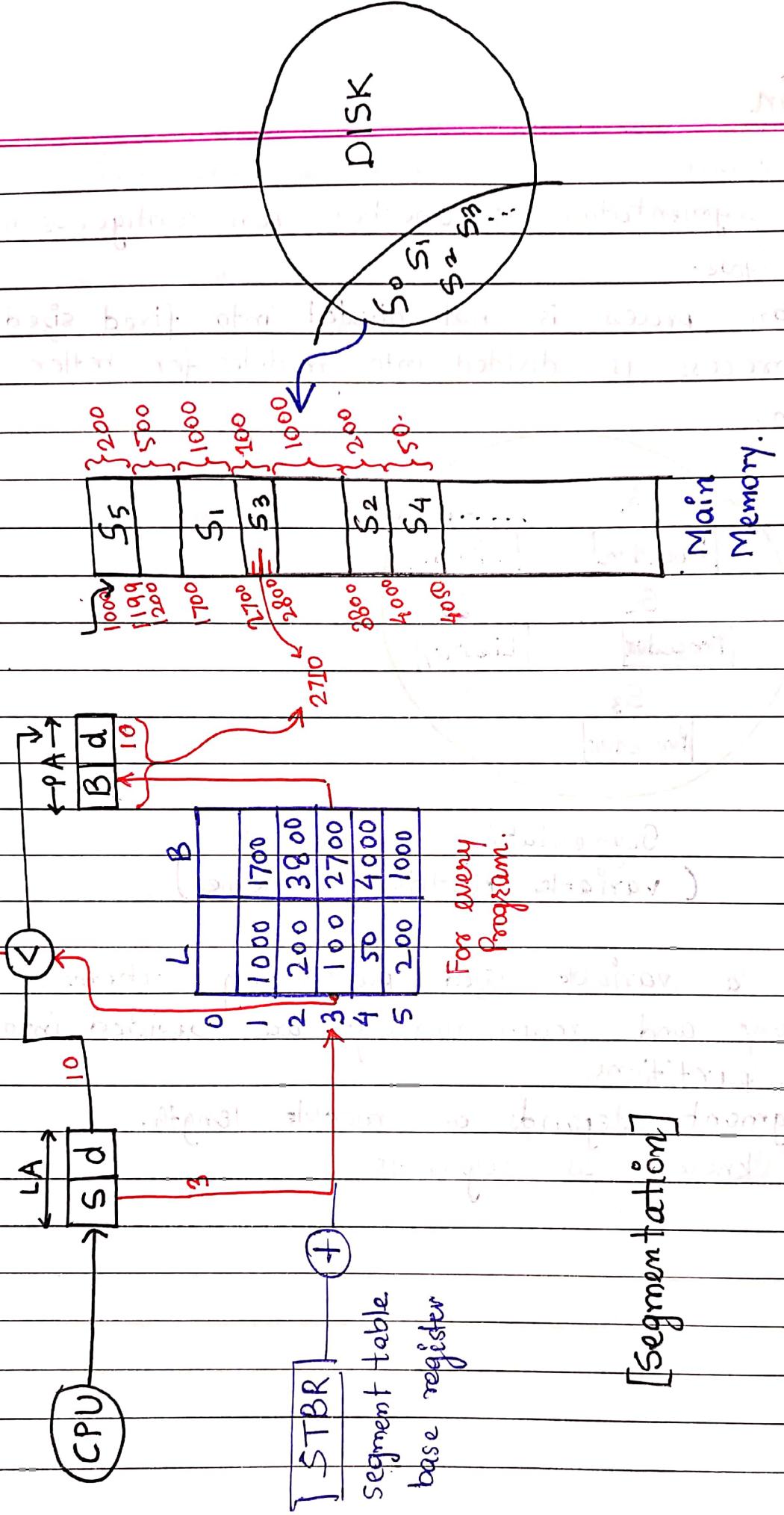


Segmentation
(variable partition scheme.)

- Segmentation is a variable sized partitioning scheme.
- Secondary memory and main memory are divided into variable size partitions.
- Size of segment depends on module length.
- Partition is known as segments.

SYSTEM

OPERATIONS



Ques) Consider following segment table.

S ₀	1219	700
S ₁	2300	14
S ₂	90	100
S ₃	1327	580
S ₄	1952	96

which of the following produces trap?

- (A) 0, 430 → 1649
- (B) 1, 11 → 2311
- (C) 3, 425 → 1752
- (D) 4, 95 → 2047
- (E) 2, 100 → 190 ✓

In segmentation, Logical Address space, segment No / segment address / Number of bits required to represent segment size or word No of segment, or word offset or word address of segment.

$$S = \log_2 \# \text{segment}$$

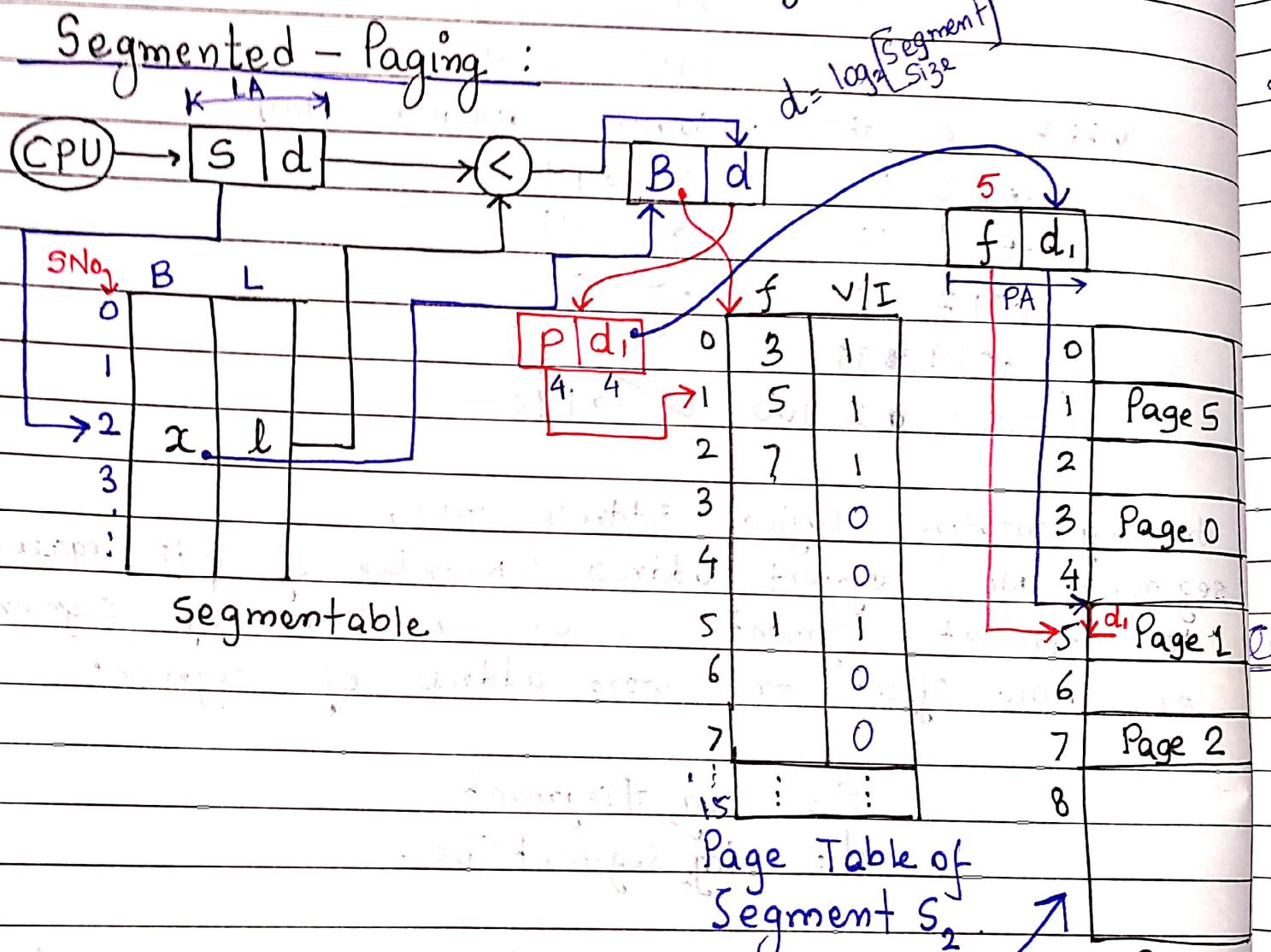
$$d = \log_2 \text{segment Size}.$$

No of entries in the segment table is equal to the number of segments in logical address space.

In segmentation = PA = B + d where B is starting address of segment, and d is the word offset in the segment.

- The variable size fragments transferred from logical address space to physical address space. Hence it is similar to variable partitioning scheme. Thus it suffers from external fragmentation.

Segmented - Paging :

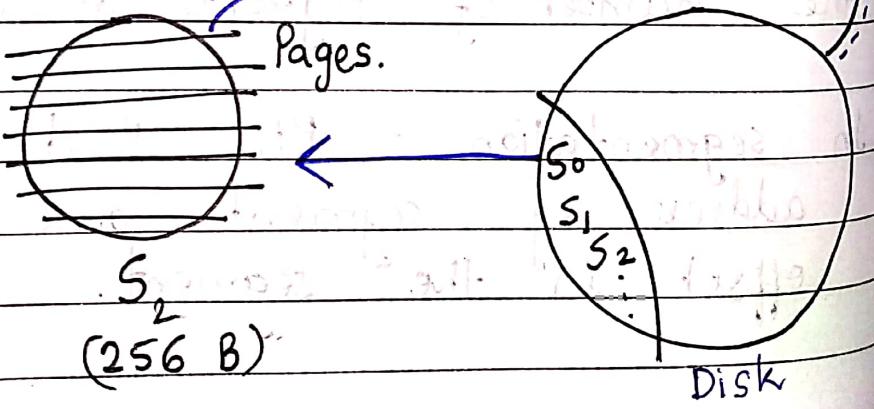


$$P_S = 16 \text{ B.}$$

$$\# \text{ Pages} = \frac{256}{16} = 16.$$

$$P_1 = \log_2 16 = 4 \text{ bits}$$

$$d_1 = \log_2 16 = 4 \text{ bits.}$$



- To avoid overhead of transferring large size segment into memory, the segmented paging will be applied. In segmented paging, the paging will be applied on segment.

$$\text{Logical Address} = s + d.$$

$$d = p + d_1$$

where p is Pagenumber of segment.
 d_1 is word number of page.

$$d = \log_2 \text{Segment size}$$

$$d_1 = \log_2 \text{Page size.}$$

$$p = d - d_1 = \log_2 \# \text{Pages in Segment.}$$

$$d_1 = \log_2 m$$

Ques Given, # segments = 2^{18}

$$Ps = 1 \text{ KW}$$

$$SS = 64 \text{ KW}$$

Find, s, d_1, p, d_1 ?

$$s = \log_2 2^{18} = 18 \text{ bits.}$$

$$d_1 = \log_2 Ps = \log_2 2^{10} = 10 \text{ bits.}$$

$$\# \text{ Pages} = \frac{64 \text{ K}}{1 \text{ K}} = 64 \text{ pages. } m = 2^6$$

$$\therefore p = \log_2 2^6 = 6 \text{ bits.}$$

$$d = 2^6 = 16 \text{ bits.}$$

Advantages of Segmented Paging:

- Reduces memory usage.
- Size of page table is limited by segment size.
- It solves the problem of external fragmentation.

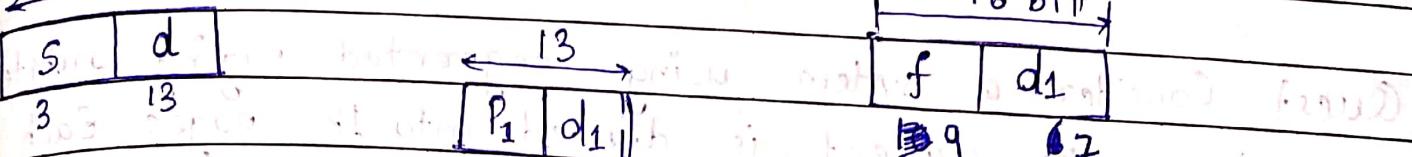
Disadvantages:

- Internal fragmentation.
- Complexity level is much higher as compared to paging.

(Ques.) A certain Computer System has segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and Physical Address space contain 2^{16} Bytes. The virtual address space divided into 8 non overlapping equal size segments. The memory management unit has a hardware segment table. Each entry of which contains the physical address of page table for a segment. Page tables are stored in the main memory and consist of 2 Bytes page table entry. What is the minimum page size in bytes so that the page table of a segment require atmost one page to store it?

$$LAS = PAS = 2^{16}$$

16 bits.



$$\# \text{ segments} = 8$$

$$\text{Segment size} = 2^{13} \text{ Bytes}$$

$$d = \log_2 2^{13} = 13 \text{ bits}$$

d is divided into P_s and d₁.

$$\text{Page table entry} = 2 \text{ bytes} = 16 \text{ bits}$$

$$\text{frame no.} = 16 \text{ bits}$$

$$\text{Total } P_s = 2 \text{ bytes} \times \# \text{ pages.}$$

$$\# \text{ pages} = 2^{13}$$

$$\# \text{ entries in page table} = N \times e_s$$

$$PT_s < P_s$$

$$N \times e_s < P_s$$

$$2^{13} \times 2 < P_s$$

$$x^2 > 2^{14}$$

$$x \geq 2^7$$

$$\text{Consequently } x = 128 \text{ Bytes.}$$

ii) Consider above problem, get the division of virtual address.

$$d_1 = \log_2 2^7 = 7 \text{ bits}$$

$$P_s = 13 - 7 = 6 \text{ bits.}$$

Paging on Segment table and segment.

(see snapshot in one note).

Ques) Consider a system using segmented paging architecture, where the segment is divided into 1k pages. Each of size 512 words. And the segment table is divided into 1K pages, each of size 256 words. The frame number require 18 bits to represent all the frame of physical address space. Page table entry size is 2 words. Memory is word addressable. Calculate, LA, PA, PT size of segment, PT size of segment table.

Solution:

Given,

$$\text{Segment size} = 1024 \times 512 \text{ words}$$

$$= 2^{10} \times 2^9 \text{ words} \\ = 2^{19} \text{ words.}$$

$\therefore \text{S+D} = 18 \text{ bits.}$

$$d_1 = \log_2 [\text{Pagesize}] = \log_2 2^9 = 9 \text{ bits}$$

$$P_1 = 19 - 9 = 10 \text{ bits.}$$

$$\therefore \# \text{Page table (for segment table)} = 2^{10} \text{ entries.}$$

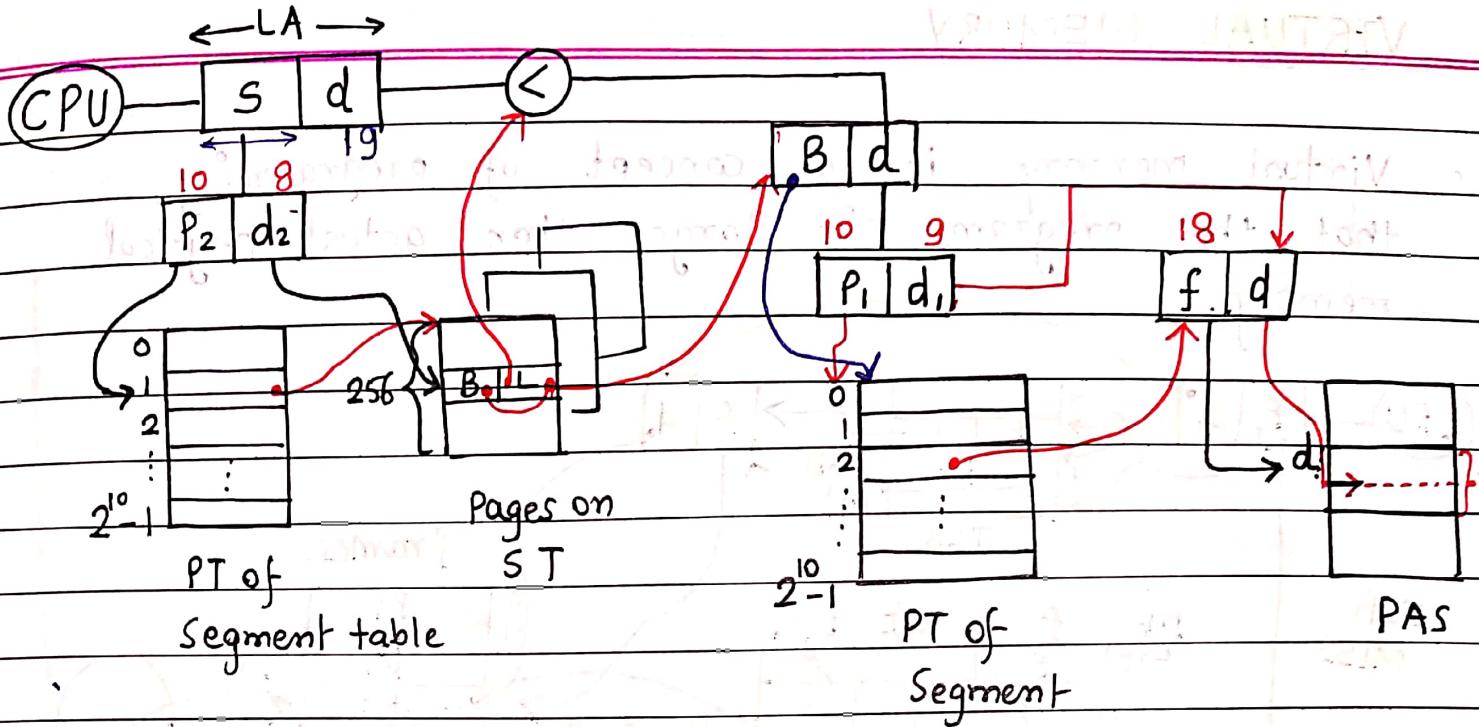
[See side diagram]

$$S+d = 18 + 19 = 37$$

$$P_2 + d_2 = 10 + 8$$

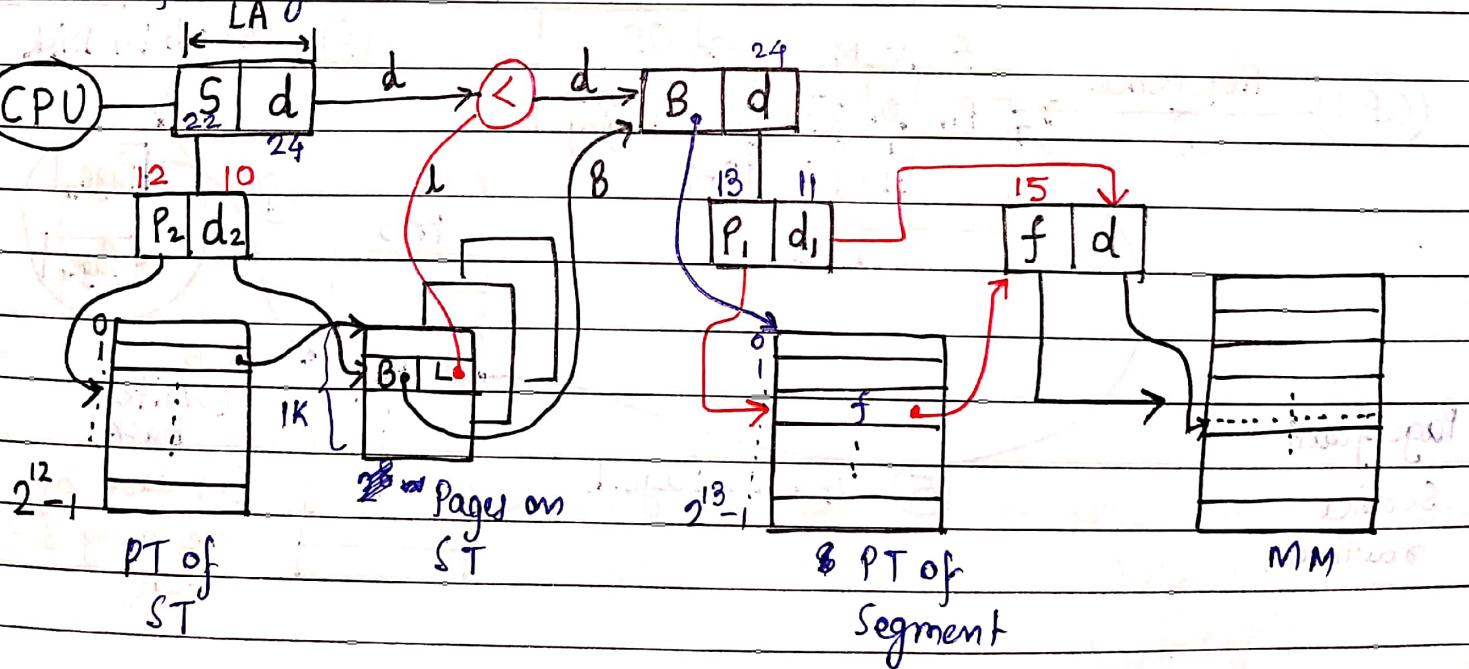
$$P_1 + d_1 = 10 + 9$$

$$f + d = 18 + 9$$



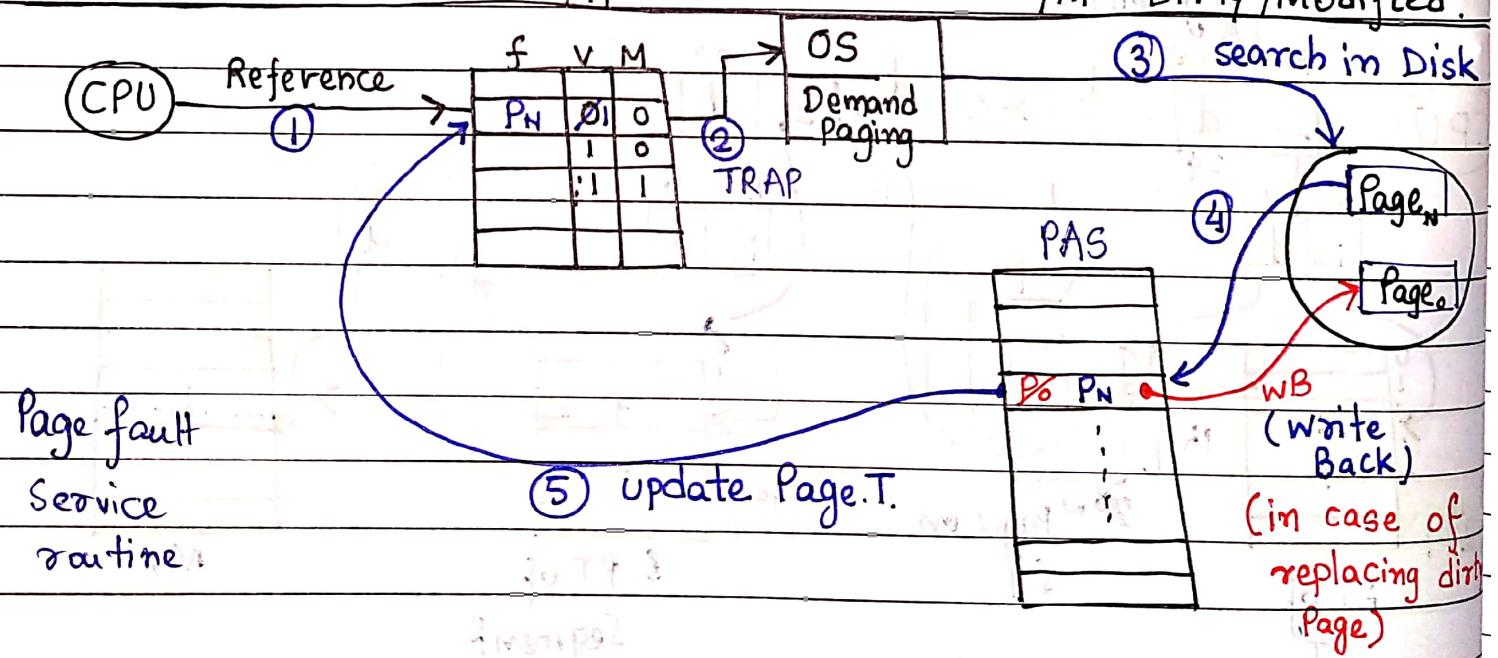
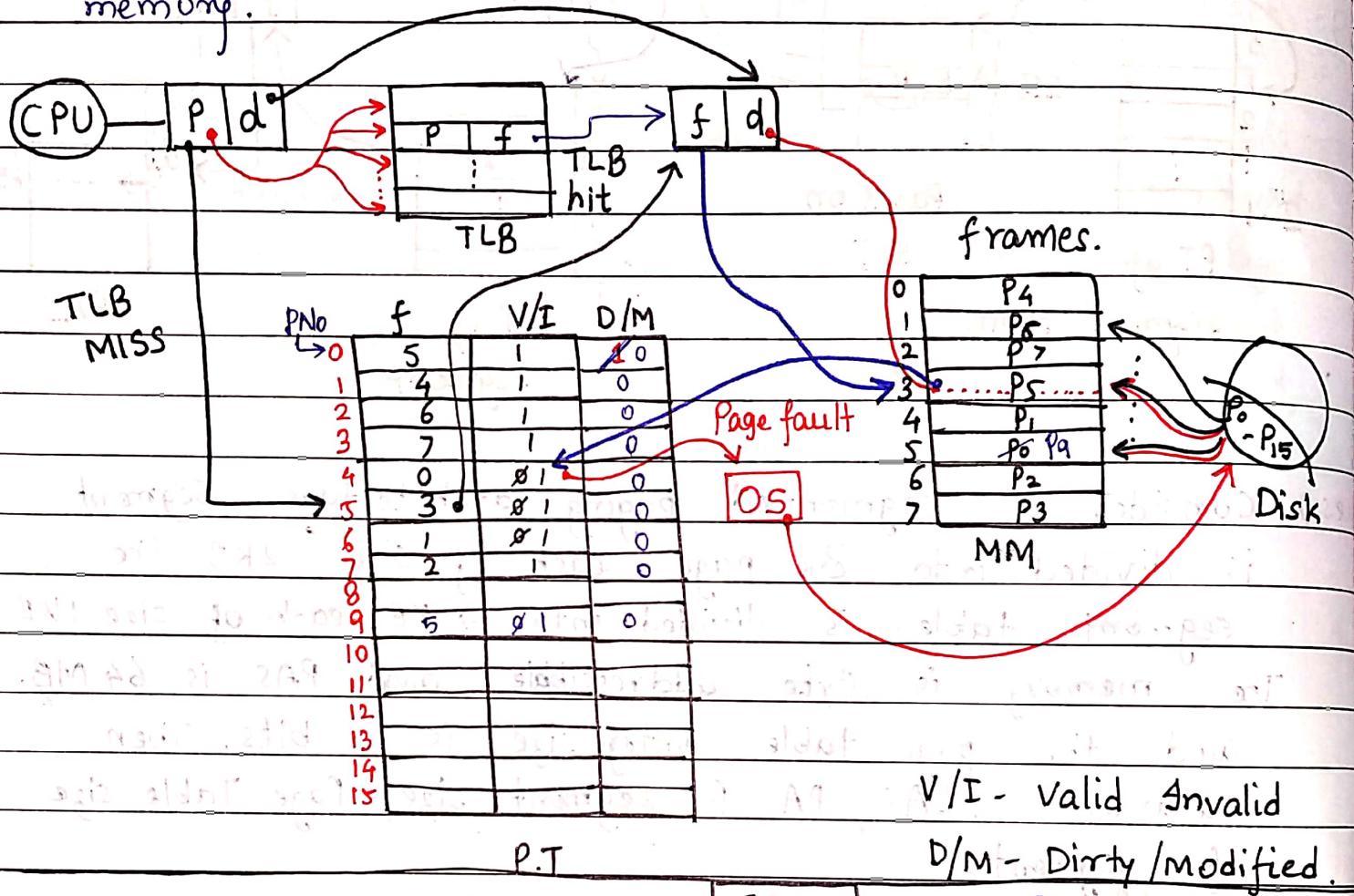
Ques.) Consider a segmented paging architecture. Segment is divided into 8K pages each of size 2KB. The segment table is divided into 4 KB each of size 1KB. The memory is Byte addressable and PAS is 64 MB. and the page table entry size is 32 bits. Then calculate LAS, PA, PT segment size, Page Table size.

Size of segment.



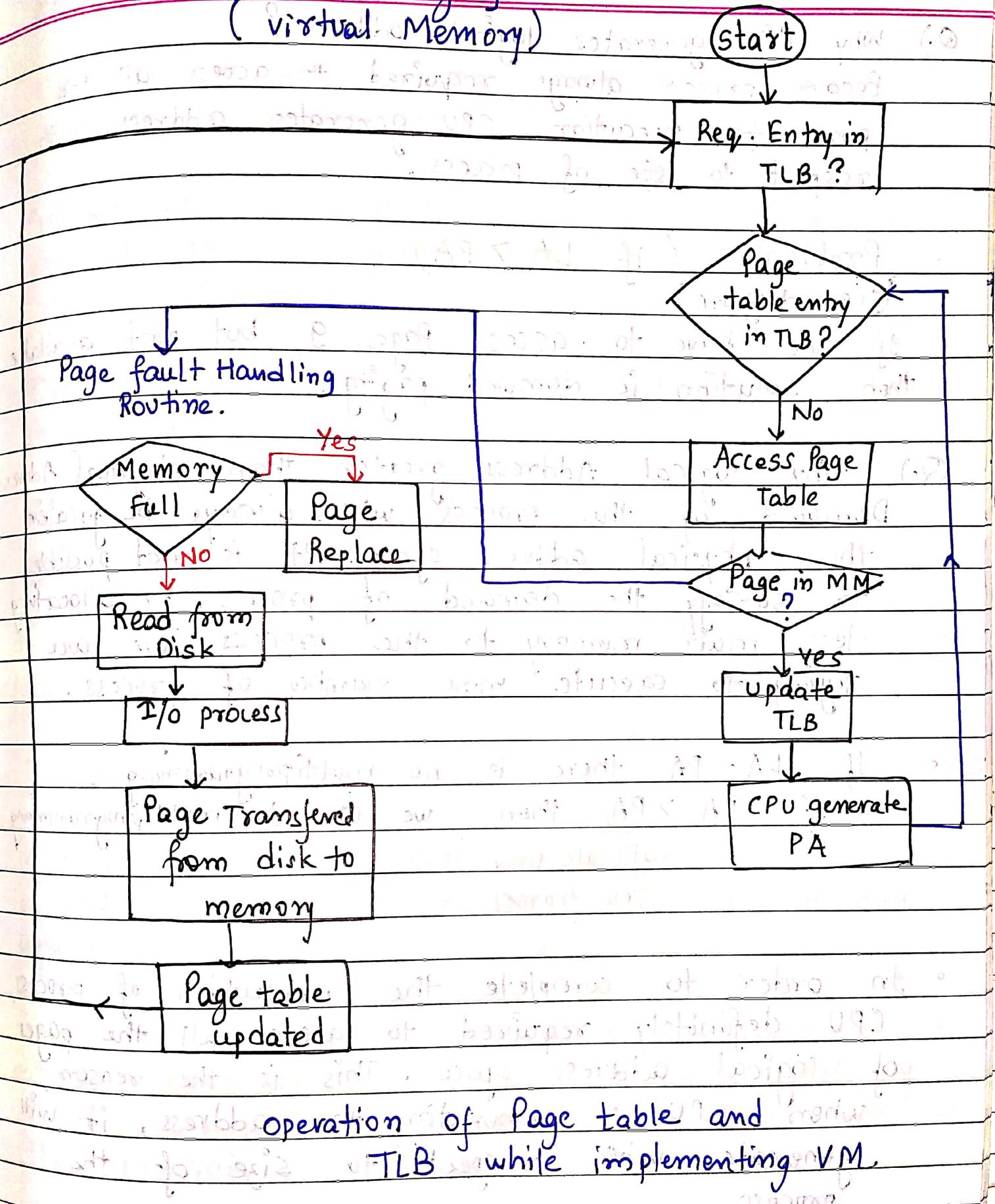
VIRTUAL MEMORY

- Virtual memory is a concept of programming, that the program size is larger than actual physical memory.



TLB and Paging

(Virtual Memory)



operation of Page table and TLB while implementing VM.

Q.) Why CPU generates logical address?

- Because process always required to access all the pages for execution. CPU generates address with respect to size of process.

Problem (if $LA > PA$)

(see diagram)

- If we have to access Page 9, but not available then solution is demand paging.

Q.) Why logical Address greater than physical Address?

Demand of the process will always be greater than physical address space. It is not possible to satisfy the demand of process by allocating less main memory to the process, we are trying to execute more number of process.

- If $LA = PA$ there is no multiprogramming.
- If $LA > PA$, then we can do multiprogramming
allocate only few frames
- In order to complete the execution of process, CPU definitely required to access all the pages of logical address space. This is the reason when CPU is generating the address, it will generate with respect to size of the process.

PAGE FAULT:

- CPU tries to access a page, but the page is not available in memory, then it is called as page fault.
- Program execution will be stopped and signal will be sent to the OS recording page fault. Then the OS validates the detail of the process.
- Operating System will search for the required page in Logical Address space.
- Required page will be transferred from logical Address space to physical address space.
- If main memory is full, then apply Page replacement algorithm.
- Decision making algorithm for replacing the page in PAS.
- Page fault will be updated in page table. If P-T is not updated, then it will result in page fault again.
- Signal will be sent to the CPU to continue the program execution. Then the CPU will access the required page in the memory, and will continue the program execution.

QUESTION TODAY

- Because of this process, program execution will stop if it cannot be observed by user.

~~What are the factors of the fault generation in demand?~~

DEMAND PAGING:

- Loading a page into main memory from LAs to PAS on demand.

- ~~STEPS~~
- The time taken to service a page fault, is called as page fault service time.
 - Page fault service time include the time required to perform all the six steps.

- If page fault service time = S ,
main memory access time = m

$$E_{mat} = (1-p)m + sp \quad (\text{using } m \ll S) \quad \# \text{miss} + \# \text{ref}$$

- ~~Ques.) Consider a system with page fault service time be 200 ns. Page hit ratio is 95%. Access time is 20 ns.~~

$$\begin{aligned} E_{mat} &= 0.95 \times 20 + 0.05 \times 200 \\ &= 19 + 10 \\ &= 29 \text{ ns} \end{aligned}$$

Ques)

Suppose an instruction take, i microseconds, and additional j microsecond. If page fault occurs what is effective memory access time, if page fault occurs on an average every k instructions?

$$\text{page fault rate} = \frac{1}{k}$$

$$E_{MAT} = i + j \cdot \frac{1}{k}$$

Ques) Let the page fault service time be 10^{-2} s with average memory access time be 20 ns. If 1 page fault is generated for every 10^6 memory access. Then what is effective MAT.

$$\begin{aligned} E_{MAT} &= \left(1 - \frac{1}{10^6}\right) \times 20 \text{ ns} + \frac{10^{-2+9} \text{ ns}}{10^6} \times 1 \\ &= \frac{(10^6 - 1)}{10^6} \times 20 + 10 \\ &= 19.999 + 10 \end{aligned}$$

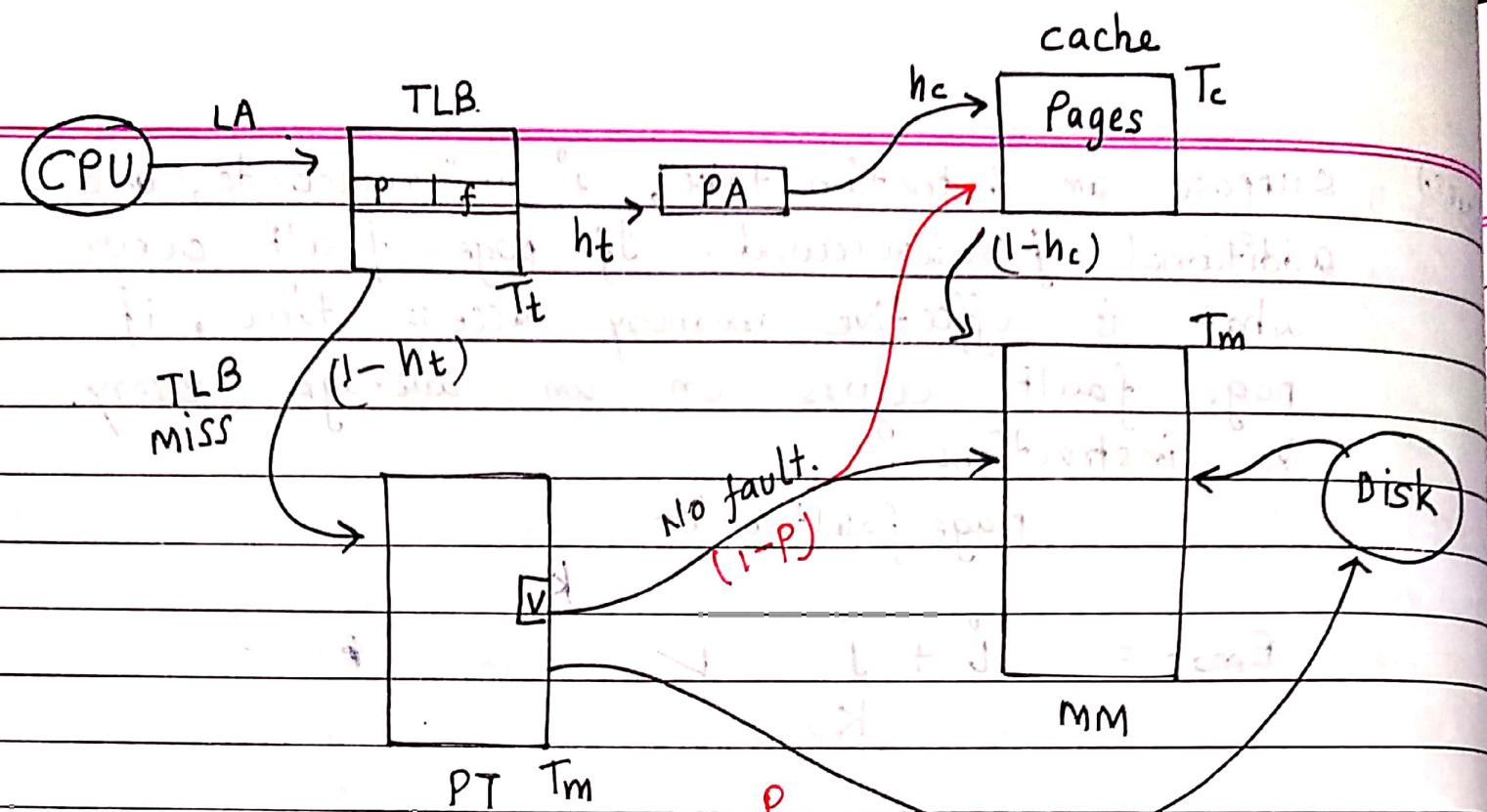
Ans) $E_{MAT} = 29.999$ ns (approximate value)

Ans) $E_{MAT} = 30 \text{ ns}$ with one page fault

Ans) E_{MAT} of the unit will be 10 ns

Ans) E_{MAT} of the system will be 10 ns

Ans) E_{MAT} of the system will be 10 ns



$$\text{EMAT} = h_t [T_t + h_c T_c + (1-h_c)(T_c + T_m)] + (1-h_t) [T_t + T_m + (1-p)[h_c T_c + (1-h_c)(T_c + T_m)] + p \times S]$$

Negligible
as compared to S

Ques) Consider a system using demand paging, the page fault service time is 200 ms and main memory access time is 10 ms. the TLB is added to improve the performance. 80% reference are found in TLB, and that of remaining, 10% cause page fault. TLB access time and Page table access time both are negligible. What is effective MAT?

$$EMAT = 0.8 \times 10 \text{ ms} +$$

$$0.2 \times [0.4 \times 0.1 \times 200 \text{ ms} + 0.9 \times 10 \text{ ms}]$$

$$EMAT = 13.8 \text{ ms}$$

Ques.) Consider demand Paging environment where if it takes 8 ms to service a page fault, if either an empty frame is available or replaced page is not to be modified. If it takes 20 ms to service a page fault if a page is modified. Main memory access time is 1 ms and further assume page to be replaced is modified 70% of the time. Then what is the maximum acceptable page fault rate to get an Emat not more than 2 ms.

$$Emat \leq 2 \text{ ms}$$

$$2 \text{ ms} \geq (1 - P) \cdot 1 \text{ ms} + P [0.7 \times 20 \text{ ms} + 0.3 \times 8 \text{ ms}]$$

$$2 \text{ ms} \geq 1 \text{ ms} - P \text{ ms} + 16.4 \text{ ms} \times P$$

$$2 \text{ ms} \geq 1 \text{ ms} - 16.4 \text{ ms} \times P$$

$$P \geq 0.0649$$

$$15.4 \text{ ms} \leq 1 \text{ ms} \times P$$

$$P \leq 0.0649$$

$$P \leq 0.0649 \approx 6.4\%$$

$$P \leq 6.4\%$$

Page Replacement Algorithm

1) FIFO

2) LRU

(1) FIFO : It replace the oldest page that has been present in the main memory for the longest time. It is implemented by keeping track of all the pages in a queue.

Ques For e.g. Consider number of frames in memory = 3

Ques What is the total number of page fault that occurred in memory using these reference.

1 4 1 2 3 0 1 2 0 3 0 4 2 3 0
 2 7 2 1 7 6 1 6 7 6 1 2 1 7 2
 3 6 7 1 1 7 1 1 7 1 0 1 2 3 0
 4 1 2 3 0 1 2 0 3 0 4 2 3 0
 5 7 2 1 7 6 1 6 7 6 1 2 1 7 2
 6 7 1 1 7 1 1 7 1 0 1 2 3 0

Ques Number of frame = 4

1 2 3 0 1 2 0 3 0 4 2 3 0
 2 7 2 1 7 6 1 6 7 6 1 2 1 7 2
 3 6 7 1 1 7 1 1 7 1 0 1 2 3 0
 4 1 2 3 0 1 2 0 3 0 4 2 3 0
 5 7 2 1 7 6 1 6 7 6 1 2 1 7 2
 6 7 1 1 7 1 1 7 1 0 1 2 3 0

At

7 3 2 1 2 0 3 0 4 1 7 1 0 1 2 3 0
 # miss = 10 # hit = 10

8 4 7 1 2 0 3 0 4 1 7 1 0 1 2 3 0

X 0

2 1 3 0 4 1 7 1 0 1 2 3 0
 If No. of frame = 3,

1 2 3 0 1 2 0 3 0 4 1 7 1 0 1 2 3 0
 2 3 0 1 2 0 3 0 4 1 7 1 0 1 2 3 0

7 2 4 0 1 2 0 3 0 4 1 7 1 0 1 2 3 0

8 3 2 1 0 1 2 0 3 0 4 1 7 1 0 1 2 3 0
 X 0 3 2 1 0 1 2 0 3 0 4 1 7 1 0 1 2 3 0
 # miss = 15 # hit = 5

Ex 1 2 3 4 1 2 5 1 2 3 4 5. (S)

Total = 12 and total no. of page fault = 10. Frame = 4.

Frame = 3 \Rightarrow 9 \Rightarrow Frame = 4. \Rightarrow 10

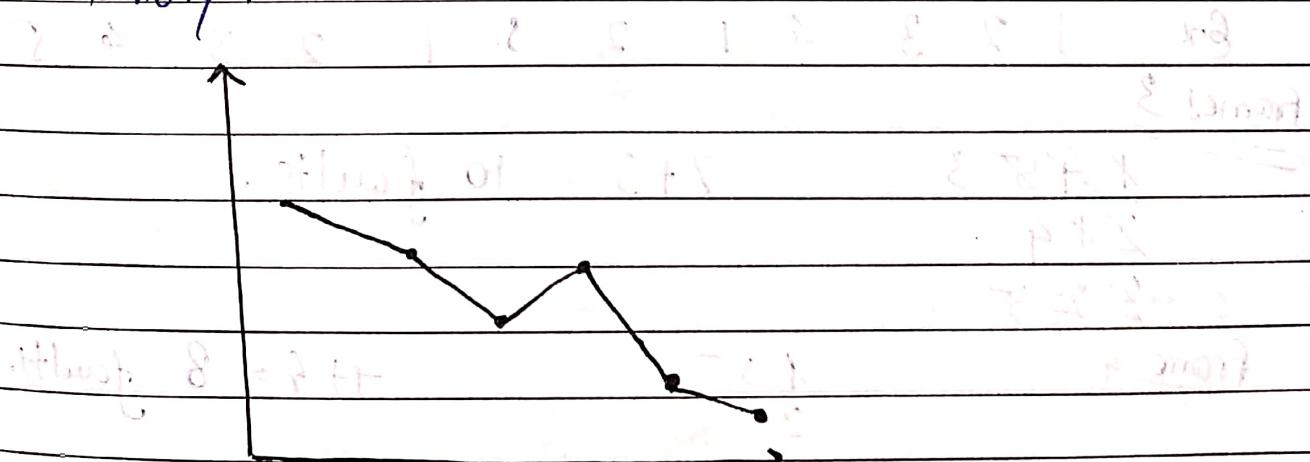
1 X 5 6 5 6 1 2 5 1 2 X 5 7 8 9

2 X 3 8 2

3 X 4 5 6 7 8 9 10 11 12 13

Ques: Effect of increasing no of frames : The no of page fault should either decrease or remain constant on increasing the number of frames in the main memory. But sometime, the unusual behaviour is observed.

- Some times by increasing the number of frames in main memory, the number of page fault also increase. This is known as Belady's anomaly. Phenomenon of increasing the page faults on increasing No of frame in main memory.



FIFO, Random page replacement algorithm and Second chance algorithm.

(2) LIFO + page replacement algo: It replaces the newest page that arrived at last in the main memory. It is implemented by using stack.

Eu 4 7 6 1 7 6 1 2 7 2.

frames \Rightarrow 3. $8 \times 8 \times 2$ $4+3=7$ faults. $\frac{1}{8} \cdot 8 = 1$

7

67-0115-3-004 In or vicinity to hospital 2000 ft 2000

frame = 4, x2, y2, width, height, color

$3+4=7$ faults.

4

(3) LRU (Least recently used): If replaces the page that has been referred by the CPU for the longest time. Replace the page that has not been used for longest period of time.

~~Ex~~ 1 2 3 4 1 2 5 1 2 3 4 5.

frames = 3

$$X \not\models S3 \quad 7+3 = 10 \text{ faults.}$$

2 x 4

325

frame = 4

15-

$$4+4 = 8 \text{ faults.}$$

88.4
43

Ex. ~~1 7 0 0 1 2 0 3 0 4 1 2 1 0 3 0 1 3 0 2 1 0 2 0~~

~~frame = 3.~~

$$\begin{array}{l} 7 2 4 0 \times 7 \\ 0 3 0 \\ \hline = 10 + 3 \checkmark \\ 12 \text{ faults.} \end{array}$$

(Ques) MRU : ~~9 1 2 3 4 1 2 5 1 2 3 4 5~~

~~frame = 3~~

~~1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16~~

Optimal page Replacement:

- Replace the page that will not be used for longest period of time in future.

Ex. ~~1 7 0 0 1 2 0 3 0 4 1 2 1 0 3 0 1 3 0 2 1 0 2 0~~

~~frame = 3~~

~~1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16~~

~~frame = 3~~

$$\begin{array}{l} 1 4 \\ 2 \\ 3 4 5 \\ \hline 4 + 3 = 7 \text{ faults. } \checkmark \end{array}$$

~~3 4 5~~

Ex. Consider following reference for 460 words program

10 11 104 170 73 309 185 245 246 434
458 364

Give

(i) the memory reference string assume page size = 100 words.

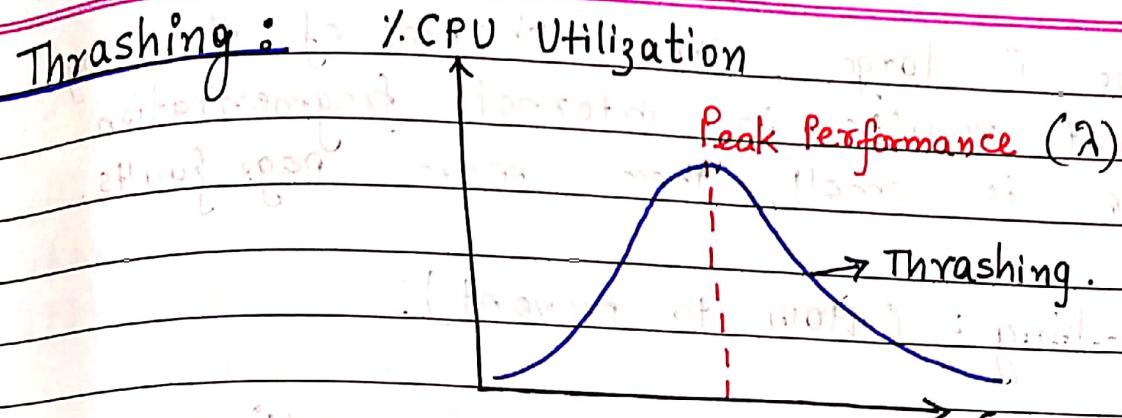
(ii) Find No of page faults. Assuming 200 words available in primary memory at a time (By using LRU).

(iii) 1 1 2 2 1 4 2 3 3 5 5 4

(iv). 1 2 5 $5 + 2 = 7$ faults.

Ques: A system uses FCFS algorithm for page replacement. It has 4 page frames, with no pages loaded to begin. The system first access 100 distinct pages, in some order, and then access same 100 pages but in reverse order. How many page faults will occur. 196 ✓

Thrashing :



- In the initial stage of multi-programming, the CPU utilization is very high and the system resources are utilized 100%. If further increase in the degree of multiprogramming, the CPU utilization will repeatedly fall down and the time taken to complete its execution will increase and the system spends more time only in page replacement.
- Every page reference will be page fault and CPU remain busy in dealing with page fault. It is called thrashing.
- High paging activity is called thrashing. A process thrashes if it is spending more time in paging than executing.
- CPU utilization is very low when the page fault rate is very high.

Reason of thrashing :

- Primary Reason : High degree of multiprogramming
- Secondary Reason : Lack of frames, Bad page replacement algorithm, Page size smaller.

- If page size is large, then chances of thrashing reduces, but results in internal fragmentation.
- If page size is small, then more page faults.

Control Thrashing : (How to prevent).

(i) Prevent : Controlling the degree of multiprogramming
 Don't allow the system to go into thrashing and instruct the long term scheduler, not to bring the process into main memory, After the point of

(ii) Detection : Low CPU utilization, low throughput, high degree of multiprogram, high paging demands from disk.

(iii) Recovery : Process suspensions, allows the system to go into thrashing and then instruct the mid-term scheduler to suspend some of the process so that the system will recover from thrashing. Or we can increase RAM size.

Ques Consider the system with below condition,

- i) 90% of the page is in disk.
 - ii) CPU utilization is 10%.
- which of the below factors will improve CPU utilization.

(A) Install the bigger disk. → NO

- ~~To increase CPU utilization have to select~~
- (B) Install the faster CPU - NO.
 - (C) Increase degree of multi programming - NO
 - (D) Decrease degree of multi programming. ✓
 - (E) Install more RAM. ✓
 - (F) Decrease page size - NO. (Because if pages req. by process will increase.)
 - (G) Increase page size ✓ (Because pages req. by process will be less.)

Frame allocation Policy

• If m = (number of frame available) in main memory.
 n = (number of process)
 s_i^o = number of frame demand of each process.

Allocation of frame for each process = $s_i^o \times m$
where s_i^o is # frames demanded by i th process
 s is $\sum s_i^o$, total frames demanded
 m , # frames in main memory.

This is called proportional frame allocation policy.

Ques For a certain system, total number of frames is 64. The size of two process P_1 and P_2 are $P_1 = 10$ and $P_2 = 127$.
How much allocation for each process?
for $P_1 = \frac{10}{137} \times 64 = \frac{640}{137} = 4.65$
 $P_2 = \frac{127}{137} \times 64 = \frac{8032}{137} = 59$.

File and Device Management

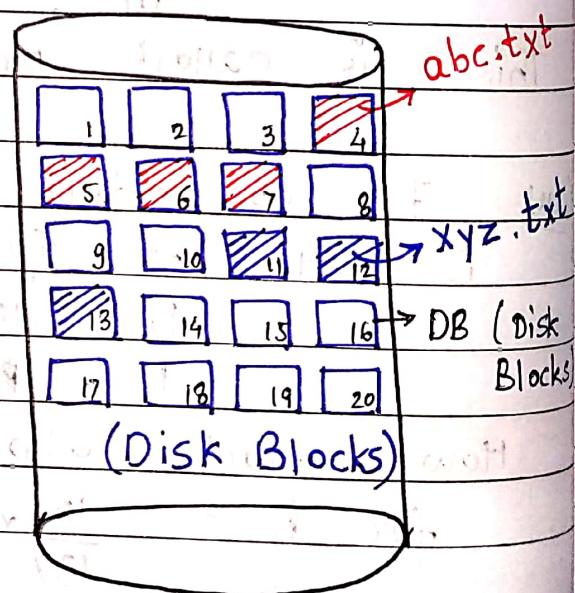
- File is a collection of logically related entities (records).
- Attributes : Name, size, type, location, creation date, modification date, owner, password, permission and so on. (File Context).
- All the attributes of file is called as file context. And the file context will be stored in file context block. (FCB)
- Types of Files : .doc, .txt, .obj, .exe, .class, .c, .java, .js etc.
- Various operations performed on file.
 - Create, append, close, read, write, save, copy, paste
 - delete, rename, save as different file.

Disk Space Allocation Methods :

(i) Contiguous allocation:

File Name	Start Address	length
abc.txt	4	4
xyz.doc	11	3

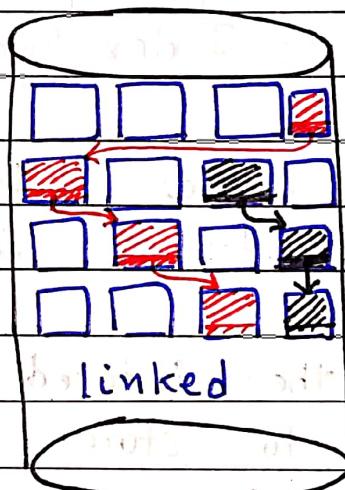
Disk Block Address (DBA)



- In the contiguous allocation, disk blocks are allocated to the file in a continuous manner.
- Increasing the file size is not always possible, because next block must be available.
- It suffers from external fragmentation.
- Internal fragmentation exists in the last disk block of the frame. It supports sequential and random access of the file.

(ii) Non-contiguous allocation

File Name	Disk	Ending
abc.txt	4	15
xyz.doc	11	20

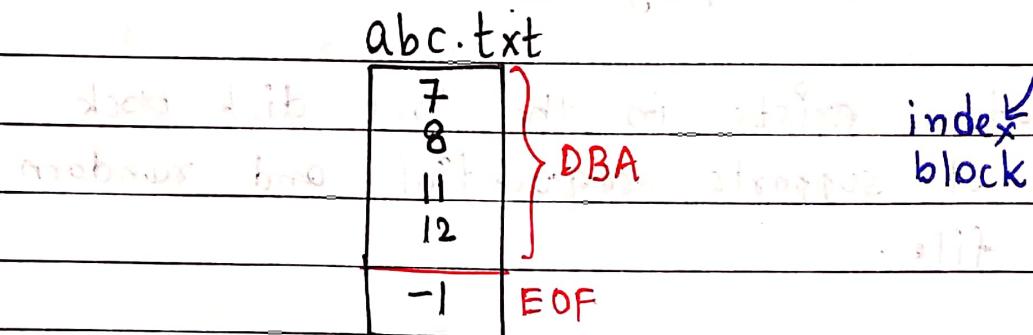


- Increasing the file size is always possible, if the free disk block is available.
- There is no external fragmentation.
- The internal fragmentation may exist in the last disk block of the file.
- It supports only the sequential access of the file.
- There is an overhead of maintaining a pointer in every disk block.

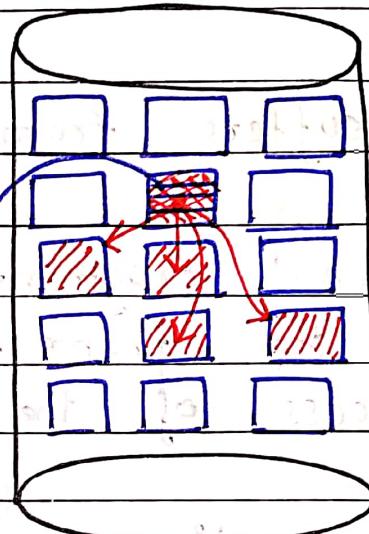
If pointer of any disk block is lost, then the file will be terminated. The ending of DBA is block address, confirm that the total file is accessed.

(iii) Indexed Allocation Method:

Allocation Table



Index Information



File name DBA (Index)

abc.txt 4

at least

- In the indexed allocation, one disk block is used just to store the DBA of the file.
- Every file is associated with its own index node.
- If the file is very large, then one disk block may not be sufficient to store the disk block of the file.
- If the file is very small, then it's wasted disk block, just to store DBA.
- ~~exix~~

UNIX INODE IMPLEMENTATION

Structure of i-Nodes:

Size of Disk Block

location

Owner

Reference Count

Date and Time

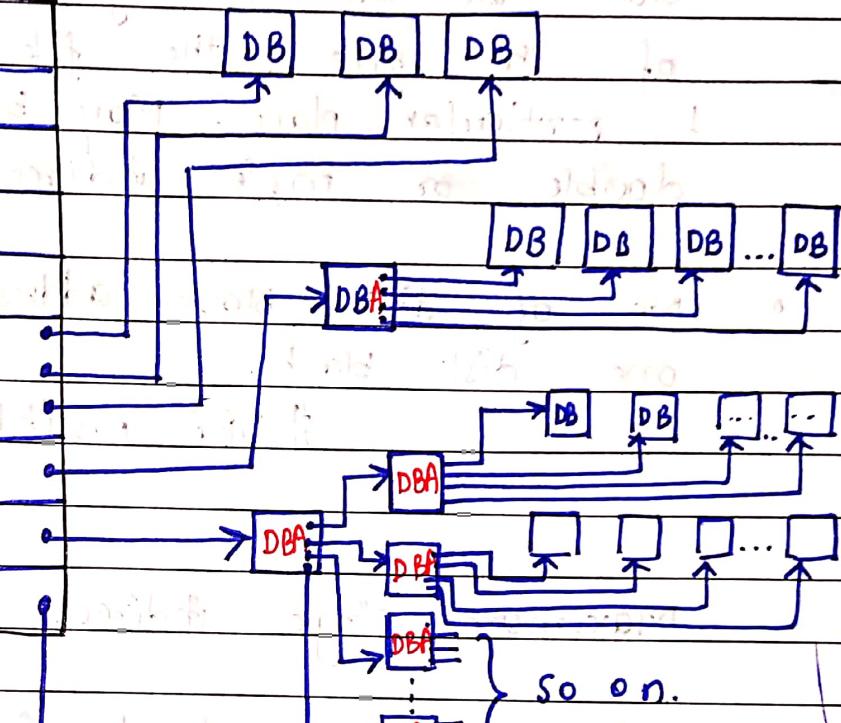
Direct

Disk BA

Single Indirect

Double Indirect

Triple Indirect



level 1 -

DBA

level 2 -

DBA

BBA

DBA

} Disk Block Addresses.

level 3 -

DBA

Actual
Data
Blocks

so on.

All the disk blocks are used for data storage and some for address storage.

inode is with every file and for every file we have its own inode.

- i-node is associated with various disk blocks. In some disk blocks we stored the data and in some block we are storing the address depending on size of the file, the file is stored only in 1 particular place. May be in direct, or in single double or triple indirect and so on.

- No of disk block address possible to store in one disk block.

$$\# \text{ DBA possible} = \frac{\text{DB size}}{\text{DBA size}} = \left(\frac{\text{BS}}{\text{ES}}\right)$$

Maximum single indirect size = $\frac{\text{BS}}{\text{ES}} \times \text{BS}$

Maximum Double indirect size = $\left(\frac{\text{BS}}{\text{ES}}\right)^2 \times \text{BS}$.

Maximum Triple indirect size = $\left(\frac{\text{BS}}{\text{ES}}\right)^3 \times \text{BS}$.

Total maximum possible size of file system

$$= \left[\# \text{ Direct} + \left(\frac{\text{BS}}{\text{ES}} \right) + \left(\frac{\text{BS}}{\text{ES}} \right)^2 + \left(\frac{\text{BS}}{\text{ES}} \right)^3 \right] \times \text{DB size}$$

(Ques) Consider the unix i-node 12 direct DBA, one single indirect, one double indirect, one triple indirect. DBA size is 32 bits and block size is 1 LKB.

$$\frac{(BS)}{ES} = \text{block size } 1KB = (256)^3$$

$$\text{possible file size} = (16777216) \times 1KB = 16GB$$

Ques: A ~~size~~ file system with 300 ~~MB~~ GB uses a file descriptor with 8 direct block address, 1 indirect block address & double indirect. Size of each block is 128 B and DBA size is 8B. Max possible file size in this system is.

$$\frac{BS}{ES} = \frac{128}{8} = 16$$

$$\therefore (8 + 16 + 256) \times 128B = 35840 \text{ bytes} \approx 35 KB.$$

Ques: A unix inode has 10 direct, 1 single indirect, 1 double, 1 triple ~~BS = 1KB ES = 4B~~.

$$\frac{(BS)}{ES} = (256)$$

Max possible file size is 2^{34} bytes or (16 GB).

10 direct

Ques: In a particular unix OS, each block size is 1024 byte. Each node has one single, one double, one triple indirect. Also each block can contain address of 128 blocks. Which of the following is approx maximum size of a file in the system?

$$\begin{aligned}
 & (128)^3 \times 2^{10} \\
 & 2^3 \times 2^{10} \\
 & = 2^{31} \\
 & = 2 \text{ GB}.
 \end{aligned}$$

SYSTEMS

Disk Free Space Management

- Consider disk of size = 20MB

Disk Block Size = 1 KB

DBA Size = 16 bits

Blocks = 20 K Blocks.

20 K Blocks = 20480 Blocks.

some used for DBA
some used for data

- There are two basic approaches for disk free space management.
- Free list approach.
- Bit map approach.

Free List approach: Some disk blocks are used to store the free disk block addresses.

DBA possible in 1 block = $\frac{DB}{DBA}$ = $\frac{1024B}{4B}$ = 512 Addresses.

for 20480 entries,
we require $\frac{20480}{512} = 40$ Blocks required.

Bitmap Approach: only 1 binary bit is used to represent each block.

Binary Bit.

0 1 0 1 * A (DB is free)

(DB is busy)

1	0	0	1	0
0	0	1	0	0
1	1	1	0	0

2560 Bytes

~~Ques.~~ Consider disk size = 128 MB, DB size = 2 KB, DBA size = 2 Bytes.

Disk blocks that will be consumed for free space management using free list approach is ?

- (A) 64
- (B) 128
- (C) 32
- (D) None

$$\begin{aligned}
 \text{Disk consumed to implement free list approach} \\
 \text{is} &= 64 \times 2 \text{ KB} \\
 &= 128 \text{ KB} \\
 &= 128 \text{ MB} \\
 &= 0.1\%
 \end{aligned}$$

Disk blocks for bitmap;

$$2^{16} \text{ bits} = 2^{13} \text{ Bytes}$$

8 KB.

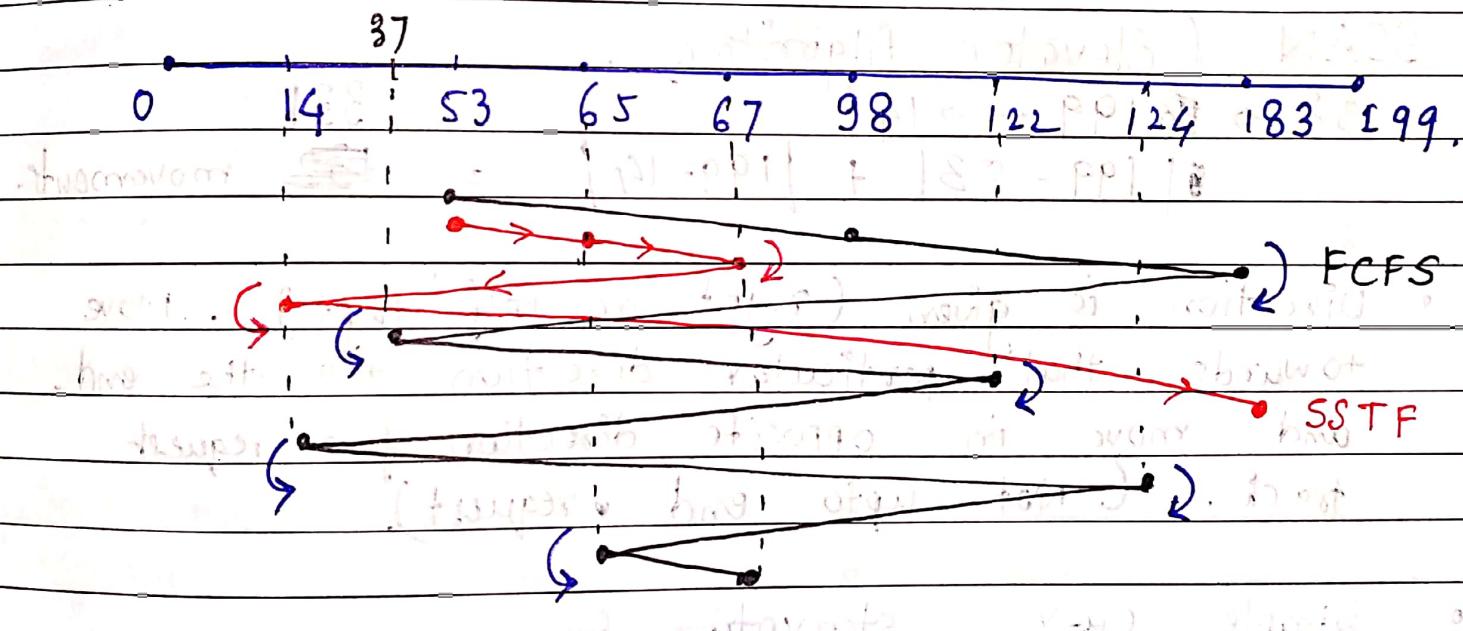
\therefore 4 Blocks required.

DISK SCHEDULING

Ex. Track Request : 98, 183, 37, 122, 14, 124, 65, 67
 Initial head at : 53.

- The main goal of disk scheduling is to minimize the average seek time of the disk. Consider cylinders are numbered from 0 to 199.

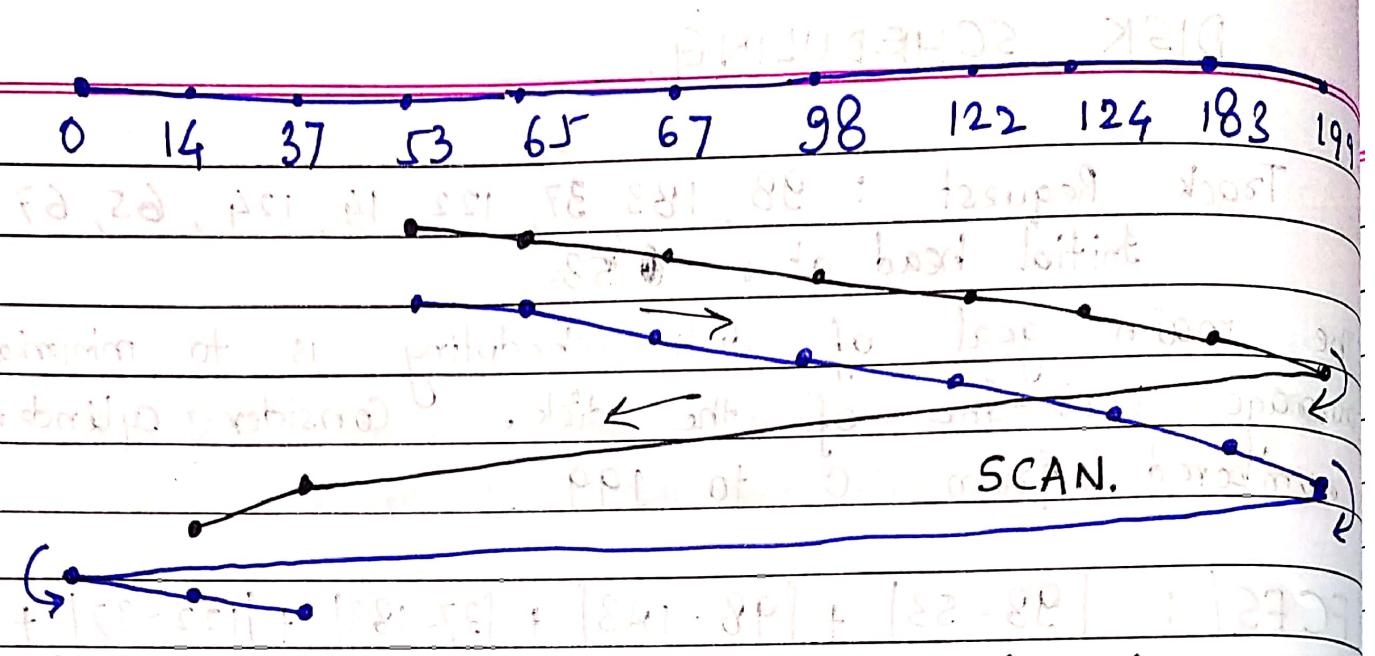
$$\begin{aligned}
 \text{FCFS} : & |98-53| + |98-183| + |37-183| + |122-37| + \\
 & |122-14| + |124-14| + |65-124| + |67-65| = 640 \\
 & = \boxed{640} \text{ movements.}
 \end{aligned}$$



- easy, starvation free.
- Increased total seek time, inefficient

$$\begin{aligned}
 \text{SSTF} : & |53-67| + |67-14| + |122-14| + |183-14| \\
 & = 236 \text{ movements.}
 \end{aligned}$$

- Reduced seek time, increased throughput.
- Extra overhead to calculate closest req.
- STARVATION



- In SSTF, the requests which are far from the head leads to starvation.

SCAN (Elevator Algorithm)

$53 \rightarrow 199 \rightarrow 14$

$$|199 - 53| + |199 - 14| = \text{movements}$$

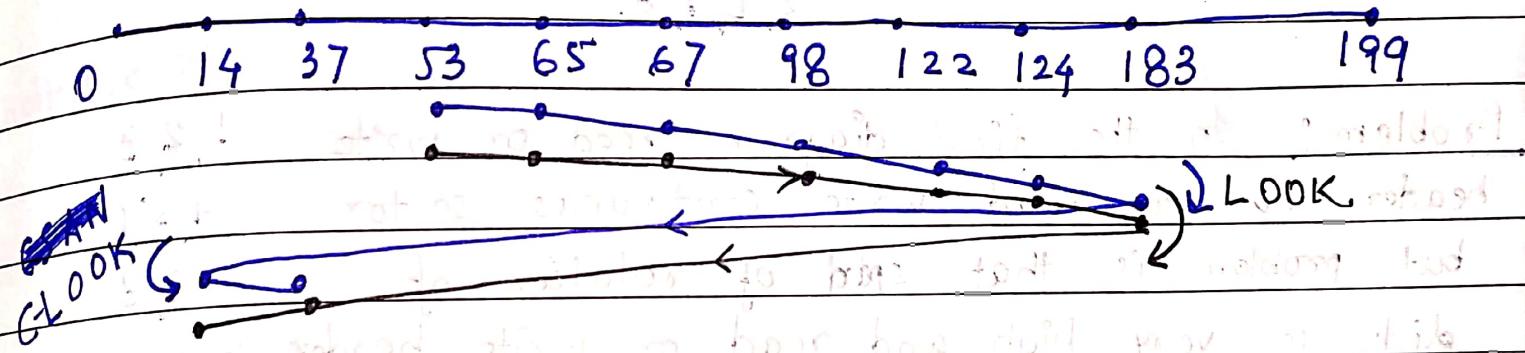
- Direction is given (right or ~~left~~ left). Move towards that particular direction till the end, and move in opposite direction for request track. (Not upto end of request).
- Simple, easy, starvation free.
- long waiting time for cylinder just visited by the head.
- Causes head to move till the end unnecessarily.

C-SCAN (Circular Scan)

$$(199 - 53) + 200 + 37 = 382 \text{ movements}$$

- It provides uniform waiting time.
- Provides better response time.
- It causes more seek movement as compared to scan algorithm.
- cause the head to move till the end of disk even if there is no request.

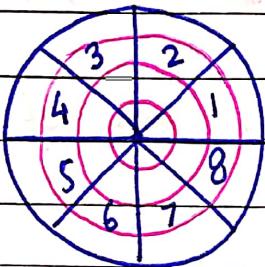
LOOK & C-LOOK (Improved SCAN & C-SCAN)



- $(183-53) + (183-14) = 299$ movement for LOOK.
- $(183-53) + (183-14) + (37-14) = 322$ for C-LOOK.
- Does not lead to starvation.
- Overhead of finding the end request.

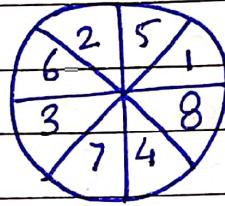
Disk Interleaving

No interleaving



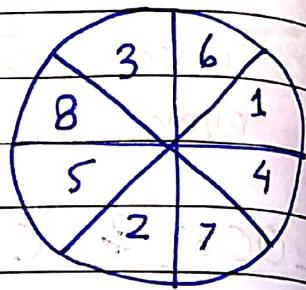
1 rotation

Single interleaving



2 rotations

Double interleaving



2.75 rotation

Problem: In the first diagram, read or write header has to read / write continuous sector but problem is that speed of rotation of disk is very high and read or write header is not able to catch next sector. ∴ It has to wait for completion of each rotation.

- Read or write header is not able to catch next sector because header is busy in processing and calculating CRC and transferring data from previous read sector.

- Solution: The above problem is solved by disk interleaving. It makes header to comfortably CRC, transfer data and being able to catch the sector.

- In no interleaving disk, one rotation time is needed to read all its sectors of the track.

- In single interleaving disk, 2 rotation time is required to read all its sectors of the track.
- In double interleaving disk, 2.75 rotation time is required to read all its sectors of the track.

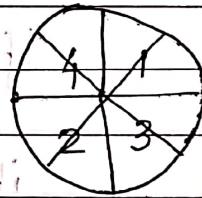
Ques.) Consider the double interleaved disk whose track is divided into 2 KB sectors. The average seek time of the disk is 30 ms, and the rotation rate of the disk is 3600 rpm. The rotational latency is still considered as half rotation time.

(i) How much time is required to read all its sectors of the track is using double interleaving disk.

$$30 \text{ ms} + \frac{1}{2} \times \frac{60}{3600} + 2 \times \frac{1}{60} \text{ sec.}$$

3600 rotation \Rightarrow 60 sec.

$$\frac{1}{2} \text{ rotation} = \frac{1}{2} \times \frac{60}{3600} = \frac{1}{120} \text{ sec. or } 8.33 \text{ ms}$$



$$= 30 \text{ ms} + 8.33 + 2.75 \times 8.33 \text{ ms.}$$

$$= 84 \text{ ms}$$

Ques.) ii) What is the time difference to read all 8 sectors of the track if it is a non interleaving disk?

$$30 + 8.33 + 16.66 \text{ ms.}$$

$$= 55 \text{ ms}$$

$$\therefore \text{Difference} = 84 - 55 = 29 \text{ ms}$$

what is DTR using double interleaving disk. special
 (45.84) ms to read 8 sectors.
 $45.84 \text{ ms} = 16 \text{ KB}$.

$$10^5 \text{ ms } \cancel{\text{ms}} - 16 \times 10^3 \text{ KB}$$

short sector disk having 45.84 ms to stabilize
 $\text{unit disk response time} = 349 \text{ KB} + 512 \text{ KB}$
 $= 349 \text{ KB}$

Fork System call

The fork is a system call which is used to create the child process from the parent process.

```
main () { int pid; code }
```

```
pid = fork();
```

```
if (pid < 0) { printf ("fork fail"); }
```

```
if (pid == 0)
```

```
{ print ("child process"); }
```

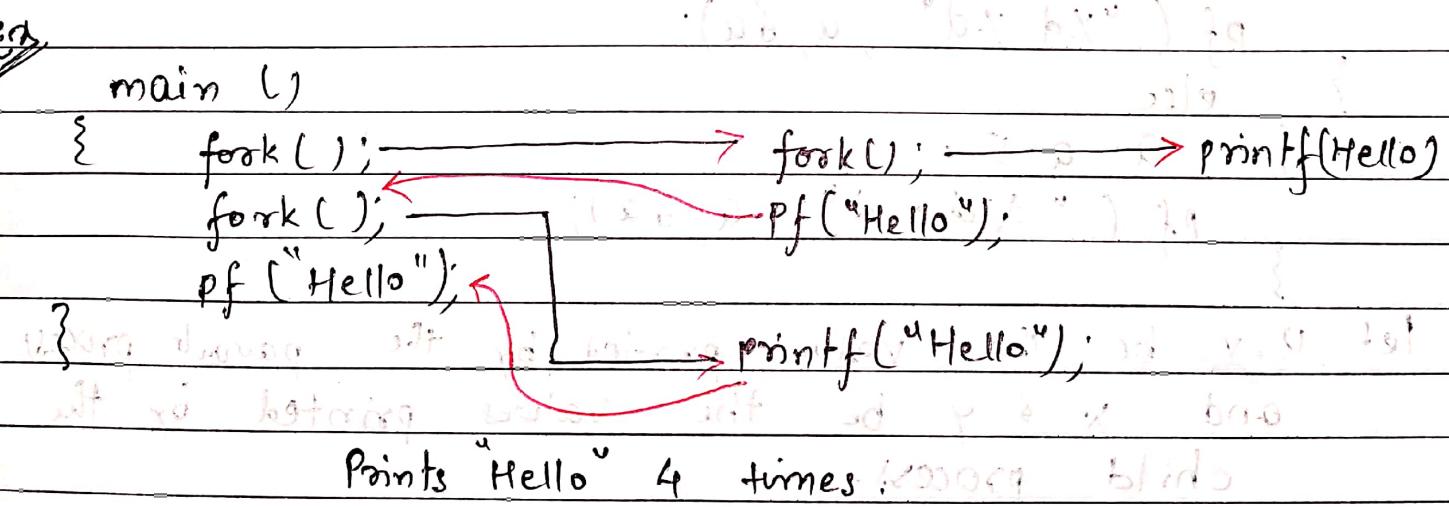
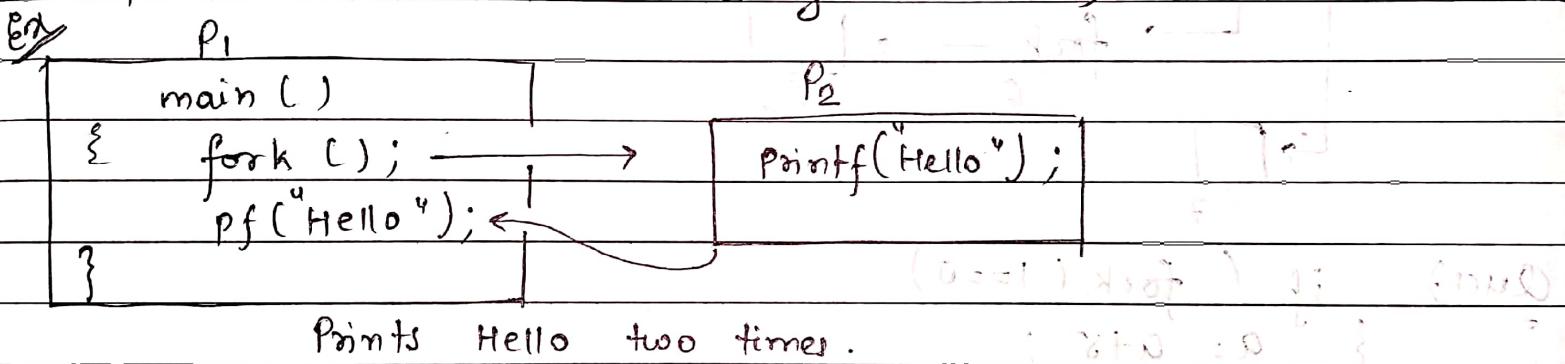
```
else { print ("parent process"); }
```

```
}
```

- The fork function return a negative value if the child process creation is unsuccessful.
- The fork return a value > 0 to the newly created child process.

2000 33.98 = 0.00

- The fork returns the pid (positive value > 0) of child process to the parent process.
- When child process is created by using the fork system call, the parent and child process will have the below address space.
- i) Relative address: It will be same for both parent and child.
- ii) Absolute address: It will be different for both.
- If we try to print the address using & then it will point relative address (Logical address).



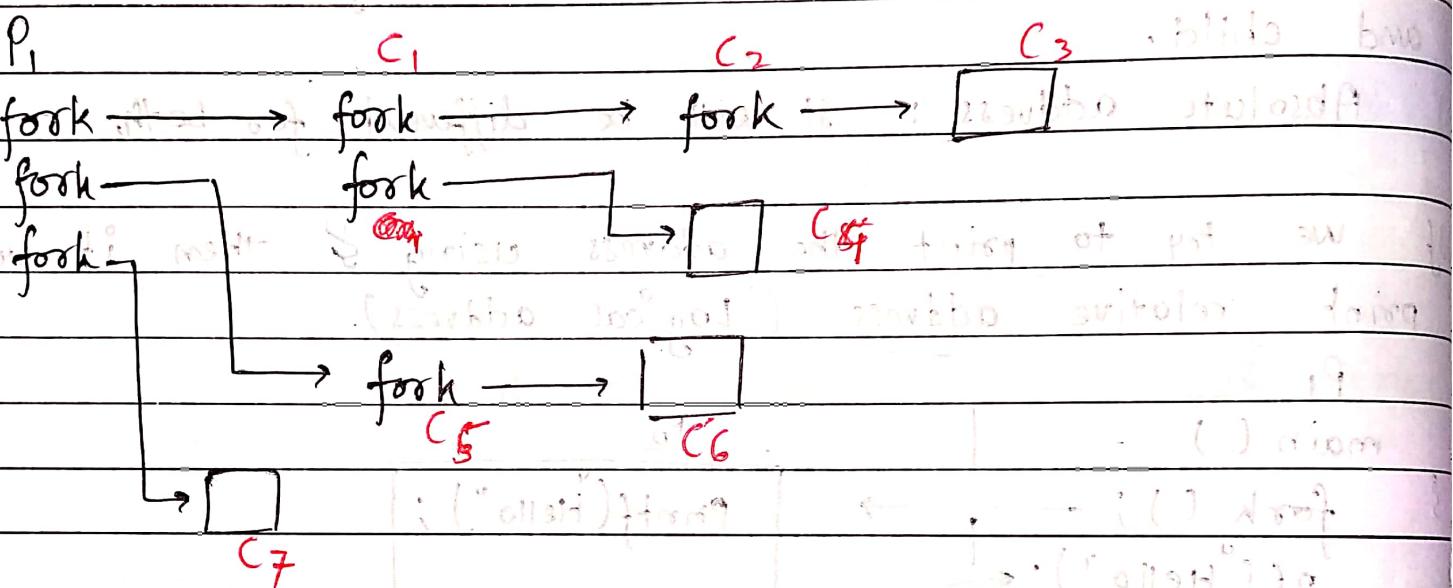
child processes = 2^n where n = No of fork calls.

Ques.) A process executes the code:

```

fork();
fork();
fork();
fork();
    
```

The total no of child process are $2^3 + 1 = 7$



Ques) if ($\text{fork}() == 0$)

$$\{ \quad a = a + 5;$$

$\text{pf}("y,d", a, &a);$

$\}$ else

$\{\quad a = a - 5; \quad \}$

$\text{pf}("x,d", a, &a); \quad \}$

Let v, v be the values printed by the parent process and x, y be the values printed by the child process.

~~$x = u + 10$~~ . $v = y$

$$x = u + 10$$

Note: The physical address of parent and child must be different but our program access virtual address (assuming we are running on OS that uses virtual memory.) The child process gets an exact copy of parent process and virtual address of a does not change in child process. Therefore we get same address in both parent and child.

Ques,) Consider following code:

O/P: 1111

```
int main ()
```

```
{ if (fork () == 0) fork (); // child
    exit (0); // parent
    int i = 1;
    printf ("%d", i); // child prints 1
}
return 0; // parent prints 1
```

Ques,) If in main () do I need to do

should { if (fork () < 0) fork (); } if

fork () < 0 { if (fork () < 0) fork (); }

if a child has no parent it will print

else if parent exits it will print

else if parent exists it will print

```
balance . do { printf ("1"); } while (point
```

note and } do { printf ("2"); } while (parent

if } else if parent exists { do { printf ("3"); } while (parent

if } else if parent exists { do { printf ("4"); } while (parent

}

open file with parent

O/P : 2 4 1 4 1 4 3 4.

Ques.) `int main() {` writing in pseudo code `int i; int k = 0;`
`for (i = 0; i < 10; i++) {`
 `if (fork() == 0) {` // child
 `if (fork() == 0) {` // grandchild
 `if (fork() == 0) {` // great grandchild
 `cout << "child " << k++ << endl;`
 `} else {`
 `cout << "parent " << k++ << endl;`
 `}`
 `} else {`
 `cout << "parent " << k++ << endl;`
 `}`
 `} else {`
 `cout << "parent " << k++ << endl;`
 `}`
`}`

O/P : 222 2222 222222 (loop)

Ques.) 4 files of size $= 11050$ Bytes

Need to be stored: (4×11050) Bytes

for storing these: $(4 \times 11050) + 4$ Bytes

many files on disk, 12640 Bytes.

We can use either

100 disk blocks or 200 Bytes disk blocks.

But cannot mix blocksize. ~~Each~~ Each block requires ~~4~~ 4 Bytes of Bookkeeping information and that also needs to be stored on the disk.

Thus the total space used, to store a file is the sum of the space taken to store the file and the space taken to store Bookkeeping information, for the block, allocated for storing the file. The Disk block can store

~~either~~ either book keeping information of a file or data ~~or~~ from a file but not both.

What is the total space required for storing the files using

Sol.) 100 KB Disk Blocks

Date _____
Page _____

200 KB Disk blocks.

$$111 \times 4 = 444 \text{ Bytes}$$

56 Blocks \Rightarrow 224

5 Blocks.

2 Blocks

~~116~~ Blocks

~~58~~ Blocks

~~50 Blocks = 200 Bytes~~

2 Blocks

28 Blocks \Rightarrow 100 Bytes

~~52~~ Blocks.

1 Block

~~52~~ Blocks = 208 Bytes

3 Blocks

~~26~~ Blocks

~~55~~ Blocks.

~~26~~ Blocks = 104 Bytes

1 Block

~~127~~ Blocks = 508 Bytes

~~27~~ Blocks.

~~6~~ Blocks

~~133~~ Blocks

64 Blocks = 256 Bytes

~~356 X 100~~

2 Blocks

~~35600 Bytes~~

~~66~~ Blocks

~~addition of 66 blocks = 177 X 200~~

~~35400 Bytes~~

Ques) The address sequence generated by tracing a particular program executing in a pure demand paging system, with 100 records per page, with 1 frame, is recorded as follows. What is number of page faults.

0100* 0200* 0499* 0499 0510* 0530

0560 0120* 0220* 0240* 0260 0320*

0370

31-58 : 16

Ques) A CPU generates 32 bits virtual address. The page size is 4 KB. The processor has a TLB which can hold a total of 128 page table entry.

and is 4 way set associative mapping. The minimum size of the TLB tag is $\lceil \log_2 128 \rceil = 7$

$$\# \text{sets.} = 128 = \frac{32 \times \text{sets of 4}}{4} = 2^5$$

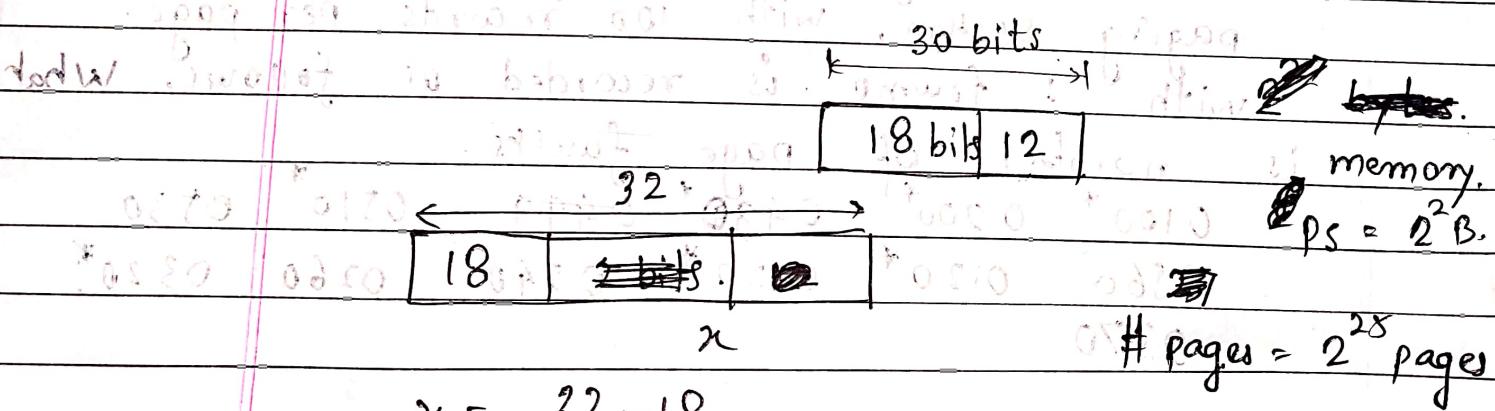
$$\text{TLB tag} = 20 - 5 = 15 \text{ tag.}$$



2 pages.

(Ques.) In a virtual memory system, size of virtual address is 32 bits. Size of physical address is 30 bits. Page size is 4 KB. Size of each page table entry is 32 bits. The main memory is byte addressable.

Which one of the following is the max no of bits that can be used for storing protection and other information in each page table entry.



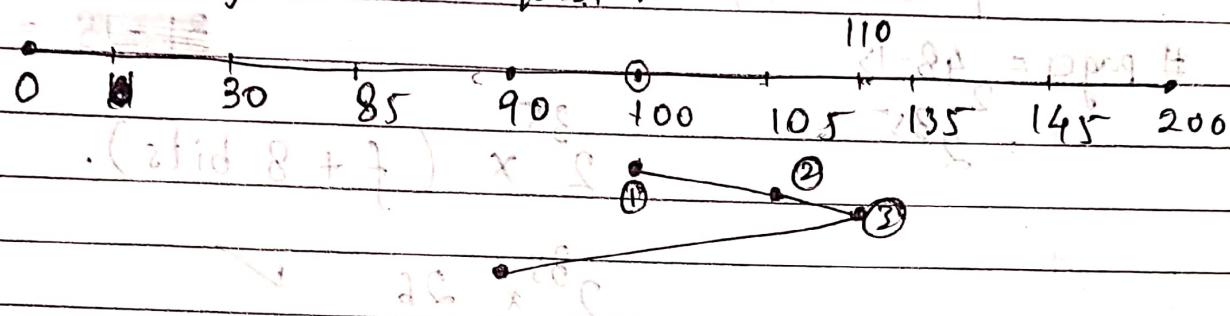
$$x = 32 - 18$$

addr. 22 bits = 14 bits

size of 14 bits = 16 bits
size of 14 bits = 8 bits to 14 bits = 8 bits
size of 14 bits = 8 bits to 14 bits = 8 bits



Ques Suppose a disk has 201 cylinders numbered from 0-200. At some time the disk arm is at cylinder 100, and the request for cylinder is 30, 85, 90, 100, 105, 110, 135, 145. If SSTF algorithm is being used for disk access then the req for cylinder 90 is serviced after servicing the request.



Ques Consider a virtual page system with page size as 2048 Bytes. Each virtual address (in the form A, B) where A = page number & B is page offset. Find the actual address of the virtual address (3, 512). Consider the following lookup table.

Virtual Page	Actual Page
0000 0000 0000 0000 0000 0000 0000 0000	0000 0000 0000 0000 0000 0000 0000 0000
0000 0000 0000 0000 0000 0000 0000 0001	0000 0000 0000 0000 0000 0000 0000 0001
0000 0000 0000 0000 0000 0000 0000 0010	0000 0000 0000 0000 0000 0000 0000 0010

Actual Page = 4 8192 2048 1023 512 256 64 16 4

2048 * 512 = 1048576

$$8192 + 512 \times 1 = 8256$$

$$= 3072 + 512 = 358704$$

✓

Ques.: Consider a logical address space of 2^{48} bytes and page size = 8 KB. = 2^{13} bytes. Physical memory = 2 GB. Each page table entry also indicates 8 bits off for own purpose. Then what is the size of page table?

$$35 \text{ bits.} \quad 13 \text{ bits.} \quad 2^{35-13} = 18 \text{ bits}$$

$$\# \text{ pages} = 48 - 13$$

$$= 2^{35-13} = 2^{22} = 2 \times (f + 8 \text{ bits}).$$

16

$$2^{35} \times 2^6$$

Ques.: A processor uses two level page table.

both are stored in main memory.

$$\text{VA} = \text{PA} = 32 \text{ bits.}$$

Memory is byte addressable. For virtual to physical translation, first 10 bits used for page table, next 10 bit used for level 2 page table. Remaining used for page offset. Page table entry size is 4B each.

LAS	10	10	12
-----	----	----	----

Processor uses TLB with hit ratio 96%.

Cache memory is used with hit ratio 90%.

$$T_m = 10 \text{ ns.}$$

$$T_c = 1 \text{ ns.}$$

$$T_t = 1 \text{ ns}$$

i) find effective memory access time.

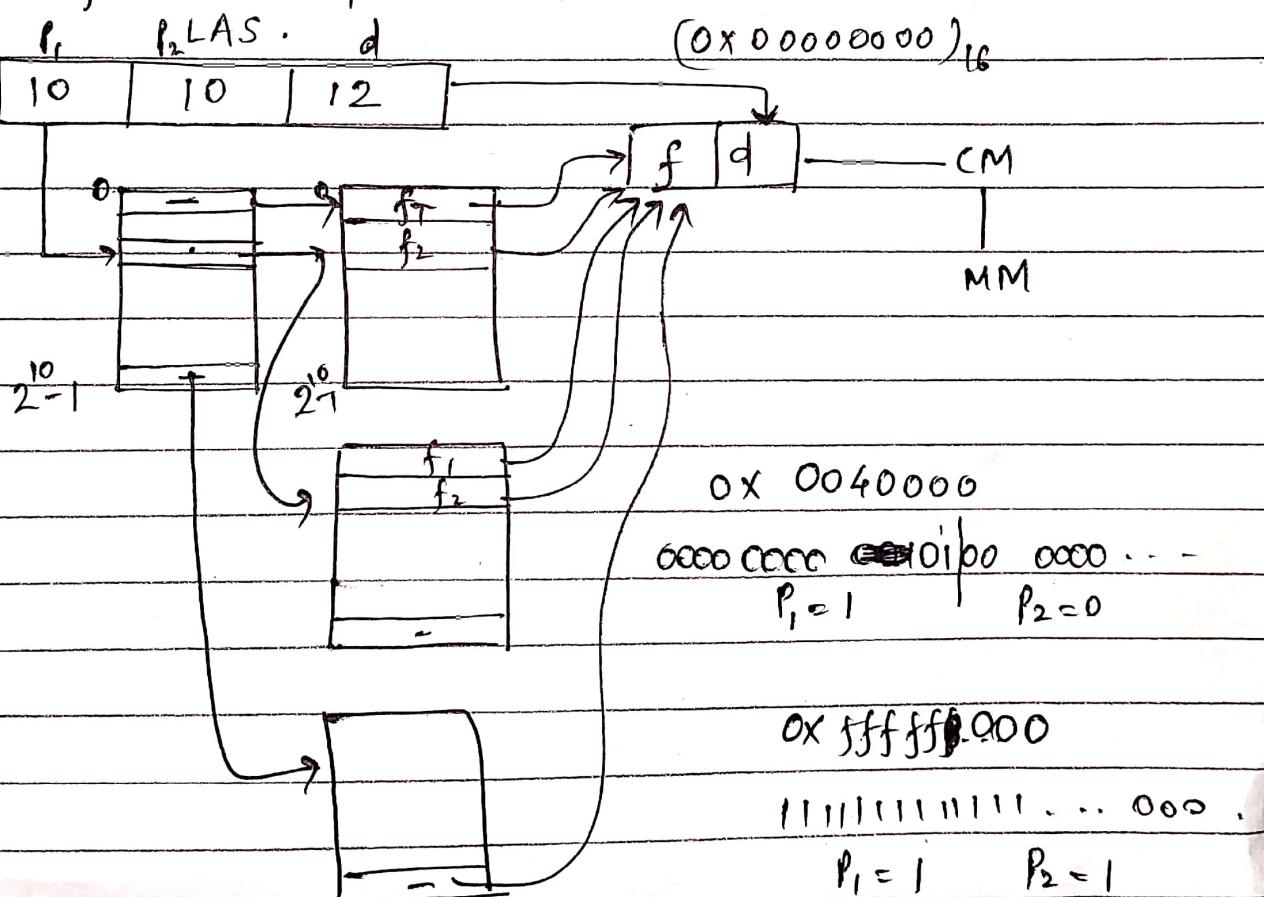
$$\begin{aligned}
 EMAT &= 0.96 \times (0.9 \times 1 + 0.1 \times 11) \\
 &\quad + 0.04 \times (1. + 10 + 10 + 0.9 \times 1 + 0.1 \times 11) \\
 &= 1.92 + 0.92 = 2.84 \text{ ns.}
 \end{aligned}$$

(ii) Suppose a process access 2 continuous code pages at virtual address 0x00000000

and 2 contiguous Data page at virtual address 0x00400000

and a stack page starting at virtual address 0x ffffff000

The amount of memory required for storing the PT of this process is?



page tables = 4

entry size = ~~is~~ 4 B each.

∴ Total memory required = $4 \times 1024 \times 4 \text{ B}$
 $= 16 \text{ KB} \checkmark$