An 8-Channel General-Purpose Analog Front-End for Biopotential Signal Measurement

Jinming Hu, Xue Yang, Zengweijie Chen, Hang Yang

***Abstract*— This paper presents system level specifications of an 8–channel CMOS analog front-end (AFE) with an 8-bit analog to digital converter, which is used for acquiring certain biopotential signals such as EEG, ECoG, ECG, and EMG, i.e. signals for brain activities, heart activities, and muscle activities. The design that being discussed in this paper must work with a microcontroller, which it may or may not acquire the clock signal from. It is also possible to use a programmed oscillator for the desired clock signal, which is 500kHz. The chip requires 3.3Vdc supply and is recommended to be achieved by using 2 x 16340 Li-ion batteries in parallel connection. The power consumption is approximately 890µW during normal operation.**

I. Introduction

Biopotentials are electrical signals; they are generated due to action potentials produced from certain types of cells which are composed of nerve, muscle, or heart tissues. Among all kinds of biopotentials, the most common ones are EEG, ECoG, ECG, and EMG. EEG and ECoG are introduced by brain cells, ECG is generated by the heart, and EMG is from muscle activity [1]. Thus, the signals are of great value in obtaining information about structure and function of tissues from which they are generated from. However, these medical benefits largely depend on the accurate acquisition of the electrical signals. In addition, with the growing number of the global aging population, demand for health monitoring devices has never been higher. Hospitals have invested substantial resources and capital to track various kinds of biopotential signals for everyone, because each type of electrical signals requires different kinds of medical equipment. Thus, it is a logical choice to build a general-purpose and accurate analog front-end for a biopotential signal recording system.

The AFE presented in this paper will be used to record EEG, ECoG, ECG and EMG signals whose amplitudes range from 5µV to 5mV and bandwidths range from dc to 2 kHz as shown in Table 1 [1]. Thus, the system must introduce very little noise, have a high common-mode rejection ratio (CMRR), and have a high-power supply rejection ratio (PSRR). Regarding the extremely low range of target signals, a low-pass filter with 2 kHz will be developed. As biopotential signals are collected through physical electrodes, the input of the system must have huge input resistance to minimize loading effect. Moreover, the differential DC offset created by tissue-electrode interface should also be eliminated to avoid output saturation. It is done by a chopper low noise amplifier (LNA).

Per Table 1, the smallest amplitude of the four signals is 5µV and the common bandwidth is around from 0.01 Hz to 2 kHz. Consequently, the bandwidth of the whole system is from 0.01Hz to 2 kHz. An analog to digital converter (ADC) has a step size granularity of 12.89µV (before amplification) is chosen to be 8 bits (256 steps).

The block diagram of the proposed system is given in Fig. 1 and the system level specifications are summarized in Table 2. This section will address each of the blocks individually.

The probes will sample the biopotential signal. Recall that the amplitudes of the sampled signals are between 5µV and 5mV, a high-gain amplification stage is needed immediately after the probes. In our system, a chopper low-noise amplifier (LNA) is applied to fulfill such duty, and to eliminate noises. The closed-loop gain is designed to be 40dB.

TABLE I
AMPLITUDES AND BANDWIDTHS OF FOUR BIOPOTENTIAL SIGNALS

Biopotential Signal	Amplitude (mV)	Bandwidth(Hz)
EEG	0.005 -0.3	0.5 – 150
ECoG	0.01-3	0.5 – 500
ECG	0.5 – 4	0.01 - 250
EMG	0.1 - 5	dc – 2k

Upon amplifying and filtering, the channels of signals will be chosen to get finely processed. A 16-2 channel selector and a buffer is used to select the channels (2 channels are chosen thanks to the differential nature of channels). A minor future update is planned to add direct control routing and enabling direct command control from the microcontroller. Therefore, the user can manually select the channel pair for data recording. Thereafter, then signals will pass a programmable gain amplifier (PGA) before finally reach the ADC. As of now, the channel selector gets control signals directly from the clock divider that divides the 500kHz clock signal to 125kHz and 250kHz. The PGA needs to provide further gain as needed due to the variance of amplitude for different biopotentials.

TABLE II
SYSTEM LEVEL SPECIFICATION

Process	0.5 um CMOS
Supply Voltage	3.3V
Power Consumption	600uW
Consumption Area	4mm^2

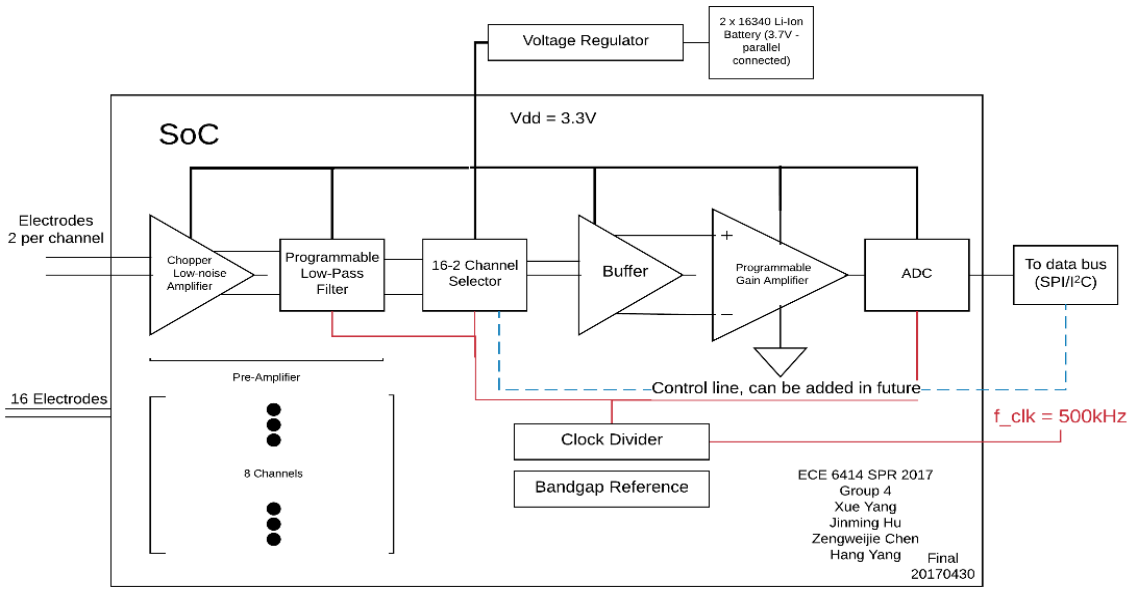

Fig. 1. System block diagram

A voltage range of 0 – 2.5 V is set for the input of the ADC which allows for some margin of error with the ADC, such as dynamic range, as well as the other stages while not needlessly expending power with a 3.3 V supply voltage.

There is great deal of selections of medical-grade electrodes available in the market. For best results of muscle-level biopotential sampling actions, it is recommended to use DEN-12SAF for EEG, DIN-75 for EMG, ECoG and ECG. All of which are sold by The Electrodes Store. [19][20]

A microcontroller is indispensable for the operation of the proposed chip, which will receive the processed biopotential signal. Also, the microcontroller may provide the system clock signal for our proposed chip, which is 500kHz. Considering of adding flexibility of applications, an external oscillator can also be used to provide the clock signal. The recommended oscillator is Silicon Labs 510CAA-AAAG [16] Programmable Oscillator, which can provide the clock signal between 100kHz and 124.999MHz with a 3.3V of power supply.

Ideally, our proposed chip and a microcontroller will be installed onto a portable device, i.e., without cumbersome cables dangling. Upon considering all available portable power solutions, we recommend to use 2 parallel-connected 16340 [17] series Li-ion batteries. There are few advantages to use proposed types of batteries: 1. Rechargeable; 2. High power density; 3. Small excessive voltage margin (3.7V rated output vs. 3.3V V_{dd}/V_{cc}); 4. Relatively low voltage drop as energy level drops. A step-down voltage regulator is needed to provide the 3.3V supply voltage. We recommend ON Semiconductor NCP114BSN330T1G [18] to handle such task, as its input voltage is between 1.7~5.5V but providing 3.3V output with the cost of US$0.08 per unit.

II. Pre-Amplifier

A. Design Considerations

The goal of the pre-amplification stage is to provide a constant gain of low amplitude signals for the programmable gain amplification stage while using a variety of methods to suppress noise, offset, and common mode signals to enhance the overall SNR of the entire system. A closed loop gain of 40 dB is selected to provide a maximum amplitude of 500 mV for a maximum input voltage of 5 mV for the different range of signals. The rest of the gain will be provided by the programmable gain amplifier stage to meet an output range of approximately 0 – 2.5 V for the ADC. The CMRR is important for the amplifier topology and is set at 80 dB or greater in comparison to other analog front end technologies [7]. Input referred noise is needs to be at minimum less than intracellular and electrode background noise, which is approximately 5-10 μV_{rms} [10]. Given the low frequency range of the signals, 1/f noise will be a major contributor to the overall input referred noise. To remedy this, a combination of chopper stabilization and a programmable high pass filter will be used in feedback with the low noise amplifier. Lastly, a high PSRR is also desired to eliminate possible deviations in our battery power supply. A 200µW power consumption is targeted for this stage to try to meet the overall 600µW power consumption for the entire system along with the other stages.

B. Amplifier Design

A fully differential folded cascode amplifier with cross coupled active loads is chosen as the topology of the amplifier, and can be referenced in Fig. 2 in the following page [9]. It is a two stage amplifier with PMOS input differential pair with a common source output stage, with M1 and M11 acting as the current source loads. Using a cascode structure is advantageous as the currents are partitioned for the maximization of the noise efficiency, which is ideal for this application [11].

M3, M4, M6, and M7 function as cross coupled active load of the first stage, and their function is to provide a low impedance for common mode signals while providing a high impedance for differential signals as the g_m of M3 and M7 are canceled by M4 and M6 [9]. The result is a very high CMRR. A full list of the transistor sizing can be seen in Table III in the following page.

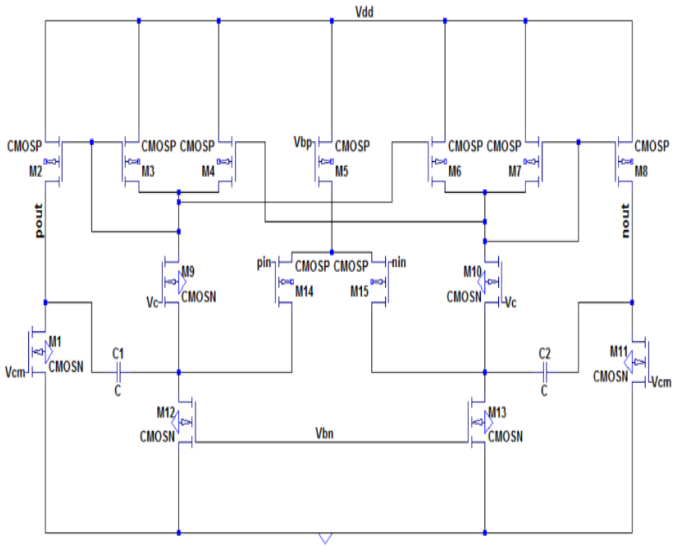

Fig. 2. Schematic of folded cascode amplifier [9].

Common mode feedback is used to stabilize the output around a DC voltage (in this case $V_{dd}/2$). The circuit schematic can be in Fig. 3 below. The PMOS differential pair compares the average of the positive and negative outputs with $V_{dd}/2$, which changes the biasing voltage for M1 and M11, moving the output up and down accordingly. The $V_{dd}/2$ input can be provided by averaging the biasing currents.

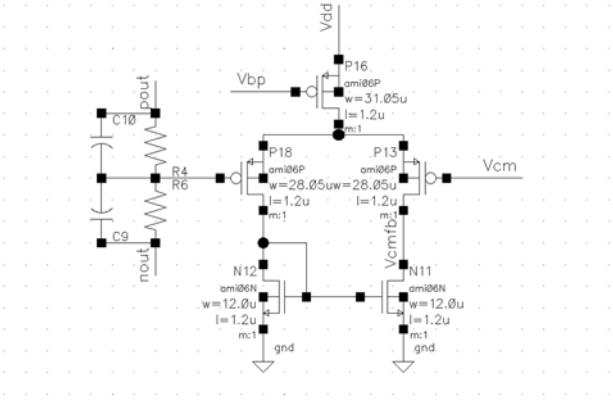

Fig. 3. Common mode feedback circuit.

C. Chopper Stabilization

Chopper stabilization is a very effective technique that shows good noise performance under low power, low frequency operations [8]. The chopper circuit operates by modulating the input frequency to a much higher frequency where flicker noise is negligible. The modulated signal is then amplified and demodulated back to the baseband, while the flicker noise remains at the specified chopper frequency [8]. A low pass filter would suffice to eliminate the up-converted flicker noise, as well as potential dc-offsets from input signals [7].

TABLE III
AMPLIFIER TRANSISTOR SIZING

Transistor	Sizing (W/L)
M1, M11	70/1.2
M2, M8	120/1.2
M3, M4,M6, M7	10/1.2
M5	40/1.2
M9, M10	24/1.2
M12, M13	24/1.2
M14, M15	30/1.2

A modulating frequency of 15 kHz is selected as it is within the closed loop gain bandwidth set at 40 dB, and is far enough from the highest possible baseband at 2 kHz such that a low pass filter will not attenuate the original signal. The topology of the chopper is seen in Fig. 4 below.

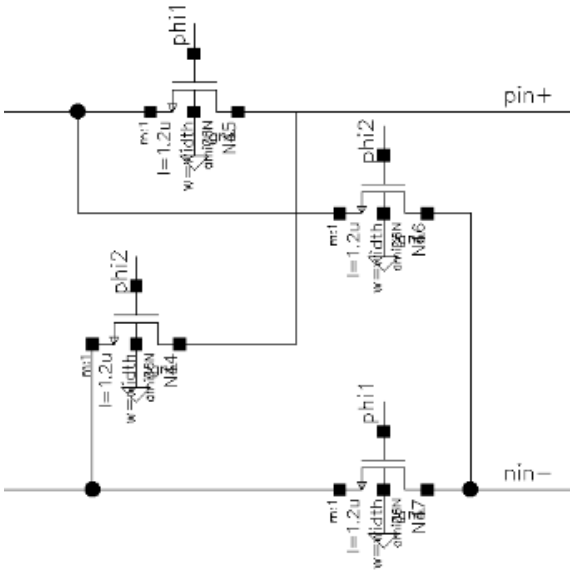

Fig. 4. Schematic of chopper modulator.

D. Programmable HPF with Tunable Pseudo-resistors

The principle of pseudo-resistor is as follows. The equation for transistor behavior in subthreshold is given by equations [21]:

$$I_D = I_{SPEC} exp\frac{V_G - V_{T0}}{nU_T}\left(exp\frac{-V_s}{U_T} - exp\frac{-V_D}{U_T}\right) \quad (1)$$

Where

$$I_{SPEC} \triangleq \mu U_T \frac{W}{L}(-Q_{SPEC}) = 2n\mu C_{ox}\frac{W}{L}U_T^2 = 2n\beta U_T^2 \quad (2)$$

V_G : *gate voltage*
V_{T0}: *threshold voltage of the transistor*
n: *linearized body effect factor* $1 < n < 2$
$U_T = \frac{kT}{q}$: *thermodynamic volltage*

If pseudo-resistance is represented by the following equation, based on (1):

$$G^* = \frac{1}{R^*} = \frac{I_{SPEC}}{V_0} exp \frac{V_G - V_{T0}}{nU_T} \quad (3)$$

then it can be seen that the gate voltage can control a pseudo-resistance through the transistors. A high, tunable resistance can be obtained which makes it possible to achieve a low cutoff frequency with a capacitance in the pF-level with feedback [21]. The feedback configuration is shown by Fig. 5.

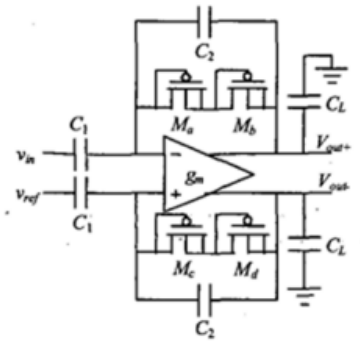

Fig. 5. Fully differential amplifier with high pass capacitive feedback [9].

The cutoff frequency for the high pass configuration is set by the following equation:

$$f_L = \frac{1}{2\pi R C_2} \quad (4)$$

Where R is the value of the pseudo-resistance. For our simulation, the pseudo-resistors are changed such that the gates are connected to an external tunable voltage, seen in figure 6. The voltages are swept from 1.5 to 2.0 V with a corresponding 2 pF resistor to achieve low pass voltages varying from near DC to 0.5 V, which is the necessary programmable range for the various biopotentials listed in Table I.

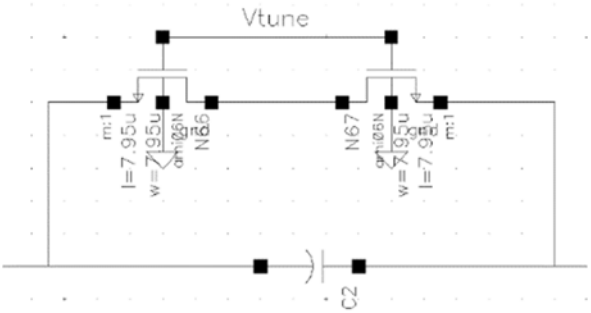

Fig. 6. Tunable pseudo-resistor implementation.

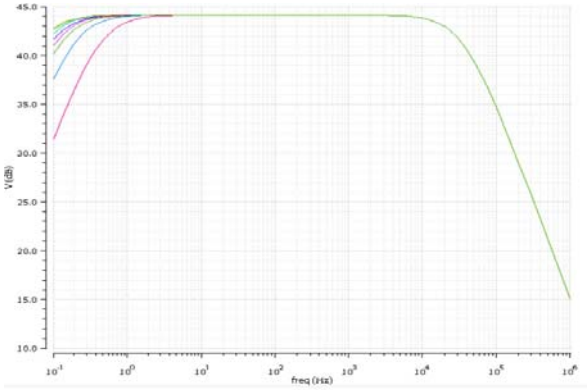

Fig. 7. Demonstrating adjustable cutoff frequency sweeping the tuning voltage of the pseudo-resistor.

D. Programmable 2nd Order Gm-C Filter

A low pass filter needs to be put at the end of the pre-amplifier stage to 1) eliminate noise transposed at chopper frequency, 2) anti-aliasing stage prior to ADC, and 3) to further improve the SNR of the system by eliminating signals beyond the bandwidth of the desired biopotential [22]. A gm-c filter is chosen for this application as the cutoff frequency, like the pseudo-resistor mentioned in the previous section can be tuned, this time through the biasing voltage of the DC biasing currents [22].

The OTA itself can be modeled as a resistor and used in conjunction with a capacitor to form a simple low pass filter. The second order gm-c filter implementation for this project can be seen in figure 9.

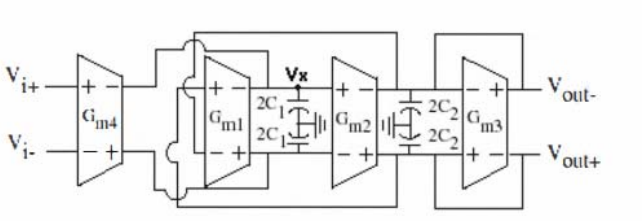

Fig. 8. 2nd order gm-c filter [22].

The transfer function for the filter as well as the cutoff frequency are given by [21]:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m2} \cdot g_{m4}}{c_1 c_2 S^2 + g_{m3} c_1 S + g_{m1} g_{m2}} \quad (5)$$

$$\omega_0 = \sqrt{\frac{g_{m1} \cdot g_{m2}}{c_1 . c_2}} \quad (6)$$

Given these equations, the manipulation of the cutoff frequencies can be done through g_{m2} and g_{m1}. Equation 6 shows that the DC gain is $(g_{m2}*g_{m4})/(g_{m2}*g_{m1})$.

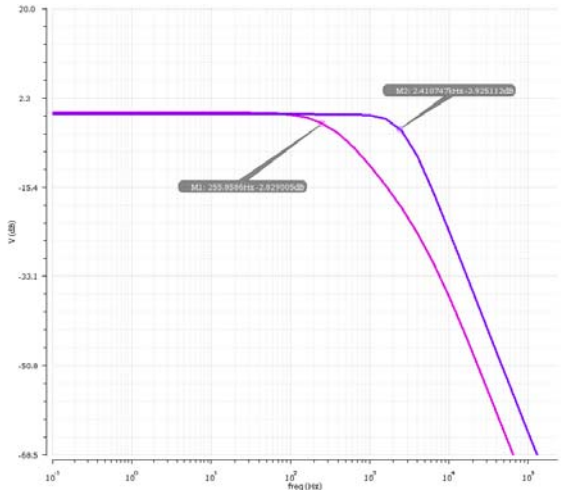

Fig. 9. 2nd order gm-c filter frequency response varying bias voltage for g_{m2}

Based on this, g_{m2} can be varied to change the frequency response without changing the gain. In addition g_{m4} and g_{m1} are set the same to achieve unity gain at DC.

The results of the gm-c filter can be seen in figure 9. The filter was able to achieve a cutoff frequency of 250 Hz and 2.5 kHz varying g_{m2}, with a DC gain of about 6 dB. However, the capacitors used are a high at 2n in order to achieve the necessary cutoff frequencies. The key in this case is to reduce g_m. A possible exploration for future work might be to build an OTA with current cancelation techniques, which can achieve g_m in the order of 10^{-9} [23].

E. Simulation results - Preamplifier

The simulation results for the overall preamplifier with feedback, chopper stabilization, and low pass filter can be seen in Table IV. The performance is compared with other papers

TABLE IV
PRE-AMPLIFIER PERFORMANCE BENCHMARKING

Spec	This Work	[24]	[25]
Tech.	AMI 0.6µm	1.5 µm CMOS	0.5 µm CMOS
Voltage	3.3 V	2.5 V	1.5 V
Gain	39 dB	39.5 dB	80 dB
Power	251 µW	80 µW	1.335 mW
CMRR	130 dB	>83 dB	117 dB
PSRR	90 dB	>85 dB	52 dB
Input-referred noise	2.2μV_{rms} (0.5 – 2kHz)	2.2 μV_{rms} (0.5 – 50kHz)	0.86 μV_{rms} (0.3 – 150Hz)

and does favorably in terms of noise, CMRR, and PSRR, all of which meet the design considerations. Additionally, frequency response and noise simulation are shown in figures 10 and 11.

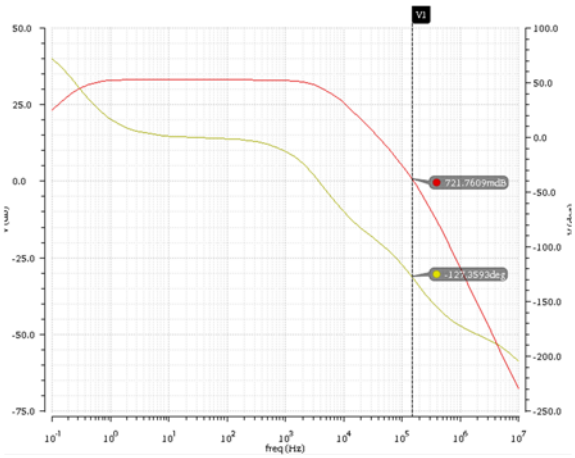

Fig. 10. Full preamplifier simulation (0.5 – 2kHz bandwidth).

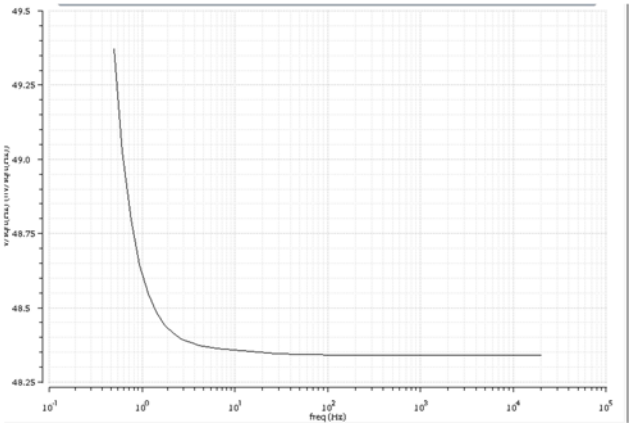

Fig. 11. Noise density (nV/ √Hz) vs Frequency (Hz).

III. 16-to-2 CHANNEL SELECTOR

As aforementioned, there will be 16 channels of electrode inputs. Particularly, 8 probes, with 2 channels of signal per probe. The channel selector should be able to provide output signals as input of CMOS switches, and therefore control the switches of each probe channel.

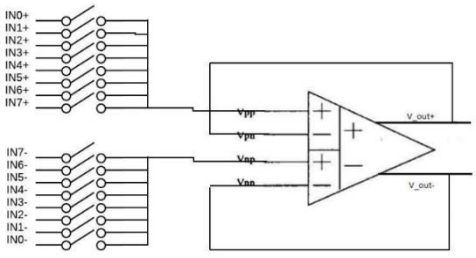

Fig. 12. Topology of 16-to-2 channel selector.

The channel selector module is comprised of a CMOS switching array, a switch control unit, and differential difference amplifier serves as a buffer (Fig. 16). The switching rate of the switches is set to 500k channels/s. Hence, a $f_{clk} = 500\ kHz$ is needed for such a module [1] [5]. In accordance to Table IV, there are 3 control signals that have different

frequencies. As shown in Fig. 9, D1 must be switching at 500 kHz, D1 is switching at 250 kHz, and D2 has the frequency of 125 kHz. In a realistic design, since there is only 1 clock frequency input, there will be a clock divider module that processes the 500kHz clock signal properly. Different clock signals were used in the simulation for sake of convenience.

During operation, the inputs will be switched to a channel's (+) and (-) nodes simultaneously. To avoid switching mistakes, i.e., signals from IN1+ and IN2- are fed into the buffer, a mechanism needs to be considered. In our design, we chose to hook every channel's (+) and (-) onto the same switch. Therefore, whenever a channel is chosen to provide output, the (+) and (-) signals will come from the same channel. The design and validation of this DDA will be done per referring [14].

TABLE V

DIGITAL CONTROL LOGIC

Data Select Signals			Output
D_2	D_1	D_0	Y
0	0	0	IN0+/-
0	0	1	IN1+/-
0	1	0	IN2+/-
0	1	1	IN3+/-
1	0	0	IN4+/-
1	0	1	IN5+/-
1	1	0	IN6+/-
1	1	1	IN7+/-

The DDA is comprised with 1 set of current mirror, 2 differential input pairs, and 2 cascode common-source amplification stages, in a fully symmetrical manner. The open-loop gain is roughly 70dB, and the close-loop gain is roughly

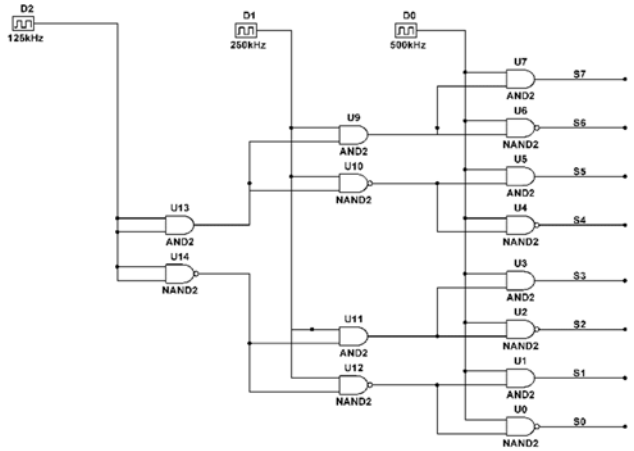

Fig. 13. Switching logic corresponds to clock signals.

0dB as it behaves as a buffer. Specifically, the actual AC gain is -0.6mdB, with the BW (-3dB) of 92.93kHz. The current consumption of this DDA during normal operation is 22.63μA. And hence, the power consumption during normal operation is $22.63\mu \times 3.3\text{V} = 74.679\mu\text{W}$.

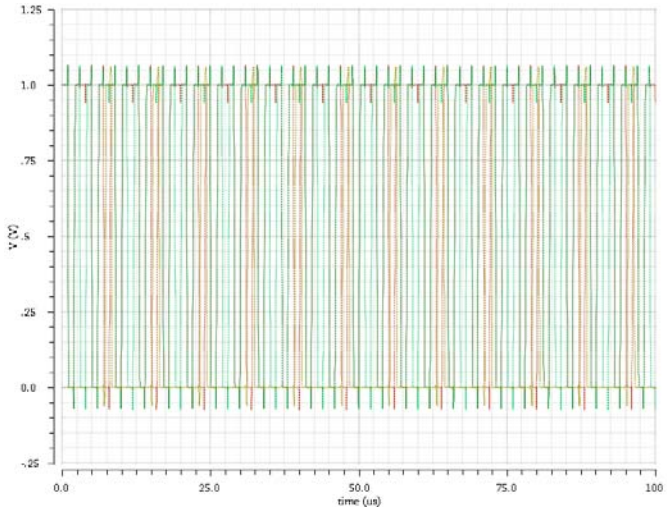

Fig. 14. Simulation result of bit 0, 4, and 7 (output S0, S4, S7).

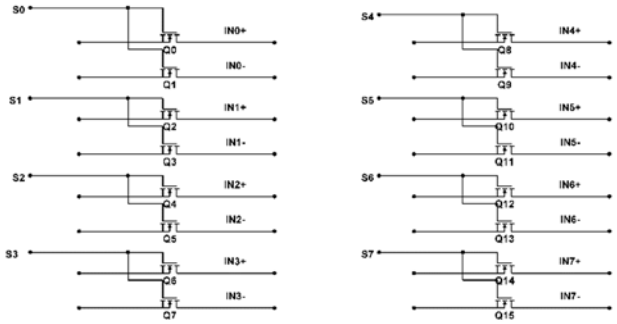

Fig. 15. Switch control signals vs. switch CMOS lines.

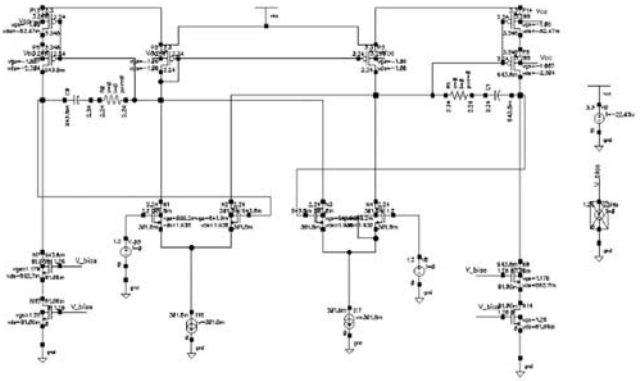

Fig. 16. Schematic of DDA [1].

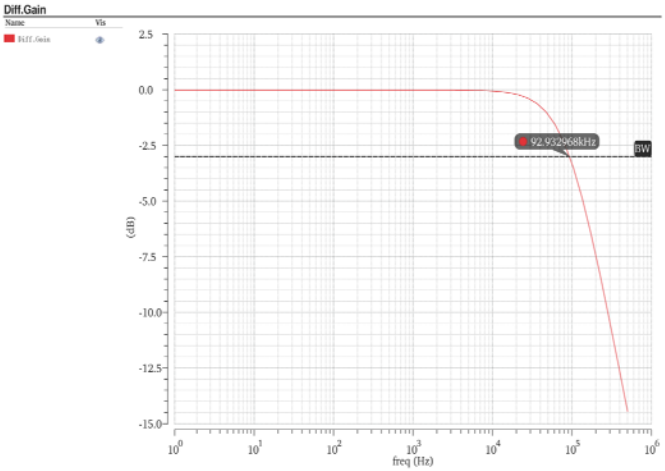

Fig. 17. Close loop frequency response of DDA, whose bandwidth is ~93kHz.

` When unity gain is reached, the phase margin is ~118°, indicating stability.

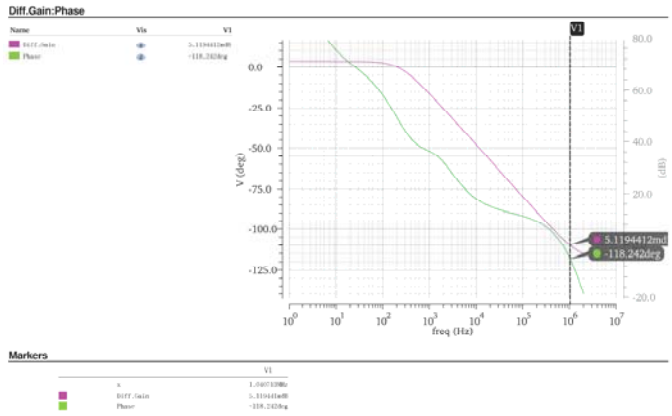

Fig. 18. Open loop phase margin.

IV. Biasing Circuit

A bandgap reference generator biasing circuit was used to provide V_{biasn} = 0.755V and V_{biasp} = 2.35V. The BGR has an outstanding feature to have CTAT and PTAT material cancel each other to reduce temperature effects on output voltages. With a swing from 0 to 75 degree Celsius, V_{biasp} changes with temperature of -40.36 ppm / Celsius, while V_{biasn} alters with temperature of -118 ppm / Celsius. V_{biasn} operates in -/+1% range of 0.75V from 2.77 - 3.42V. Since the circuit is operating in sub threshold, it consumes ultra-low power, 2.89 uW.

V. Programmable Gain Amplifier

For benefits of the entire analog front-end, a programmable gain amplifier in Fig. 20 is selected. The selected differential switched-capacitor amplifier has a good amount of advantages: offset voltage cancellation without requiring the output to slew to ground each time the amplifier is reset, insensitivity to low op-amp gain, clock feedthrough cancellation, and both inputs of this differential amplifier can be sampled at the same time [12].

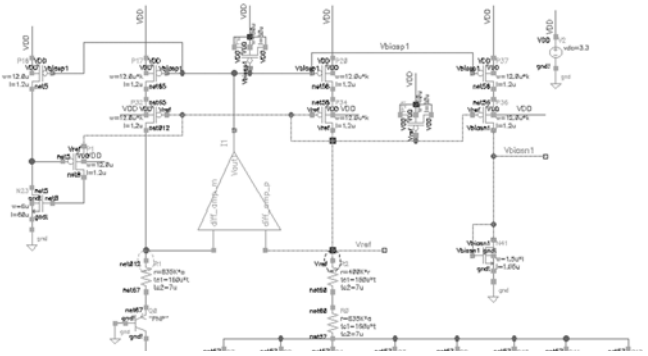

Fig. 19. A Bandgap Reference Generator [26].

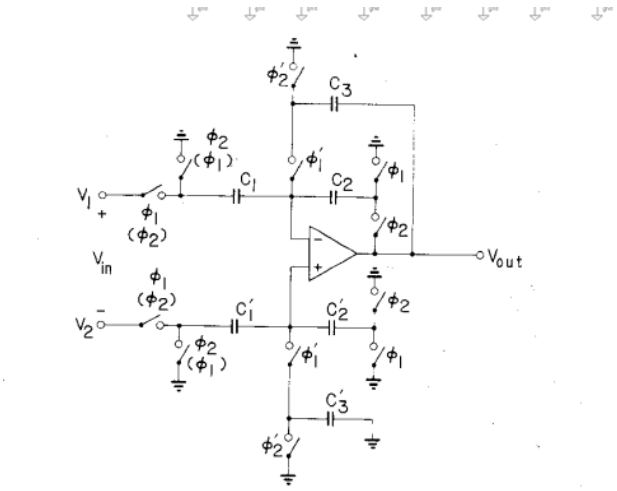

Fig. 20. A Switched-Capacitor Differential Amplifier [12].

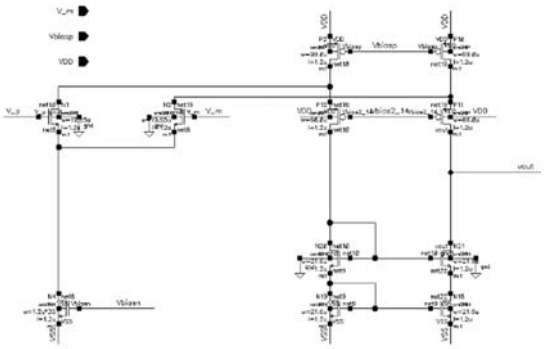

Fig. 21. 60-dB Folded Cascode OTA.

The OTA has the following characteristics: a gain of 60dB, a f-3dB bandwidth of 3.25K, a GBW of 3.25 MHz, a slew rate of 2.93V/us, a CMRR of 93.29 dB, a phase margin of 84.36 degrees, an ICMR of 0.706 - 3.158V and output range of 0.607 - 3.30V.

With a 1V peak-to-peak sine wave input, the above output was generated at Figure 23. The clock feedthrough and the dc offset were typically 5 - 15 mV at the output [12]. With a finite gain, the gain error is set to be proportional to A^{-2}. The

following transfer function is presented for low frequencies [12]:

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2}\left[1 - \frac{C_1 + C_2}{C_2 A^2}\right]. \quad (7)$$

This switched - capacitor amplifier can reach a gain of 1V/V, 3V/V and 11V/V. Because the amplifier will be used to process signals from EEG, ECoG, ECG and EMG, the amplification level of Vin can be adjusted by varying C1 values, i.e. arranging other C1_EEG, C1_ECG, etc. to be in parallel with existing C1 with switch signals sent by other clock signals. An example below:

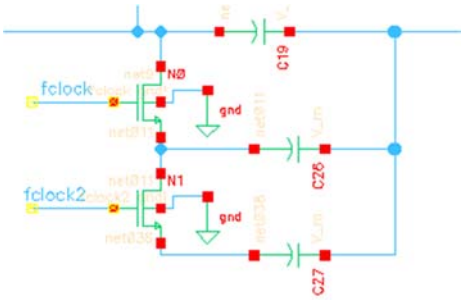

Fig. 22. Capacitors to make the amplifier programmable.

Here, C19, C26, and C27 may represent a different capacitance value each corresponding to a different gain, which can be controlled by f_{clock} and f_{clock2}, supplied by the microcontroller. For the sample simulation in Fig. 23, C1 and C2 are both set at 125pF; because the gain A is large this configuration per (7) is unity. A clock frequency of 500kHz is used in this case.

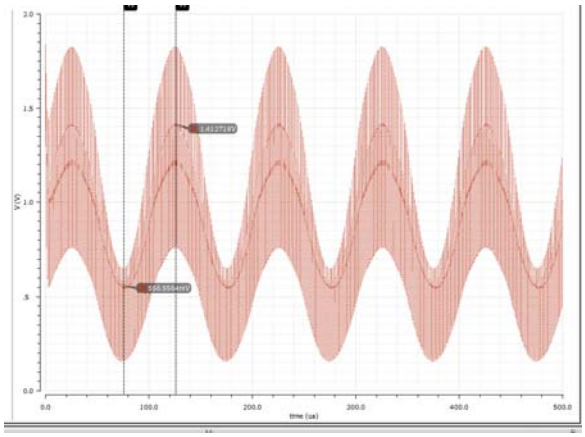

Fig. 23. Unity Gain Switch Capacitor Amplifier Output

VI. SAR ADC

A. *Overall design*

To process and analyze biopotential signals, the analog signals must be digitized. The analog-to-digital converter in this AFE receives analog signals from the PGA and convert them into digital codes. [2][3]

We considered four types of ADC, and decided to use an SAR ADC in our system because it is frequently the

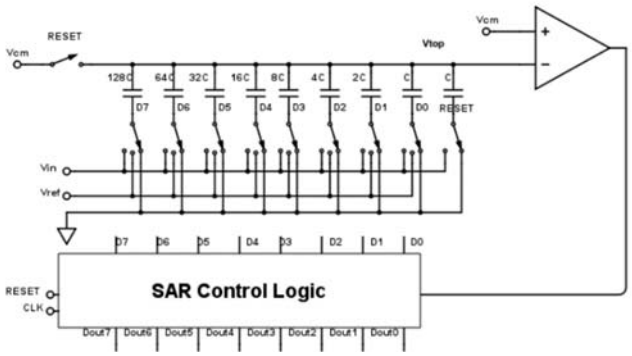

Fig. 24. SAR ADC topology

architecture of choice for 8 to 16-bit resolution applications with sample rates under 5 MSPS [2]. A pipeline ADC is undesirable because our input signals do not have large bandwidth, and it has huge power consumption and large die area [3]. A delta-sigma ADC is seemingly suitable for our application as it is low power, high resolution and low cost. However, considering the workload required to understand and implement the delta-sigma structure, we thought it would be inefficient to apply it. As the bandwidth of our signals of interest is below 2kHz, and the whole system does not require extremely high resolution, an SAR structure is chosen to be the ADC in our design.

Our group is going to design an 8-bit successive approximation routine ("SAR") ADC. It has an LSB value of 12.89 mV, given the VDD to be 3.3V. Since the smallest amplitude of the four bio-potential signals, which is EEG per Table 1, is 5μV, at most a total gain of 68.23 dB from all the gain stages preceded is required.

The topology of the 8-bit SAR ADC is presented in the Fig. 24 [15]. This design consists of a capacitive redistribution DAC, a comparator, a single throw double pole switch, eight single throw triple pole switches, a capacitor array, a SAR control logic and a code register.

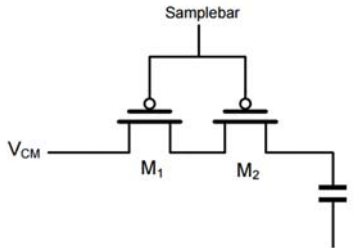

Fig. 25. Schematic of top plate switch

The DAC employed has a built-in sample and hold function. The design of the top plate switch is shown in Fig. 25 and the topology of the single throw triple pole switch is presented in the Fig. 26.

There are three phases of operation for the DAC. Firstly, the sample switch is closed and the bottom plate switch connects to Vin. After the sampling period, the sample switch

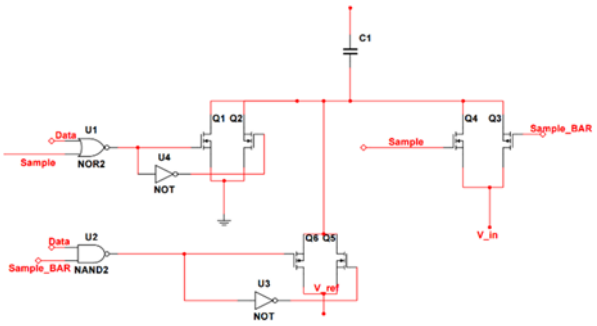

Fig. 26. Schematic of bottom plate switch

opens and the bottom one connects the bottom plates of capacitors to ground. Thus, a charge of $-V_{in} + V_{cm}$ is hold in the capacitor array. In the final redistribution phase, the digital code is fed into the corresponding switches, connecting certain capacitor to the V_{ref}. Thus, the corresponding output of the DAC is created and compared to the V_{cm}, and the output of the comparator goes into the SAR logic, updating the corresponding digital code. In this phase, nine clock cycles are used to determine the 8-bit digital code and one clock cycle is used to sample the input. At the end of the phase, all the bits are generated successively and the output of the DAC in the last step is defined as below:

$$V_{out_{DAC}} = -V_{IN} + V_{CM} + D_7 \cdot \frac{V_{REF}}{2} + D_6 \cdot \frac{V_{REF}}{2^2} + \cdots + D_0 \cdot \frac{V_{REF}}{2^8} \qquad (8)$$

Since V_{ref} is 3.3 volts and V_{cm} is 1.65 volts, the range of the DAC is from 0 to 3.3. Thus, a rail to rail comparator is required in this design. The schematic of the comparator is shown below. [5]

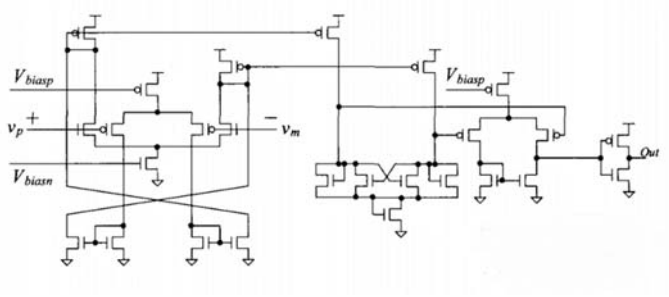

Fig. 27. Schematic of the comparator

Fig. 28 is the design of the SAR logic. There are in total 18 flip flops and they form a shift register and a code register. The shift register shifts '1' through the flip flops from MSB to LSB and the code register store the corresponding output from the flip flop. The flip flop design is shown in Fig. 29.

DNL represents the difference between the actual values of DAC output and theoretical values. INL shows the difference between the actual transition point to the ideal transition point of the VTC curve of the DAC. Our measured IND and DNL are shown below.

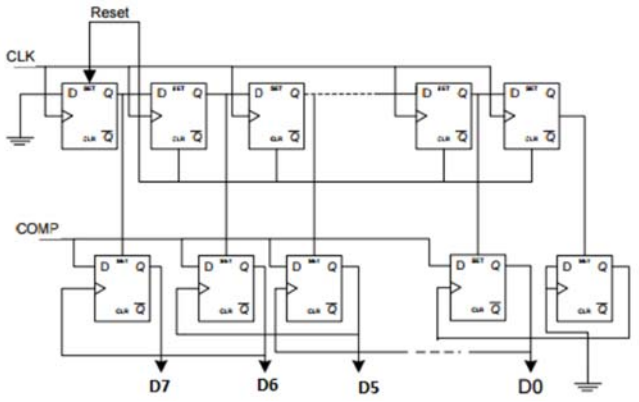

Fig. 28. Schematic of the SAR logic

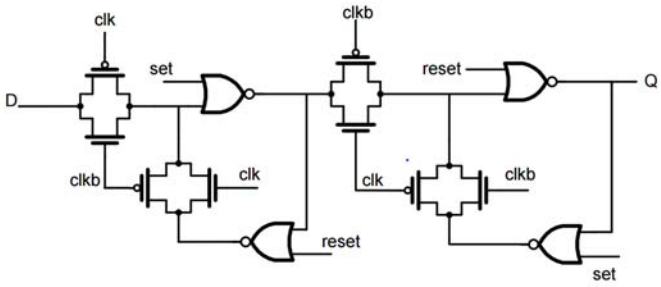

Fig. 29. Schematic of the set reset flip flop

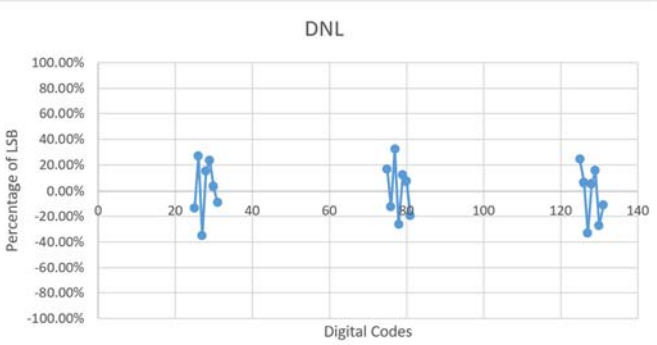

Fig. 30. Schematic of the DNL

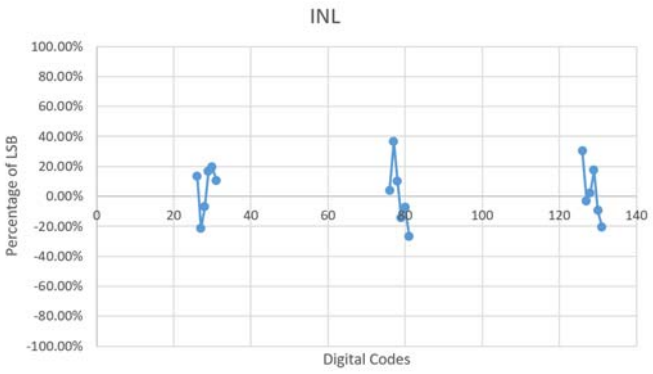

Fig. 31. Schematic of the INL

The DNL and INL shows good performance as no error exceeds .5 LSB in the codes that we tested. The dynamic range of this design is from 0 to 2 volts. It doesn't goes rail to rail because the switch resistance is too high, causing capacitor array taking too much time to charge and discharge. The dynamic range can be improved by increasing the width

of the transistors in the transmission gate to decrease their resistances. The power consumption of the design is 473.55 µW.

VIII. Layout and Results

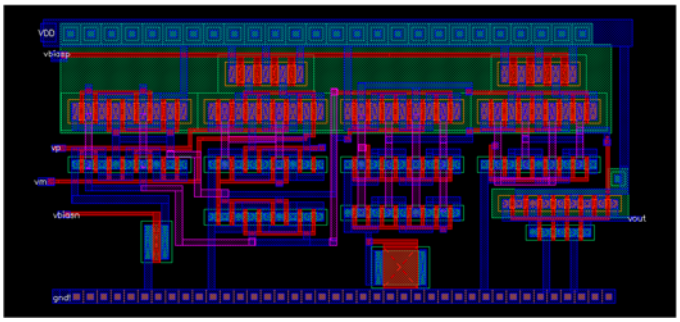

Fig. 32. Layout of comparator.

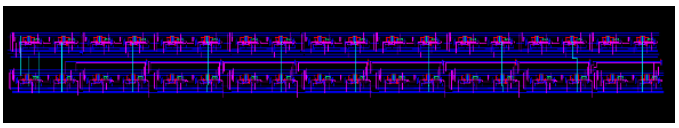

Fig. 33. Layout of SAR Logic.

Unfortunately, we were not able to do post-layout simulations as the layout for the DAC was incomplete. In terms of system simulations, we were only to ascertain the overall power consumption, seen in Table VI below.

TABLE VI
POWER CONSUMPTION OF INDIVIDUAL BLOCKS

Functional Block	**Power Consumption [µW]**
Chopper Amplifier (Pre-Amp)	251
Buffer (DDA)	75
Programmable Gain Amplifier	101
ADC	463
Total	890

The power consumption mostly comes from the ADC, which in turn consumes most power from the comparator, at 360 µW dynamic power. For future work, a different comparator topology might be researched for low power applications. In addition, the system lacks an on-chip voltage regulator, which is necessary to down-convert the batteries to 3.3 V. In terms of system results, an overall maximum gain of 60 dB can be achieved through the pre amplifier and the PGA stages, which is not enough to achieve the 68 dB needed for the lowest amplitude operation at 5µV. Further increasing the gain or using a higher bit ADC would be necessary for performance across all signals.

IX. Conclusion

This paper discussed the characteristics of major biopotential signals. In addition, this paper also discussed a feasible design of an Integrated Circuit (IC) that can receive, amplify, and forward the signal for further analysis. This design is best to be used in a portable device that collects biopotential signal and handles to a microcontroller for transmission and thorough analysis. The front end of the design is a chopper filter that interacts with the electrodes, which collect biopotential signals directly from the patient through medical-grade electrodes. The filtered and amplified signal will be passed through a clock-driven channel selector. Thereafter, the chosen processed signal will be fed into a programmable gain amplifier for final tuning before being fed into the ADC. Finally, digital signals will be available to microcontroller via data buses, i.e., SPI/I^2C bus. This paper also listed recommended power sources and other chips that are needed to make the system fully functional.

X. Tasks and Division of Labor

Jinming Hu	Pre-amplifier; choppers; Gm-C filter; SAR logic schematic/layout.
Xue Yang	Bandgap reference; PGA; Comparator schematic/layout.
Zengweijie Chen	Channel selector; DDA buffer; triple throw switch layout; system specs.
Hang Yang	ADC design; DAC schematic; DNL/INL simulations.

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