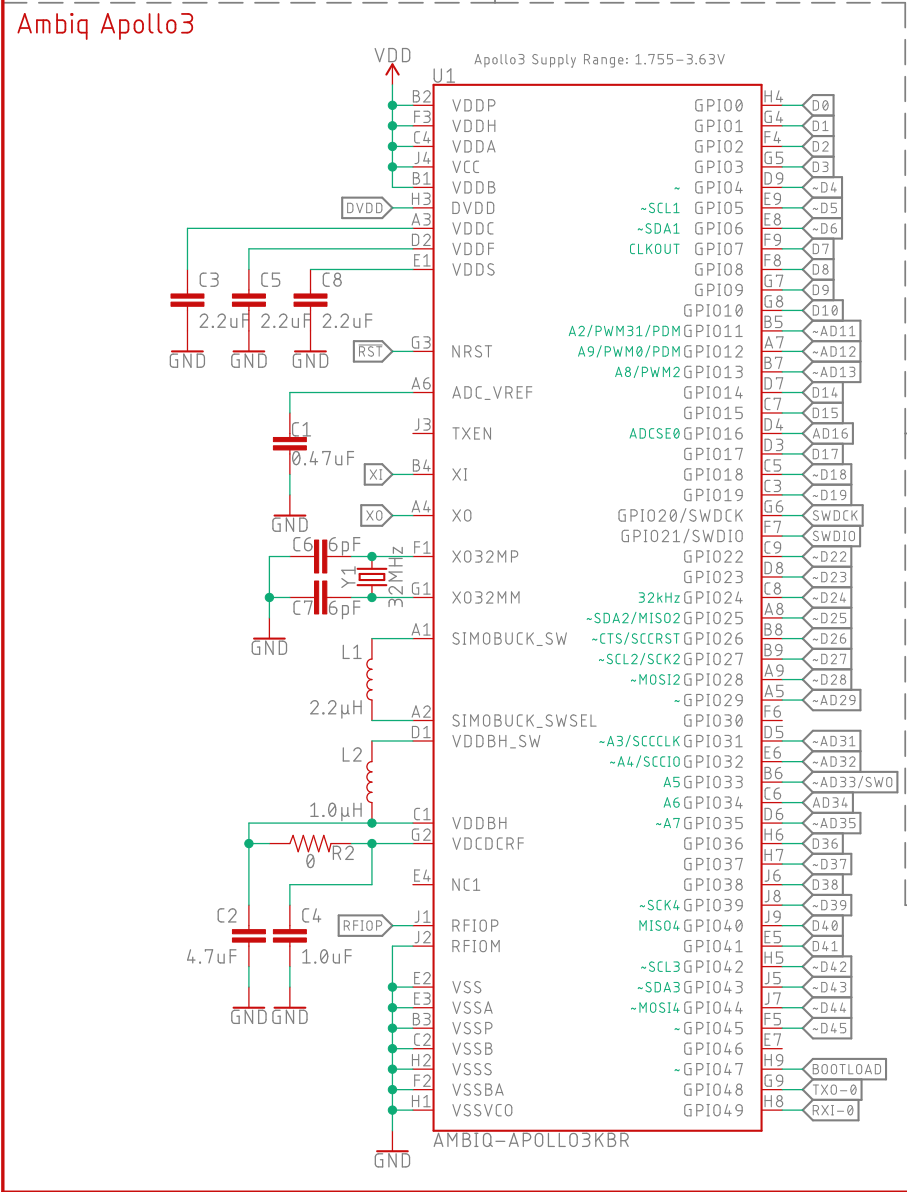


## Apollo3 Decoupling

The diagram illustrates the decoupling circuit for the Apollo3 microcontroller. It shows six power pins at the top, each with a corresponding decoupling capacitor connected to ground. The pins and their capacitor values are:

- DVDD (H3):** Connected to capacitor C11 (47nF).
- VDDP (B2):** Connected to capacitor C12 (1.0uF).
- VDDH (F3):** Connected to capacitor C13 (1.0uF).
- VDDA (C4):** Connected to capacitor C14 (1.0uF).
- VCC (J4):** Connected to capacitor C15 (1.0uF).
- VVDD (B1):** Connected to capacitor C16 (2.2uF).

Each capacitor is connected to its respective power pin and to a common ground (GND) line at the bottom. The capacitors are represented by two parallel lines, with their values labeled below them.



**Primary**

VDD J36  
VDD J37  
RST J50  
TX0-0 J9  
RX1-0 J3

P/SCL5/SCK5/TX0  
P/SDA5/MISO5/RX0

P/MOSI5/RX1/32kHz

BOOTLOAD J7

SWDIO J10  
SWDCK J2  
-AD33/SW0 J30

P/A/SW0

XI J35  
X0 J34

GND J1  
GND J59  
GND J22  
GND J38  
GND J39  
GND J47

## Secondary

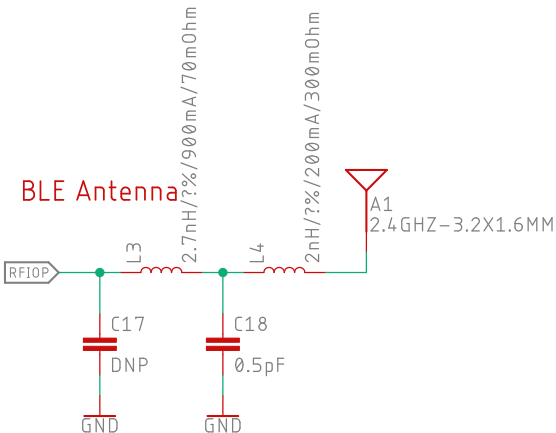
P/SDA0/MISO0/I2SDAT ~D6 J23  
 MISO1/CLKOUT D7 J13  
 P/SCL0/SCK0 ~D5 J12

P/TX1/32kHz ~D24 J16  
 P/SDA2/MISO2/RX1 ~D25 J25

P/SCL4/SCK4/TX1 ~D39 J4  
 SDA4/MISO4/RX1 D40 J5

Tertiary	
A/P	-AD11 J32
A/P	-AD12 J26
A/P/12	-AD13 J28
P/SCL2/SCK2	-D27 J1
P/MOSI2/I2SWCLK	-D28 J21
A/P/PDMDATA	-AD29 J33
A/P/SCIO	-AD32 J24
A/P/I2SDAT	-AD35 J14
P/MOSI4	-D44 J58
P/CTS1/SCRST	-D26 J27
P/A/RTS1/SCCLK	-AD31 J44
P/A/SDA3/MISO3/RX1	-D43 J52
MISO3/RX1	D38 J56
P/SCL3/SCK3/TX1	-D42 J53
RX1/PDMDATA	D36 J55
P/PDMCLK/SCIO	-D37 J57
P/PDMCLK	-D22 J17
P/RX1	-D4 J15
SCL1/SCK1/TX1/SCCLK	D8 J1
MOSI1/TX1/PDMCLK	D10 J8
A1/MISO1/RX1/SCIO	D9 J6

Quaternary	
SLSCK/SLSCL/CLKOUT	D0 J51
SLMOSI/SLSDA	D1 J49
SLMISO	D2 J48
SLnCE	D3 J51
ADCD1P	D14 J20
ADCD01N	D15 J29
A/CMPIN0	AD16 J4
CMPRF1	D17 J4
P/CMPIN1	~D18 J41
P/CMPRF0	~D19 J40
P/CMPOUT	~D23 J1
A/CMPRF2	AD34 J33
BLEIF_IRA/SWO	D41 J45
P/SWO	~D45 J4



Board thickness: 0.8mm  
Er: 4.6  
RF Trace Width: 11.55mil/0.293mm  
Polygon Isolation: 5mil/0.127mm  
Distance between Layer 1/2: 0.2mm

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Design by: N. Seidle

Sheet: 1/1

REV:  
v01