

LG290P (03) Reference Design

GNSS Module Series

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About the Document

| Document Information | | | | |
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| - | 2023-11-30 | Creation of the document |
| 1.0 | 2024-08-19 | First official release |



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1 Reference Design

1.1. Introduction

This document provides the reference design of Quectel LG290P (03) GNSS module, including the design of block diagram, MCU circuit and power supply, module interfaces and antenna interface. It also comprises SCH and PCB design checklists.

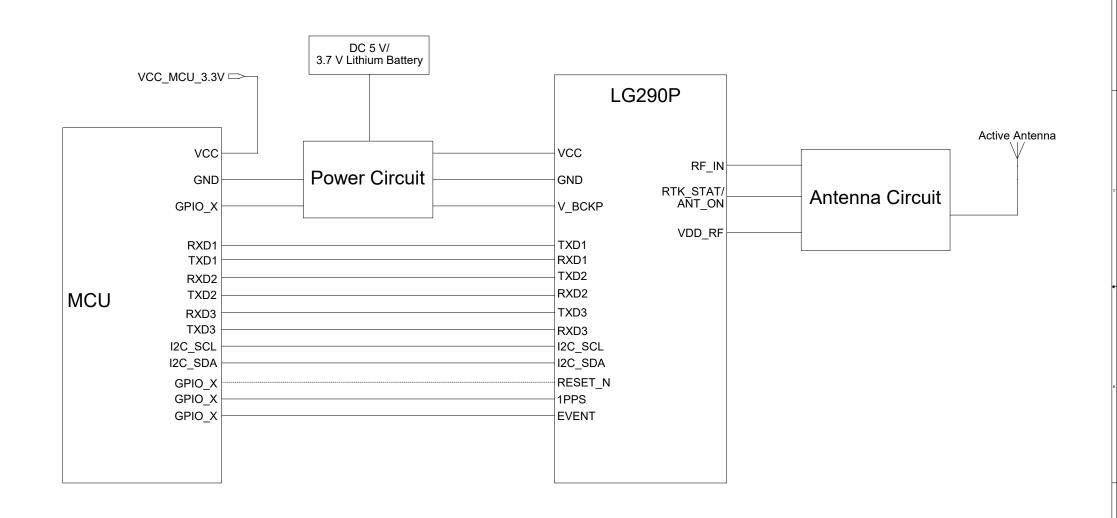
1.2. Reference Schematics and Design Checklists

The schematics and design checklists illustrated in the following pages are provided for your reference only.

NOTE

Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

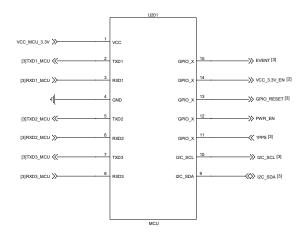
Block Diagram



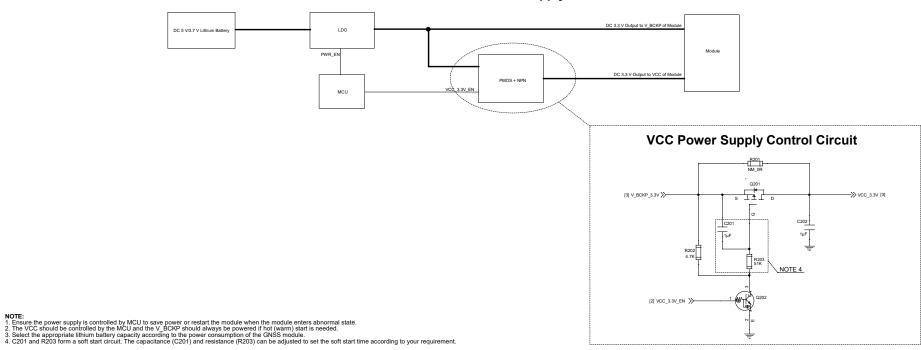
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| PROJECT LG290P (03) | PROJECT LG290P (03) | | 1.0 | | | |
| DRAWN BY Vijay ZHAO/Yasuo MAO | CHECKED BY Storm BAC |) | SIZE A2 | | | |
| DATE Monday, August 19, 2 | 024 SHEET | - 1 | OF 4 | | | |

MCU Circuit and Power Supply

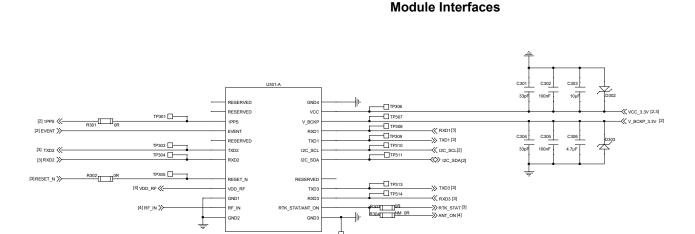
MCU Circuit

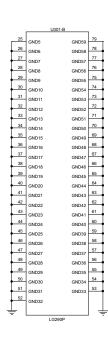


Power Supply Circuit



Module Interfaces





- NOTE:

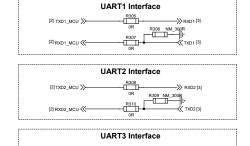
 1. The IZC interface has been pulled up internally and does not need to be pulled up externally.

 2. The power supply design must meet the sequence requirements in hardware design. See the hardware design document for details.

 3. A level-shifting circuit must be used when the IIO voltage of MCU is not matched with that of module.

 Recommended level-shifting orbip: SNY4AVC4T245. Level-shifting chips with series resistors such as TXB series are not recomended
- Reserve test points for debugging the module.

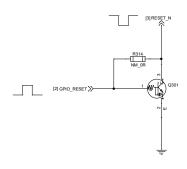
UART Interface Circuits



NOTE:
1. The above circuits are used when UART interfaces voltage of MCU is consistent with that of the module.
2. It is recommended that R306, R309, and R312 reserve resistor bits for adjusting level matching.

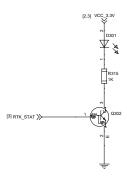
[2] RXD3 MCU <<-

RESET_N Circuit



- **NOTE:**1. The RESET_N pin is internally pulled up to VCC with a 20 k Ω resistor, thus no external pull-up circuit is allowed for this pin. An OC drive circuit is recommended to control the RESET_N pin.
 2. The RESET_N must be connected so that it can be used to reset the module if the module enters an abnormal state.

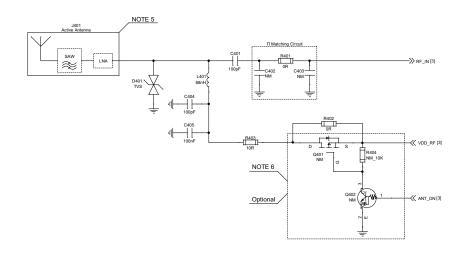
RTK_STAT Circuit



NOTE:
If the RTK_STAT outputs a high level, it indicates that the module enters the RTK fixed mode. If the pin outputs a low level, it indicates that the module exits the RTK fixed mode.

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Antenna Interface



- NOTE:

 1. R401, C402 and C403 form a IT matching circuit for antenna impedance matching. By default, R401 is 0 \(\Omega\$, C402 and C403 are not mounted.

 2. D401 is an electrostatic discharge (ESD) protection device to protect RF components inside the module from the damage caused by ESD through the antenna inrterface.

 3. The impedance of the RF trace line on the main PCB should be controlled to \$0 \Omega\$ and the trace length should be kept as short as possible.

 4. L401 is used for preventing the RF signal from leaking into the VDD. RF and preventing noise propagation from the VDD. RF to the antenna.

 5. To further mitigate the impact of out-of-band signals on GNSS module performance, you must choose the active antenna whose SAW filter is placed in front of the LNA in the internal framework.

 DO NOT place the LNA in the front.

 6. The VDD. RF pin is used by default. Please select the relevant design according to the actual usage.

 7. See the hardware design document for details.

 8. The passive antenna is not recommended.

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Table 1: SCH Design Checklist

| Pin | Pin Name Checklist | | Result | t | | |
|-----|--------------------|--|--------|------|-----|---------|
| No. | | | Pass | Fail | N/A | Comment |
| 1 | RESERVED | The RESERVED pin must be left N/C. | | | | |
| 2 | RESERVED | The RESERVED pin must be left N/C. | | | | |
| 3 | 1PPS | Connect to the GPIO of the MCU. | | | | |
| 4 | EVENT | Connect to the GPIO of the MCU. | | | | |
| 5 | RESERVED | The RESERVED pin must be left N/C. | | | | |
| 6 | TXD2 | | | | | |
| 7 | RXD2 | Connect to MCU through 0 Ω resistors or a level-shifting circuit. Reserve test points. | | | | |
| 8 | RESET_N | Connect to the GPIO of the MCU through a 0 Ω resistor (not mounted by default) or an OC drive circuit to control the module reset. Reserve a test point. | | | | |
| 9 | VDD_RF | Supplies power for an external active antenna or LNA. | | | | |
| 10 | GND | Reference ground of the module. The GND pin must be connected to ground. | | | | |
| 11 | RF_IN | π matching circuit must be added for impedance modification. It is recommended to select an ESD protection device with junction capacitance lower than 0.6 pF. The inductor used in the power supply circuit of the active antenna is at least 68 nH and the inductor's pad which is close to RF_IN should be placed on the RF line. | | | | |
| 12 | GND | Reference ground of the module. The GND pin must be connected to ground. | | | | |

| Pin | Pin Name | Checklist | Result | | | |
|-----|------------------|--|--------|------|-----|---------|
| No. | | | Pass | Fail | N/A | Comment |
| 13 | GND | Reference ground of the module. The GND pin must be connected to ground. | | | | |
| 14 | RTK_STAT/ANT_ON* | RTK_STAT is recommended to connect to an indication circuit. ANT_ON is connected to the transistor's base to control the power supply of VDD_RF for an external LNA or active antenna. | | | | |
| 15 | RXD3 | | | | | |
| 16 | TXD3 | Connect to MCU through 0 Ω resistors or a level-shifting circuit. Reserve test points. | | | | |
| 17 | RESERVED | The RESERVED pin must be left N/C. | | | | |
| 18 | I2C_SDA | Connect to MCU through 0 Ω resistors or a level-shifting circuit. Reserve test points. | | | | |
| 19 | I2C_SCL | | | | | |
| 20 | TXD1 | | | | | |
| 21 | RXD1 | Connect to MCU through 0 Ω resistors or a level-shifting circuit. Reserve test points. | | | | |
| 22 | V_BCKP | It is recommended to place a TVS, and a combination of a 4.7 μF, a 100 nF and a 33 pF decoupling capacitor near the V_BCKP pin. Ensure that V_BCKP is controlled by MCU. Reserve a test point. V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed. | | | | |
| 23 | VCC | It is recommended to place a TVS, and a combination of a 10 μF, a 100 nF and a 33 pF decoupling capacitor near the VCC pin. Ensure that VCC is controlled by MCU. | | | | |

| Pin | Pin Name Checklist | Result | | | Comment | |
|-------|--------------------|--|------|------|---------|---------|
| No. | | CHECKIST | Pass | Fail | N/A | Comment |
| | | 3. Reserve a test point. | | | | |
| 24~79 | GND | Reference ground of the module. The GND pin must be connected to ground. | | | | |

NOTE

- 1. If the I/O voltage of MCU is not matched with the module, a level-shifting circuit must be selected.
- 2. All GND pins must be connected to ground and reserved a GND test point. Leave RESERVED and unused pins N/C (not connected).
- 3. Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

Table 2: PCB Design Checklist

| Pin | B's Mana | | Result | | | 0 |
|-----|----------|--|--------|------|-----|---------|
| No. | Pin Name | Checklist | Pass | Fail | N/A | Comment |
| 1 | RESERVED | | | | | |
| 2 | RESERVED | 1 | | | | |
| 3 | 1PPS | Surround the signal trace with ground. Avoid routing near strong interference. Keep the routing as short as possible and keep fewer vias to avoid parasitic capacitance and inductance. | | | | |
| 4 | EVENT | Surround the signal trace with ground, and avoid routing near the strong interference. | | | | |
| 5 | RESERVED | 1 | | | | |
| 6 | TXD2 | Surround the signal traces with ground. Keep the routing short and stay away from interference. | | | | |
| 7 | RXD2 | 2. Reep the fouting short and stay away from interference. | | | | |
| 8 | RESET_N | Surround the signal trace with ground, and avoid routing near the strong interference. | | | | |
| 9 | VDD_RF | Power routing should be surrounded by GND and avoid being parallel with other line(s). | | | | |
| 10 | GND | Confirm that there are no isolated shapes in the ground layer. Module GND pads must be completely covered by the ground plane. | | | | |
| 11 | RF_IN | 1. The characteristic impedance of the RF signal line(s) is kept at 50 Ω , and the RF trace is as short and straight as possible, with smooth lines (without bumps, with consistent geometry–it would be ideal for the footprints to be blended into the RF trace, with curved rather than sharp angles). | | | | |

| Pin | Pin Name | | Result | | | Comment |
|-----|------------------|--|--------|------|-----|---------|
| No. | Pin Name | Checklist | Pass | Fail | N/A | Comment |
| | | Ensure that there are no vias in the RF signal path. Ensure that RF signal path is surrounded by ground. RF signal line(s) and GNSS antenna are kept away from noise sources such as MCU(s), crystal(s) and other RF antenna(s). | | | | |
| 12 | GND | Confirm that there are no isolated shapes in the ground layer. Module GND pads must be completely covered by the ground plane. | | | | |
| 13 | GND | Confirm that there are no isolated shapes in the ground layer. Module GND pads must be completely covered by the ground plane. | | | | |
| 14 | RTK_STAT/ANT_ON* | Surround the signal trace with ground. Avoid routing near strong interference. | | | | |
| 15 | RXD3 | Surround the signal traces with ground. Keep the routing short and stay away from interference. | | | | |
| 17 | RESERVED | | | | | |
| 18 | I2C_SDA | Surround the signal trace with ground. | | | | |
| 19 | I2C_SCL | 2. Keep the routing short and stay away from interference. | | | | |
| 20 | TXD1 | Surround the signal traces with ground. | | | | |
| 21 | RXD1 | 2. Keep the routing short and stay away from interference. | | | | |
| 22 | V_BCKP | The power supply first passes through the TVS, and then through the subsequent components. | | | | |

| Pin | Din Name | Chaaklist | Result | | Result | | Result | | Result | | Result | | Result | | Result | | Result | | Result | | Result | Result | | ılt | | | ult | Comment |
|-------|----------|--|--------|------|--------|---------|--------|--|--------|--|--------|--|--------|--|--------|--|--------|--|--------|--|--------|--------|--|-----|--|--|-----|---------|
| No. | Pin Name | Checklist | Pass | Fail | N/A | Comment | | | | | | | | | | | | | | | | | | | | | | |
| | | The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements. | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 3. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated. | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1. The power supply first passes through the TVS, and then through the subsequent components. | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 23 | VCC | The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements. | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 3. The routing width of the power supply is at least 1 mm per ampere. The longer the routing, the wider it should be. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated. | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 24–75 | GND | Confirm that there are no isolated shapes in the ground layer. Module GND pads must be completely covered by the ground plane. | | | | | | | | | | | | | | | | | | | | | | | | | | |

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