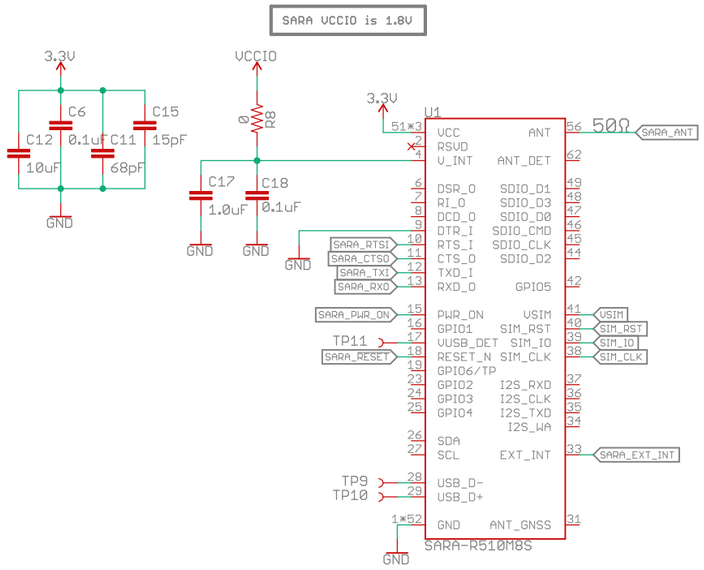
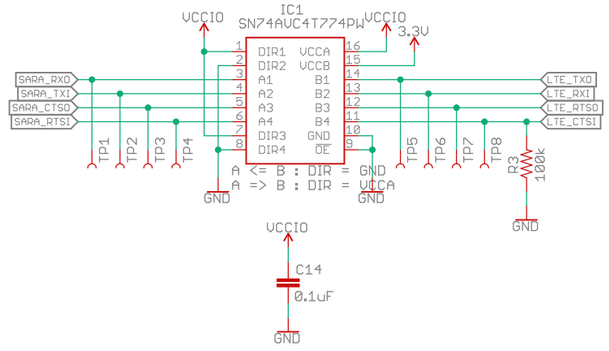
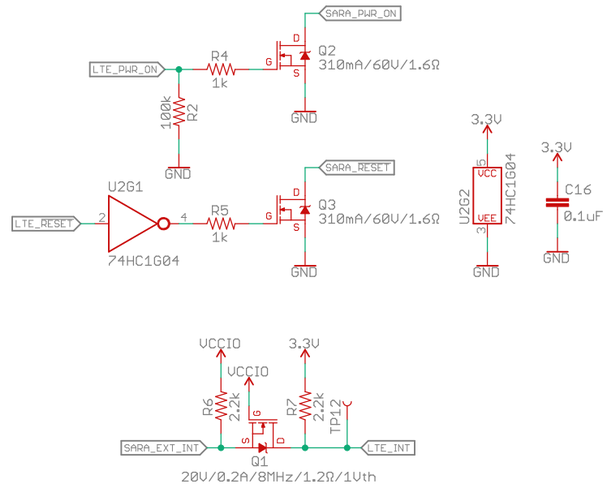
SARA-R5

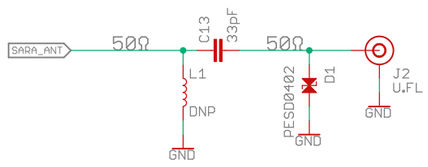


SARA Level Shifting

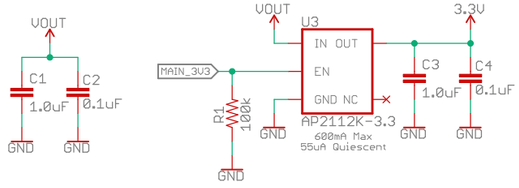




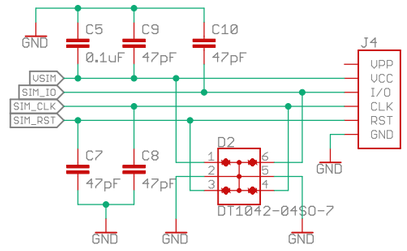
LTE Antenna



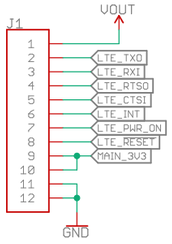
Voltage Regulation



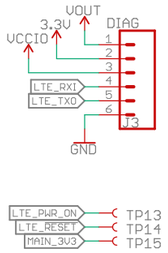
SIM



FPC To Mainboard



DIAG



Microstrip Calculation:

JLCPCB JLC7628 4-layer Impedance Control
Copper Thickness (1oz): 1.4mil/0.035mm
Board thickness: 1.6mm
Prepreg dielectric thickness (layer 1 to 2): 0.2mm
Er: 4.6
Polygon Isolation: 8mil/0.2032mm
RF Trace Width: 13.8mil/0.35mm
https://cheanandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm

SARA ANT and ANT_GNSS pads do not require restrict on layer 2 as the prepreg thickness is >= 200µm

SARA-R5 VCC Design Notes:

VCC: Min. 3.3V Typ. 3.8V Max. 4.4V
VCC Extended: Min. 3.0V Max. 4.5V

Worst case:
Maximum current draw during Tx: 395mA
AP2112-3.3 drop out voltage: ~175mV at: 400mA output current; Vout = 3.3V; 25°C

Typical:
Typical current draw during Tx/Rx: 195mA at 23dBm
AP2112-3.3 drop out voltage: ~125mV at: 300mA output current; Vout = 3.3V; 25°C

sparkfun

open hardware

Special Instructions

TITLE: SparkFun RTK Facet - Cellular

Design by: Paul Clark

REV: v10

Date: 04/10/2021 11:33

Sheet: 1/1