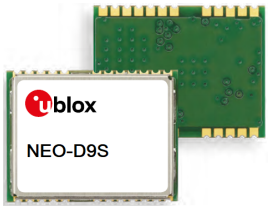
NEO-D9S

u-blox D9 correction data receiver

Data sheet



Abstract
Technical data sheet describing the u-blox D9 correction data receiver. This NEO form factor module provides easy access to satellite L band GNSS corrections globally.

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Document information

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Product status	**Corresponding content status**	
In development / prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Firmware version	PCN reference
NEO-D9S	NEO-D9S-00B-00	PMP 1.04	N/A

Contents

1 Functional description

1.1 Overview

NEO-D9S can receive the data stream of a GNSS correction service, broadcast via satellite L band and compliant to the specification the product is designed for. Integrated with a high precision GNSS receiver, such as from the u-blox F9 platform, it enables the positioning system to reach down to centimeter-level accuracy.

1.2 Performance

Parameter		Specification
Receiver type		NEO-D9S correction data receiver

L band satellite		Specification
Time to first frame [1]		< 10 s at 2400 bps
Sensitivity acquisition [2]		-133 dBm for BER <10e-5 at 2400 bit/s
Specification compliance		L band SESTB28A
Boot time		<1 s
Center frequency configuration steps		1 Hz
Center frequency search window		0 to 65 kHz
User data rates		600, 1200, 2400, 4800 bps
Service identifier		Configurable
De-scrambler		Configurable
De-scrambling initialization vector		Configurable
Pre-scrambler		Enable/disable
Number of concurrent reception channels		1
UniqueWord		Configurable
Frequency range		1525 MHz to 1559 MHz [3]
Communication interface		UART/USB/I2C/SPI
Communication speed		Up to 921600 baud UART, USB 2.0
Software back-up mode		Available
Vehicle dynamics	Dynamics	+/- 2g acceleration for all data rates (600 bit/s, 1200 bit/s, 2400 bit/s, 4800 bit/s)
	Velocity	Up to and including 300 km/h

Table 1: NEO-D9S performance

1.3 Supported GNSS augmentation systems

1.3.1 Satellite L band

The satellite L band communication system allows GNSS correction service providers to broadcast a variety of services on specific channels, satellites and beams. Please consult with the service

1 With respect to an L band signal using a 20-25 dB external LNA

2 Success rate of acquiring an L band signal > 95% using a 20-25 dB external LNA

3 C/N0 drops 2.5 dBHz at 1534 MHz, 1 dBHz at 1540 MHz, 0.5 dBHz at 1542 MHz respectively

provider of choice on the region their service covers and the specific frequency used. The NEO-D9S must be configured according to the specific service as initial identification and decoding of the service provider stream is required.

1.4 Supported protocols

The NEO-D9S supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary

Table 2: Supported protocols

For specification of the protocols, see the u-blox NEO-D9S Interface description [2].

2 System description

2.1 Block diagram

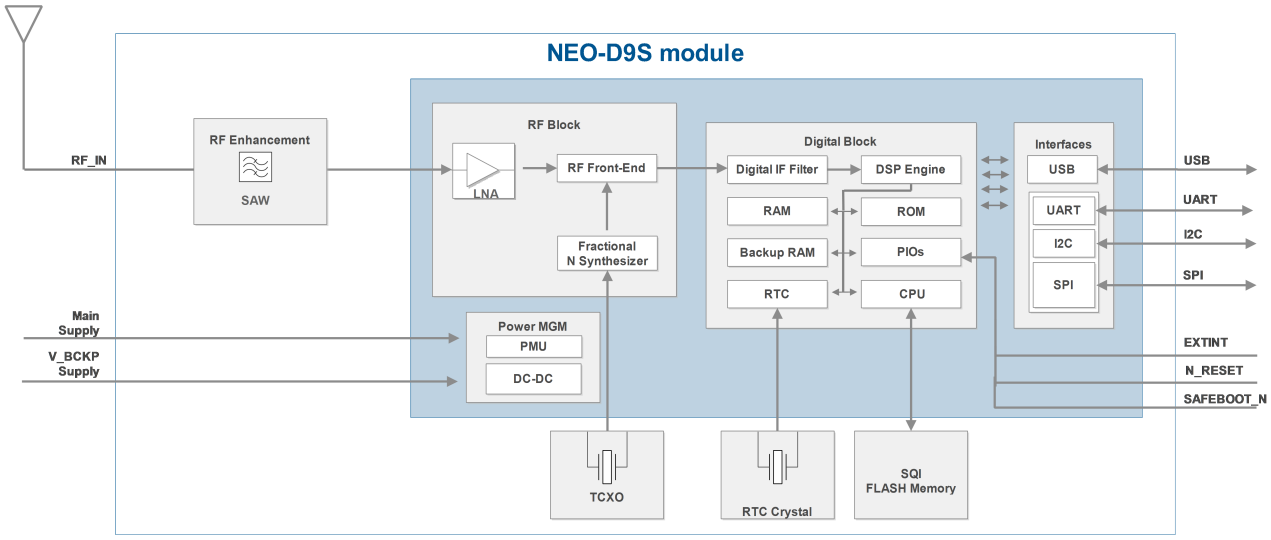

Figure 1: NEO-D9S block diagram

☞ An active antenna is mandatory with the NEO-D9S.

3 Pin definition

3.1 Pin assigment

The pin assignment of the NEO-D9S module is shown in Figure 2. The defined configuration of the PIOs is listed in Table 3.

☞ UART2, V_BCKP software function, are not available in the current software version. V_BCKP hardware pin must be connected to VCC to ensure correct hardware operation.

UART2 is reserved for future direct connection to u-blox F9 high precision GNSS receivers. It will be enabled in following FW versions.

☞ Do not permanently connect the NEO-D9S UART2 with the ZED-F9 UART2 as the current software in both modules does not support this. A conflict could possibly occur with the default software settings in both modules. Instead, provide a jumper to connect the two UART2 ports when the firmware is supported.

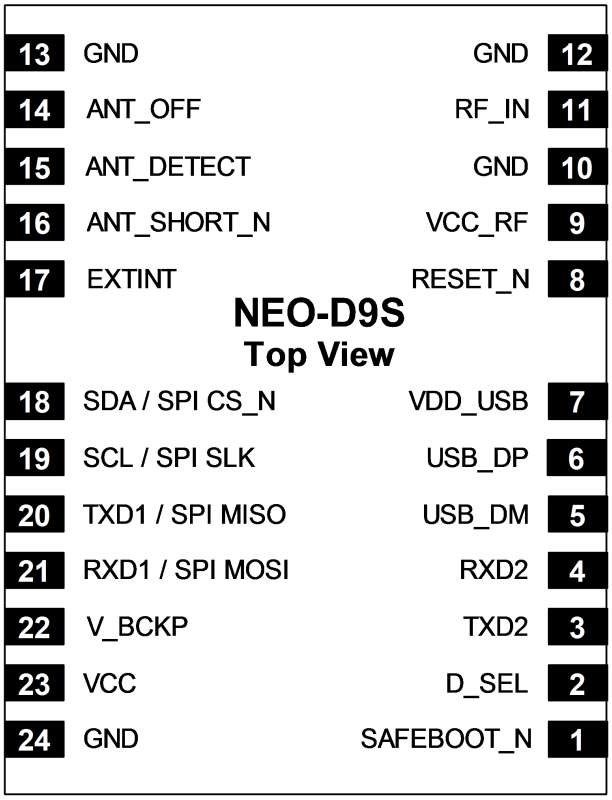

Figure 2: NEO-D9S pin assignment

Pin no.	Name	I/O	Description
1	SAFEBOOT_N	I	SAFEBOOT_N (used for FW updates and reconfiguration, leave open)
2	D_SEL	I	UART 1 / SPI select. (open or high = UART 1)
3	TXD2	O	UART 2 TXD
4	RXD2	I	UART 2 RXD
5	USB_DM	I/O	USB data (DM)
6	USB_DP	I/O	USB data (DP)

Pin no.	Name	I/O	Description
7	V_USB	I	USB supply
8	RESET_N	I	RESET (active low)
9	VCC_RF	O	External LNA power
10	GND	I	Ground
11	RF_IN	I	Active antenna L band signal input
12	GND	I	Ground
13	GND	I	Ground
14	ANT_OFF	O	External LNA disable - default active high
15	ANT_DETECT	I	Active antenna detect - default active high
16	ANT_SHORT_N	O	Active antenna short detect- default active low
17	EXTINT	I	External interrupt pin
18	SDA / SPI CS_N	I/O	I2C data if D_SEL = VCC (or open); SPI chip select if D_SEL = GND
19	SCL / SPI SLK	I/O	I2C clock if D_SEL = VCC (or open); SPI clock if D_SEL = GND
20	TXD / SPI MISO	O	UART output if D_SEL = VCC (or open); SPI MISO if D_SEL = GND
21	RXD / SPI MOSI	I	UART input if D_SEL = VCC (or open); SPI MOSI if D_SEL = GND
22	V_BCKP	I	Connect to VCC
23	VCC	I	Supply voltage
24	GND	I	Ground

Table 3: NEO-D9S pin assigment

☞ For detailed information on the pin functions and characteristics see the u-blox NEO-D9S Integration manual [1].

4 Electrical specification

The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or at any other conditions above those given below is not implied. Exposure to limiting values for extended periods may affect device reliability.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Input pin voltage	Vin		-0.5	VCC + 0.5	V
VCC_RF output current	ICC_RF			100	mA
Supply voltage USB	V_USB		–0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.5	V
Input power at RF_IN	Prfin	source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	Tstg		-40	+85	°C

Table 4: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. Voltage spikes exceeding the power supply voltage specification, given in the table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

4.2 Operating conditions

All specifications are at an ambient temperature of 25 °C. Extreme operating temperatures can significantly impact the specification values. Applications operating near the temperature limits should be tested to ensure the specification.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
SW backup current	I_SWBCKP		0.36		mA	
Input pin voltage range	Vin	0		VCC	V	
Digital IO pin low level input voltage	Vil			0.4	V	
Digital IO pin high level input voltage	Vih	0.8 * VCC			V	
Digital IO pin low level output voltage	Vol			0.4	V	Iol = 2 mA
Digital IO pin high level output voltage	Voh	VCC – 0.4			V	Ioh = 2 mA
DC current through any digital I/O pin (except supplies)	Ipin			5	mA	
VCC_RF voltage	VCC_RF		VCC - 0.1		V	
VCC_RF output current	ICC_RF			50	mA	
Receiver chain noise figure[4]	NFtot		11		dB	
Recommended LNA gain into module	LNA_gain		20		dB	

[4] Only valid for the L band band

Parameter	Symbol	Min	Typical	Max	Units	Condition
Operating temperature	Topr	-40	+25	85	°C	

Table 5: Operating conditions

☞ Operation beyond the specified operating conditions can affect device reliability.

4.3 Indicative power requirements

Table 6 lists examples of the total system supply current including RF and baseband section for a possible application.

☞ Values in Table 6 are provided for customer information only, as an example of typical current requirements. The values are characterized on samples by using a cold start command. Actual power requirements can vary depending on FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	L - band SESTB28A	Unit
I_{PEAK}	Peak current	Acquisition & tracking	130	mA
$I_{AVERAGE}$	Average current	Acquisition & tracking	35	mA

Table 6: Currents to calculate the indicative power requirements

All values in Table 6 are measured at 25 °C ambient temperature.

5 Communications interfaces

There are several communications interfaces including UART, SPI, I2C[5] and USB.

5.1 UART interface

UART1 is the main UART interface for UBX protocol host control and message output. UART2 software functionality will be added in the future for direct connection to the ZED-F9x UART2 interface. The NEO-D9S UART2 and the ZED-F9x UART2 hardware interfaces must not be permanently connected. Use an open jumper so it can be connected when the firmware supports this function.

Symbol	Parameter	Min	Max	Unit
R_u	Baud rate	9600	921600	bit/s
Δ_{Tx}	Tx baudrate accuracy	-1%	+1%	-
Δ_{Rx}	Rx baudrate tolerance	-2.5%	+2.5%	-

Table 7: NEO-D9S UART specifications

5.2 SPI interface

The NEO-D9S has an SPI slave interface that can be selected by setting D_SEL = 0. The SPI slave interface is shared with UART1. The SPI pins available are: SPI_MISO (TXD), SPI_MOSI (RXD), SPI_CS_N, SPI_CLK. The SPI interface is designed to allow communication to a host CPU. The interface can be operated in slave mode only. Note that SPI is not available in the default configuration because its pins are shared with the UART and I2C interfaces. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

This section provides SPI timing values for the NEO-D9S slave operation. The following tables present timing values under different capacitive loading conditions. Default SPI configuration is CPOL = 0 and CPHA = 0.

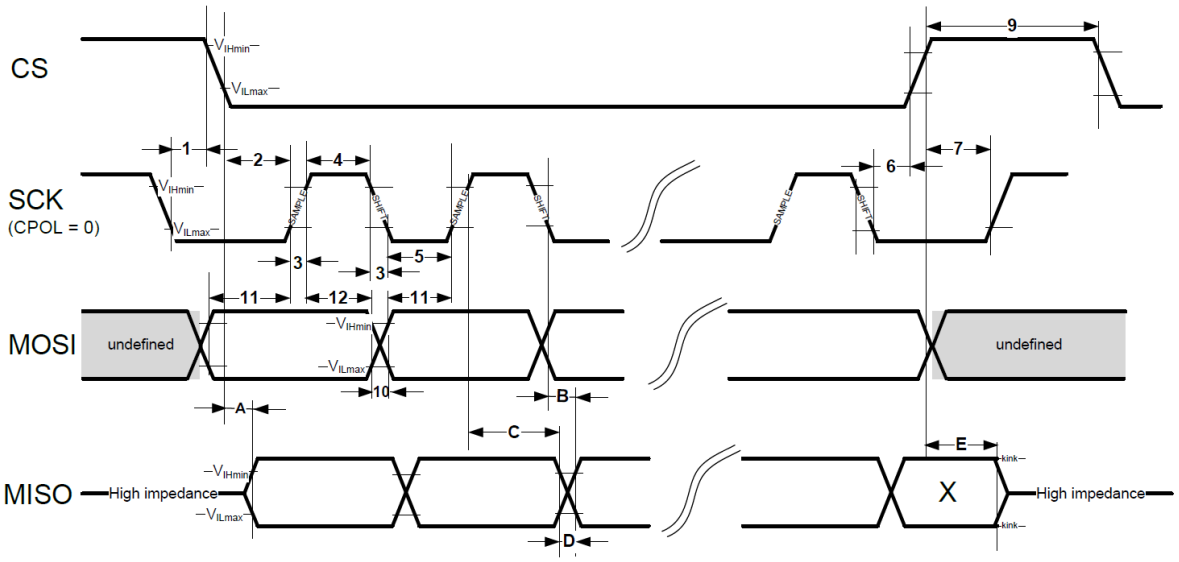

Figure 3: NEO-D9S correction data receiver SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

5 I2C is a registered trademark of Philips/NXP

Timings 1 - 12 are not specified here.

Timing value at 2 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	14	38
"B" - MISO data valid time (SCK) weak driver mode	21	38
"C" - MISO data hold time	114	130
"D" - MISO rise/fall time, weak driver mode	1	4
"E" - MISO data disable lag time	20	32

Table 8: NEO-D9S SPI timings at 2pF load

Timing value at 20 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	19	52
"B" - MISO data valid time (SCK) weak driver mode	25	51
"C" - MISO data hold time	117	137
"D" - MISO rise/fall time, weak driver mode	6	16
"E" - MISO data disable lag time	20	32

Table 9: NEO-D9S SPI timings at 20pF load

Timing value at 60 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	29	79
"B" - MISO data valid time (SCK) weak driver mode	35	78
"C" - MISO data hold time	122	152
"D" - MISO rise/fall time, weak driver mode	15	41
"E" - MISO data disable lag time	20	32

Table 10: NEO-D9S SPI timings at 60pF load

5.3 Slave I2C interface

An I2C compliant interface is available for communication with an external host CPU. The interface can be operated in slave mode only. It is fully compatible with the I2C industry standard fast mode. Since the maximum SCL clock frequency is 400 kHz, the maximum bit rate is 400 kbit/s. The interface stretches the clock when slowed down while serving interrupts, therefore the real bit rates may be slightly lower.

The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D_SEL = 0, the I2C interface is not available.

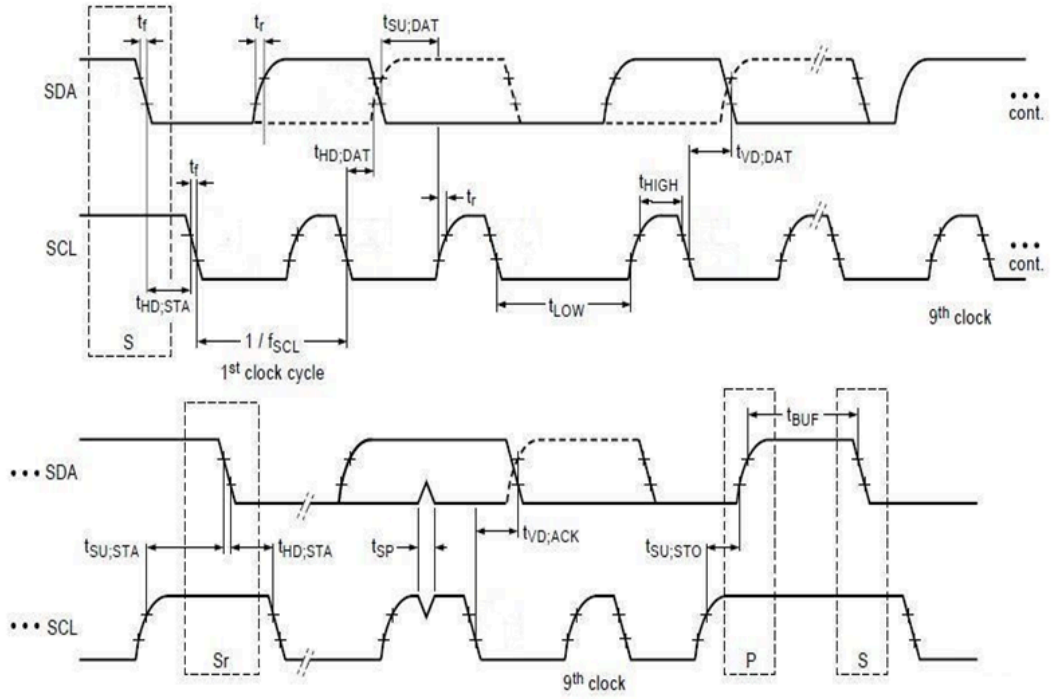

Figure 4: NEO-D9S correction data receiver I2C slave specification

Symbol	Parameter	Min (Standard / Fast mode)	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	4.0/1	-	µs
t_{LOW}	Low period of the SCL clock	5/2	-	µs
t_{HIGH}	High period of the SCL clock	4.0/1	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	5/1	-	µs
$t_{HD;DAT}$	Data hold time	0/0	-	µs
$t_{SU;DAT}$	Data set-up time	250/100		ns
t_r	Rise time of both SDA and SCL signals	-	1000/300 (for C 400pF)	ns
t_f	Fall time of both SDA and SCL signals	-	300/300 (for C 400pF)	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0/1	-	µs
t_{BUF}	Bus free time between a STOP and START condition	5/2	-	µs
$t_{VD;DAT}$	Data valid time	-	4/1	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	4/1	µs
V_{nL}	Noise margin at the low level	0.1 VCC	-	V
V_{nH}	Noise margin at the high level	0.2 VCC	-	V

Table 11: NEO-D9S I2C slave timings and specifications

5.4 USB interface

The USB 2.0 FS (Full Speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V_USB pin supplies the USB interface.

5.5 Default interface settings

Interface	Settings
UART	9600 baud, 8 bits, no parity bit, 1 stop bit. Output protocol: UBX. Input protocols without need of additional configuration: UBX.
USB	Output messages activated as in UART. Input protocols available as in UART.
I2C	Output messages activated as in UART. Input protocols available as in UART.
SPI	Output messages activated as in UART. Input protocols available as in UART.

Table 12: Default interface settings

☞ The boot message is still output using $GNTXT messages, this is output when the NEO-D9S is powered up.

☞ Refer to the u-blox NEO-D9S Interface description [2] for information about further settings.

6 Mechanical specification

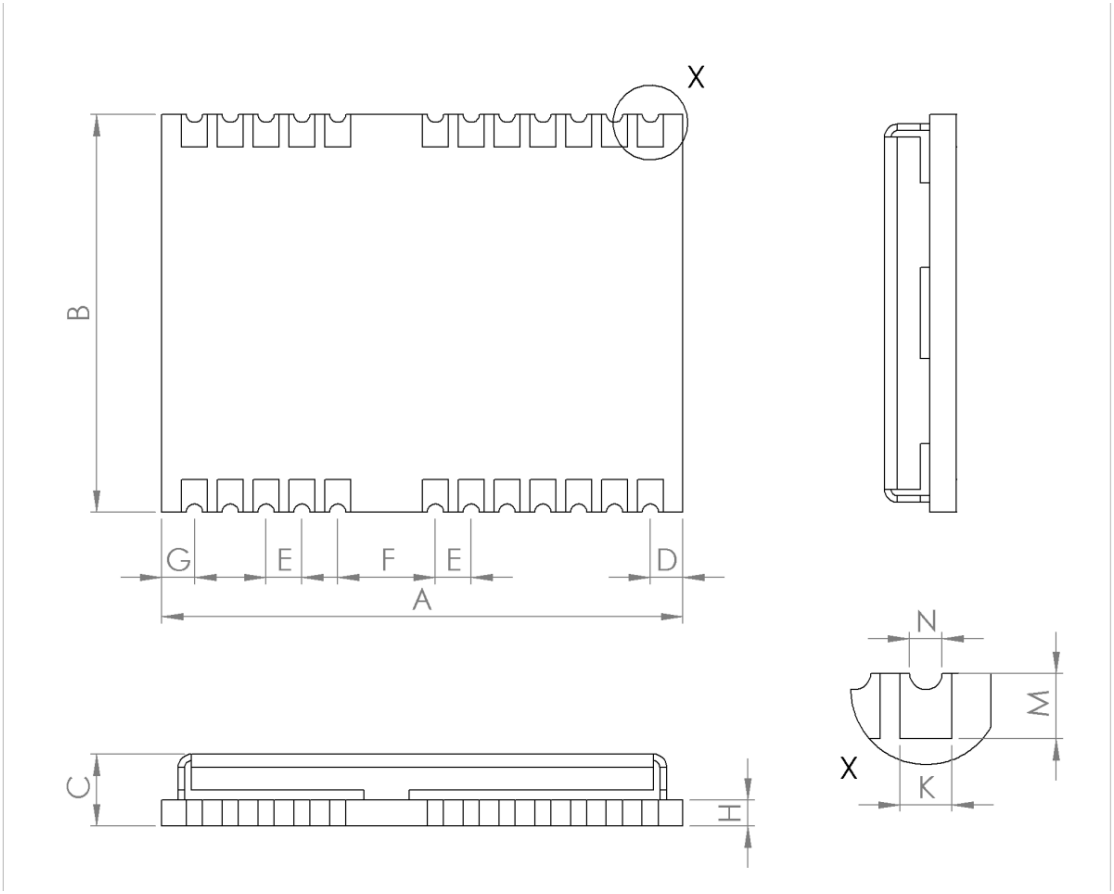

Figure 5: NEO-D9S mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)
A	15.9	16.0	16.6
B	12.1	12.2	12.3
C	2.2	2.4	2.6
D	0.9	1.0	1.3
E	1.0	1.1	1.2
F	2.9	3.0	3.1
G	0.9	1.0	1.3
H	0.72	0.82	0.92
K	0.7	0.8	0.9
M	0.8	0.9	1.0
N	0.4	0.5	0.6
Weight		1.6g	

Table 13: NEO-D9S mechanical dimensions

7 Reliability tests and approvals

7.1 Approvals

The NEO-D9S is designed to in compliance with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

The NEO-D9S complies with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

Declaration of Conformity (DoC) is available on the u-blox website.

8 Labeling and ordering information

This section provides information about product labeling and ordering. For information about product handling and soldering see the NEO-D9S Integration manual [1].

8.1 Product labeling

The labeling of the NEO-D9S modules provides product information and revision information. For more information contact u-blox sales.

8.2 Explanation of product codes

Three different product code formats are used. The **Product name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering code** includes options and quality, while the **Type number** includes the hardware and firmware versions. Table 14 below details these three different formats.

Format	Structure	Code for this product
Product name	PPP-TGV	NEO-D9S
Ordering code	PPP-TGV-NNQ	NEO-D9S-00B
Type number	PPP-TGV-NNQ-XX	NEO-D9S-00B-00

Table 14: Product code formats

The parts of the product code are explained in Table 15.

Code	Meaning	Example
PPP	Product family	NEO
TG	Platform	D9 = u-blox D9
V	Variant	S = L band corrections
NNQ	Option / Quality grade	NN: Option [00...99] Q: Grade, A = Automotive, B = Professional
XX	Product detail	Describes hardware and firmware versions

Table 15: Part identification code

8.3 Ordering codes

Ordering code	Product	Remark
NEO-D9S-00B	NEO-D9S correction data receiver	u-blox D9 correction data receiver for L band broadcast

Table 16: Product ordering codes

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: https://www.u-blox.com/en/product-resources.

Related documents

[1] NEO-D9S Integration manual, UBX-19026111

[2] NEO-D9S Interface description, UBX-19048765

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage https://www.u-blox.com.

Revision history

Revision	Date	Name	Status / comments
R01	26-Mar-2018	jhak	Objective Specification
R02	26-Apr-2019	jhak	Objective Specification
R03	28-June-2019	ghun	Objective Specification - V_BCKP removed
R04	26-Nov-2019	ghun/jhak	Advance Information - V_BCKP pin connect to VCC. I2C, SPI, antenna supervisor, EXTINT, software back-up mode added.
R05	05-Feb-2020	ghun/jhak	Early production information - USB added to Absolute maximun ratings table. Vil and Vih updated in Operating conditions table.
R06	27-Oct-2020	dama	USB Interface section update. UART interface section update

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