Inter-IC Sound (I2S) Example Project
2.0

Features

- Demonstrates how to configure DMA transfers from memory to the I2S and from I2S to memory

General Description

The I2S interface is a continuous interface that requires an uninterrupted stream of data. For most applications, this requires use of DMA transfers to prevent an underflow of the Tx direction or an overflow of the Rx direction.

This example project demonstrates how to configure the DMA transfers from the memory to I2S and from I2S to the memory. Data transmitted on Tx and data received on Rx is displayed on the character LCD on the CY8CKIT-001 Development Kit.

Development Kit Configuration

1. The PSoC 3 or PSoC 5LP Processor Module must be installed on the PSoC Development Kit (DVK)
2. Configure the pin connections as shown on the project schematic
3. Apply power to the PSoC DVK
4. Build the project and program the hex on to the target device using a MiniProg3 programmer
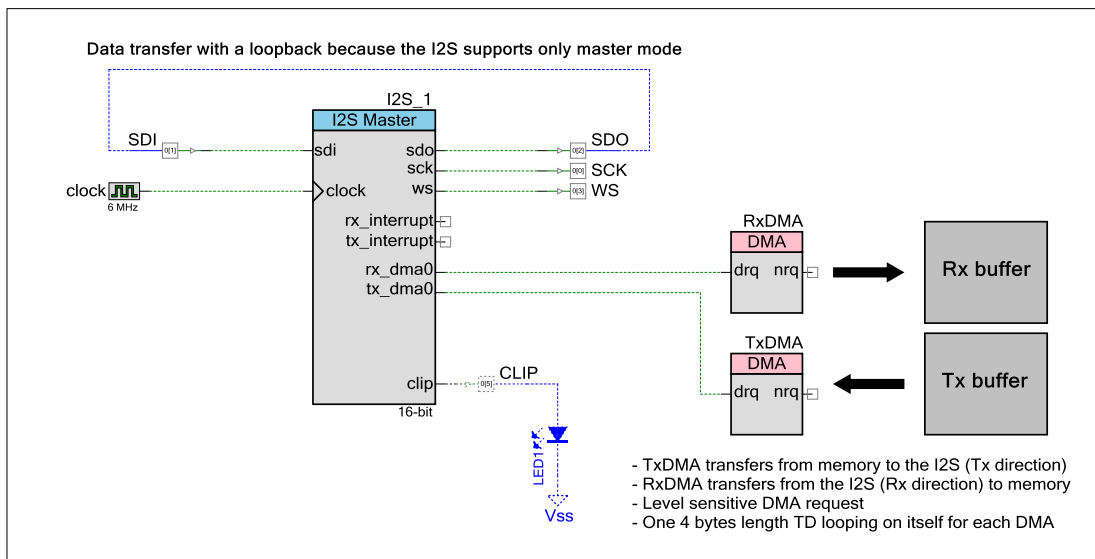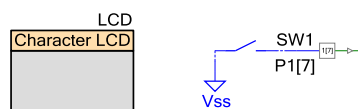
Project Configuration

The example project consists of I2S, DMA, and Character LCD components. The design schematic is shown in **Figure 1**. The blue annotation components in the schematic show the external connections required. As shown in the schematic, two instances of the DMA component named "TxDMA" and "RxDMA" are connected to the tx_dma0 and rx_dma0 terminals of the I2S component. The I2S component has been configured with the DMA request enabled for both Tx and Rx directions. The DMA request signals from the I2S component are level (instead of edge) signals, so the DMAs are configured appropriately.

Figure 1. I2S Component Example Project Schematic

The I2S component configuration windows are shown below. In the General tab, the component is configured to operate in the Rx and Tx mode, the bit resolution is static, the data bits is 16, and the word select period is 64. The byte swap is unchecked for both Rx and Tx.
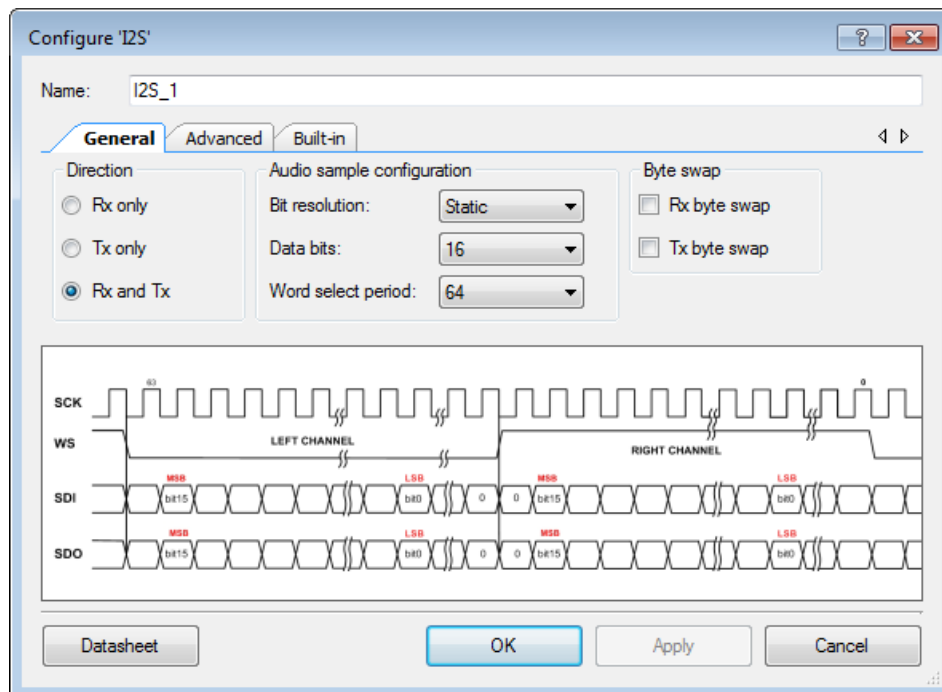
Figure 2. I2S component configuration – General tab

In the Advanced tab, the number of Rx and Tx channels is set to stereo, the data interleaving is configured to interleaved, and the DMA requests are enabled for both Rx and Tx. The Rx clip detection is enabled, and the positive and negative thresholds are set to 64 and -64 respectively.
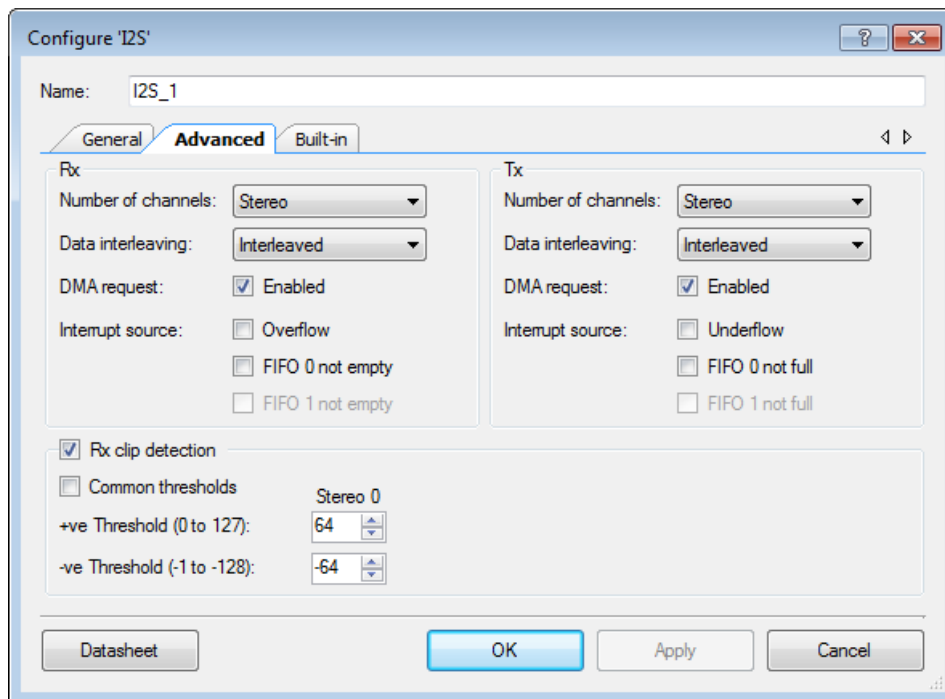
Figure 3. I2S component configuration – Advanced tab

Project Description

In the main firmware routine all the components are started, the DMA transfers are configured and enabled for both Tx and Rx directions. Data is continuously transmitted by Tx and received by t Rx through an external loopback connection. The TxDMA transfers the data from a transmit buffer in SRAM to the I2S Tx FIFO. The RxDMA stores the data received by the Rx in a receive SRAM buffer. Transmitted and received data is displayed on the LCD.

Pressing SW1 on the development kit increments the value of the first element in the transmit buffer. The receive data will be updated respectively after the new data is transmitted. If the received data value crosses the negative and positive clipping thresholds, the LED1 is turned on.

Expected Results

The Character LCD displays the data sent by the Tx direction and received on the Rx direction.

LED1 should be ON when the MSB of a data sample being received is greater than or equal to the positive clip threshold (64 or 0x40 in hexadecimal) and lower than negative clip threshold (-64 or 0xC0 in hexadecimal).