

SP6214-1.8V

 Iout (max): 100mA
 Vin (max): 7.0V
 Vdrop (max): 250mV
 Iq: 65uA

Figure 1 illustrates the pin connections for the ATmega328P. The top section shows three voltage pins: VREF1 connected to 3V0, 1.8V connected to 1V8, and VDD connected to VDD. The bottom section shows four digital pins: GPIO0 connected to FLSH_CEN, CS0 connected to FLSH_S0, and two pins connected to FLSH_S1 and FLSH_SCLK.

ARTIC R2

RF Amp

RF Track Impedance: Coplanar Waveguide with Ground Calculations
<https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator/>
 JLCPCB JLC7628 4-Layer 0.8mm Impedance Control Stackup (Er = 4.6)
 TX: 400MHz
 Ground is on layer 2.
 Prepreg thickness: 0.2mm
 12 mil track with 4 mil gap = 49.5 Ohms
 RX: 466MHz
 Ground is on layer 15 (there is a cut-out on layer 2 as per AnSem's design guide)
 Prepreg (0.2) + layer 2 (0.0175) + core thickness (0.265) = 0.4825mm
 20 mil track with 4 mil gap = 49.9 Ohms

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Special Instructions



Special Instructions

REV:
X01

Sheet: 1/1